Lessons learned probing power management devices in multi-DUT test format

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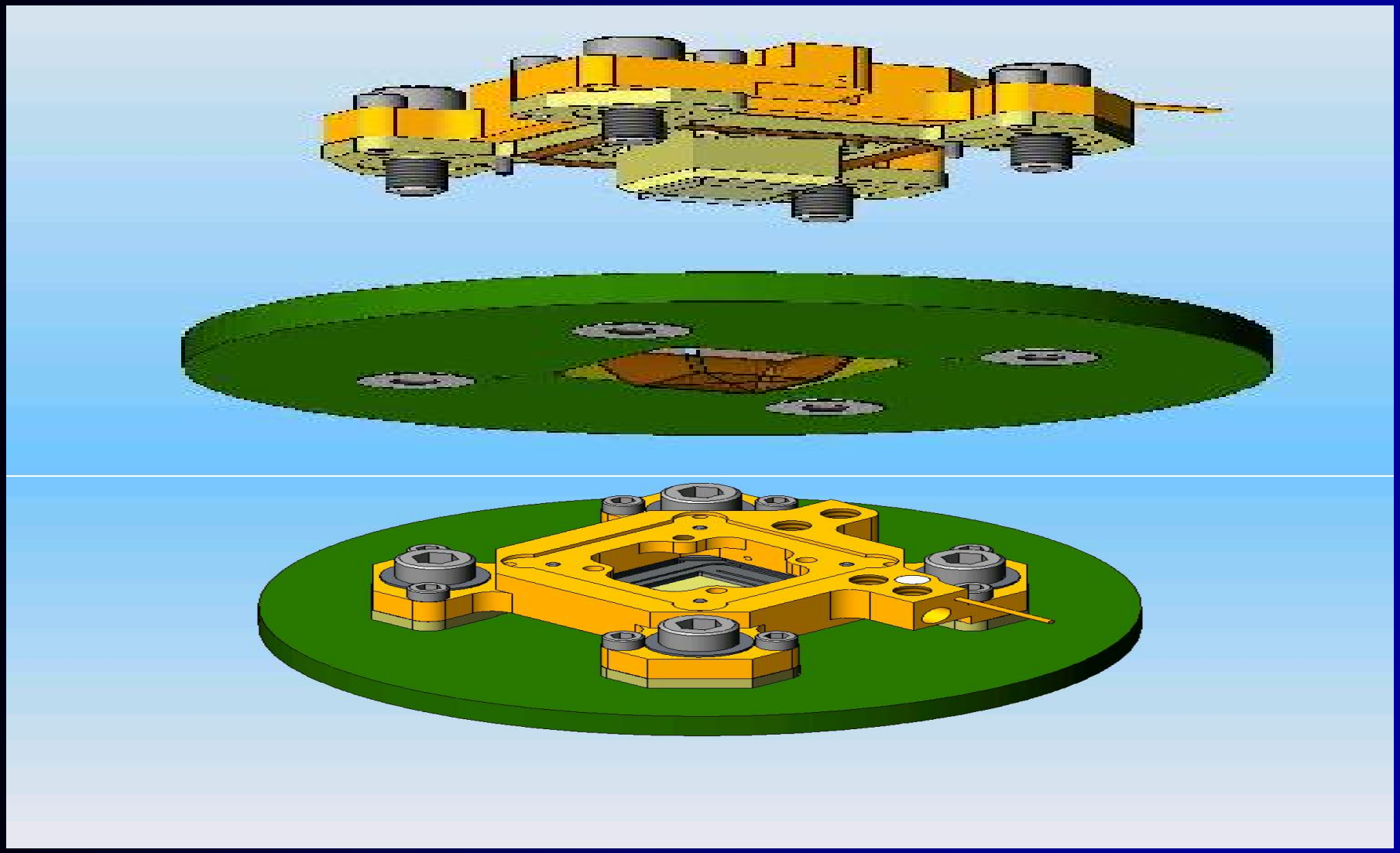
What we will NOT be covering…

- Multi-DUT economics as applied to cost of ownership models etc.
- RF modelling / performance / characterisation.
- Sales pitch . This is a TECHNICAL paper, intended to illustrate potential problems and corrective actions as controlled by the laws of physics.

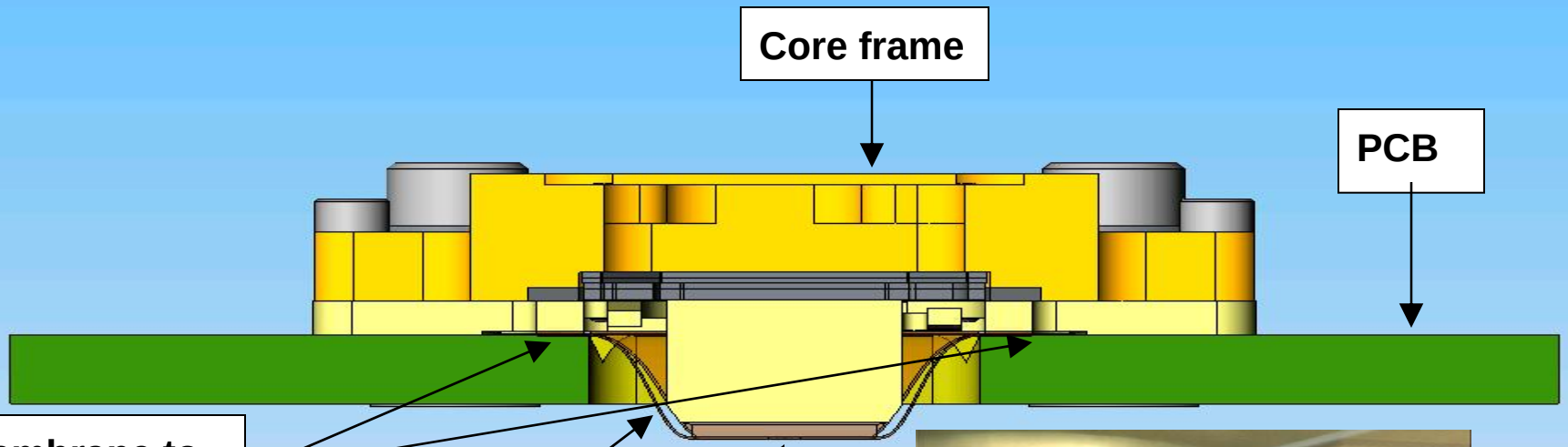
Main topics in this presentation:

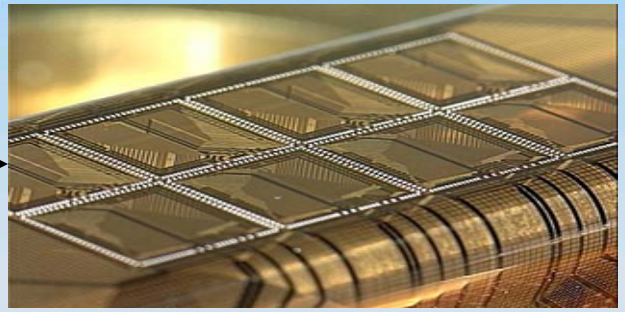
- Overview of Pyramid Probe® technology
- Power management device overview
- Our first quad site power management probe card
- Results from a cantilever card
- Analysis of the problem
- Simulation of probe card and DUT
- Quad site probe card: Take 2.
- Results from the test floor
- What did we learn from this?
- Conclusion & acknowledgements

Pyramid Probe® Cards



Mechanical Core Assembly





Main parts of a cell phone

Applications RISC

On-chip shared memory controller/DMA

Applications DSP

Internal SRAM

Boot/secure ROM

Graphics HW accelerator

Support logic blocks: timers, interrupt controllers, etc.

Video HW accelerator

Security and encryption

Power & Clock Controller

External memory controllers

UARTs and interfaces

Digital baseband

Analog baseband

WLAN MAC

WLAN PHY

Bluetooth MAC/baseband

GPS digital baseband

RF transceiver

WLAN AFE

BT transceiver

GPS, RF receiver

Power amplifiers Multiplexers Switches

Camera module

Touchscreen

Audio codec amplifier

MMC/SDIO-card transceivers

SIM module

Keypad

Color LCD

A new probing challenge

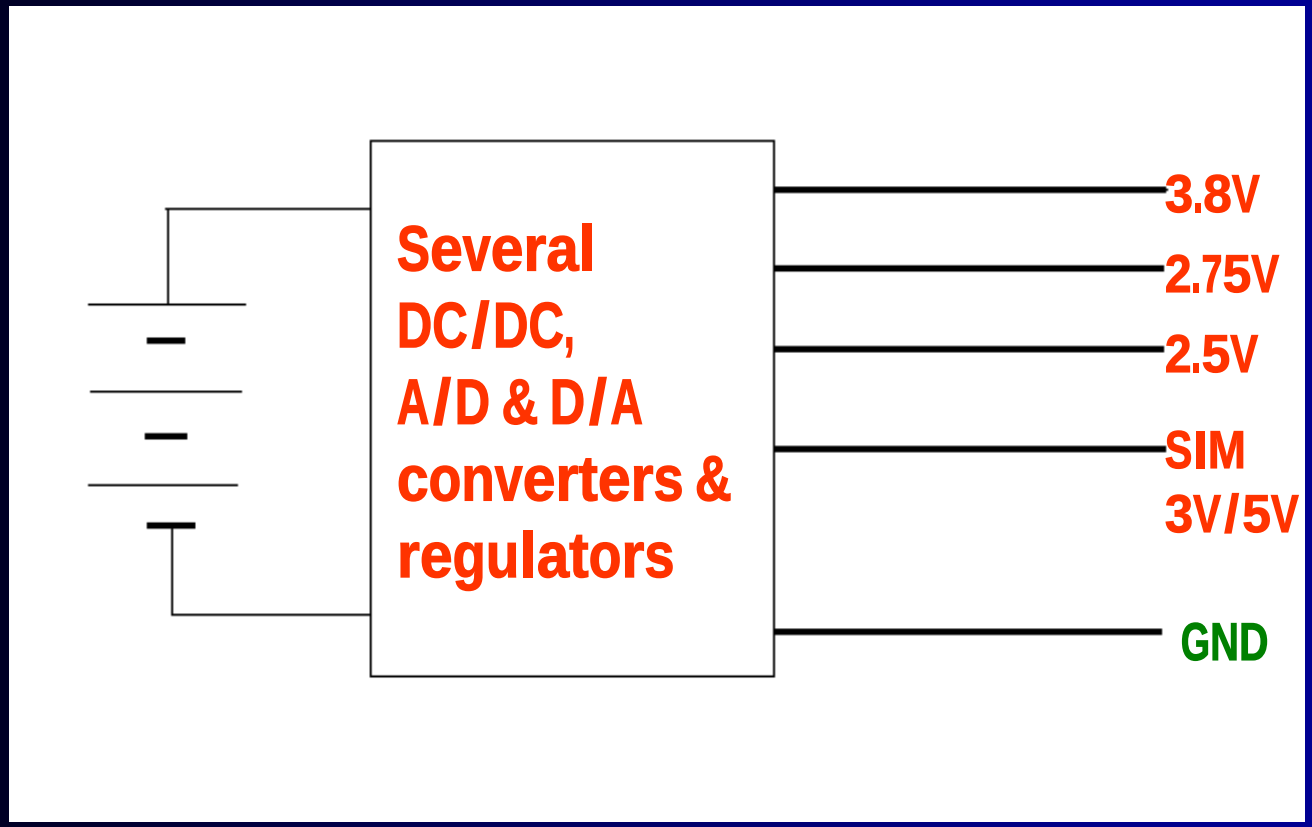
Currently probed with membrane

Battery pack

NOR and NAND Flash

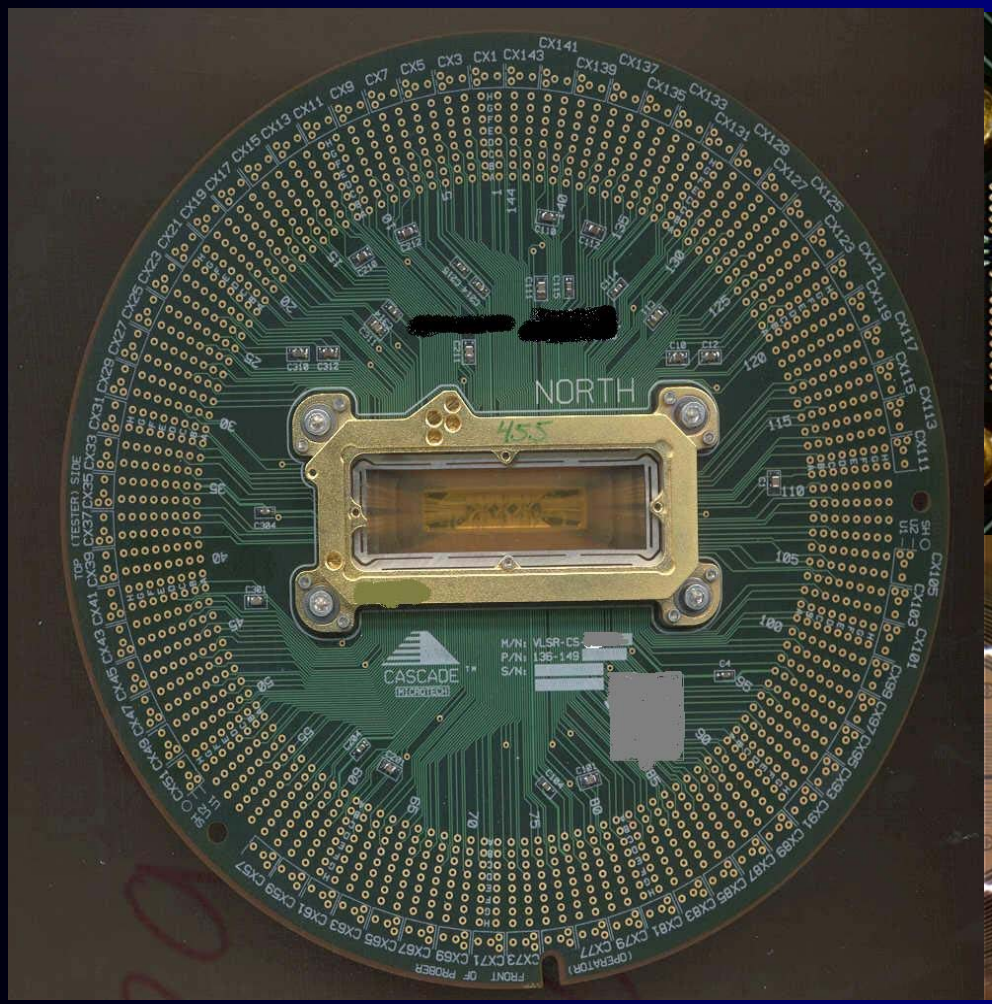
DDR DRAM

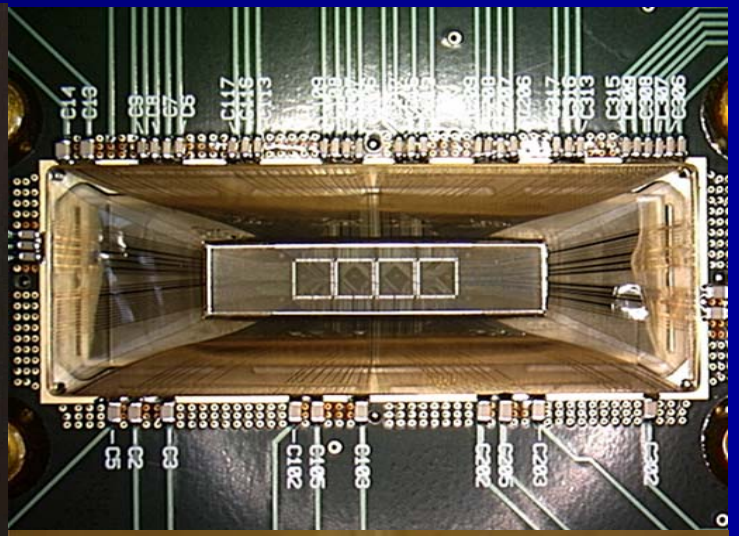
Extremely simplified cell phone power management device overview

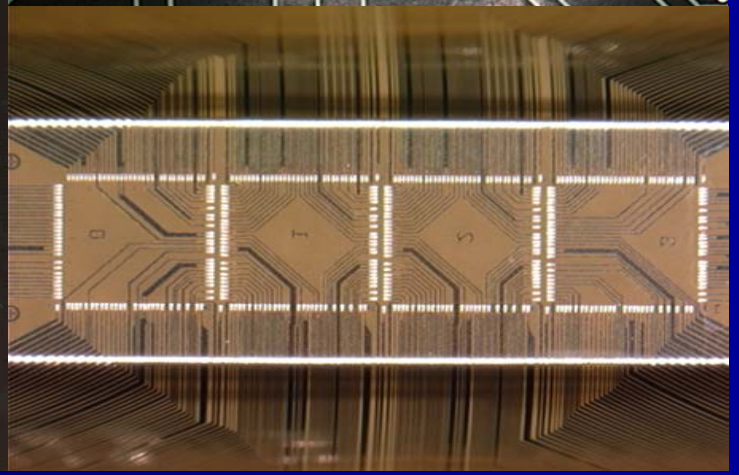


Real DUT has >100 bond pads!

Our first quad DUT power management probecard…..



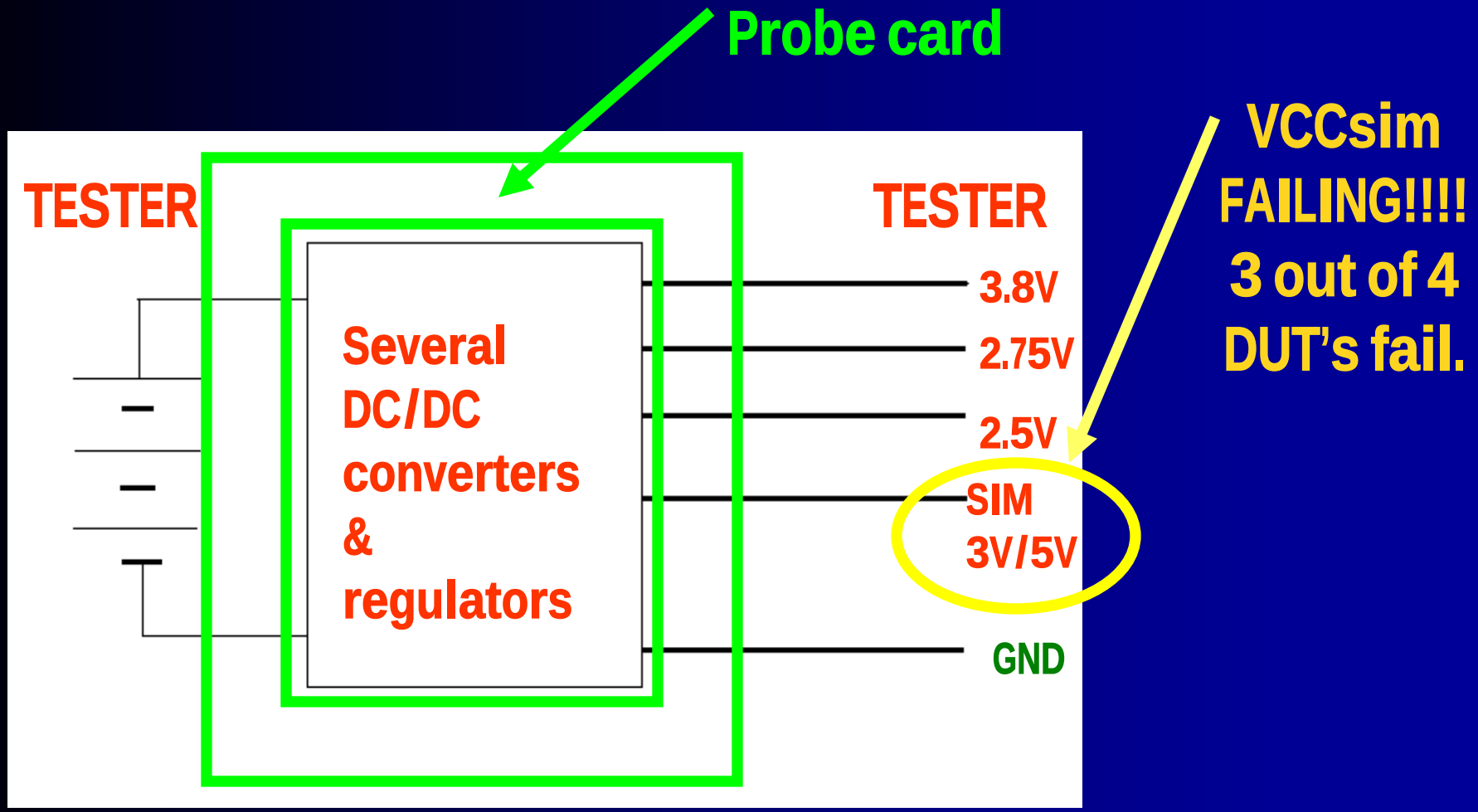




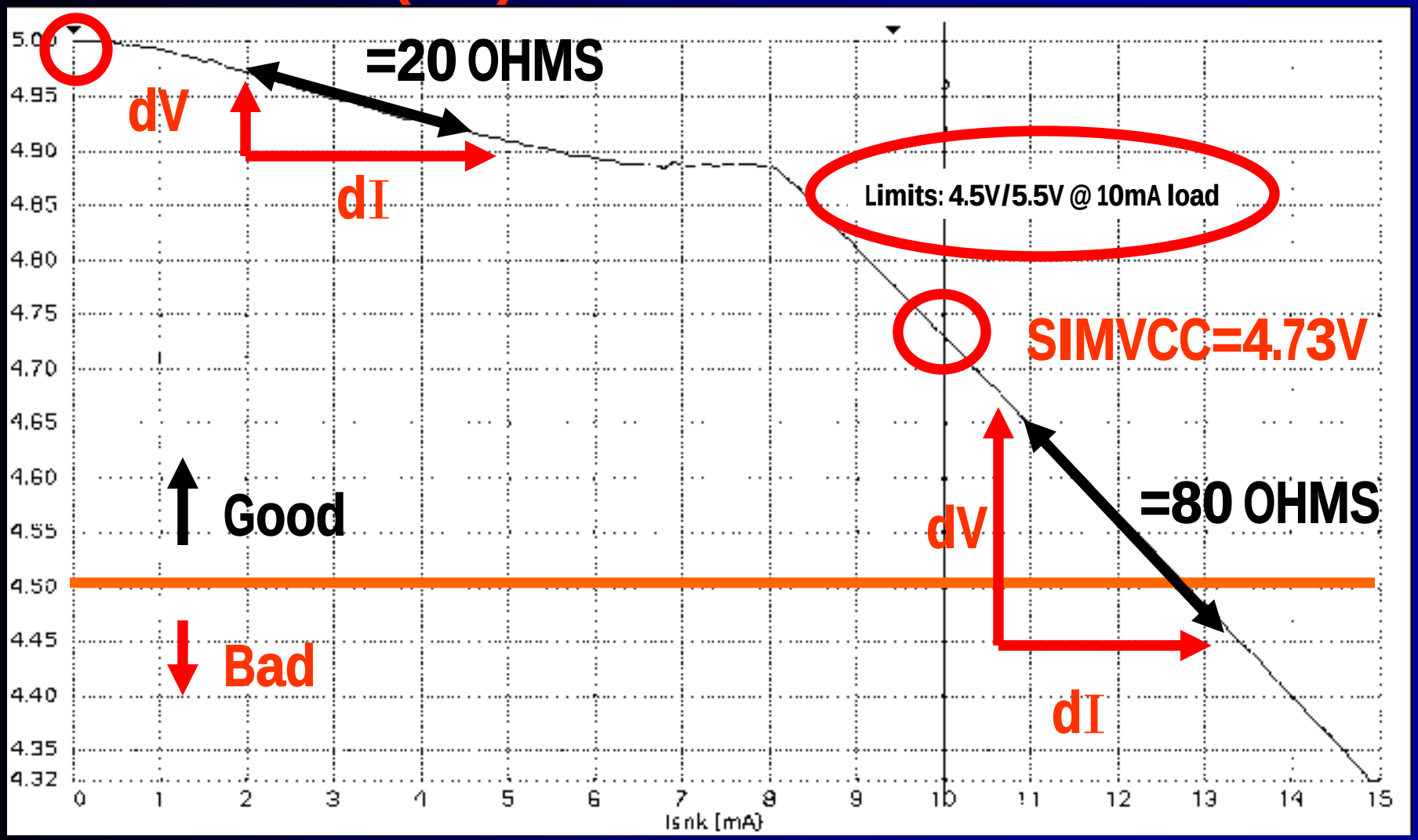
And then you get a phone call…..

- The new probe card is delivered to site.
- There is a substantial backlog of wafers waiting.
- A single site needle card is available, which is working.
- There is high pressure to have the quad site card running.
- This project has the attention of senior management.
- **Your new probe card does not appear to work.**
- **One DUT is fine, the other 3 are failing.**
- **We need this fixed NOW!**
- **What time is your flight?**

What exactly is the problem?



Single site Cantilever measurement



What does this tell us about the DUT?

- Pass & Fail limits are set by the end user, so the customer is not at liberty to change them.
- Best case is 5.0V, when the current flowing is zero.
- Device seems to have 2 modes, presumably when the regulator is working (Zo=20 ohms) and when the regulator is not working (Zo=80 ohms)
- This is a very marginal test. Even with cantilever at 4.73V, there is only 230mV headroom.

Measurements from quad site card.

Pass level for SIMVCC (5V mode) test is between 4.5V and 5.5V

Cantilever measures 4.73V

4.55V PASS!

4.32V FAIL!

4.38V FAIL!

4.46V FAIL!

But only by 50mV

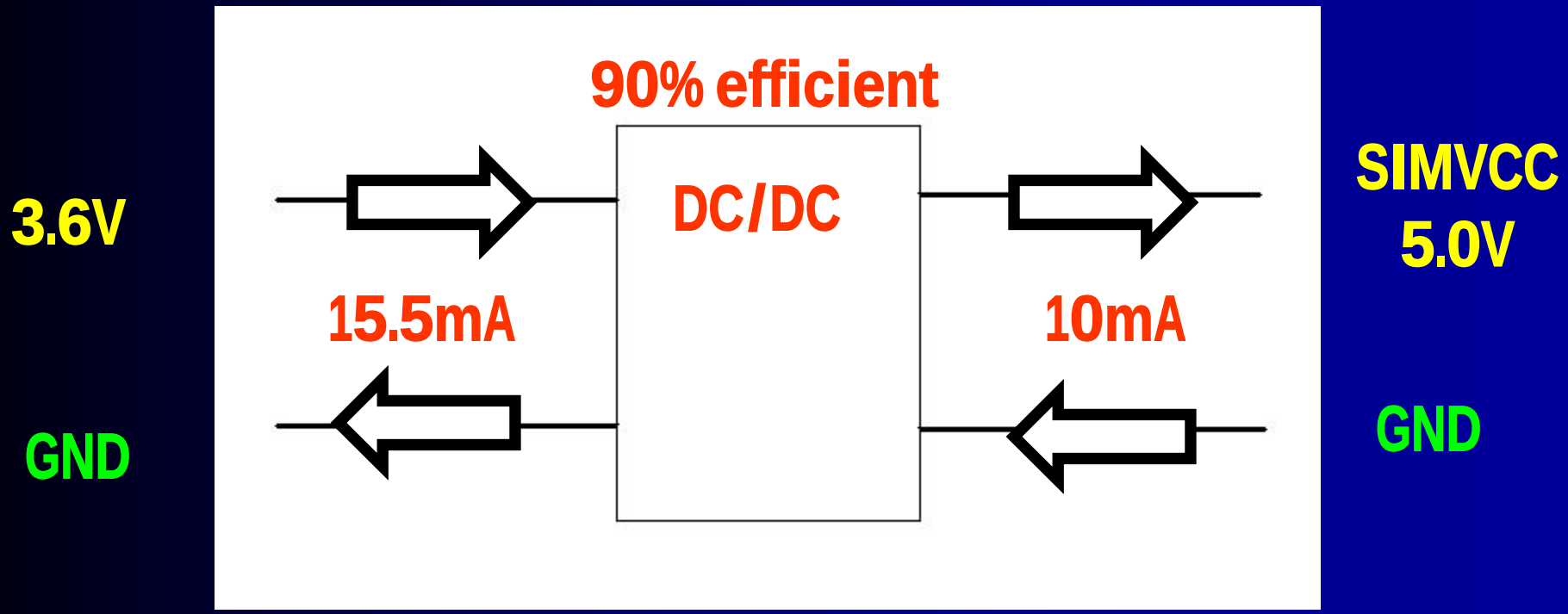
Notice also variation in results of 230mV from die to die

Let's take a step back

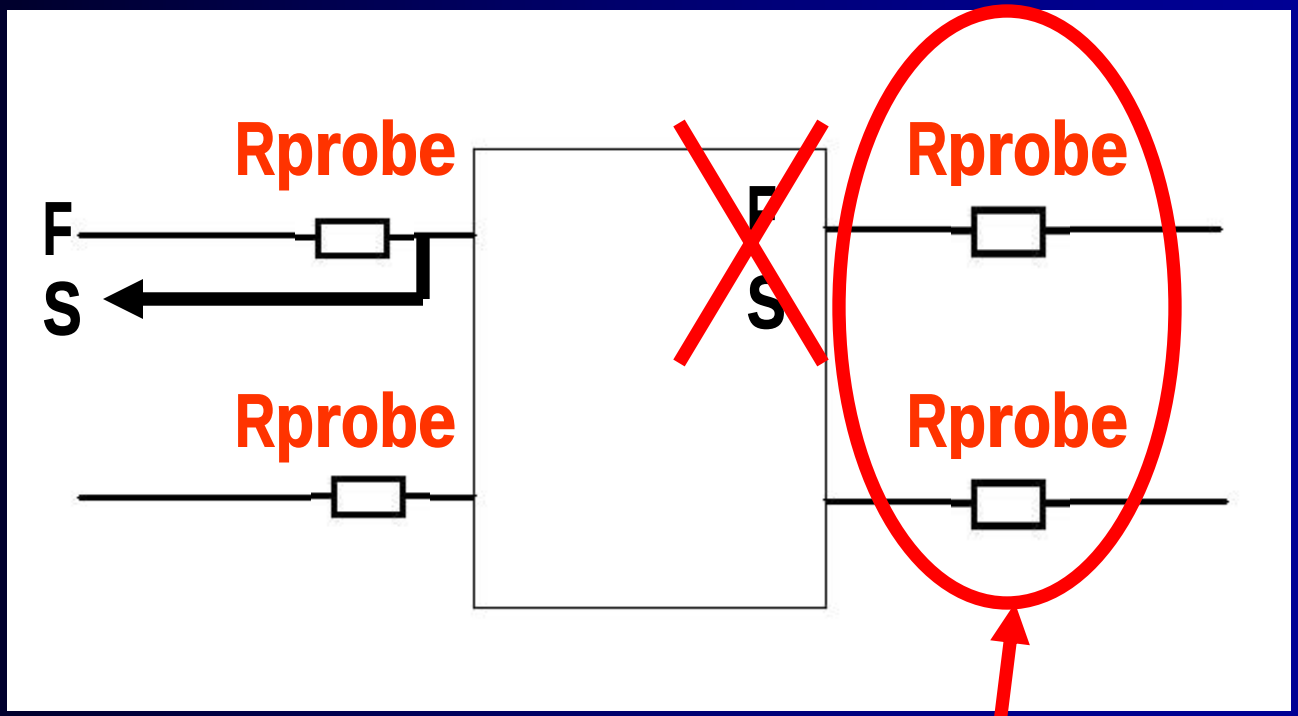
Version	Site 0	Site 1	Site 2	Site 3	Var.
rev A	4.55V	4.32V	4.38V	4.46V	230mV

- Why is only one DUT passing (barely) and the others failing?
- Why do we see such a large spread in the measurements?

What are the ideal test conditions?

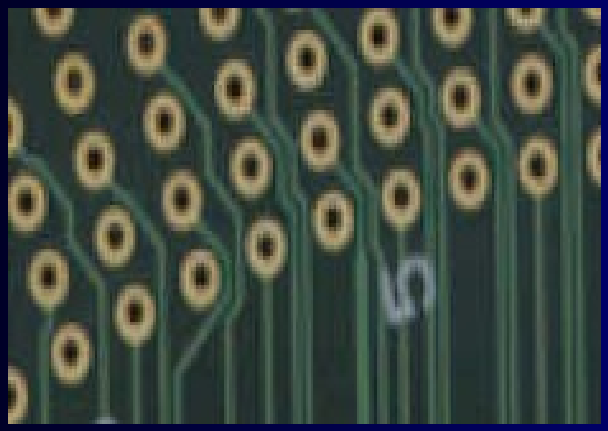


What's REALLY happening?



We need to make an estimation of Rprobe

- R_{probe} is comprised of 5 series elements:
  - A) R_{pogo}. This is the resistance between the pogo pin and the PCB.



We know it is low, typically 0.1 ohm.

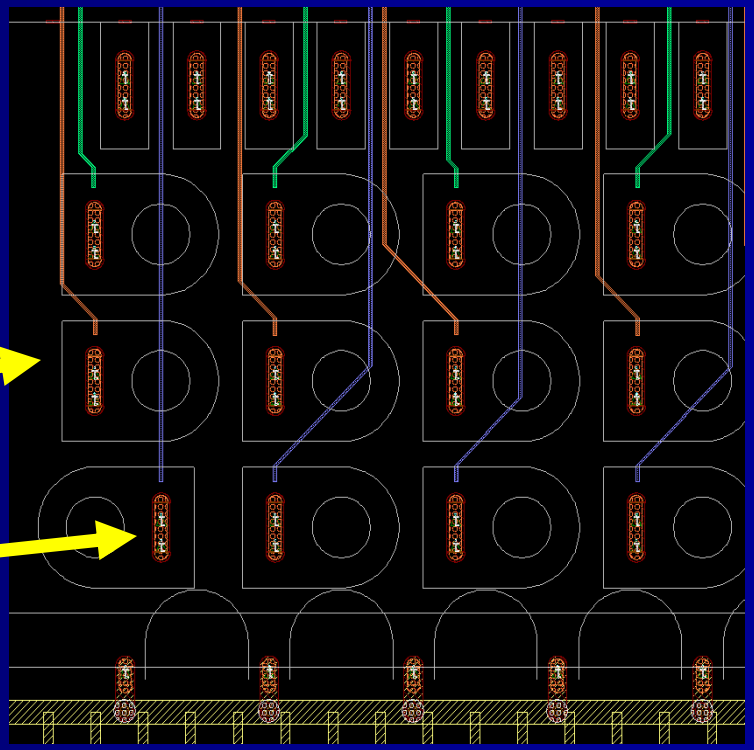
Continuing to make an estimation of R_{probe}

- B) Rpcb. This is the resistance of the trace on the PCB. Using R=rho x L / A, where:
- Rho=59.6E6 ohm meter (for copper)
- L is typically 5cm, but can vary from 3cm to 9cm depending on where it is and how many layers it uses.
- A is the cross sectional conducting area, an 8 mil wide, 1.4 mil thick copper trace

This gives R_{pcb} as around 4 ohms

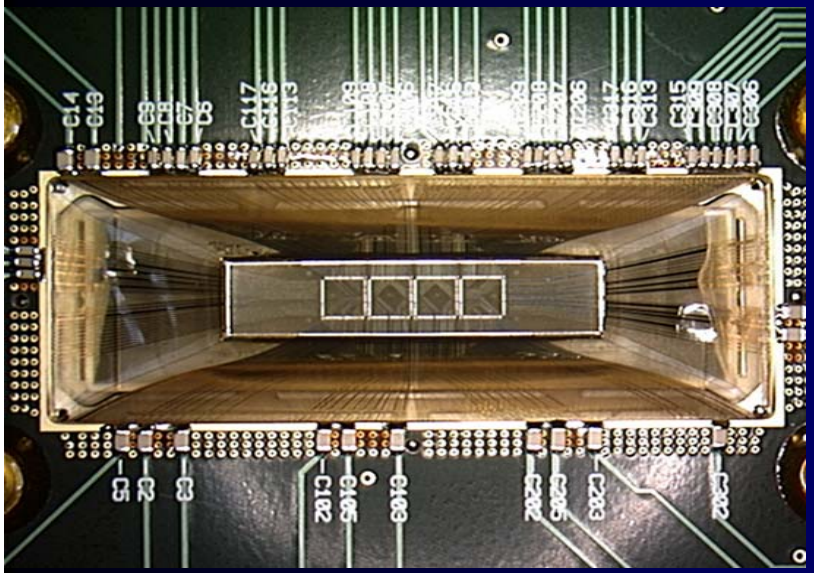
Continuing to find Rprobe

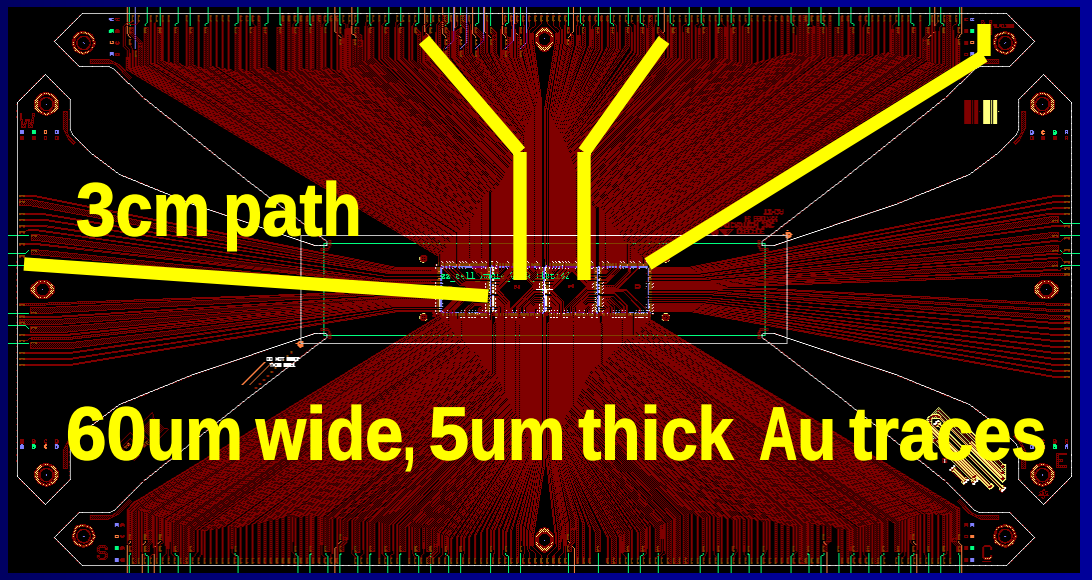
R_{int} is the resistance between the PCB and the membrane interface



Typically around 0.1 ohms

Membrane DC path resistance



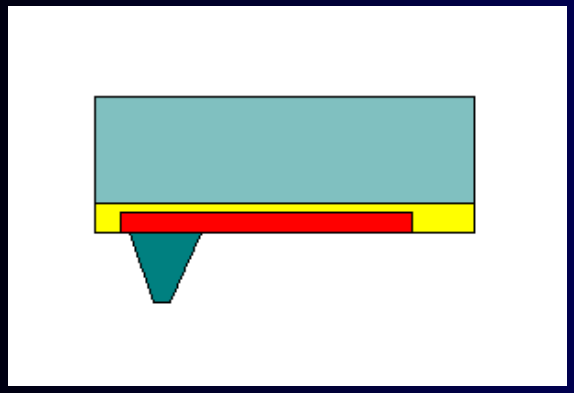


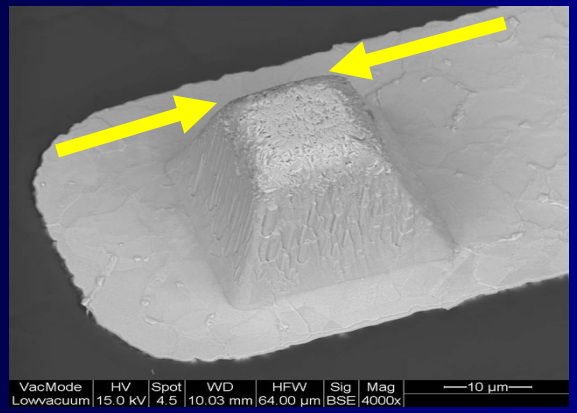
Using same formula, R_{memb} comes out to:

R=(4.5e7 x 30e-3)/(60e-6 x 5e-6) Around 5 ohms.

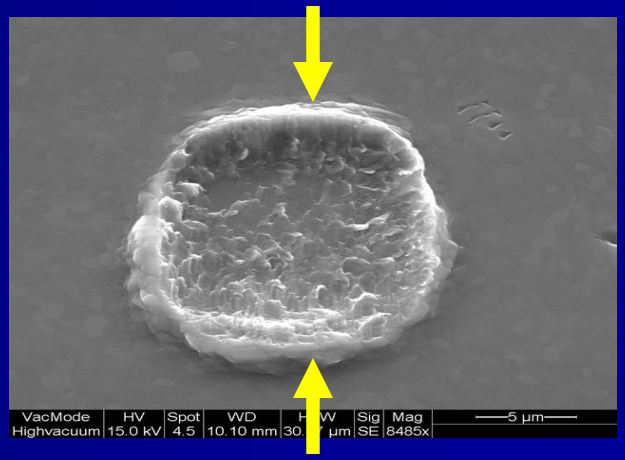
But, note the different path lengths between DUT's.

Contact tip resistance on Aluminium

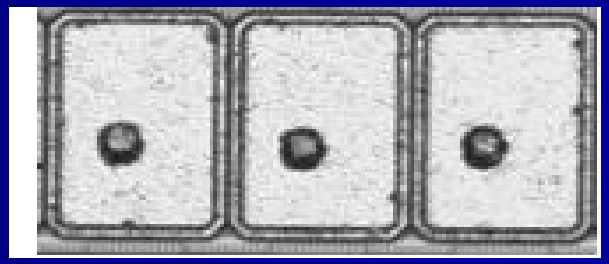




12 microns

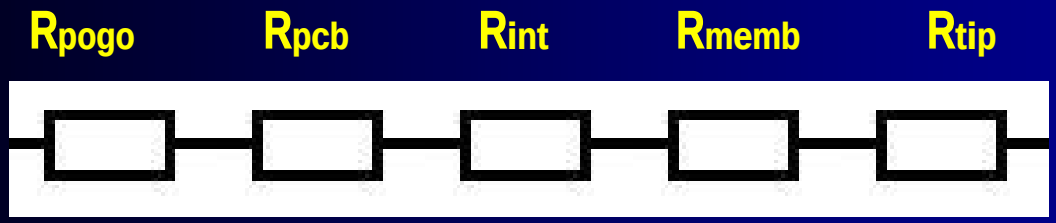


15 microns



From previous data, we know this is around 0.2 ohm

Put it all together and what do you get?



= 0.1 +4.0 +0.1 +5.0 +0.2 ohms

= 9.4 ohms

WAY TOO HIGH! We should be targeting 2-3 ohms or less.

Modelling and simulation of SIMVCC using Rev A probe card

Version	Site 0	Site 1	Site 2	Site 3	Cantilever
rev A	4.55V	4.32V	4.38V	4.46V	4.73V
Loss	180mV	410mV	350mV	270mV	0.00mV

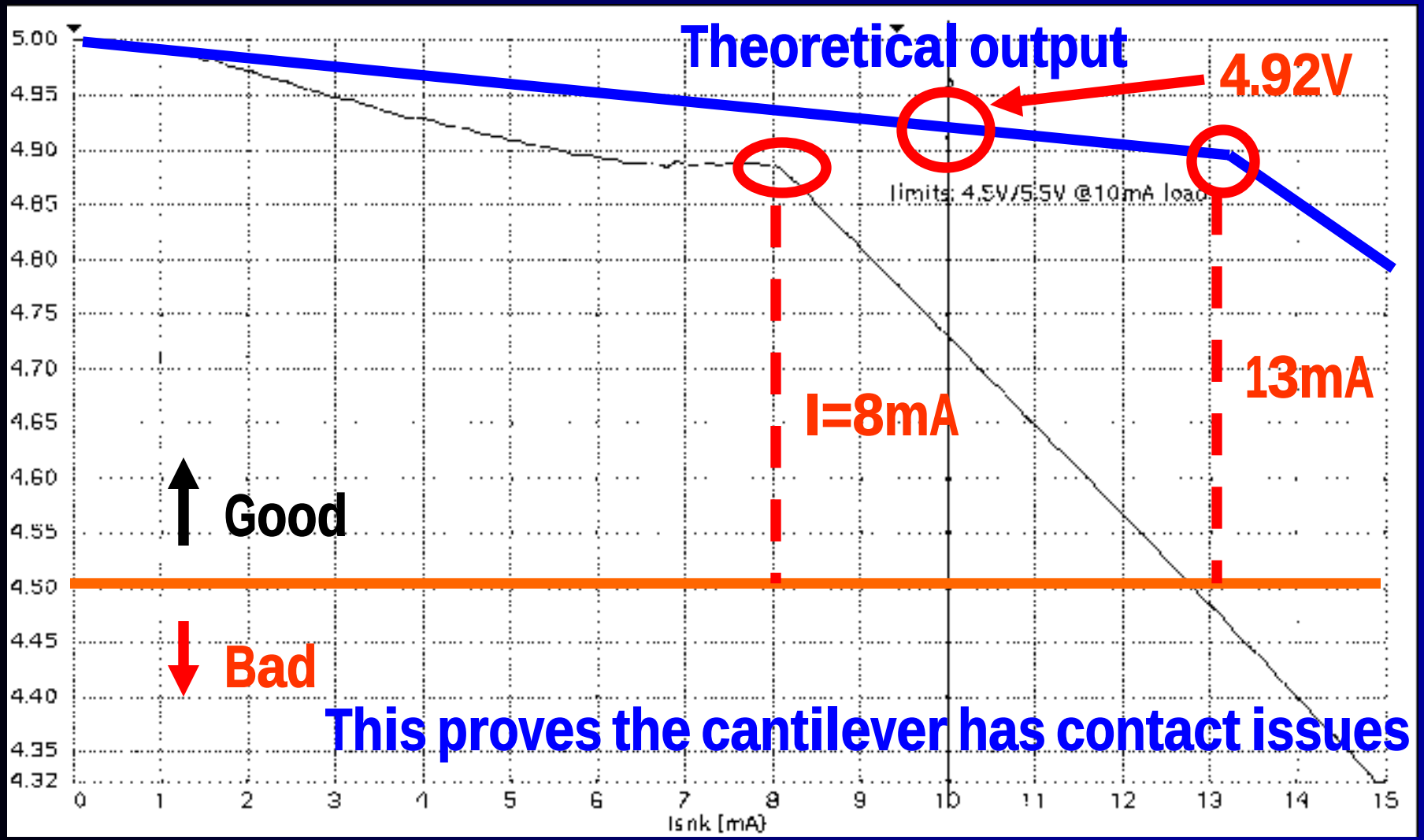
DUT	Rmemb ohms	Rpcb ohms	Rprobe1 ohms	Rmemb ohms	Rpcb ohms	Rprobe2 ohms	Rtotal ohms	current mA	Vdrop mV	measured loss mV
0	5.4	4.2	10	5.1	0.5	5.9	15.9	10mA	159	180
1	6.3	4.9	11.6	6.4	0.5	7.2	18.8	10mA	188	410
2	6.3	8.4	15.1	6.3	0.5	7.1	22.2	10mA	222	350
3	5.9	5.3	11.6	5.4	0.5	6.2	17.8	10mA	178	270

Probe card resistance varies significantly DUT to DUT

But this does not explain fully the measured differences

Is the 4.73V from cantilever a valid number?

Is the cantilever measurement valid?



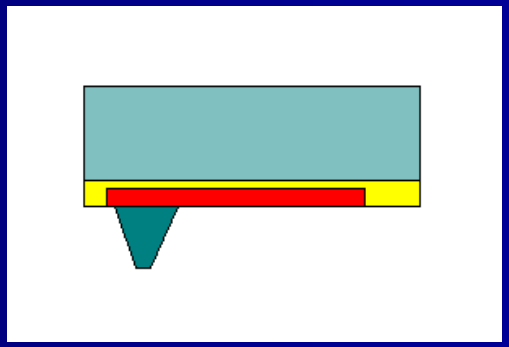
Now we know why we have problems

Version	Site 0	Site 1	Site 2	Site 3	Var.
rev A	4.55V	4.32V	4.38V	4.46V	230mV

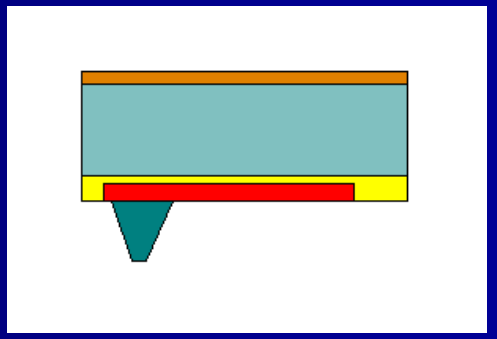
- Why is only one DUT passing (barely) and the others failing?
- Because the probe card resistance (Rprobe) is too high
- Why do we see such a large spread in the measurements?
- Because the membrane & PCB path lengths vary from DUT to DUT, and the reference value from the cantilever card is not stable.

So what can we do to fix this?

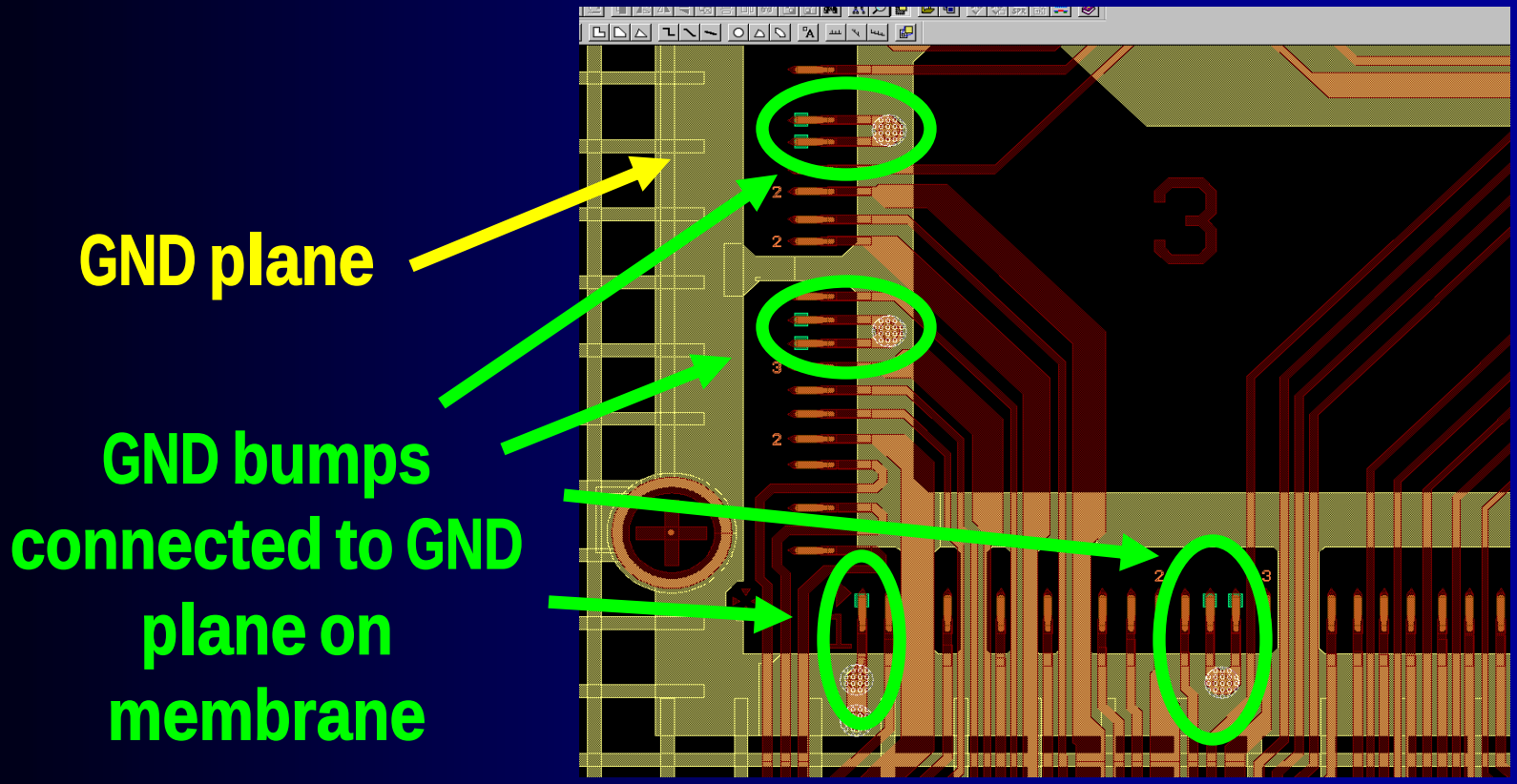
Rev A was made with one metal layer



We can use 2 metal layers, signal & ground.

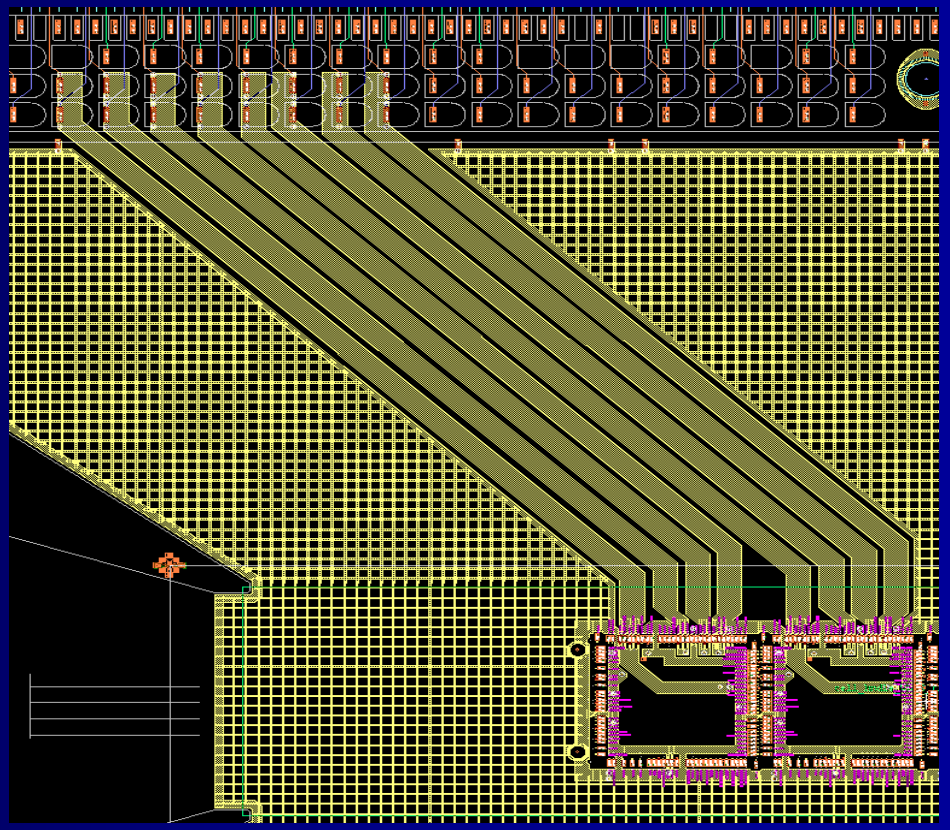


Let's connect all GND pins to GND plane on the new membrane.



Identify & prioritise all critical outputs from the DUT.

- 4 DC outputs per DUT
- identified & widened
- from 60um to 500um
- use isolated sections of the membrane ground plane as a conducting layer

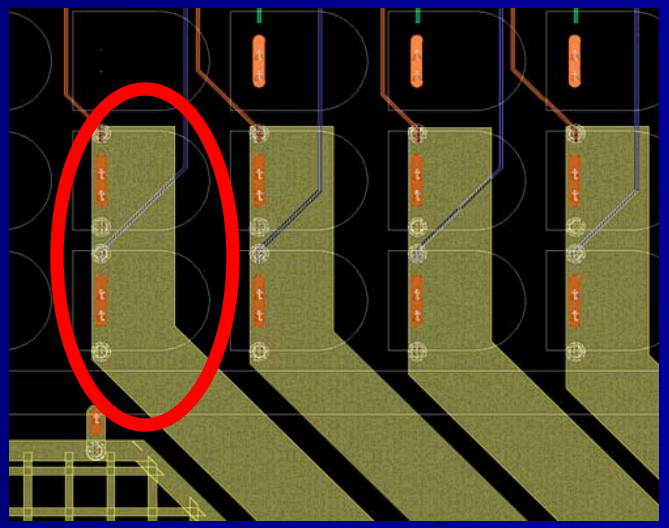


Note: the symmetrical layout, to give equal path lengths for all 4 DUT's

What else can we do?

Use 2 PCB interface points instead of 1

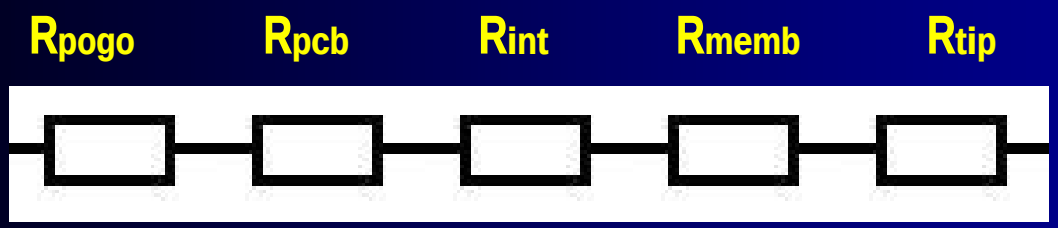
For each of the sensitive signals to halve the value of R_{int}



Redesign the PCB to use dedicated power planes for these signals.

This will reduce Rpcb significantly.

Now what do we have for Rprobe?



= 0.1 +0.5 +0.05 +0.8 +0.2 ohms

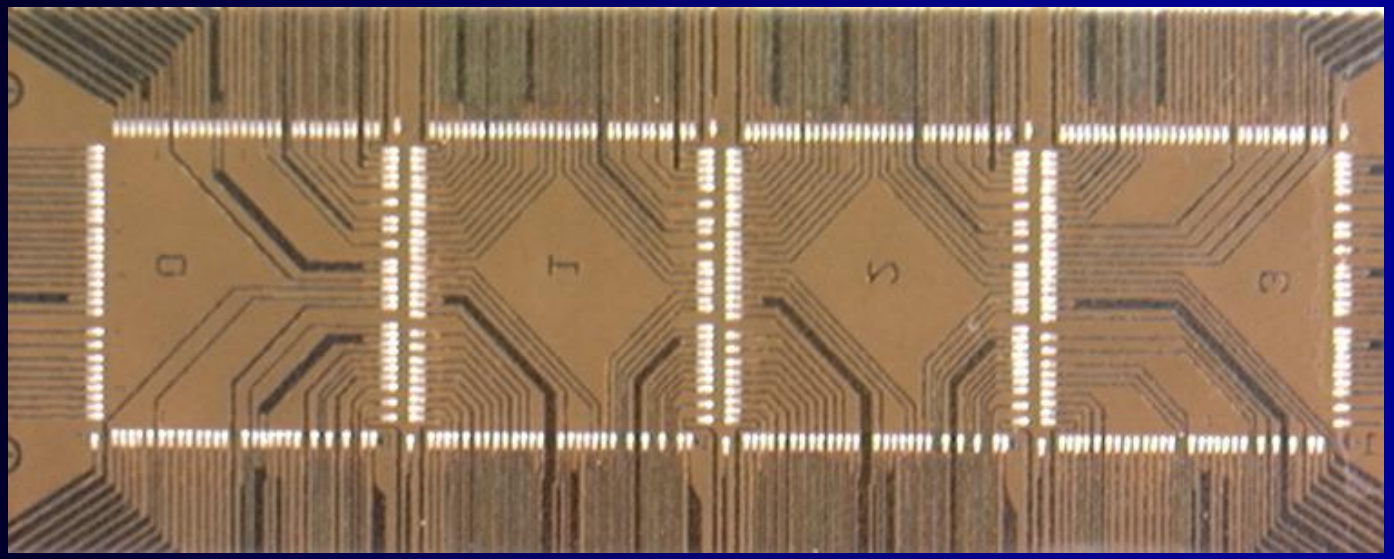
= 1.7 ohms

Much better. But does it work?

Old compared to new

OLD
rev A

1 metal
layer

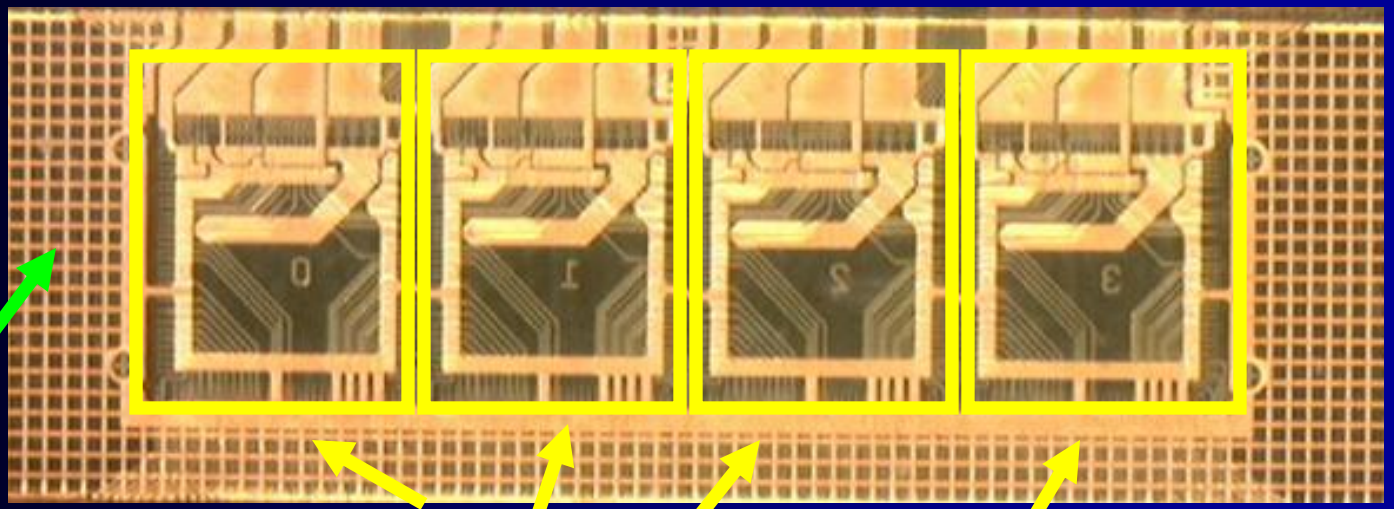


NO
symmetry

Thin
traces

NEW
Rev B

GND



Symmetry over all 4 sites

Our new results from the test floor

Target is 4.5V to 5.5V, cantilever = 4.73V, Theoretical=4.92V

Version	Site 0	Site 1	Site 2	Site 3	Var.
rev A	4.55V	4.32V	4.38V	4.46V	230mV
rev B	4.86V	4.84V	4.88V	4.85V	40mV

All 4 die show bin 1 , & higher (almost theoretical) SIMVCC

same DUT	4.86V	4.87V	4.87V	4.86V	10mV

Contact the same die 4 times by jogging the probecard 1 DUT

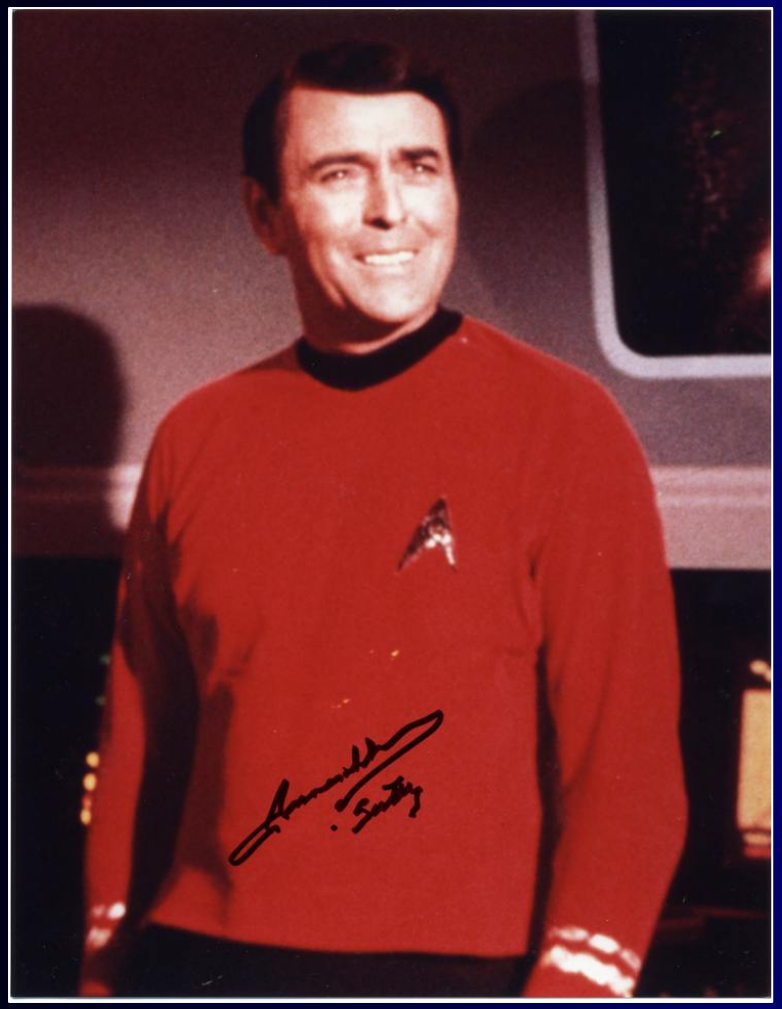
DUT to DUT variation of probe card now minimal

Result-Happy customer, and confidence in the laws of physics

So what did we learn?

- Laws of Physics always apply. Everything on the test floor (tester, prober, DUT, probe card etc) obeys them.
- Understand the function of the device. It's key to making a good probe card. Important to have communication between IC designer, test engineer, probe card apps engineer & membrane designer.
- Don't always trust your first set of measurements.
- Identify and prioritise sensitive signal paths where minimum resistance is necessary.
- New design rules implemented in Cascade design centre following this learning experience. These rules are constantly updated as we continue to learn.
- Since this event, >20 multi-DUT power management designs have been built and used successfully by customers around the world.

Conclusion (and personal tribute)



James Doohan 1920-2005

"Ye can'nae change the laws of physics!"

But at least you can try to understand and apply them to keep your customer happy and build a better product.

Acknowledgements

- From Cascade Microtech®
  - Ken Smith
  - Daniel Garrett
  - Eric Hill
  - Mike Bayne
- From Texas Instruments GmbH
  - Michael Janssen
  - Rainer Friedrich
  - Herbert Blenk
  - Andreas Berdzentis