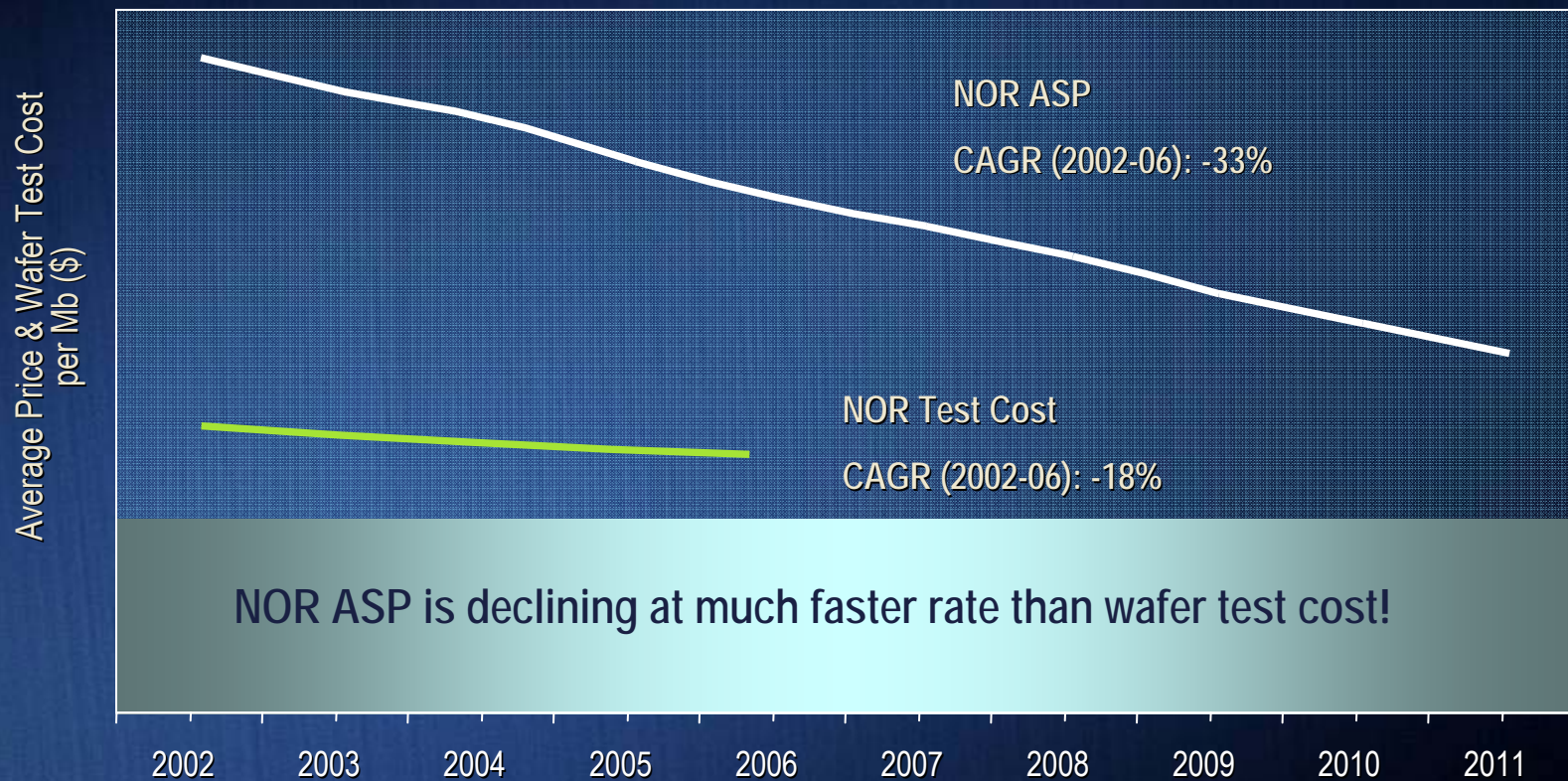# Agenda

- Wafer Test Cost Crisis

- Opportunities for Test Innovation

- Case Study

  - Proposed Test Flow Repartitioning

  - Assumptions

  - Scenario 1: Reduce Package Cost

  - Scenario 2: Reduce Test Cost

  - Scenario 3: Improve Product Yield

  - Case Study Summary

- Conclusions

Wafer Test Cost Crisis
Dangerous trend in device ASP and test cost

Average Price & Wafer Test Cost per Mb ($)

NOR ASP

CAGR (2002-06): -33%

NOR Test Cost

CAGR (2002-06): -18%

NOR ASP is declining at much faster rate than wafer test cost!

2002　2003　2004　2005　2006　2007　2008　2009　2010　2011

Source: Gartner & FFI Marketing

Wafer Test Cost Crisis
Cost challenges lead to industry consolidation

2004	2007	2010
1 SPANSION	SPANSION	SPANSION
2 intel	intel	SAMSUNG
3 ST	ST	[intel ST] ?
4 SHARP	SAMSUNG	?
5 RENESAS	RENESAS	
6 TOSHIBA	SST	
7 SAMSUNG		
8 SST		
9 MXIC		
10 ATMEL		

Wafer Test Cost Crisis

CHINESE CHARACTERS FOR *"CRISIS"*

危机

Danger　　　　*Opportunity*

Opportunities for Test Innovation

Test Flow

Sort 1

Sort n

Assy

Burn-in
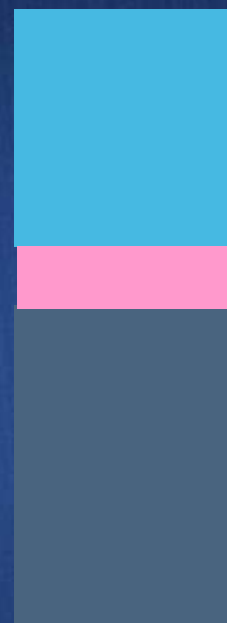
FT

• Test Innovation: Migrate test upstream

• Cost reduction can move ahead of device ASP decline

100% Cost

<50% Cost

Case Study
Proposed Test Flow Repartitioning

Typical Test Flow

SORT 1	SORT 2		PKG'ING	PKG BI	FINAL TEST

Proposed Test Flow

BURN-IN	SORT TEMP 1	SORT TEMP N	@ SPEED TEST	PKG'ING	PKG BI	FINAL TEST

FORMFACTOR
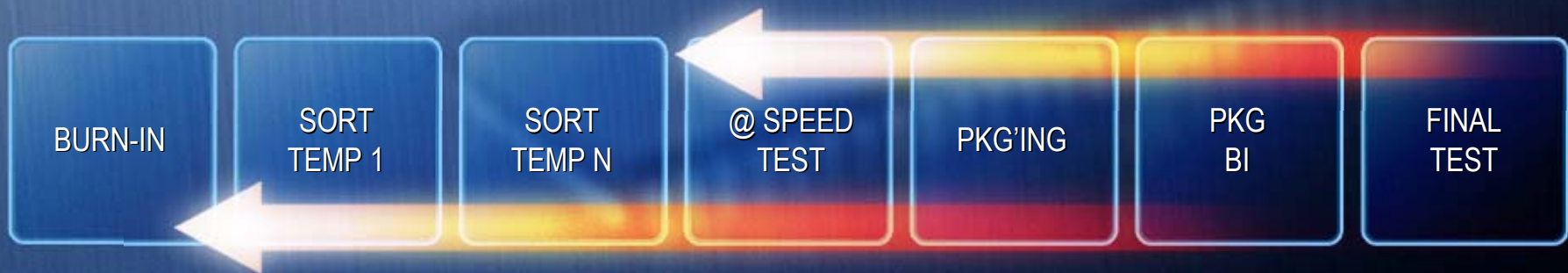
Case Study
Probe Card Products

Wafer Level BI
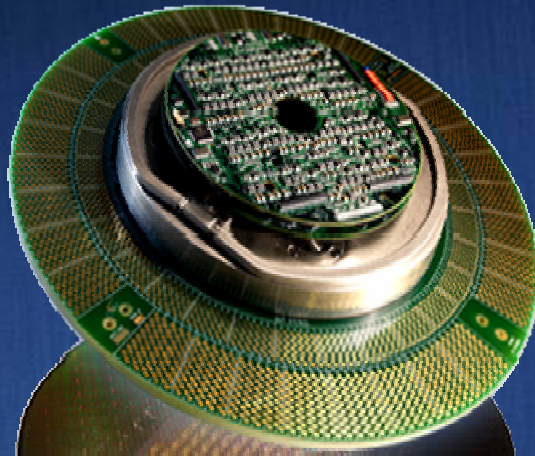
At speed Test

FFI UPStream Probe Card
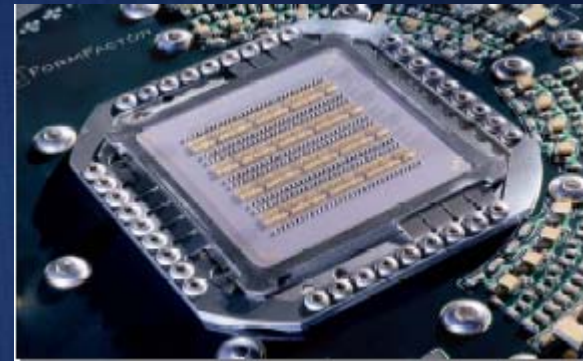
FFI High Frequency
Probe Card (HFTAP)

Case Study
Assumptions

- Die/200mm Wafer Eqv: 800 dpw
  - Typical Devices: 70nm 512Mb DDR2, 90nm 256Mb NOR
- Run Rate: 100,000 wspm (200mm eqv.)
  - Typical 300mm fab maximum capacity: ~40-45k WSPM
- Yield Assumptions:
  - 95% Wafer Test Yield
  - 95% Package Yield
  - 98% Final Test Yield
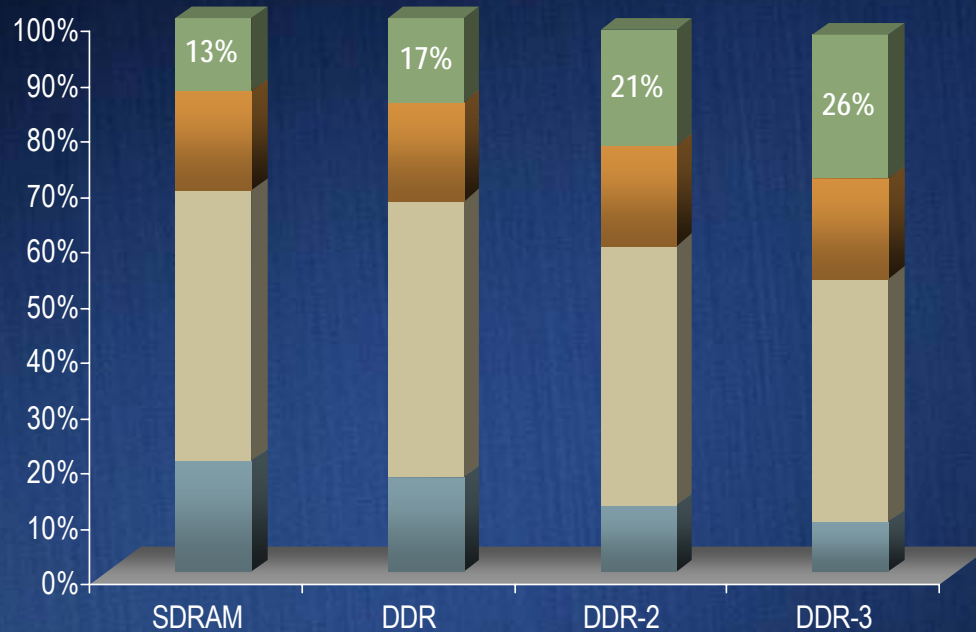
Scenario 1: Reduce Package Cost

Scenario 1: WLBI eliminates more non-repairable dies

- Save package cost for the non-repairable dies

Scenario 1: Reduce Package Cost
Wafer Test Opportunity to Reduce Packaging Cost

Raw Wafer   Front-end Processing   Testing Costs   Packaging Costs

- **Increasing packaging cost as % in product cost**

- ***1% wasted package = $12M annual revenue loss***
  - BGA: -> $1 per unit
  - 300 Million Units/Qtr

Source: Gartner & FFI Marketing
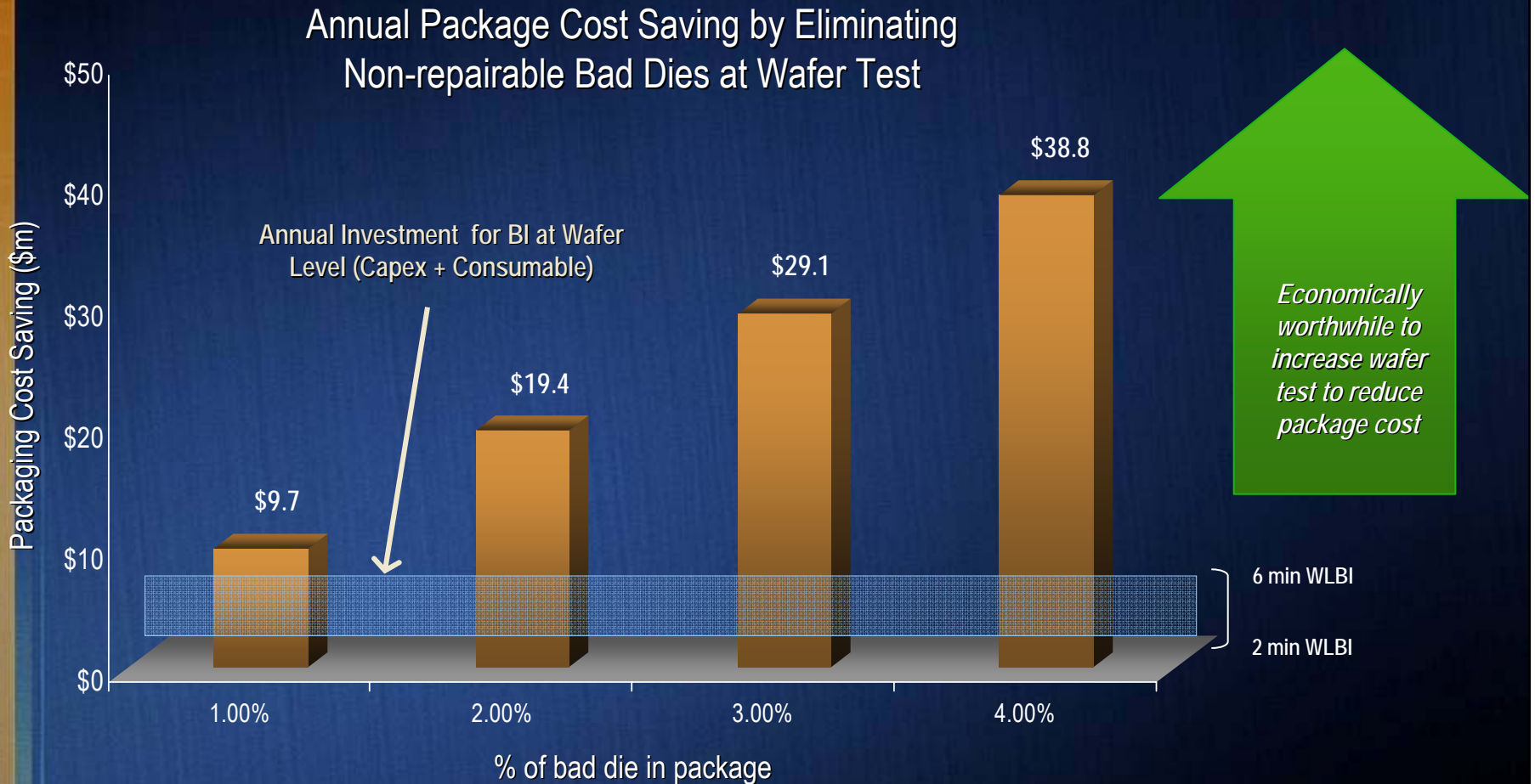
Scenario 1: Reduce Package Cost
Trade-off Questions

Question: But I have to spend more $ on wafer test Capex and probe card. How does it compare to the package cost saving?

Answer is …

Scenario 1: Reduce Package Cost
Packaging Cost Saving vs. Increased Wafer Test Investment

Annual Package Cost Saving by Eliminating Non-repairable Bad Dies at Wafer Test

Packaging Cost Saving ($m)

- $50
- $40
- $38.8
- Annual Investment for BI at Wafer Level (Capex + Consumable)
- $30
- $29.1
- $20
- $19.4
- $10
- $9.7
- $0

1.00%　　2.00%　　3.00%　　4.00%

% of bad die in package

6 min WLBI

2 min WLBI

Economically worthwhile to increase wafer test to reduce package cost

Scenario 2: Reduce WLBI Test Cost
*Introduce High Temp BI at Wafer Level*

Case 2: Add High temperature WLBI to reduce BI cost

- Reduce package BI time
- Detect more early life failures
- Earlier and more data for feedback to Fab

Scenario 2: Reduce WLBI Test Cost
BI Test Cost Reduction

- Decreased total test cost
  - 41% with WLSBI @ 125°C
  - 64% with WLSBI @ 140°C
- Increased yield
  - 2% yield increase after package BI
- Reduced package BI time
  - BI time cut in half with 140°C
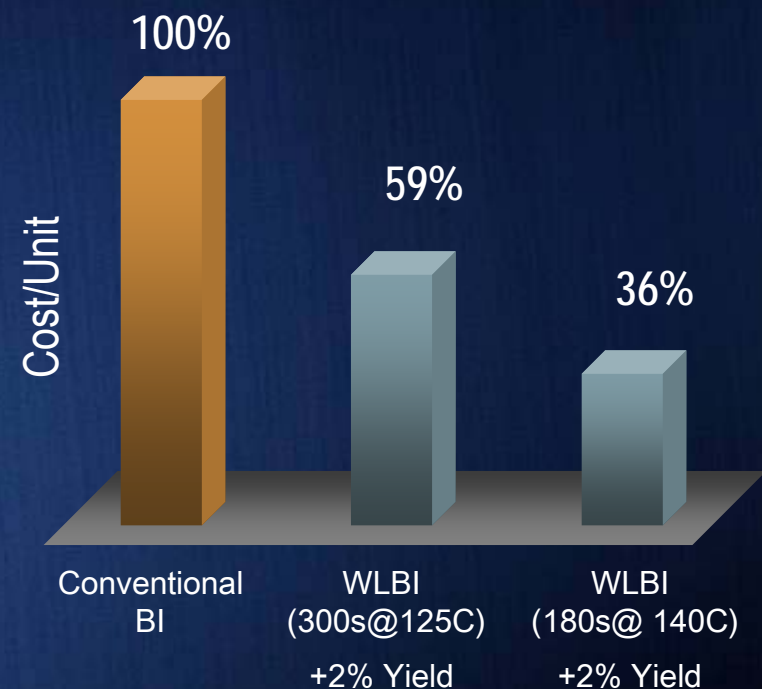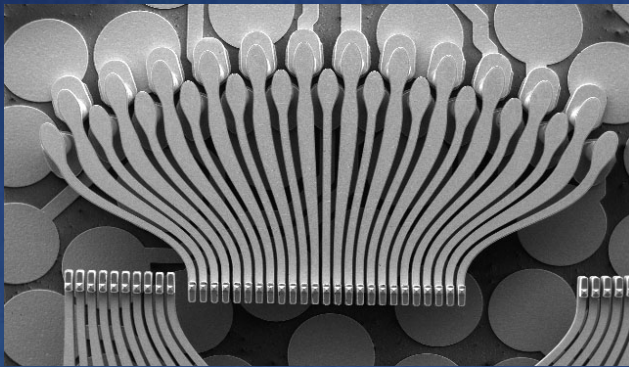
Scenario 2: Reduce WLBI Test Cost
Trade-off Questions

Question: Can the probe card work reliably at high temperature in production environment?
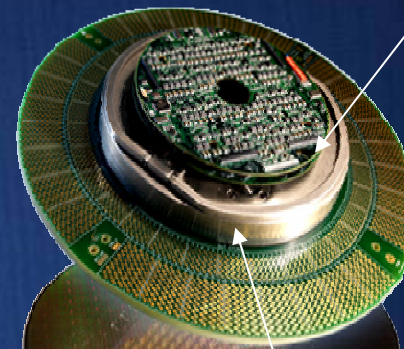
Answer is …

Scenario 2: Reduce WLBI Test Cost
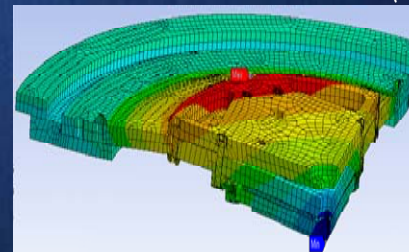## *High Temperature BI Probe Card*

- WLBI probe card needs to be optimized for
  - High temperature
  - High parallelism
  - Low pad damage

MicroSpring™ optimized for tight pitch at high temperature

Selection of high temperature electronic component

FFI proprietary thermally optimized system for stable planarity at high temperature

Scenario 3: Improve Product Yield
Migrate Partial Final Test to Wafer Level

- **Scenario 3: Moving some final test to wafer**
  - Detect and repair more dies to improve product yield
  - Higher probing temperature to replicate final test conditions
  - At speed test to validate device performance
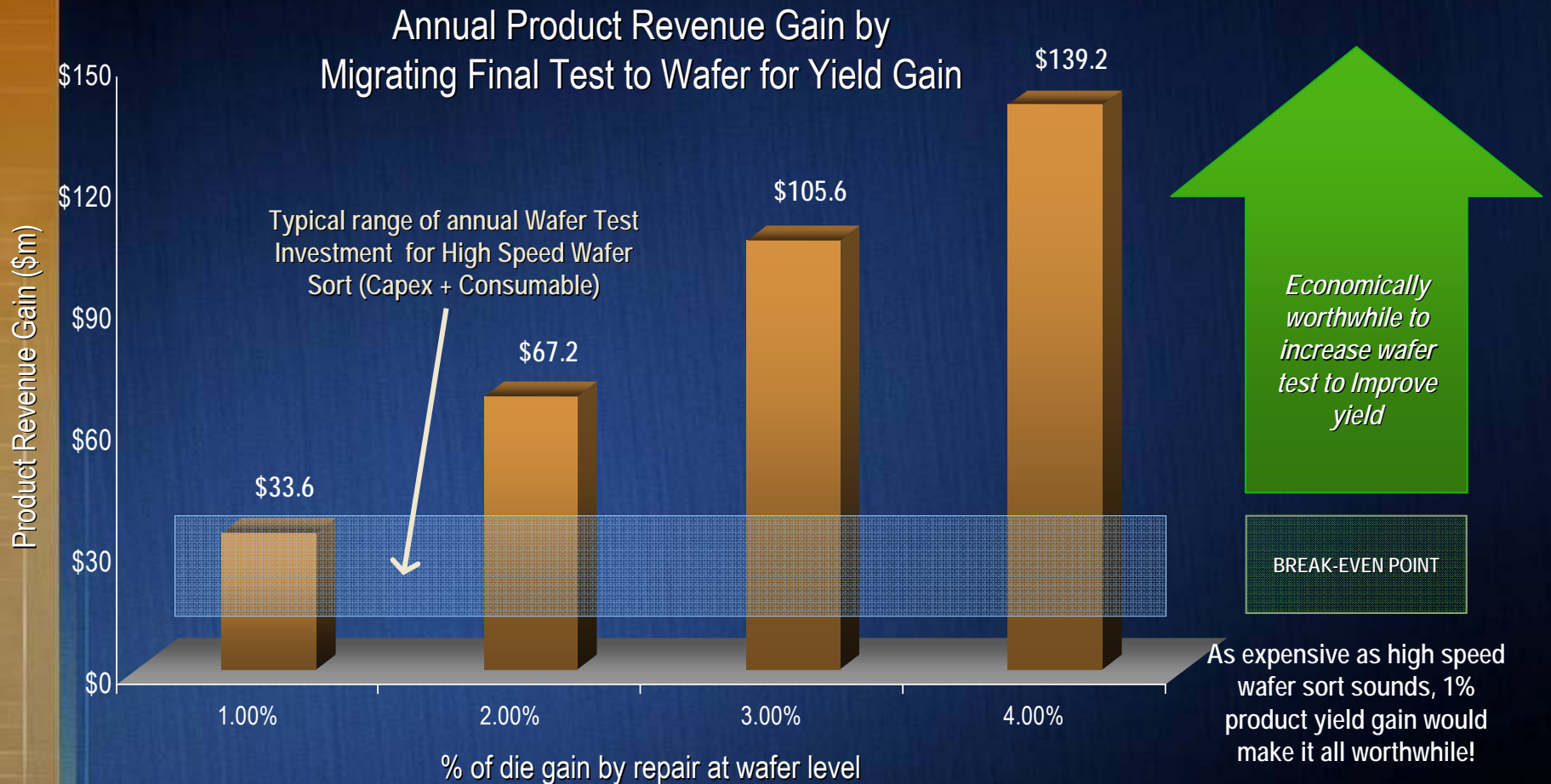
Scenario 3: Improve Product Yield
Trade-off Questions

Question: High speed testers are very expensive. How much yield gain do I need to make it worthwhile?

Answer is …

Scenario 3: Improve Product Yield
Yield Gain vs. Increased Wafer Test Investment

**Annual Product Revenue Gain by
Migrating Final Test to Wafer for Yield Gain**

Product Revenue Gain ($m)

$150

$120

$90

$60

$30

$0

Typical range of annual Wafer Test
Investment for High Speed Wafer
Sort (Capex + Consumable)

$33.6

$67.2

$105.6

$139.2

1.00%   2.00%   3.00%   4.00%

% of die gain by repair at wafer level

*Economically
worthwhile to
increase wafer
test to Improve
yield*

BREAK-EVEN POINT

As expensive as high speed
wafer sort sounds, 1%
product yield gain would
make it all worthwhile!

Scenario 3: Improve Product Yield
Trade-off Questions

Question: Will high frequency sort work in high parallelism?
Where are the limits?

Answer is …

Scenario 3: Improve Product Yield
Trade-off Questions

Question: Will high frequency sort work in high parallelism?
Where are the limits?

- Answer …

    - Simulations look promising

    - FFI has proven expertise on high frequency probing
        - Demonstrated x2 TRE @ 100MHz (SWTW Paper 2004)
        - Demonstrated up to 500MHz for non TRE

    - So there is only one way to find out whether it works: *Try it!*

    - The benefits are there, go for them!

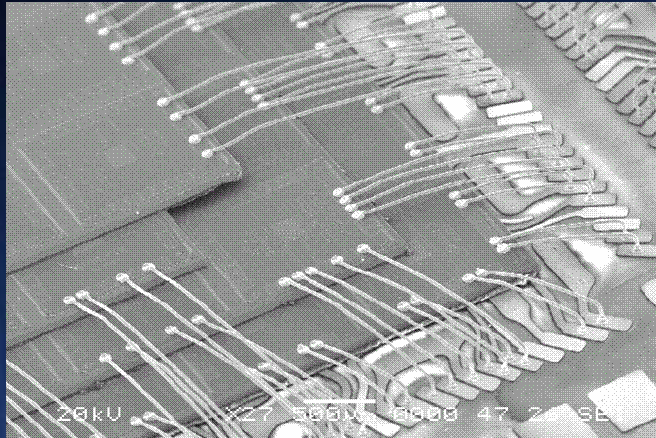# Case Study Summary
Economics Benefits

Annual Product Cost Benefit by Test Flow Optimization

- Scenario 3: Product Revenue Gain
- Scenario 1: Package Cost Saving
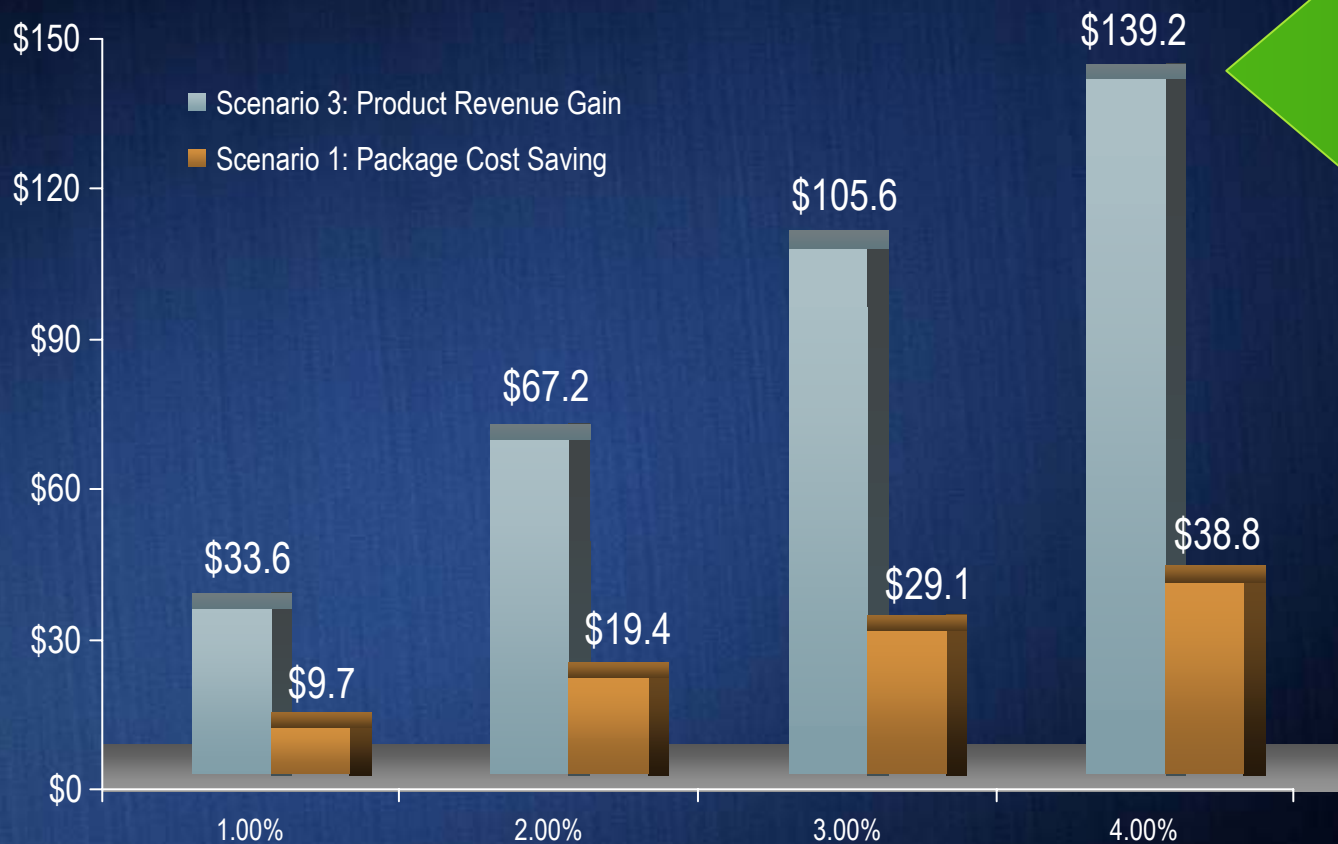
Economically worthwhile if gain > 1% yield difference
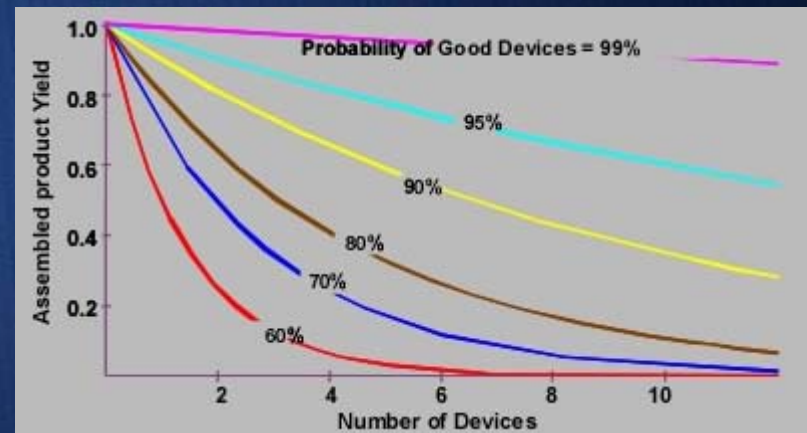
Case Study Summary
Economics Benefits for MCP

Picture of Multi-chip-package (MCP)

- Economic benefits for MCP will be even bigger!
- 1% yield delta for single chip = 5% yield delta for 5-die MCP

MCP Yield Curve vs. Single Die Yield

Conclusions

- Memory device market price pressure calls for test innovation to reduce product cost

- Migrating test upstream can provide earlier feedback for improved yield and down-stream manufacturing cost savings for the non-repairable device on wafer

- The incremental increase in wafer test spending can be easily justified if >1% yield difference is realized

- The benefits are there, go for them!