SWTW

INNOVATION PUT TO THE TEST

TeraProbe

FormFactor®
Advanced Wafer Probe Solutions

26k Probes – A new Dimension in Probe Count

Presenter: Michael Huebner (FormFactor)

San Diego, CA USA June 4th 2007

About this paper

- Joint presentation between Tera Probe and FormFactor
- Authors
  - Yosuke Kawamata – Tera Probe Inc.
  - Shoichi Matsuo – Tera Probe Inc.
  - Satoshi Hatsumori – FormFactor Inc.
  - David Pritzkau – FormFactor Inc.
  - Michael Huebner – FormFactor Inc. (Presenter)

About Tera Probe

Company Profile

Company Name : Tera Probe, Inc.
Major Operations : Wafer & PKG test services
Other test-related businesses and technology development, etc.
Established : August 2005
Capital : 9,600 million-yen

Corporate Mission

To contribute to a better, digitally empowered future by promoting more efficient high-tech development processes and providing top-quality test technologies and services.

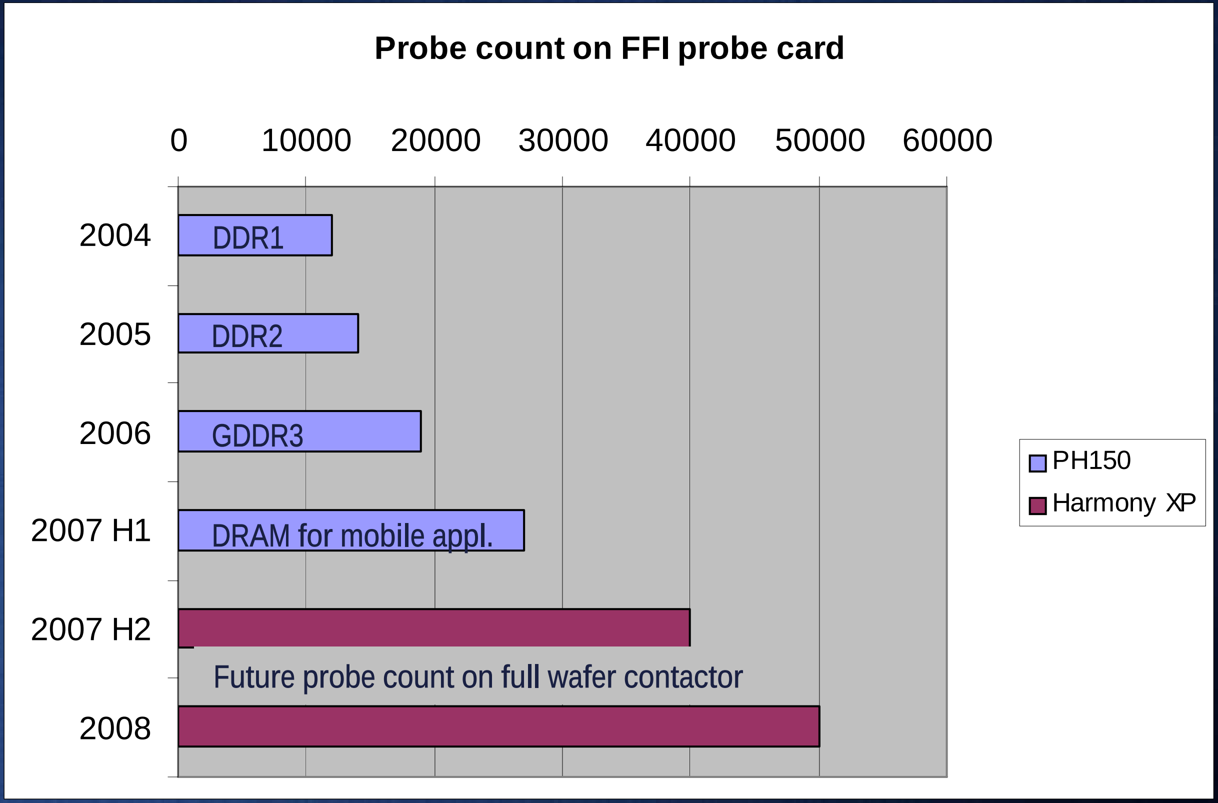
- Innovate advanced technologies and improve mass production techniques based on the most advanced 300 mm wafer probe technologies.
- Provide a wide range of wafer test services.
  (DRAM / SRAM / flash memories / logic devices / SoC (System-on-Chip))
- Offers the services and solution to meet customer's need.

Outline

- First part: Why do you need high probe count?
  - Industry trend: Increasing probe count
  - What is driving probe count?
  - The impact of probe count on power delivery
- Second part: The 26k probe card built for Tera Probe

Industry Probe Count Trend

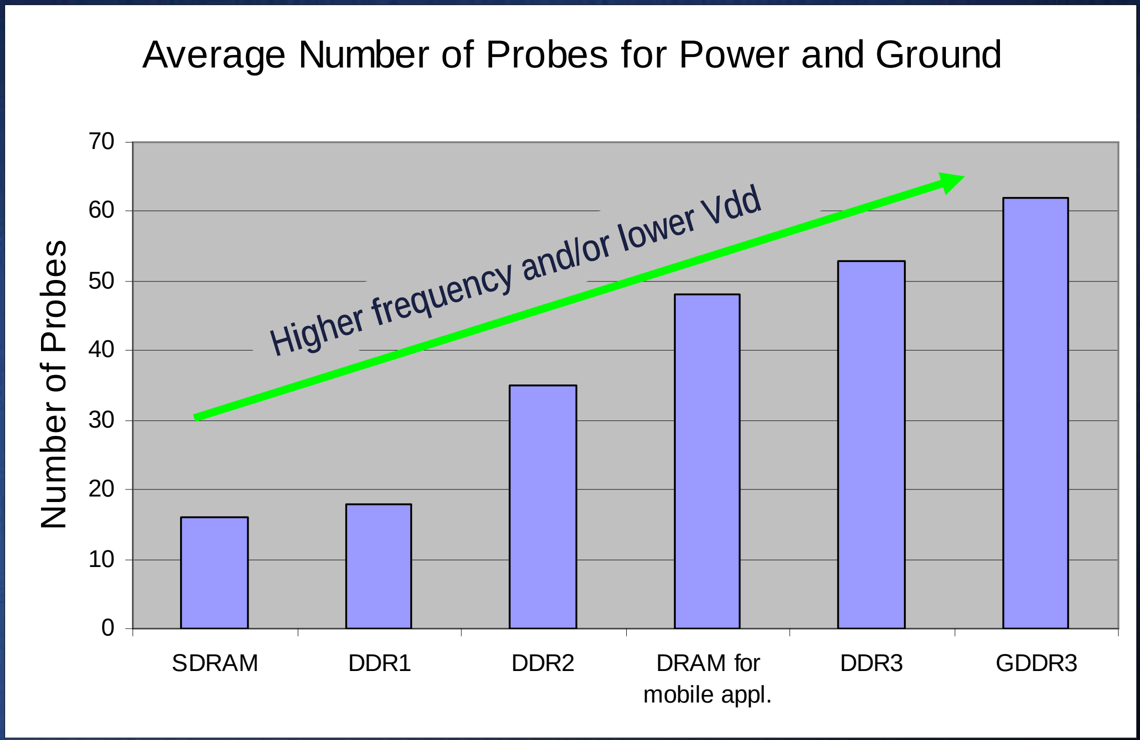
- Total probe count has increased significantly in recent years
- This increase was not driven by increasing parallelism
- However parallelism is expected to increase to 384 DUT and higher
  - This will act as a multiplier on the total probe count leading to 40 - 50k probes



This data is based on FFI's whole customer base

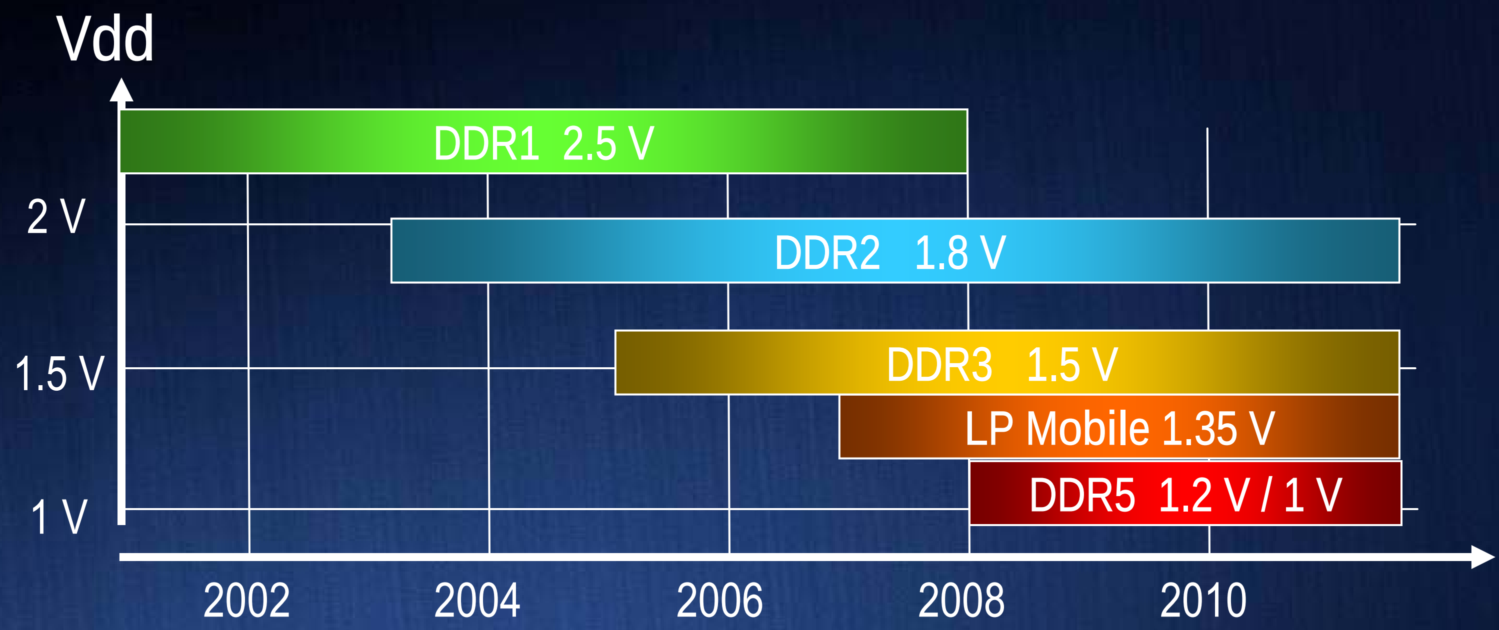
Industry Probe Count Trend

- Number of probes per DUT is increasing
  - Mainly Power and GND – especially VDDQ and VSSQ (Output driver)
  - Number of signals used for high parallel wafer sort has not changed significantly for most applications



This data is based on FFI's whole customer base

DRAM Vdd Trend



This data is based on FFI's whole customer base and JEDEC

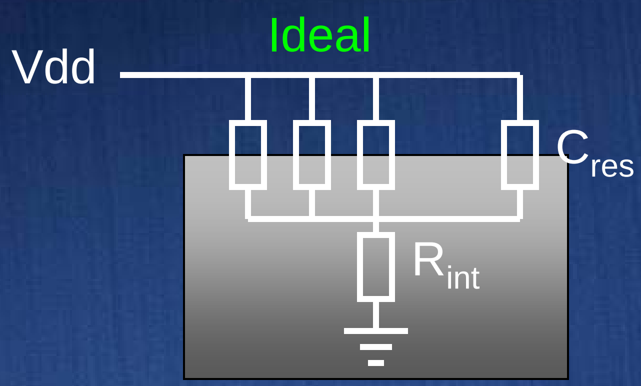
- Vdd is decreasing over time
- V_{IL}/V_{IH} and V_{OL}/V_{OH} decreases - allowable noise margin decreases
- Better probe card is required
  - "Clean" power and ground are becoming more critical

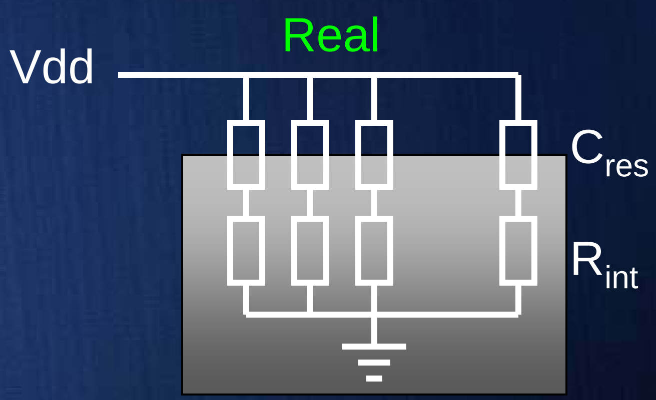
What is a better probe card?

Why do we need more probes for power and ground?

Improved Power Delivery *Static (DC) Case*

- Low and stable Contact Resistance (C_{res}) is a must
- Use all power and ground pads available on the chip
  - $C_{res} = 1/(1/C_{res1} + 1/C_{res2} + \ldots 1/C_{resN})$ - this assumes perfect power distribution on chip
  - In reality some probes carry most of the current
  - Bad contact performance can be compensated by high probe count only to some extent





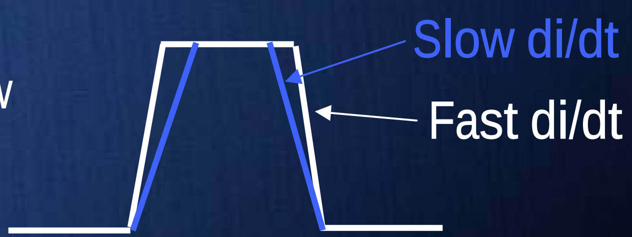
- Voltage drop is function of C_{res} and current: $\Delta V = C_{res} \times I_{dd}$
  - With lower Vdd the tolerable voltage drop ΔV is also decreasing

Need full spring population and low C_{res} on every single probe for best performance

Power Delivery System (PDS) *Dynamic Case*

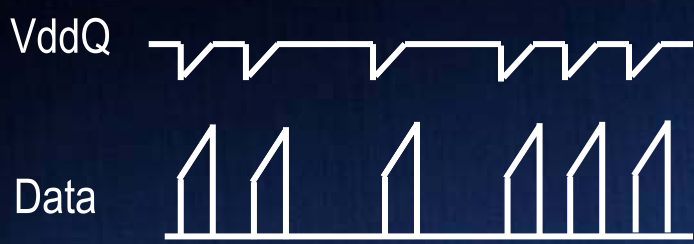
- Transient current from Switching I/Os causes noise
  - Causes ground bounce and Vdd rail collapse (sagging)
    - Transient voltage drop (ripples) across PDS
    - Reduces operating frequency of DUT
- Impedance of PDS needs to be low to minimize this effect
  - Loop inductance and resistance of power and ground paths
  - Keep impedance low over wide frequency range (DC to ~ 3x clock speed)

Faster di/dt (slew rate) requires low impedance at higher frequencies



Running faster devices at low speed will not help because of faster slew rates

Vdd Collapse and Ground Bounce



- Vdd rail collapse occurs because of the non-zero impedance of the power delivery system and I/O switching current. Ground bounce occurs as a consequence due to voltage difference between DUT ground and board ground
  - A channel referenced to DUT ground that is driven to ‘0’ will see a voltage that could be falsely interpreted as a ‘1’
  - PDS impedance must be small to accommodate lower VIH to prevent a false ’1’
  - Same effect occurs with Vdd rail collapse where false ‘0’ may occur

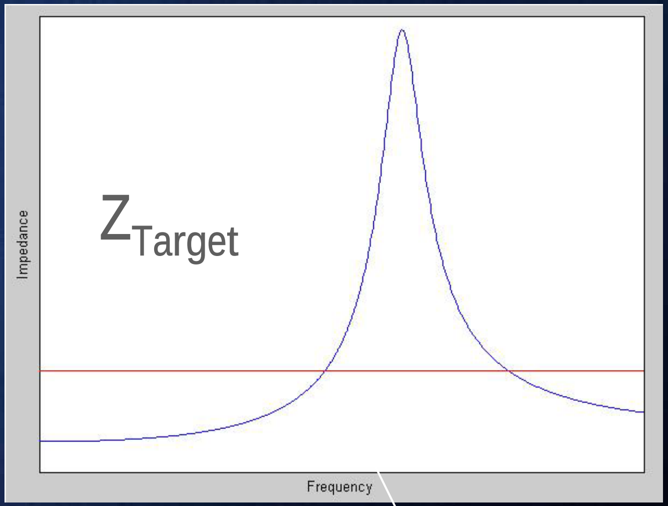
Low PDS impedance necessary to prevent misinterpreted data

Target PDS Impedance

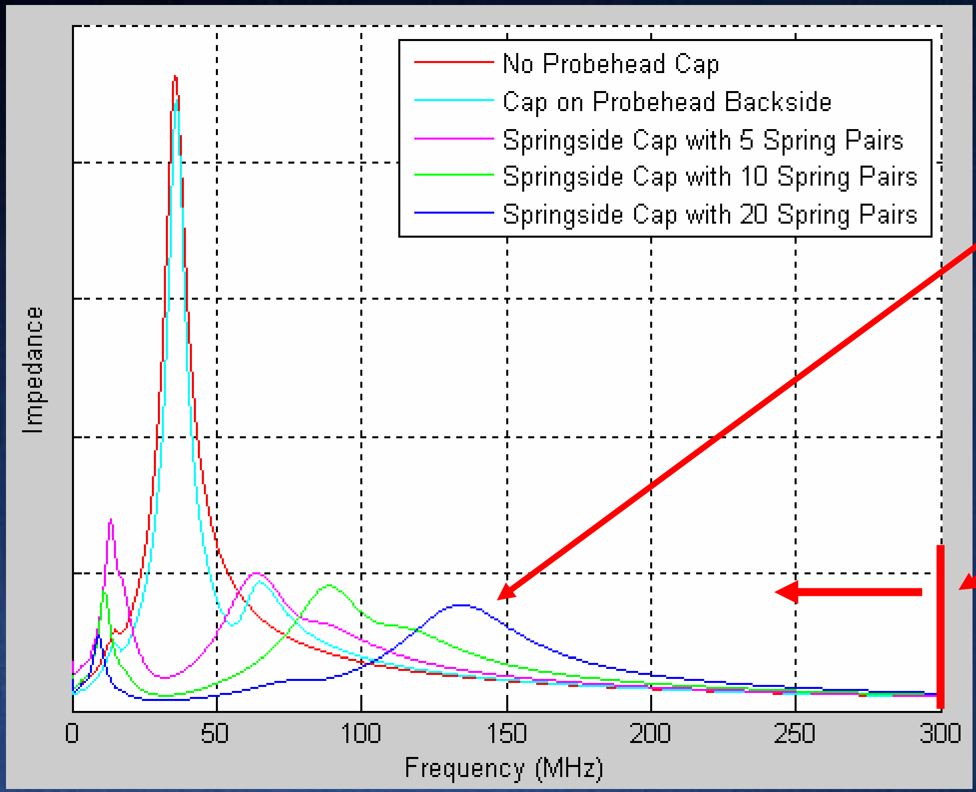
- Impedance of PDS from DUT to source must be lower than some target impedance over desired frequency range
- Which impedance is needed?

$$Z_{\text{Target}} = \frac{\Delta_{\text{ripple}} V_{\text{dd}}}{I_{\text{avg}}}$$

- V_{dd} is the nominal operating voltage (1.5 V)
- I_{avg} is the average device current (250 mA)
- Δ_{ripple} is the allowed percentage ripple (10%)
- $\Delta_{ripple} V_{dd}$ is the allowed ripple voltage (0.15 V)
- $Z_{Target} = 0.6\ \Omega$



PDS Impedance as Function of Probe Count



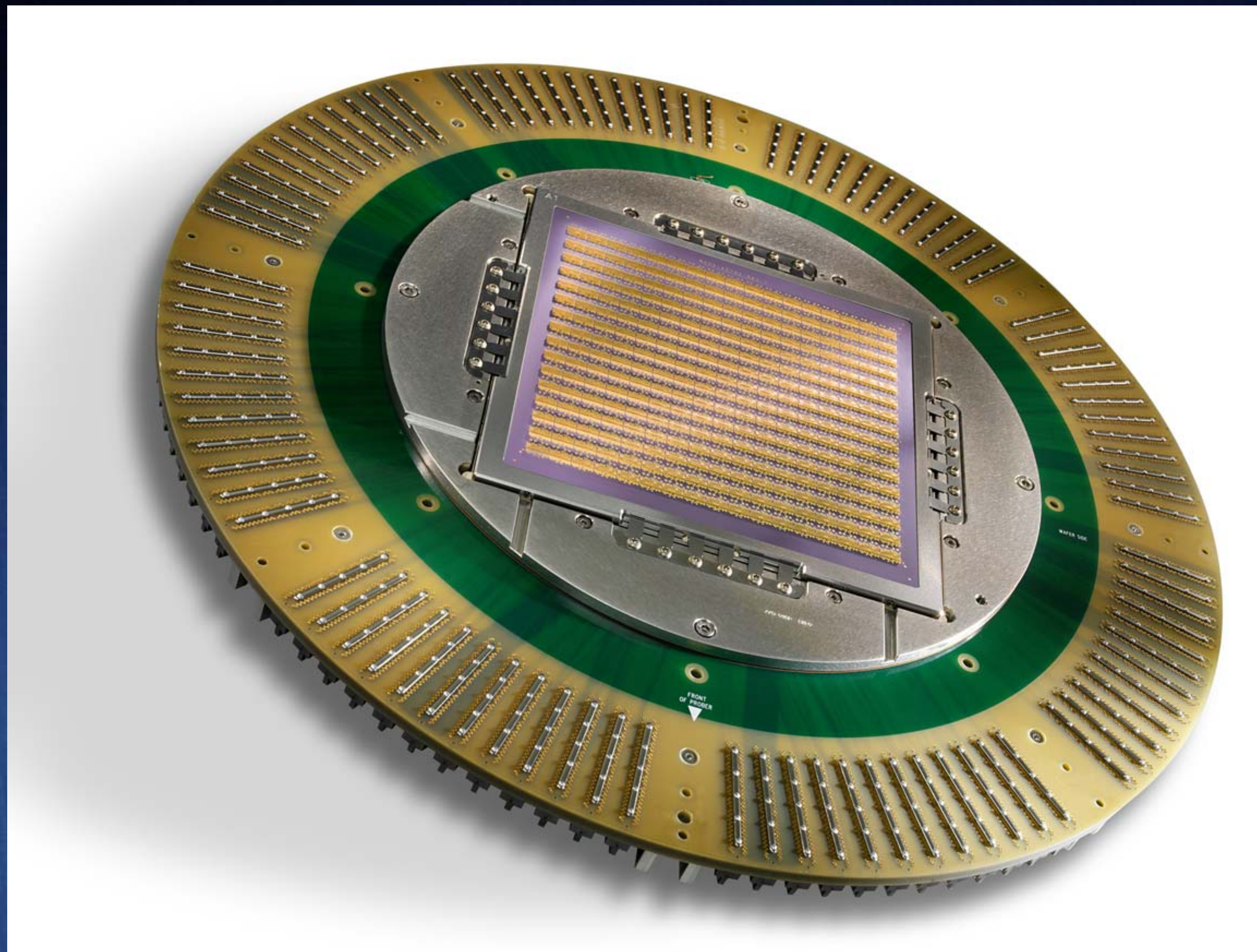
Move resonant peak to higher frequencies out of relevant frequency range

Need low impedance from DC to at least 3x clock frequency

Lowest impedance can be achieved by increasing the probe count

Capacitors close to the DUT have a big impact too

Probe card with 26k probes – PH150XP



Probe card with 26k probes

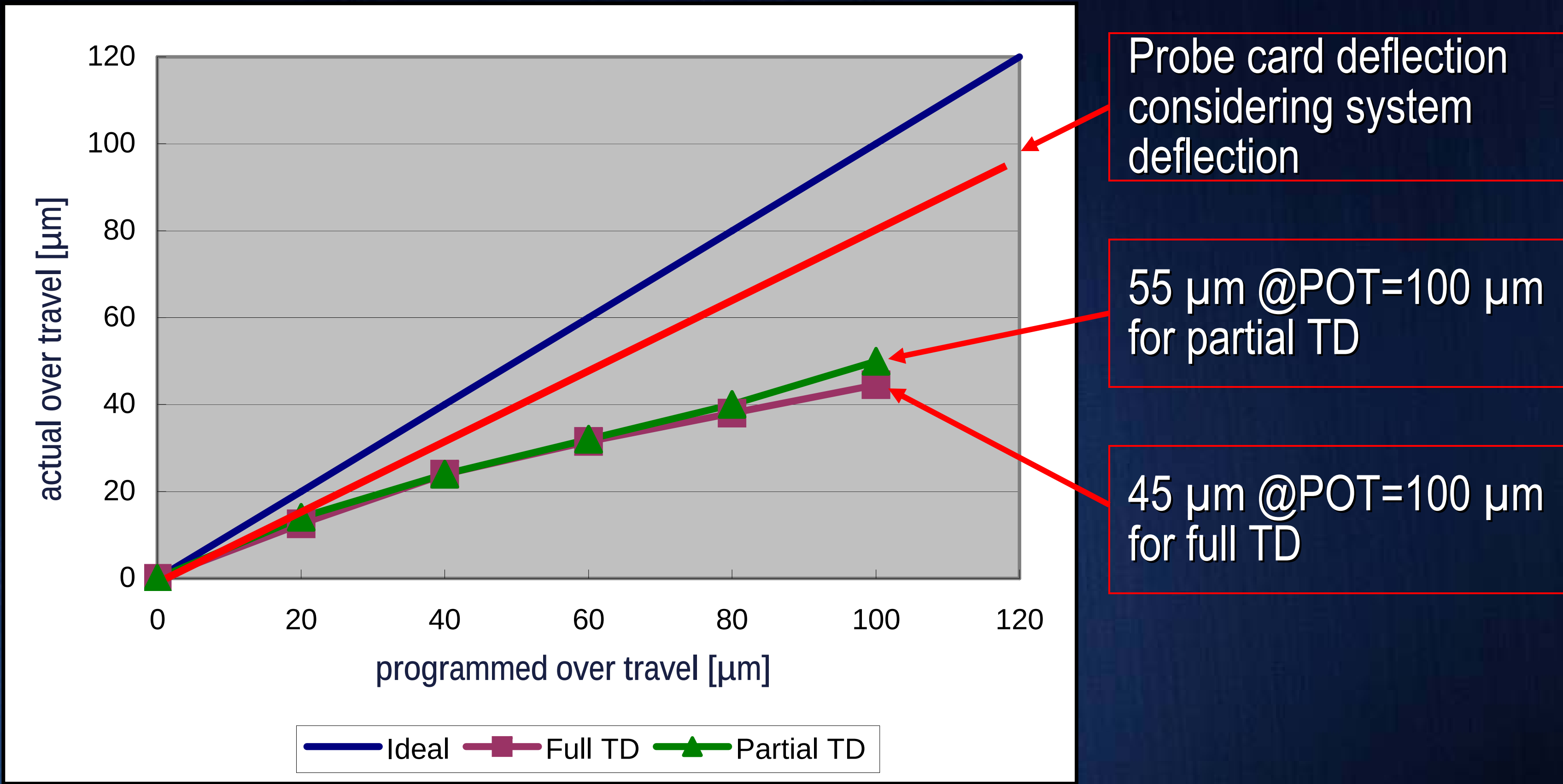
- Probe count = 26,656 probes
- Probing area 150 mm x 150 mm
- Used for test of DRAM for low voltage application

System Deflection

- High probe count probe cards create a significant force which leads to deflection in the whole test cell
  - Deflection of the probe card itself
  - Deflection of the chuck
  - Deflection of the head plate
  - Coupling wafer motherboard and prober head plate

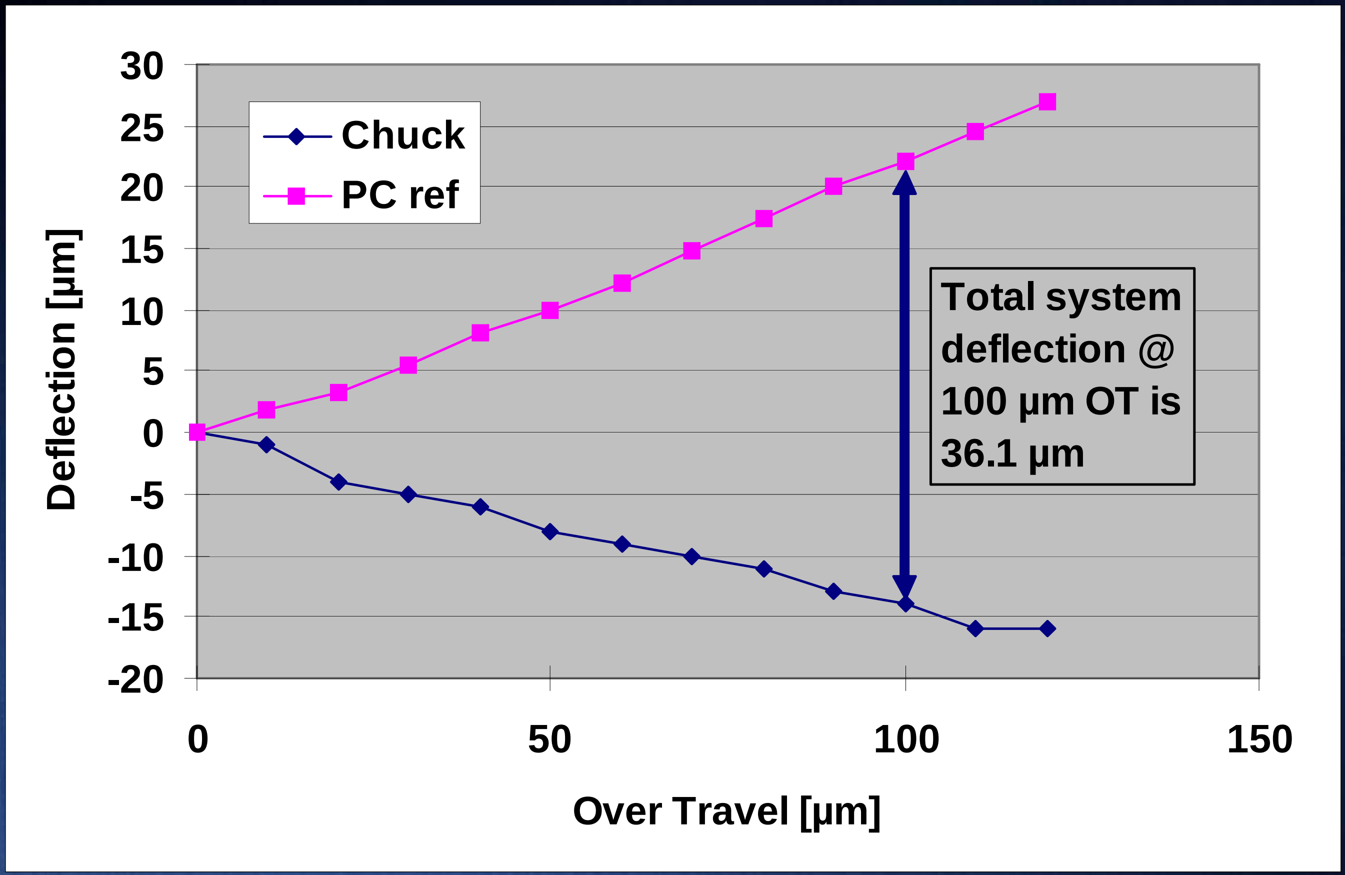
  The return path for the probe force
- How much of the programmed over travel is really achieved on each probe?

System Deflection



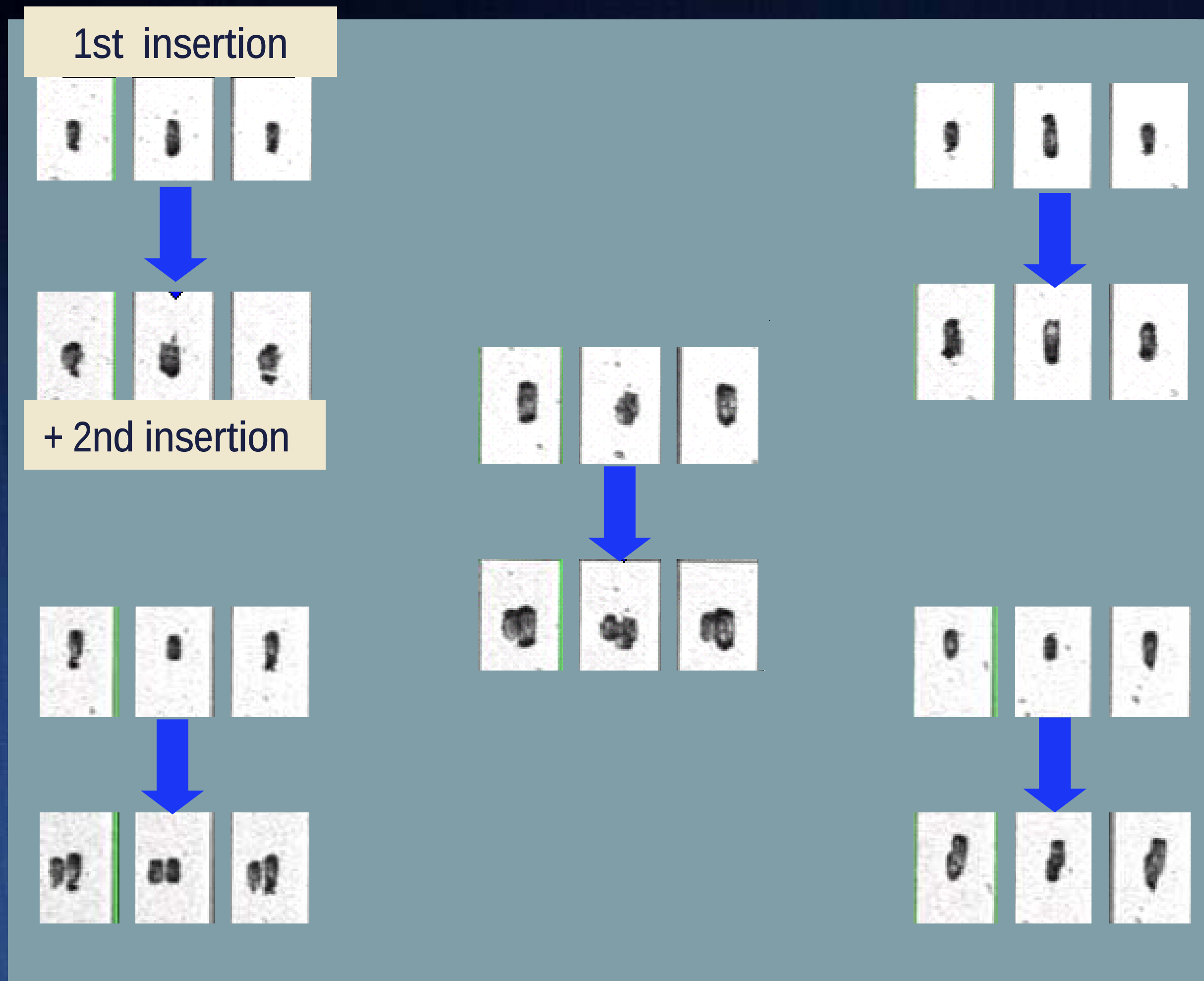
- Actual over travel measured on the test system under production conditions
- Lower deflection on partial touchdowns is caused by ~25% less probes touching down on the wafer in this case

System Deflection



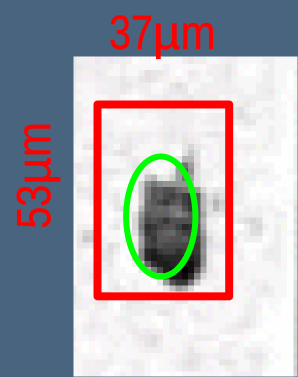
Probe card deflection itself is around 10 to 20 µm

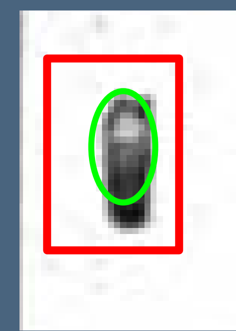
Probe marks on the wafer – Center Touchdown



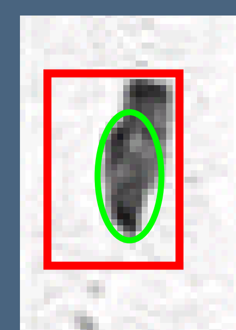
26k probe card was used in the 2nd test insertion

Probe marks on the wafer – Details on Scrub Window



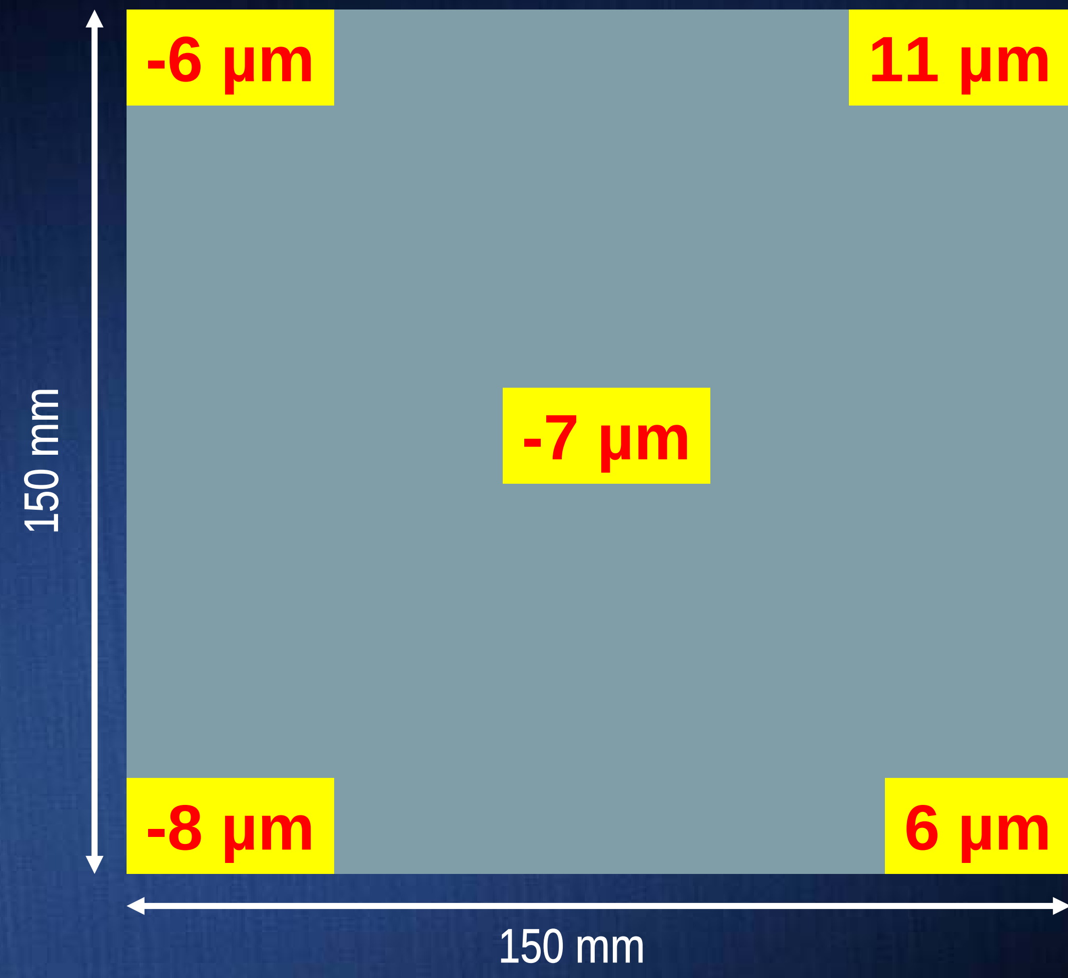


- The scrub window is 37 µm x 53 µm based on 2 test insertions
- Prober setup can be optimized for better probe to pad alignment



Planarity data of the probe card

- Planarity of the card was adjusted to be 19µm (optical measurement)



Probe card with 26k probes - Results

- Shipped to Tera Probe in February 2007
- Successful correlation with lower parallelism and lower probe count probe card
- Used in volume production since March 2007
  - Stable and consistent Yield results
- Other designs with similar probe count are currently built

Summary

- Power delivery is more critical with decreasing supply voltage and higher frequency
- Power delivery can be improved by increasing probe count

- Shipped first probe card with probe count more than 26k – in use at the customer

- Proven ability to build 26k+ probes on 150 mm x 150 mm area
- Enables 50 – 60k probes on 300 mm area contactor (Harmony XP)
  - Needed in the near future with increasing parallelism which comes with new tester platforms and/or new test strategies

Acknowledgements

Special thanks' to:

- Masahide Ozawa and Hiroyuki Koike (TeraProbe)
- Nick Sporck, Sunil Wijeyesekera, Brian Carpenter, Kaoru Nemoto, Toshiaki Katoh, Tetsuya Miyoshi (FormFactor)
- Many others at TeraProbe and FormFactor
- ACCRETECH for their support during the installation