IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Revolutionary new C4 Wafer test probing technologies

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Outline

- Motivation for looking at new technologies
  - Technical wall
  - Commercial wall
- Process of finding/developing new technologies
  - Next Generation Supplier Investigation Strategy
- Feedback to the C4 wafer test probe card industry
- Successful solutions for next generation C4 wafer test needs
- Key characteristics of the successful wafer test solutions
- Summary

Why we needed to find new alternative technologies

Next generation requirements extend past current capabilities.

Pitch → 175um ⟶ X

Cu Bump Φ →105um ⟶ X

- Tighter scrub control capability
- Tighter alignment and scrub variance control

Parallel Sort → 2x ⟶ X

- Large array size
- High probe count (beyond 5000)

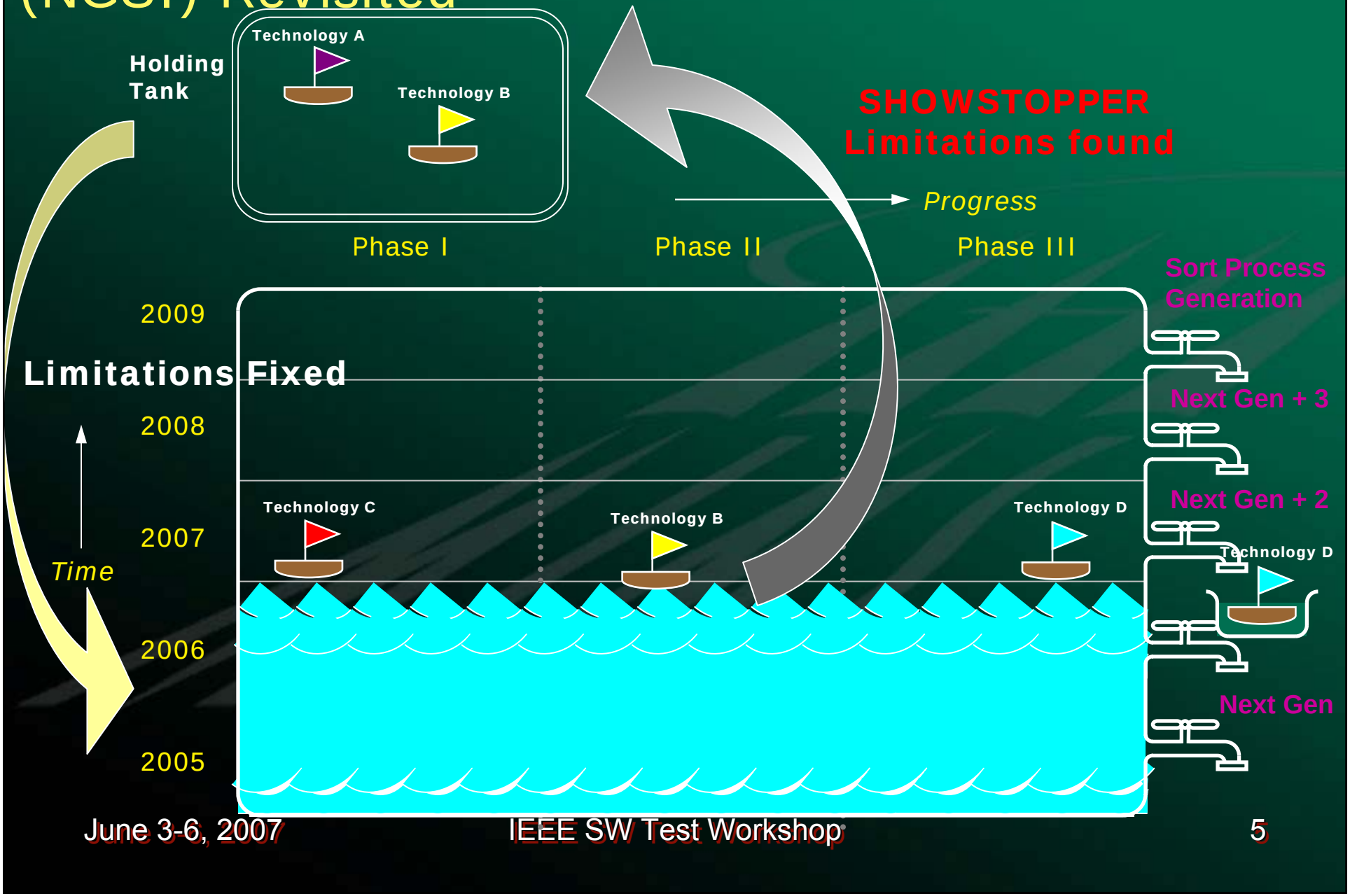
Bottom Line: Intel's current probe card suppliers cannot meet next generation technical requirements.

Why we needed to find new alternative technologies

- **Current technologies bound to high cost**
  - Manufacturing process is Labor intensive
  - Manufacturing Process highly complex
  - Cost scales with probe count
    - Limits the ability to extend to parallel sort

Bottom line: Probe card cost is the key limiter to Intel's wafer test process cost reduction capability.

Next Generation Supplier Investigation (NGSI) Revisited

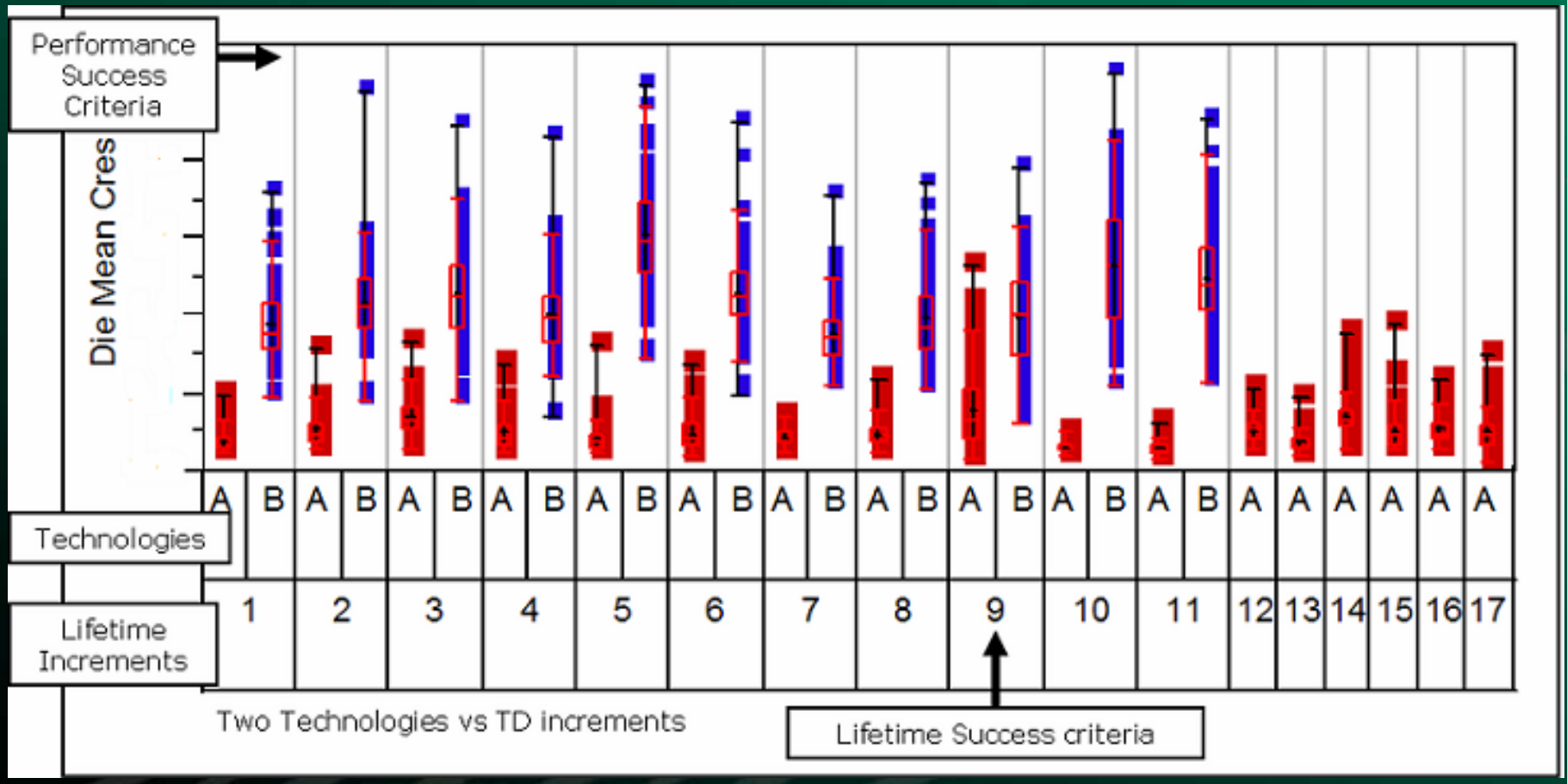


A lot of amazing innovation happening in the probe card industry!!

- **Investigated multiple new unique probing technologies.**
  - Leveraging their core competency and experience.
  - Worked closely with Intel to develop around limitations found
  - **Most solutions have not gone public**
    - **Cannot show the great achievements of these companies.**
- **Most technologies did not meet our NG requirements.**
  - Many fell out to focus on other business applications.
  - Some still need further development to intercept our process requirements.

Many new probing technologies coming soon!

Two capable new technologies found!!

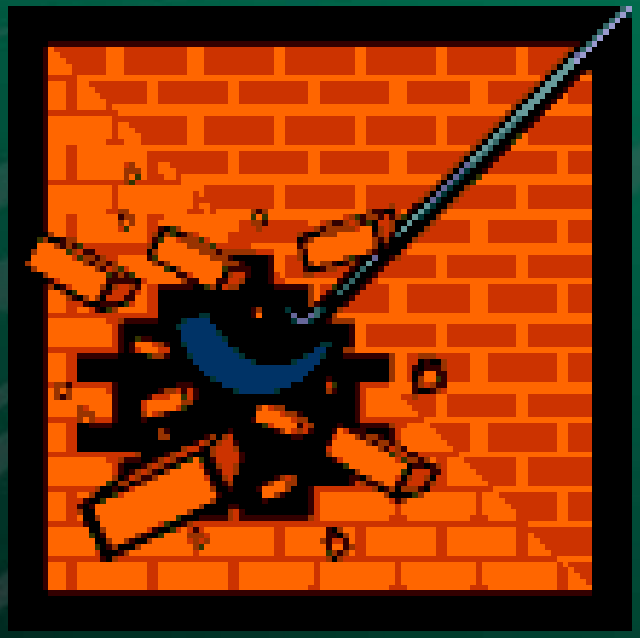


- Lifetime results on two technologies with NG wafer reqs shows proof of concept for these new technologies capable of next generation needs.

Technical Wall Broken

Able to meet critical parameters:

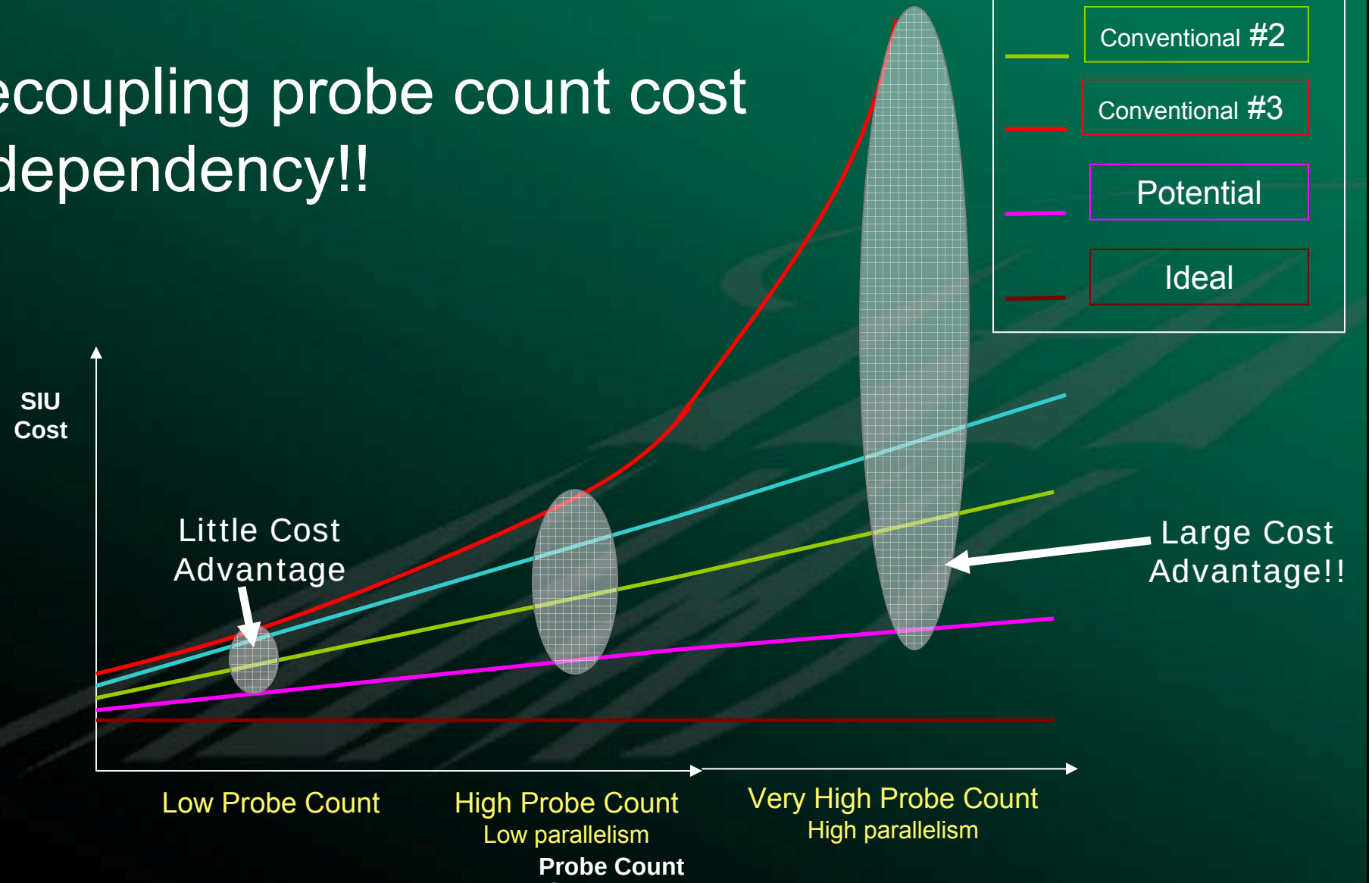
- Reduce pitch (beyond 175um)
- Reduce bump diameter (beyond 100um)
- Parallel sort (beyond 2x)
- Not compromising on other key requirements
  - Current carrying capability
  - Probe Force
  - Inductance
  - Cres Stability
  - Lifetime



- Scalable beyond next generation
  - Not just passed the technical wall but leaps and bounds over the wall for critical requirements.

Commercial wall broken

Decoupling probe count cost dependency!!



Probe Characteristics that could break the walls.

- Simple probe geometry
  - Low cost mfg
  - Easy to trouble shoot
- Probe Designed for Simple prober integration
  - Provides simple robust performance
  - Facilitates process development and troubleshooting
- Lithography manufacturing process
  - Batch process mfg reduce probe cost
  - Tight control of probe geometries to control key probe specs

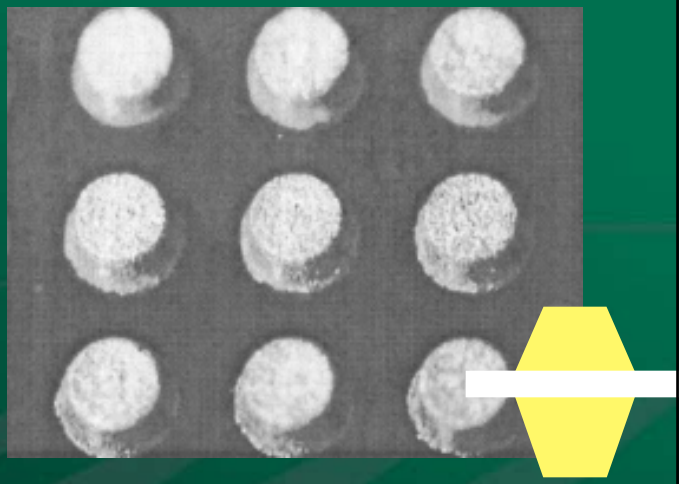


*Figure 1. Elastomer Buttons

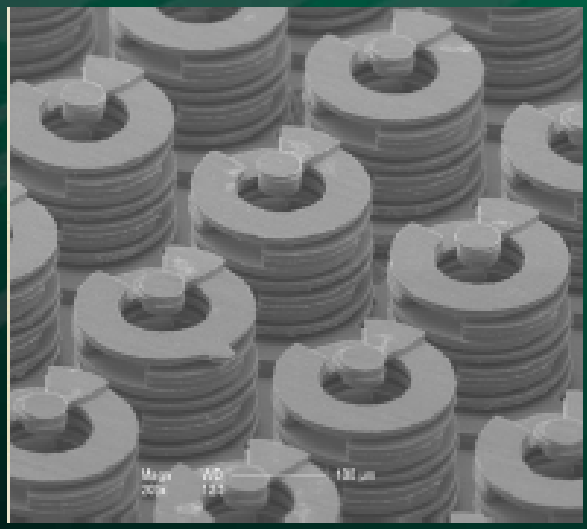


*Figure 1. Probes manufactured through EFAB™ Micro-Fabrication process

* See Reference in back for Figure 1 and 2.

Summary

- NGSI methodology used successfully
- Many innovative solution emerging in C4 wafer test probe card industry
  - Exciting time for C4 wafer test solutions!
- Proof of concept demonstrated to overcome technical and commercial walls.
  - Need to further develop for high volume capability

The Revolution has begun . . .

References

- Swart, R and Caughey, E; “New Pathfinding and Supplier Investigation Strategy”; Intel Corporation; Semiconductor Wafer Test Workshop; June 2007
- Bang, C and Vandelli, N; “Vertical Micro-probe Design Based on the EFAB ™ Micro-Fabrication Process”; MEMGen Corporation; Southwest Test Workshop; June 2003
- Xie, J; Hillman, C; Sandborn, P; Pecht, M. G.; Hassanzadeh, A; DeDonato; Assessing the Operating Reliability of Land Grid Array Elastomer Sockets; IEEE Transactions on Components and Packaging Technologies. Vol. 23, NO. 1, March 2000