IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

Andrei Berar
NanoNexus, Inc.

Advanced Probe Card Technology Enables High Speed, High Parallelism Wafer Test

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Overview

- Problem statement
- Underlying technology
- Electrical characterization
- Value Added
- Summary

Note: Measurements developed in collaboration with GigaTest Labs.

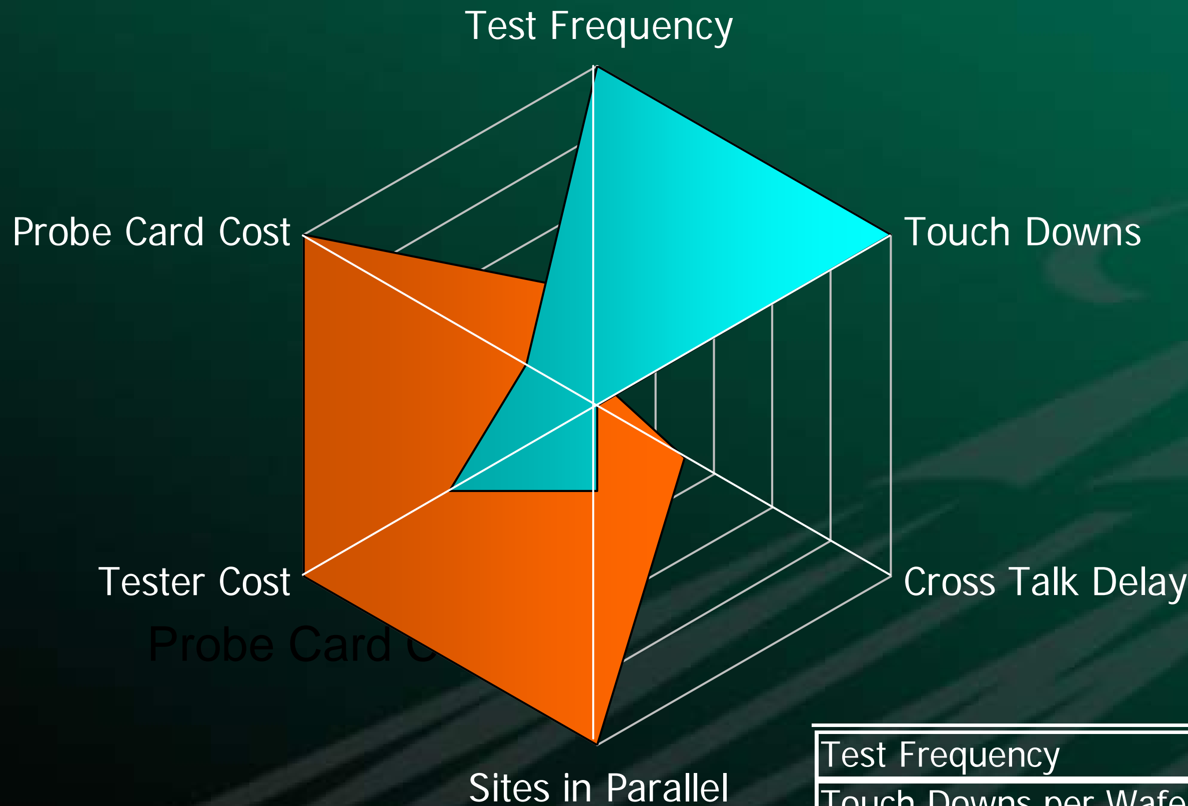
Problem Statement

Portable Consumer Device market is one of the fastest growing with a diverse portfolio of applications (PSRAM, SRAM, DSP, etc.) having fundamental test challenges that are

Limited by Probe Card Technology

• High Frequency @ High Parallelism	> 500 MHz
• Cost effective parallelism	Saturate test cell channels
• Shrinking geometries	< 50 μm pad pitch
• Short manufacturing lead time	< 45 days
• Fast ramp to production	

High Speed vs. High Parallelism



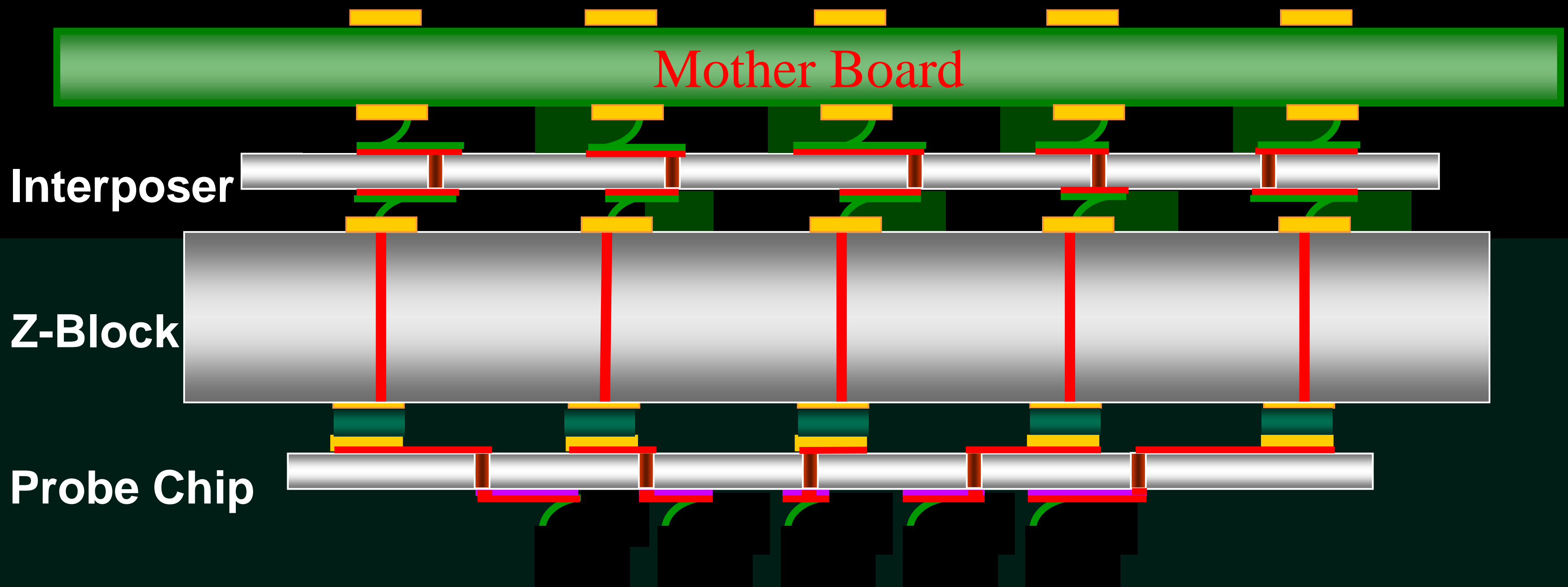
	Case 1	Case 2
Test Frequency	133 MHz	500 MHz
Touch Downs per Wafer	4	16
Cross Talk Delay	0.3 ms	0
Sites in Parallel	256	64
Tester Cost	$ 3 M	$ 1.5 M
Probe Card Cost	$ 250 K	$ 60 K

Relative Test Cost
Speed vs. Parallelism

	Case 1	Case 2
Frequency	133	500
Touchdowns	4	16
Test cell Cost	$3.5M	$1.85M
Stepping time	1.2s	4.8s
Test time/TD	240s	63.8s
Parallelism	256	64
Relative test cost	2.05	1

Lower total test cost with the added benefit of speed sort at probe

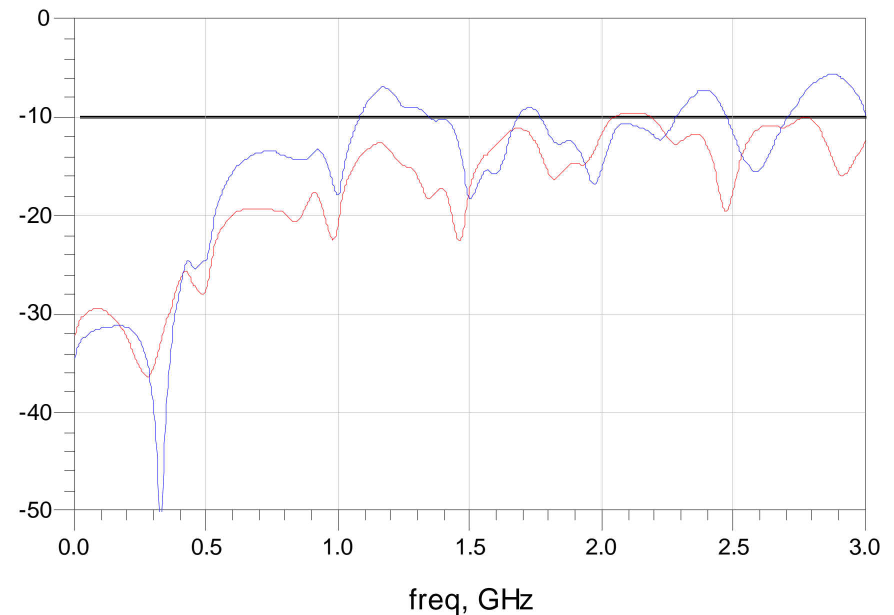
Underlying Technology



Testing Set-up

- GTL – 5050 2-sided probe station
- Agilent – 8735E Network Analyzer
- GTL – 20 GHz coaxial cables
- GGB ECP18-GS/SG-750-DP-75 probes
- GGS CS-11 calibration substrate
- GGB CK-11750 SOLT calibration kit

PC 1 – Electrical Characterization

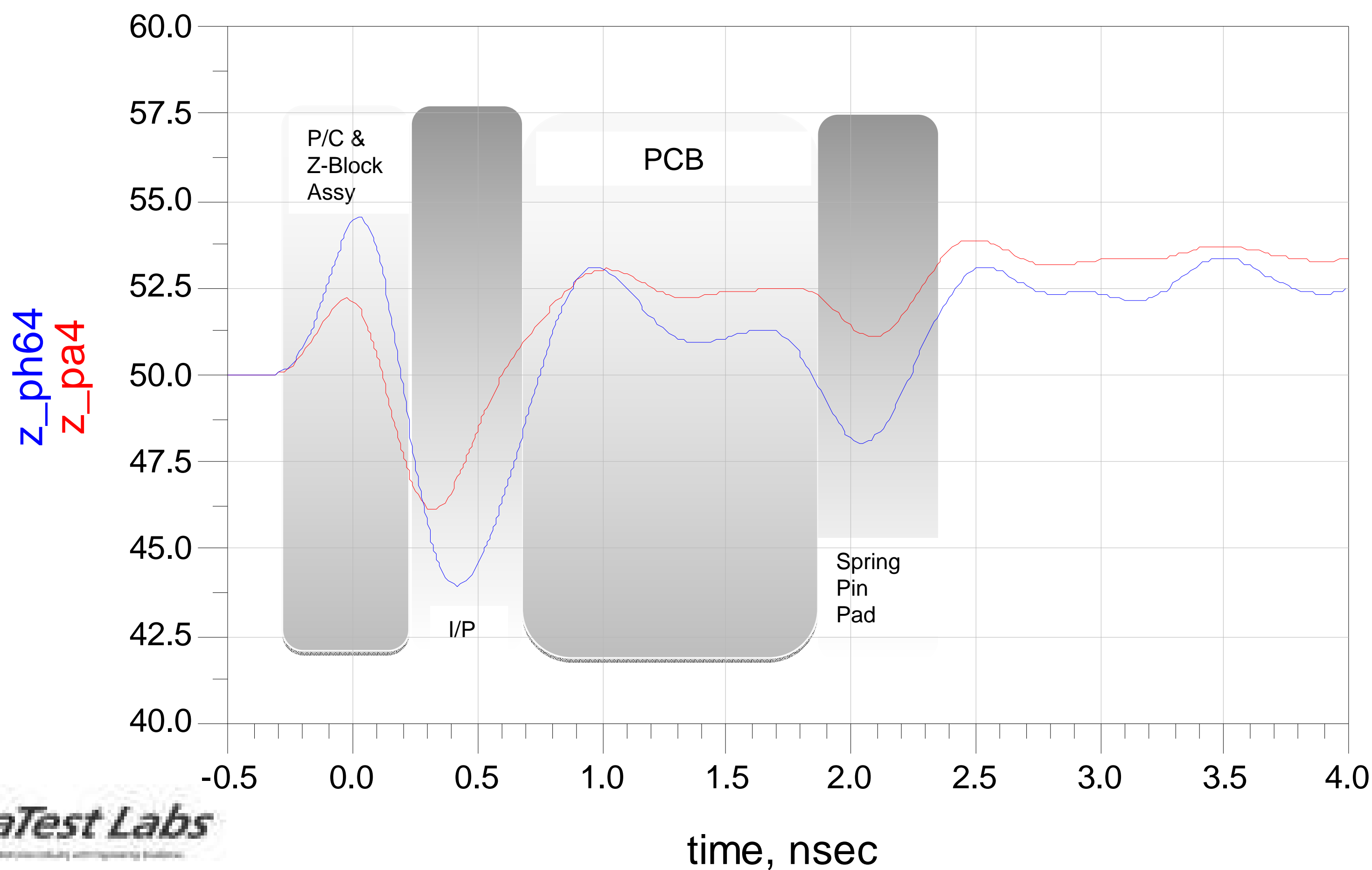


Probe Card Configuration:

Site in Parallel = 16 sites
Pitch = 60 μm
Total Number of Pins = 944

PC 1 – Impedance Profile

Tr=333ps (10-90%)



GigaTest Labs

PC 1 – Model Fit

S-PARAMETERS

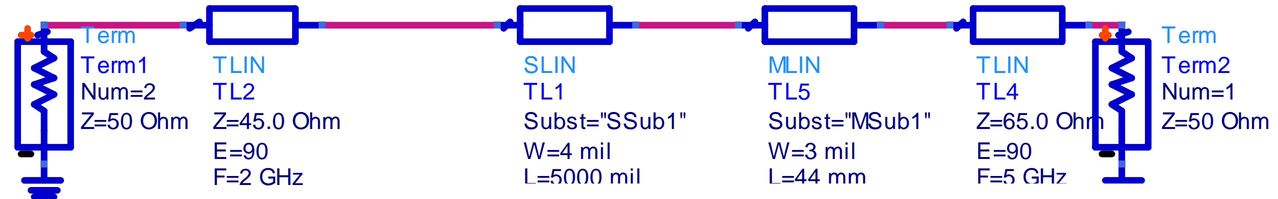
S_Param
SP1
Start=3.75 MHz
Stop=3.00375 GHz
Step=3.75 MHz

MSub

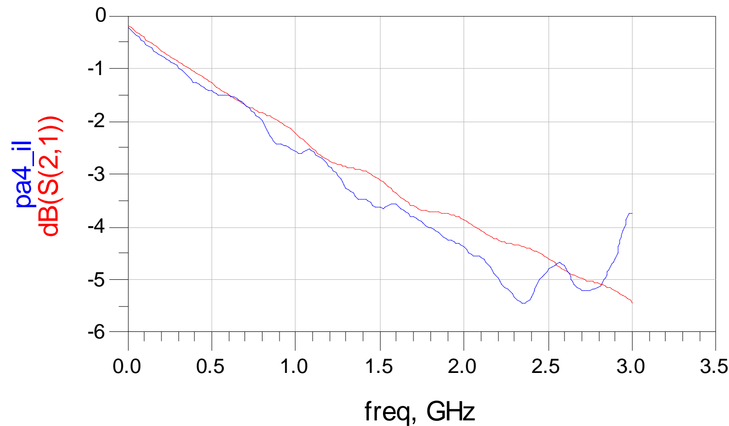
MSUB
MSub1
H=(0.75*1.6) mil
Er=3.2
Mur=1
Cond=5e7
Hu=3.9e+034 mil
T=0.7 mil
TanD=0.035
Rough=0.07 mil

SSub

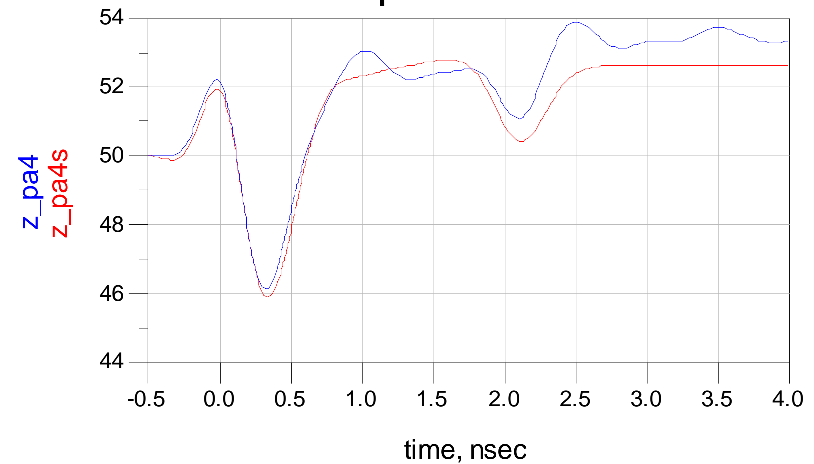
SSUB
SSub1
Er=2.8
Mur=1
B=8 mil
T=0.7 mil
Cond=5e7
TanD=0.035



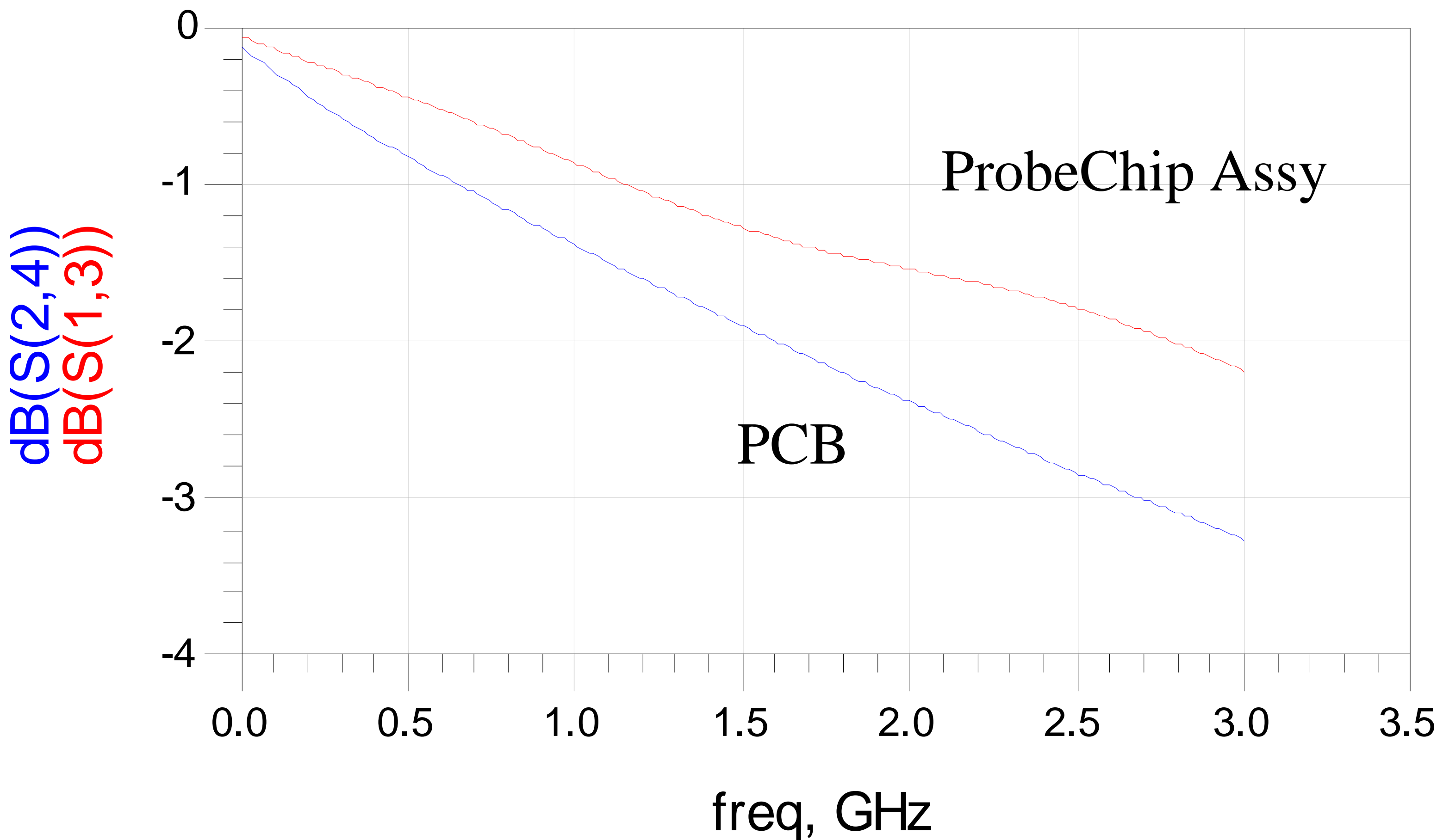
Insertion Loss



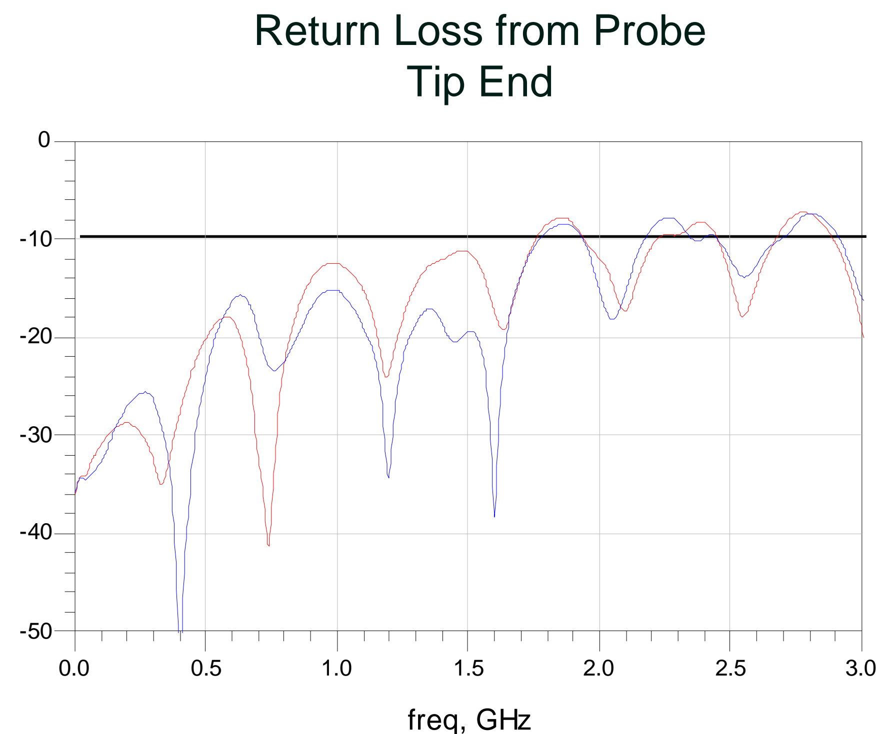
Impedance Profile



PC 1 - Relative Losses



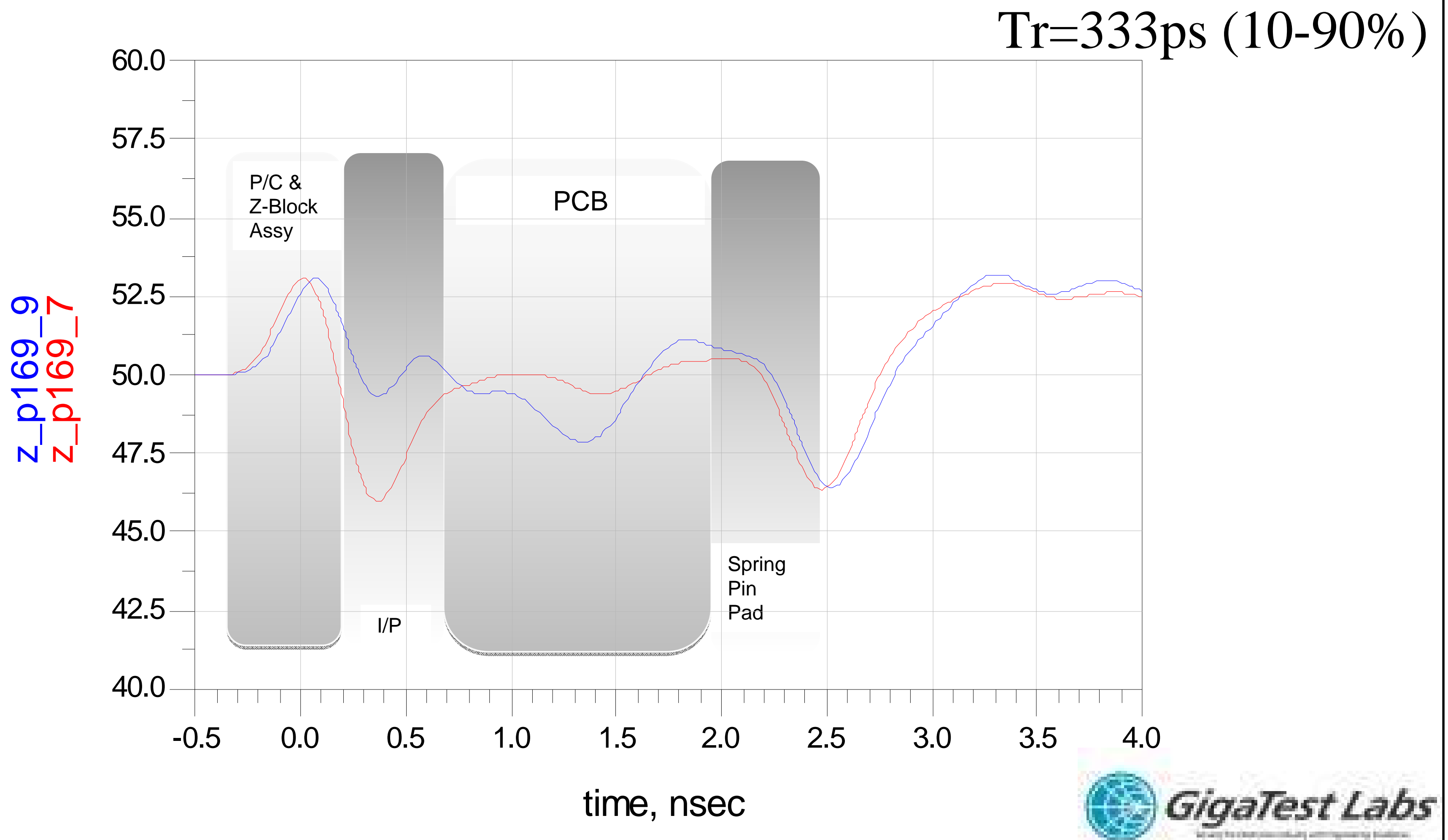
PC 2 – Electrical Characterization



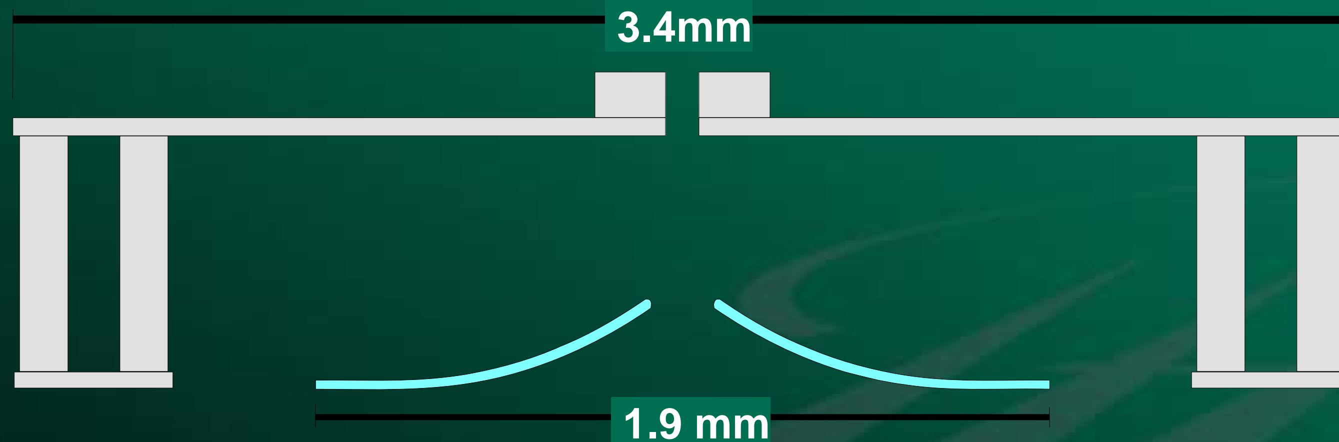
Probe Card Configuration:

Site in Parallel = 72 sites
Pitch = 65 μm
Device Pins = 6,912

PC 2 – Impedance Profile



Self Assembled nanoContactors©



Individually Assembled MEMS

Contactors

- Scalability
  - Lower trace impedance allows higher frequency
- Reduced Cycle times
  - Architecture allows standard components
- Cost Effective
  - Simple 2-D structure, built using standard IC processing, self-assembles for 3-D contactor

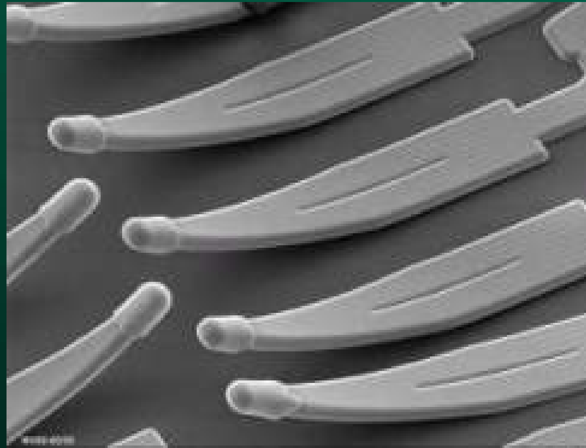
Tunable & Scalable Technology

Pad Size & Pad Pitch

- Smaller scrub window
  - Tighter lithography X & Y tolerance
  - Tighter Y window w/ improved planarity because of reduced OD
  - Scalable tip size

Active Area / Parallelism

- Larger active area
  - Larger substrates & scale "front end" process
  - Tiling for whole wafer
- Increased signal count
  - Escape technology
  - PCB



Frequency / Switching Noise

- Short paths
  - Low inductance
  - Direct path to controlled impedance
- Close coupled components
  - Active or passive components on back of ProbeChip

Force

Pad Material

- Al: 10 gF
- Cu: < Al
- Au: ~0.1gf
- ITO: ~0.1gF
- Solder: variable

Today's Technology

- 30,400 contactors per probe chip
- Pitch < 60 μm
- Probe chip & Z-Block impedance ~ 50 Ω
- Probe chip & Z block + Interposer impedance ~ 50 Ω
- Probe chip & Z block + Interposer + PCB impedance averages 50 Ω ± 10 %

Multi-sites (32 / 64 / 128) tested at speed (>1GHz)

Tomorrow's Requirements

Immediate Benefits

- Cost effective Known Good-Die testing
  - Optimized multi-sites (>128) at speed (> 500 MHz)
  - Saturate channels of existing high frequency testers
- Fine pitch (< 60 μm)
- Rapid cycle time
  - Cycle time less than first silicon cycle time
  - Available for Engineering evaluation
  - Minimize inventory
- High cycle life (> 2,000,000 TDs)
- Maintenance benefits of advanced probe cards