IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Multi-Site Probing for Consumer RF Applications

CASCADE® MICROTECH

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Outline

- Introduction / Background
- Objectives / Goal
- Methods / Materials / Procedure
- Results / Relevant Findings / Key Data
- Discussion of Results / Strengths / Weaknesses, etc.
- Summary / Conclusion

Introduction / Background

- What makes the world go around?
  - In school, we are taught that it is gravity

$$F = G\frac{m_1 m_2}{r^2}$$

- What *really* makes the world go around?
  - In business, we learn that it is money
- Apply this to test of RF devices
  - Implement multi-DUT testing to lower cost
  - Improve yield at later steps with KGD testing

Objectives/Goal

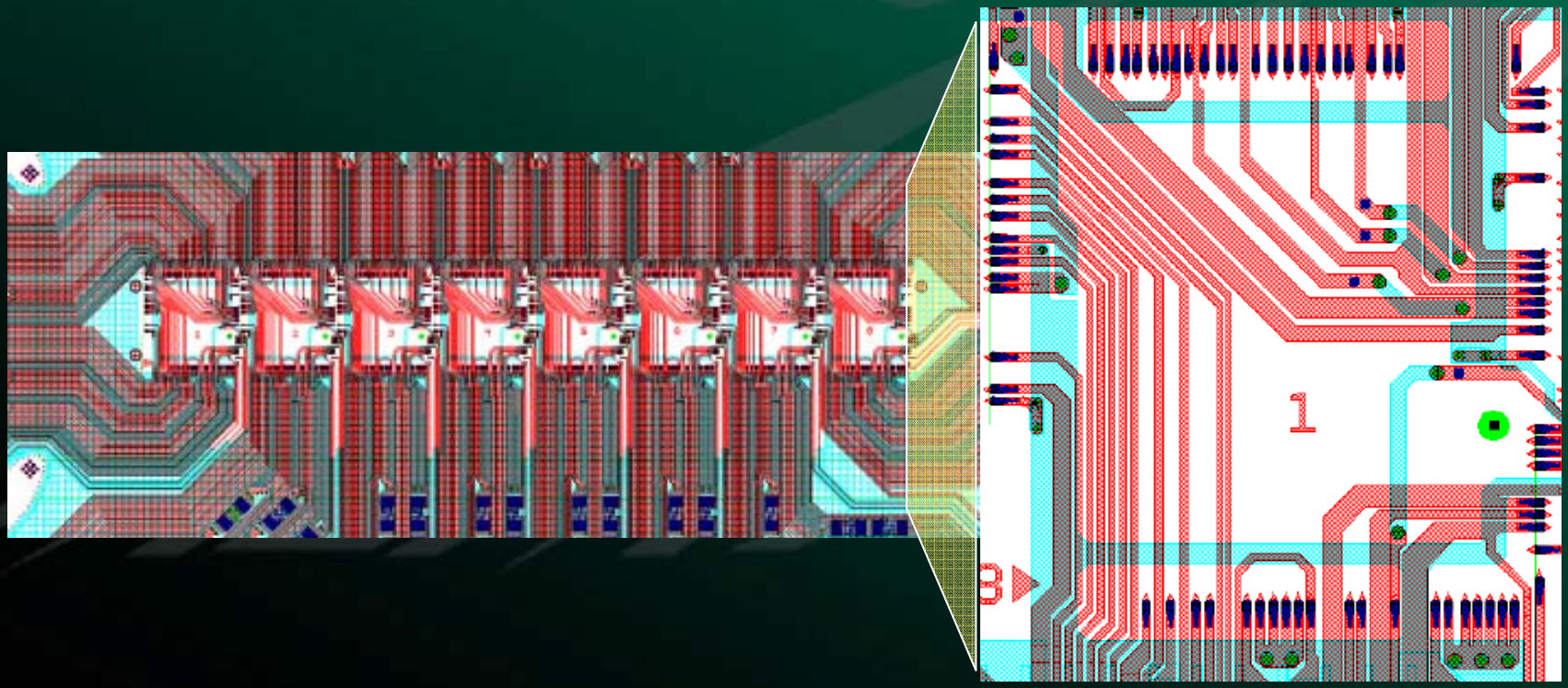
- Objective – Reduce cost of test for RF devices.
- Strategy
  - Implement Multi-DUT testing
  - Perform known good die (KGD)

Strategy

- Multi-DUT
  - Why
    - Perform tests in parallel
    - Fully utilize tester resources
    - Reduce the number of prober indexes
  - How
    - Design to reduce site-to-site variation
    - Reduce crosstalk
    - Debug a complex solution

Multi-DUT
Site-to-Site Correlation

- Reduce site-site variation by making routing very similar
  - One DUT routed as a “cell” and repeated for all 8.



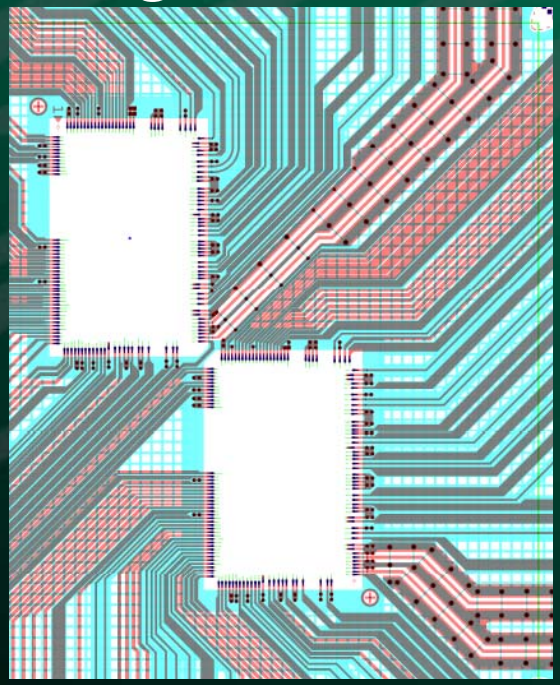
Multi-DUT Crosstalk

- Reduce crosstalk
  - Minimize impedance mismatches
  - Maximize spacing

Multi-DUT Crosstalk

- Minimize impedance mismatches by providing device impedance from DUT to tester of from DUT to matching network.

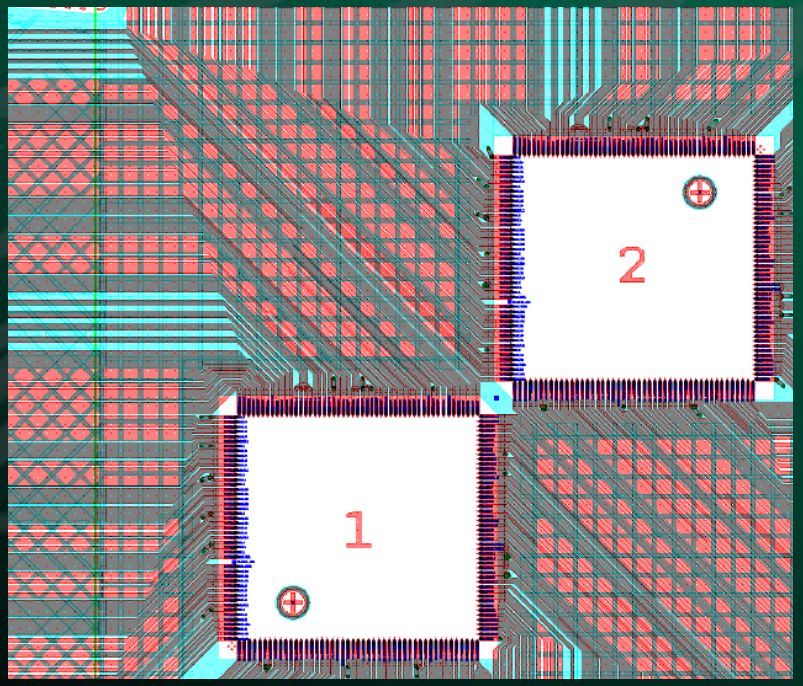
- Dual-DUT
- Cellular transceiver
- 50 ohm microstrip
- 100 ohm CPW



Multi-DUT Crosstalk

- Minimize impedance mismatches by providing device impedance from DUT to tester of from DUT to matching network.

- Dual-DUT
- Decoder
- 50 ohm microstrip
- 37.5 ohm microstrip

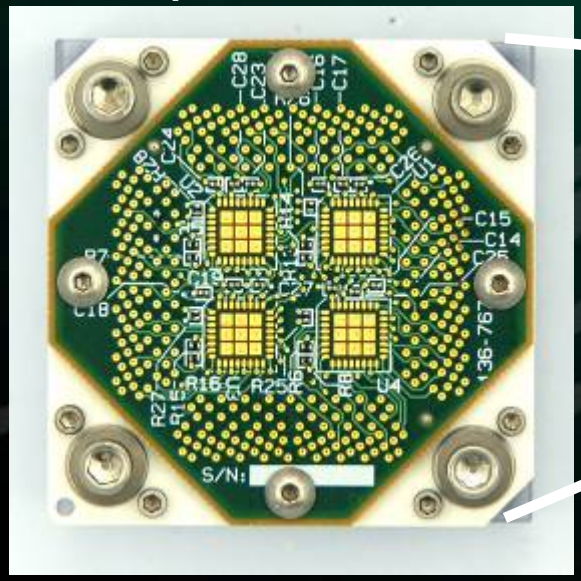


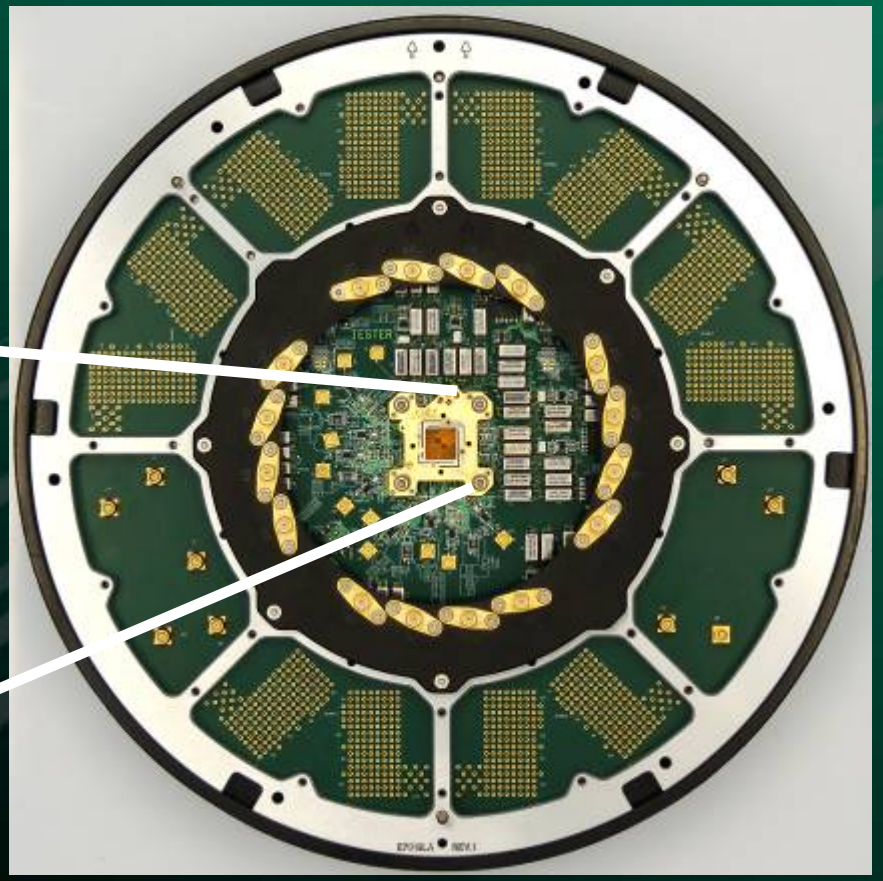
Multi-DUT Debug Tool

- Debug complex probe cards and programs
  - Remove dependence on prober availability
  - Compare package to die
    - Debug program
    - Debug probe card

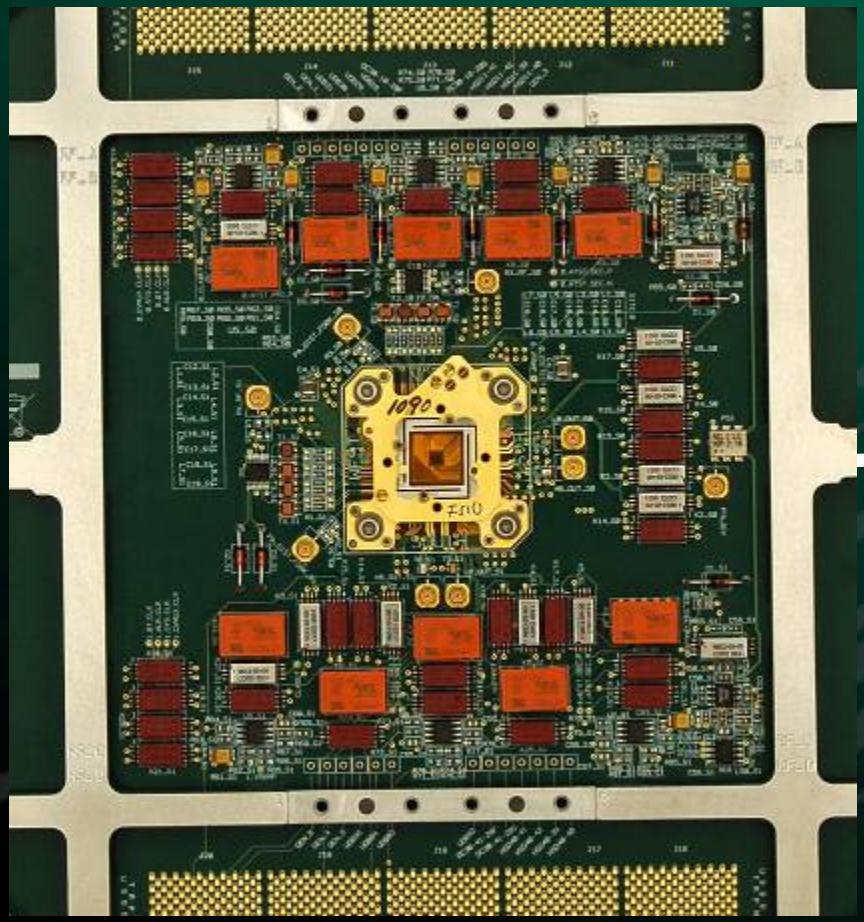
Multi-DUT Debug Tool

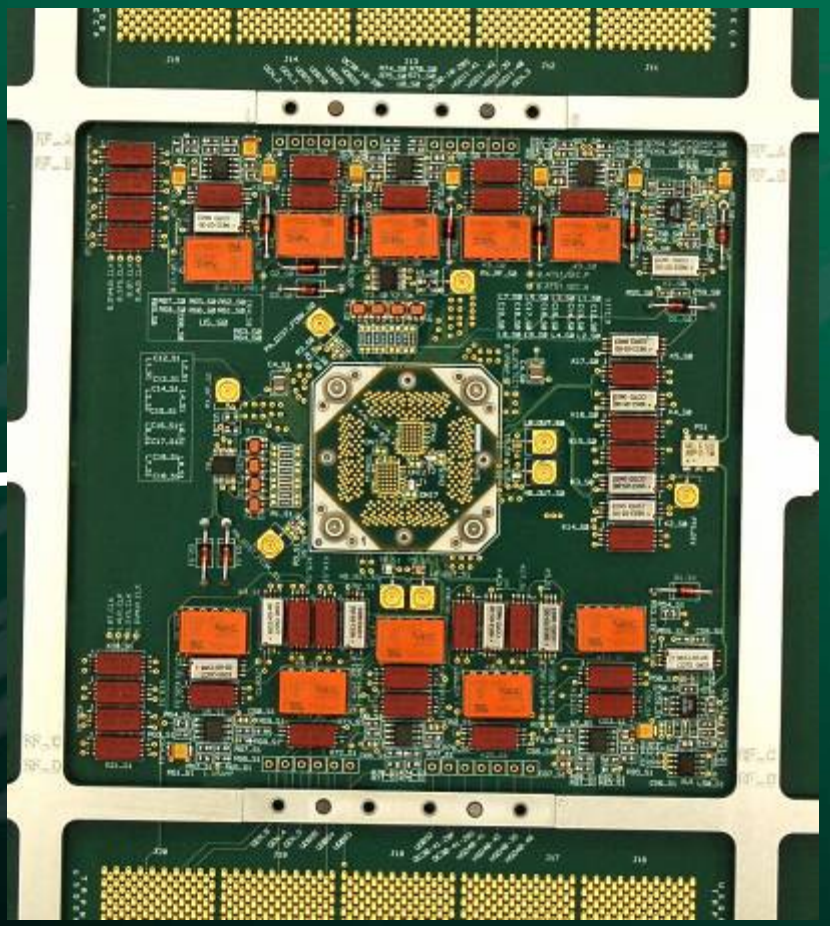
- Debug complex probe cards and programs
  - Replace the DUT contacts with a PCB containing package parts





Multi-DUT Debug Tool





Strategy

- KGD
  - Why
    - Save package loss
    - Save module loss
    - Provide faster feedback to manufacturing
  - How
    - Lower ground inductance
    - Stable power supply
      - Decoupling capacitors near DUT
      - Lower supply inductance
    - Emulate package inductance
    - Tune VCO
    - Avoid coupling with the DUT

Strategy
KGD

"KGD impose new requirements on the wafer test floor to recreate the high speed and high precision of package test but in the wafer-test environment."

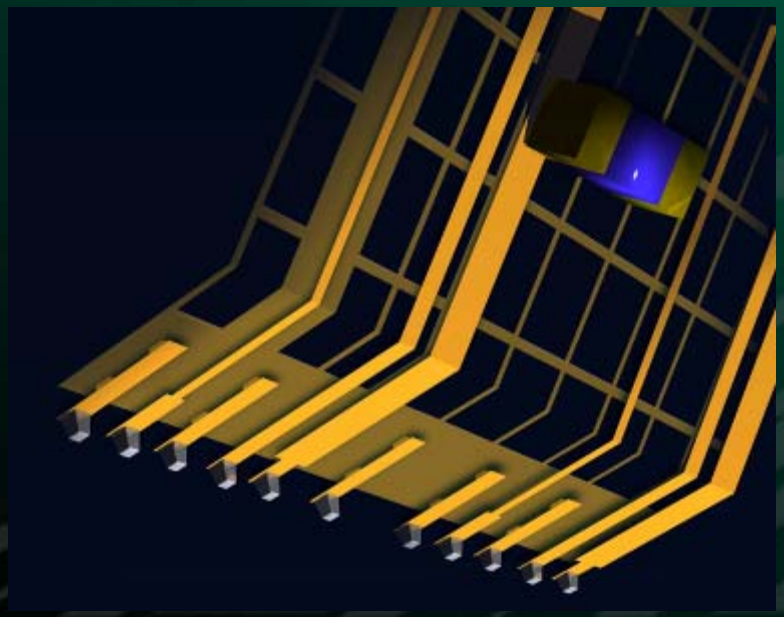
- Mark Brandemuehl (Sept. 2000) *Parallel Test Reduces Costs At Wafer Probe*. Evaluation Engineering

KGD
Lower Ground Inductance

- Strategies to lower ground inductance
  - Wider path
    - Not always practical. Probe cards use uniform diameter paths to get more consistent mechanical performance.
  - Multiple paths in parallel
    - Used at package. Most probe cards take advantage of the large bond area and also use multiple parallel connections.
  - Shorter path
    - Bring the ground plane as close to the DUT as possible

KGD
Lower Ground Inductance

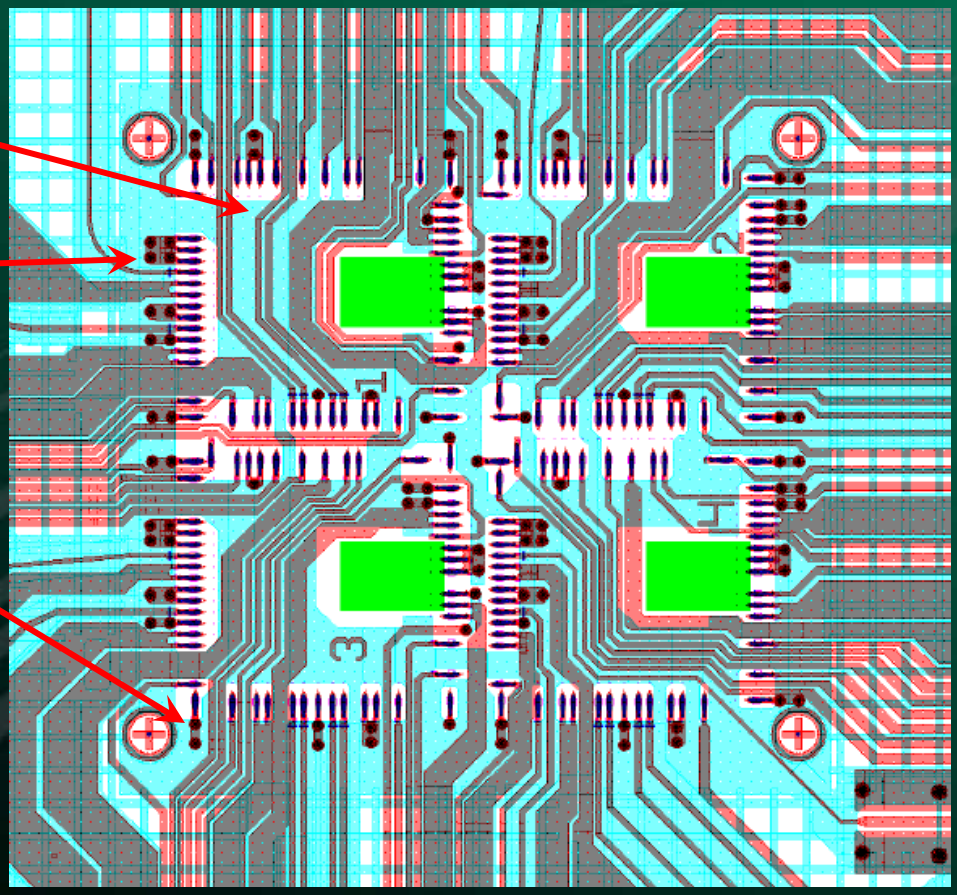
- Use a flex circuit with a ground plane to bridge the gap between the PCB and the DUT.
- Connection from ground plane to DUT is 40 pH



KGD
Lower Ground Inductance

- For a multi-DUT application, do all three
  - Wider paths
  - Multiple paths in parallel
  - Shorten path

Example shows 2x2 quad-site, satellite tuner



KGD
Stable Power Supply

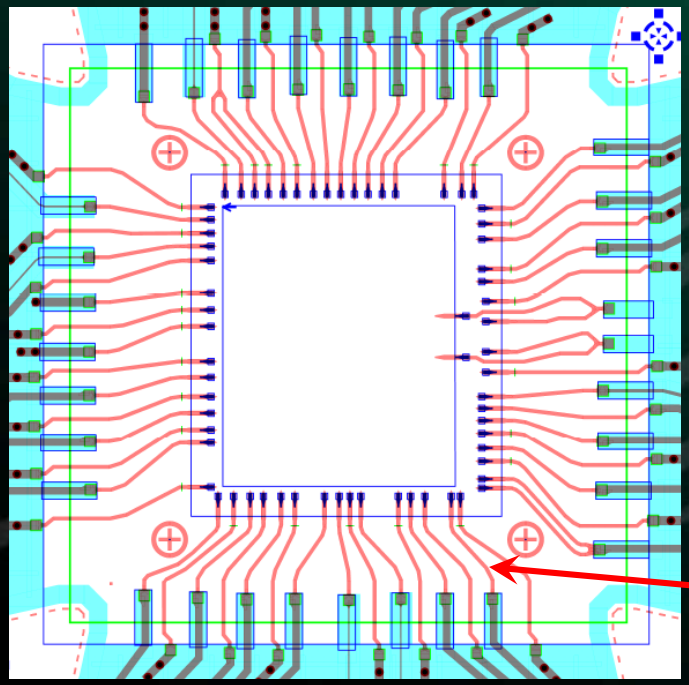
- Strategies for stable power supplies
  - Decoupling close to DUT
  - Lower power inductance
    - Wider path
    - Lower the impedance by creating microstrip structure

KGD
Emulate Package Inductance

- First order goal is to reduce inductance
- Packages, especially wire-bond have unavoidable parasitic inductance
- Some devices are designed to expect the parasitic inductance and will only work properly (at speed) with wire bond inductance.
  - Filters
  - RF Switches
  - Transceivers

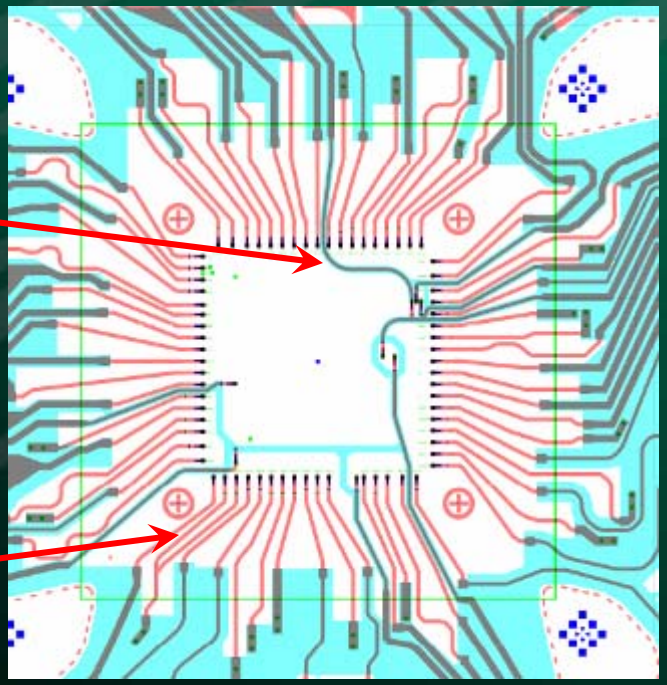
KGD
Emulate Package Inductance

- Transceivers with inductance between DUT and ground plane.



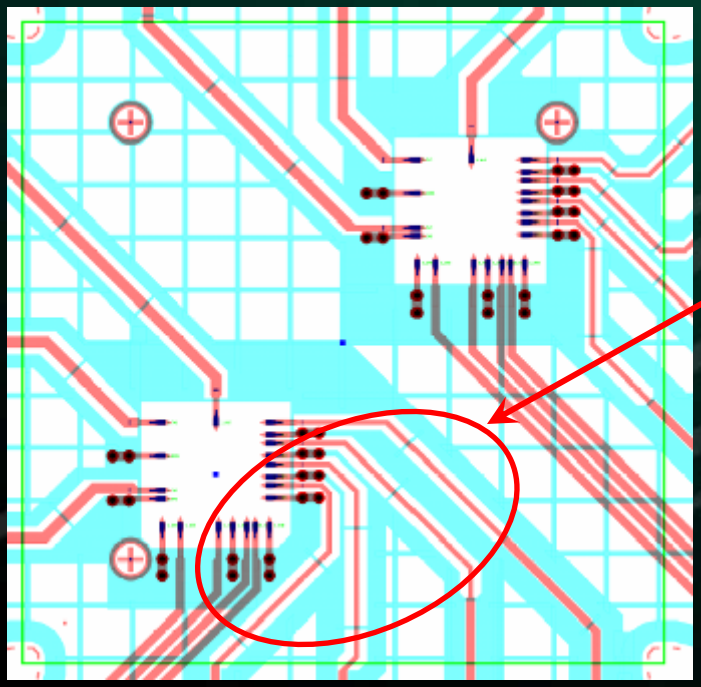
Select paths of 50 ohm to the DUT pad

Inductive paths to emulate wire bonds



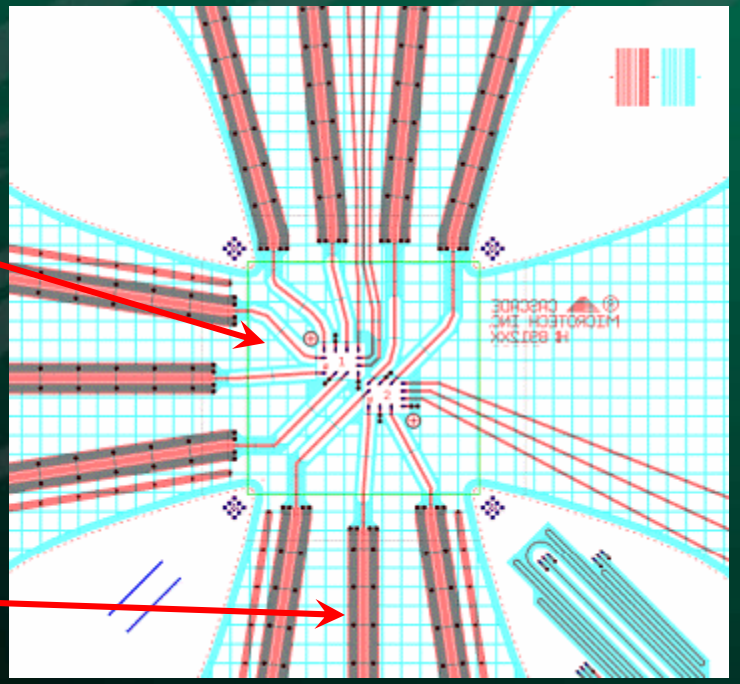
KGD
Emulate Package Inductance

- RF switches with inductance in the signal paths



Inductive signal paths to emulate wire bonds

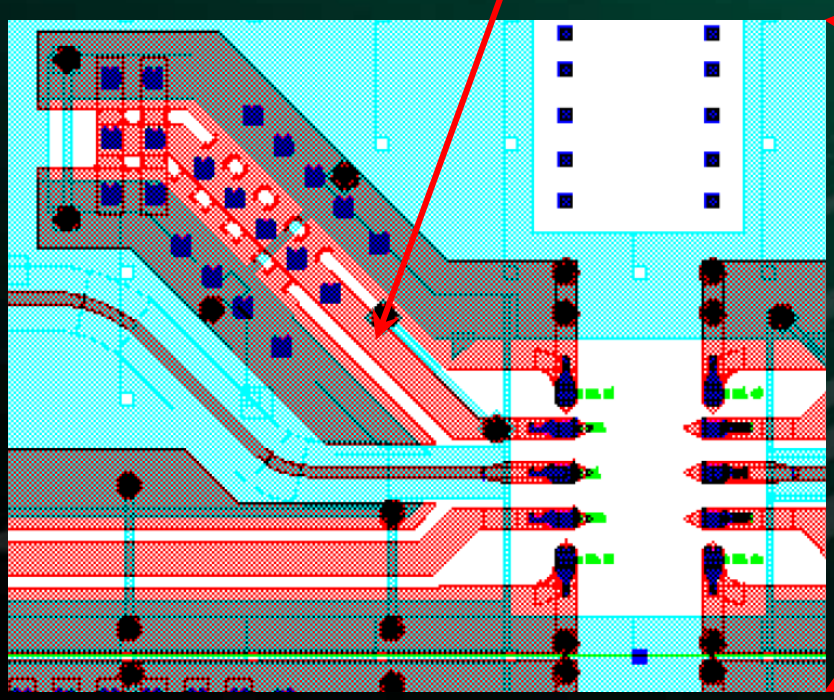
Coplanar waveguide for high power signals

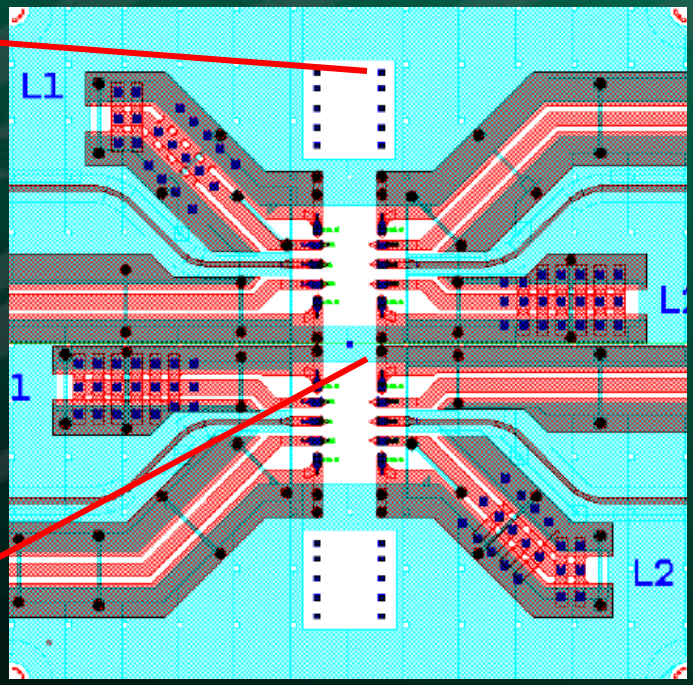


KGD
Emulate Package Inductance

- RF filters with inductance in the ground paths

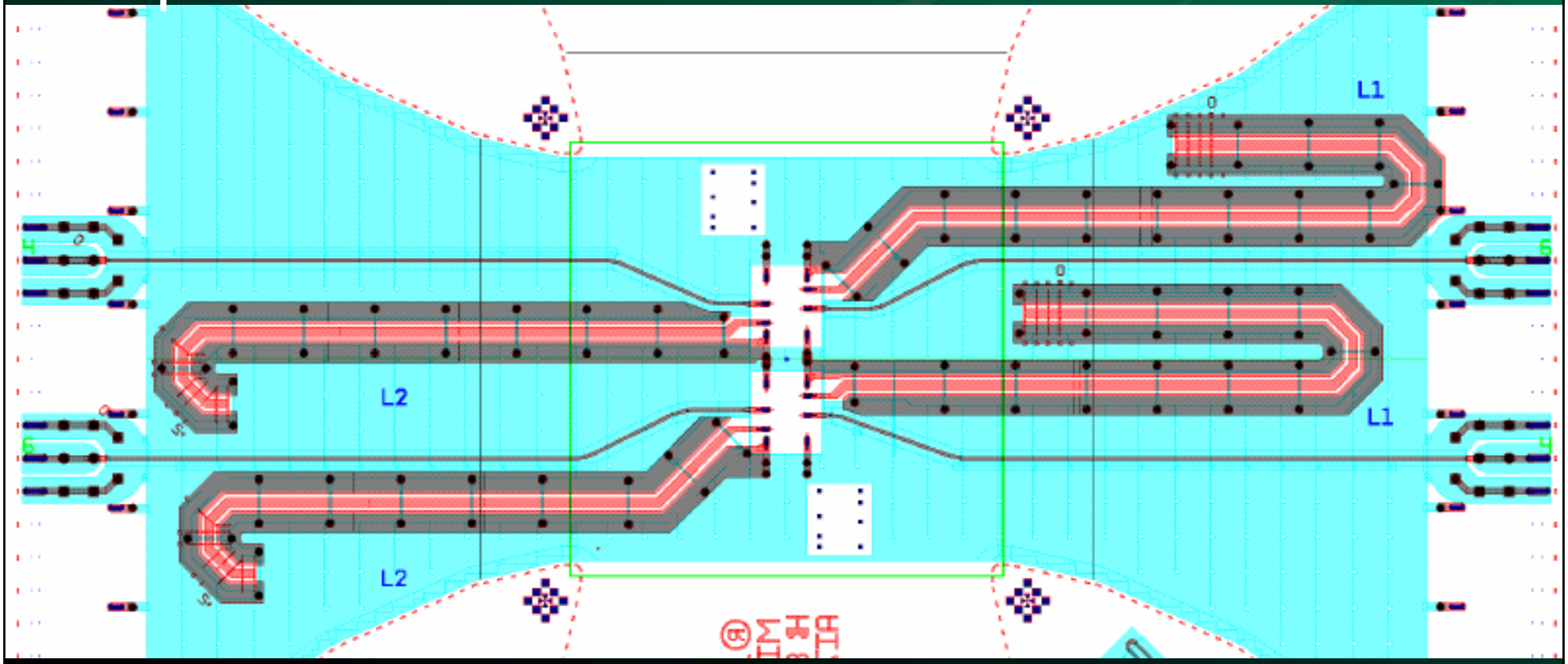
Long inductive ground path between signal and short ground path





KGD
Emulate Package Inductance

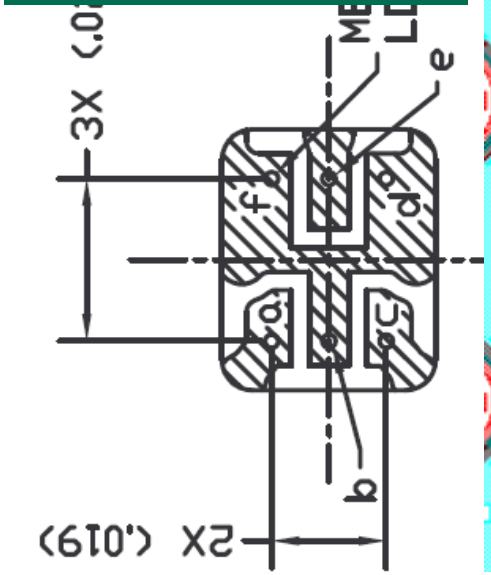
- RF filters with inductance in the ground paths



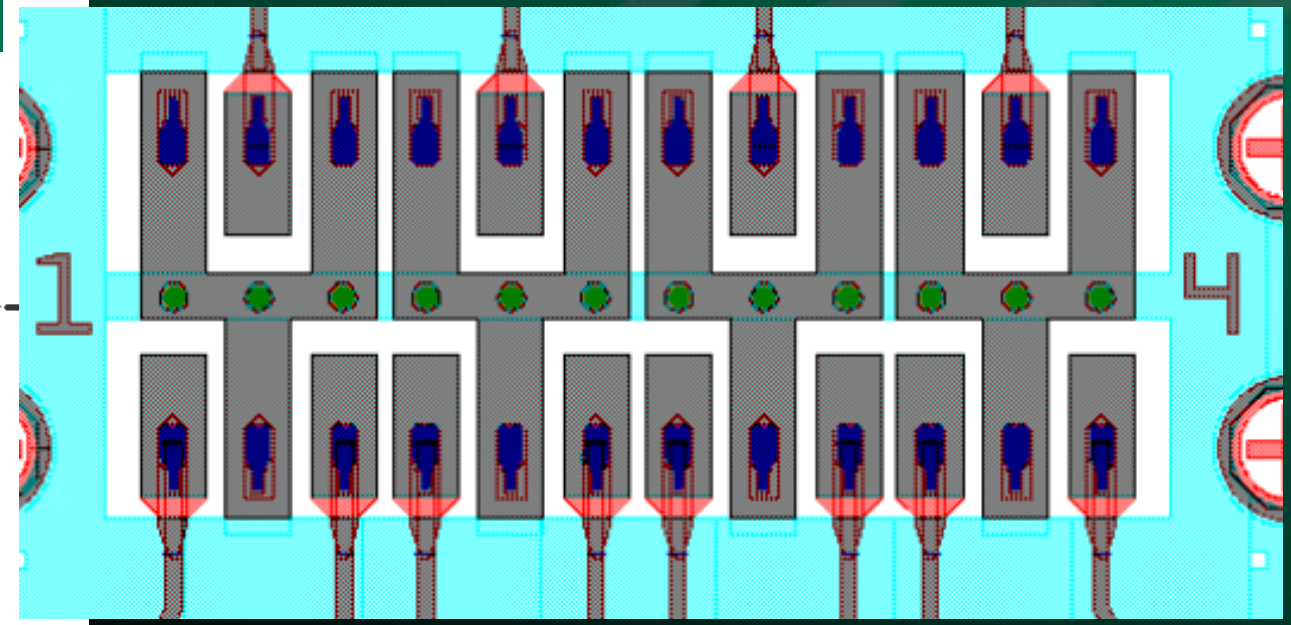
KGD
Emulate Package Environment

- RF filters with large capacitive ground structures

Package design



Membrane x4 design

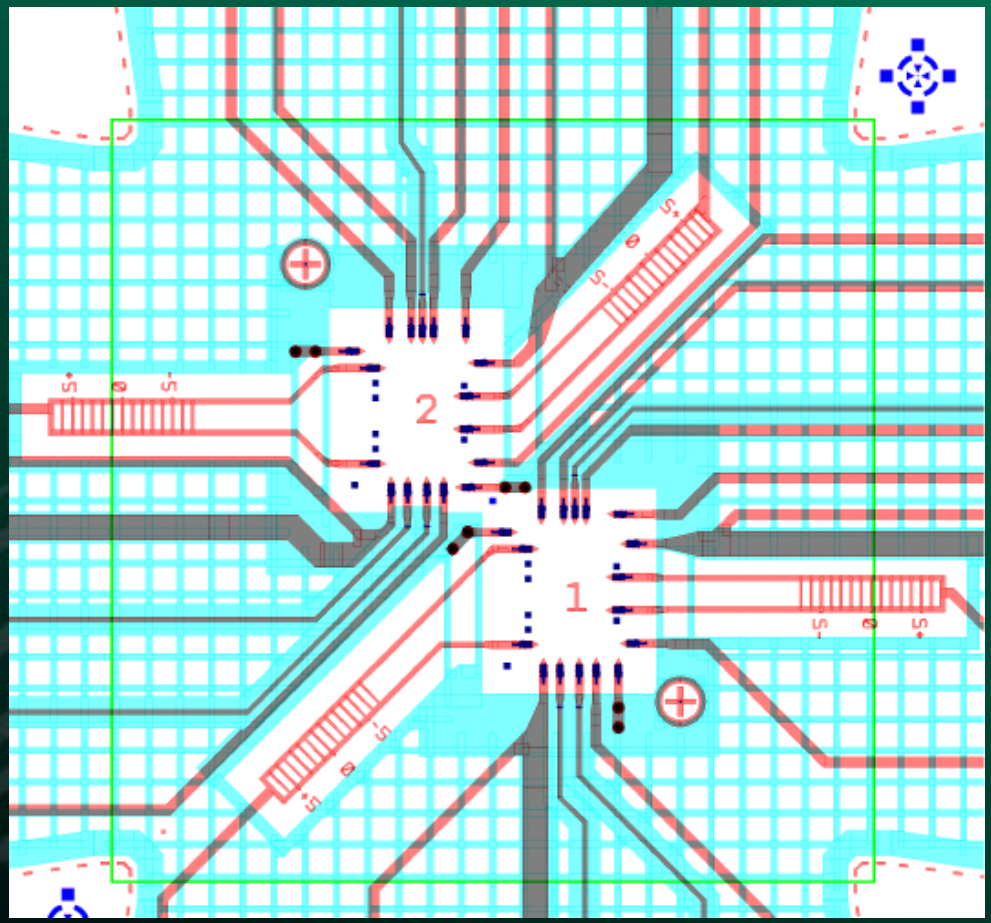


KGD
Tune VCO

- VCO tuning needs a small inductor.
  - Sometimes too big to be on the chip and too small compared to parasitics of path to PCB.

KGD
Tune VCO

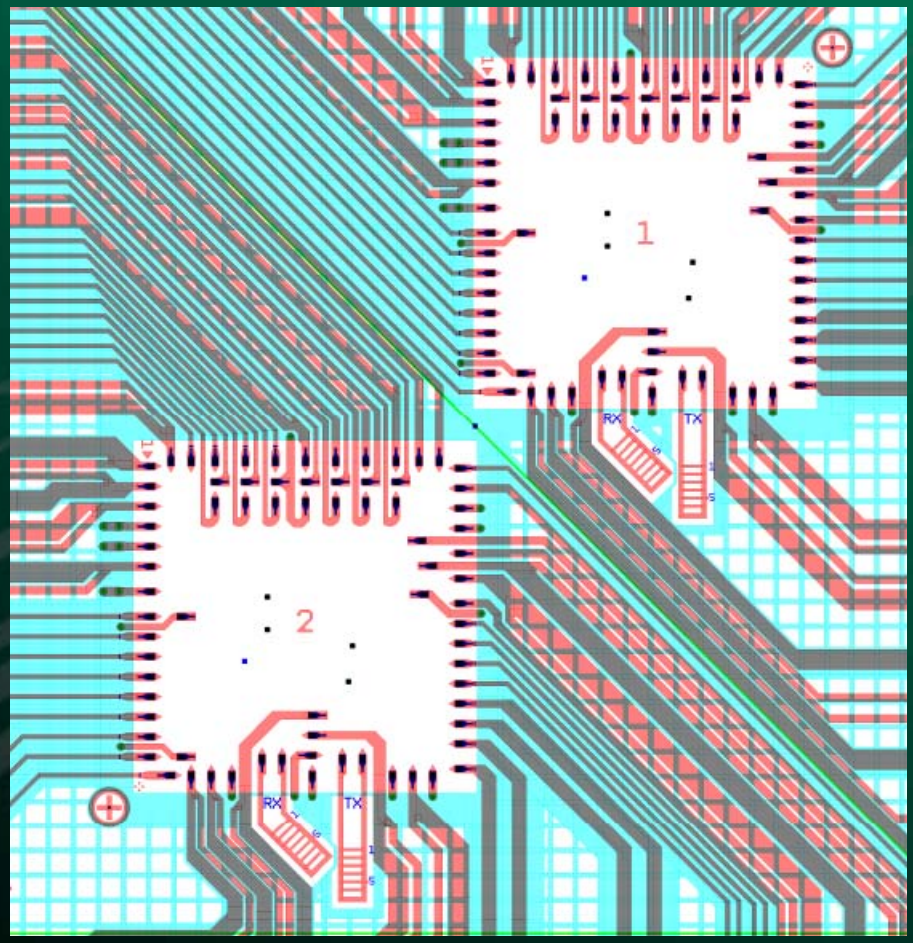
- Dual-DUT
- Triple band VCO (GSM and DCS/PCS)
- Package contains tank circuit
- 2.0 and 2.2 nH inductors



KGD
Tune VCO

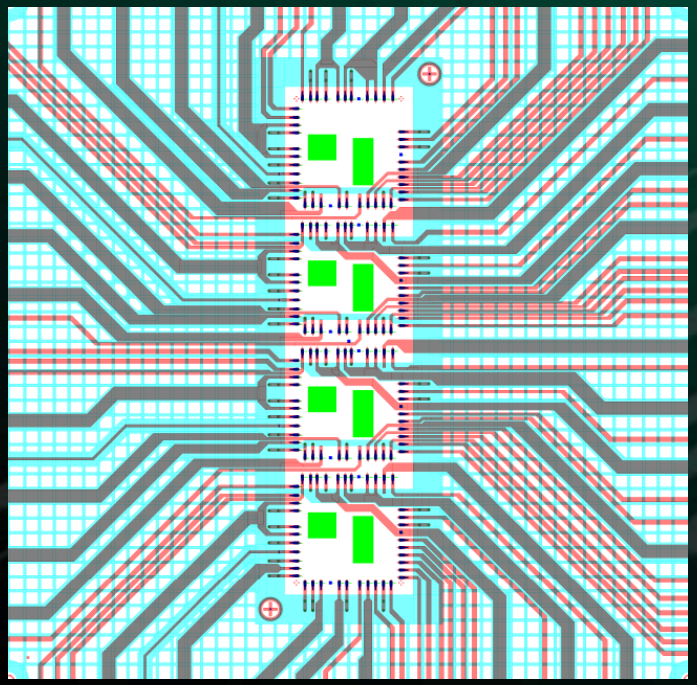
- Dual-DUT
- GSM transceiver
- Package substrate inductors for the VCO
- 0.51 and 0.54 nH inductors

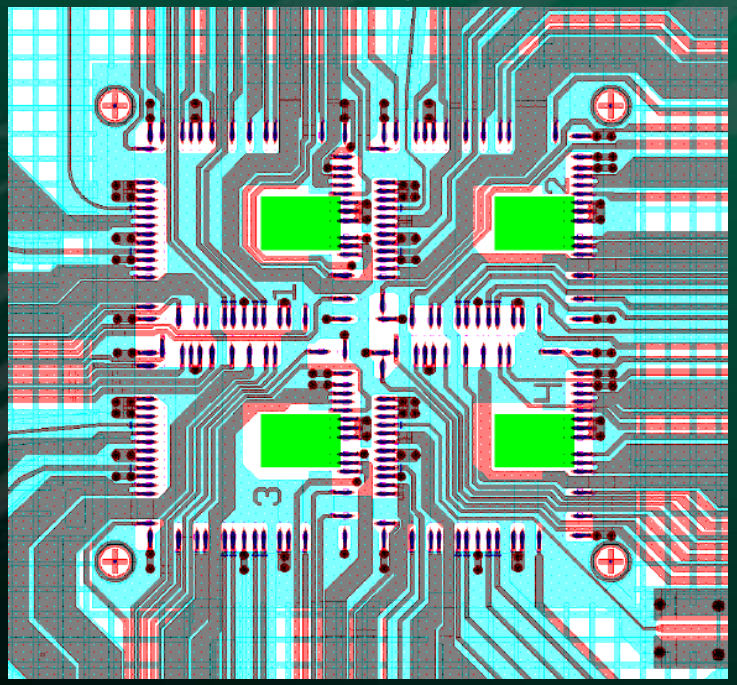
- Q can not be too high



KGD
Avoid Coupling to the DUT

- Many transceivers have the VCO and its tuning inductor in the DUT.
  - Metal structures can couple with the inductor and change the VCO frequency.
  - Take care to avoid the inductor during routing.





Summary/Conclusion

- Objective – Reduce cost of test for RF devices.
- Strategy
  - Implement Multi-DUT testing
    - Design to reduce site-to-site variation
    - Reduce crosstalk
    - Debug a complex solution
  - Perform known good die (KGD)
    - Lower ground inductance
    - Stable power supply
    - Emulate package inductance
    - Tune VCO
    - Avoid coupling with the DUT