IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

Brian Moore

Scanimetrics, Inc.

Advanced Probecard Architecture for Lower-cost RF Wafer Testing

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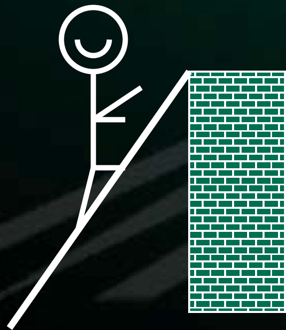
Overview

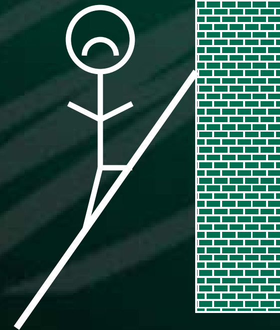
- Existing Issues Time/Cost/Thru-put
- The RF Testing Challenge
- The Multi-site Challenge
- Cantilever Solution
- Test and Simulation Results
- Architecture/Test Changes
- Summary

The RF testing wall Time/Cost/Complexity Challenge

Test:

- 1 RF Channel
- x1 parallelism
- 1 function/format (Tx, Rx, GSM, CDMA, etc.)





Test:

- 5 RF Channels
- x8 parallelism
- GSM and CDMA and BlueTooth etc.

Multiband, Multi-protocol

Signal Integrity Challenge

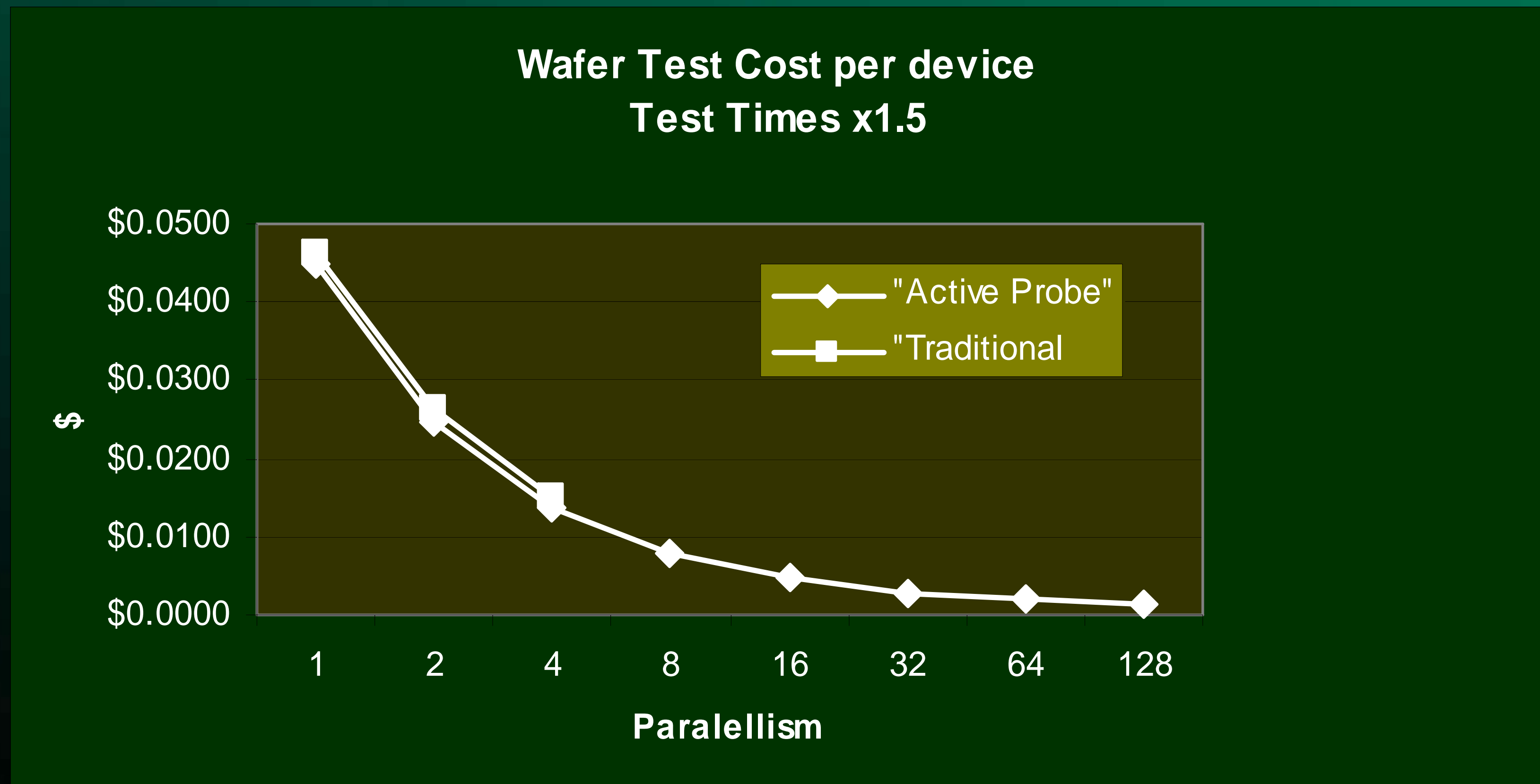
- RF is tough to do in the best of circumstances.
  - Load Board, Probe Card, Wiring, Needles all mask true nature of high speed and RF signals.

- Specific signal integrity issues involve:
  - Slew and delays due to low pass nature of long convolved signal paths. A 2GHz signal turns into a 200 MHz signal
  - Differential timing due to different signal path lengths. A signal edge arrives too early or late compared to its companion signals.
    - Impairments See K. Helmreich ……..… SWTW 2001

The Goal
Lower cost RF device Test

- Provide a method to efficiently measure RF devices on the wafer level
  - High parallelism possible
  - No RF resources required from tester
  - Allow fast verification of basic RF signals
- No modifications to the circuit are required

Multi-site Cost Advantage



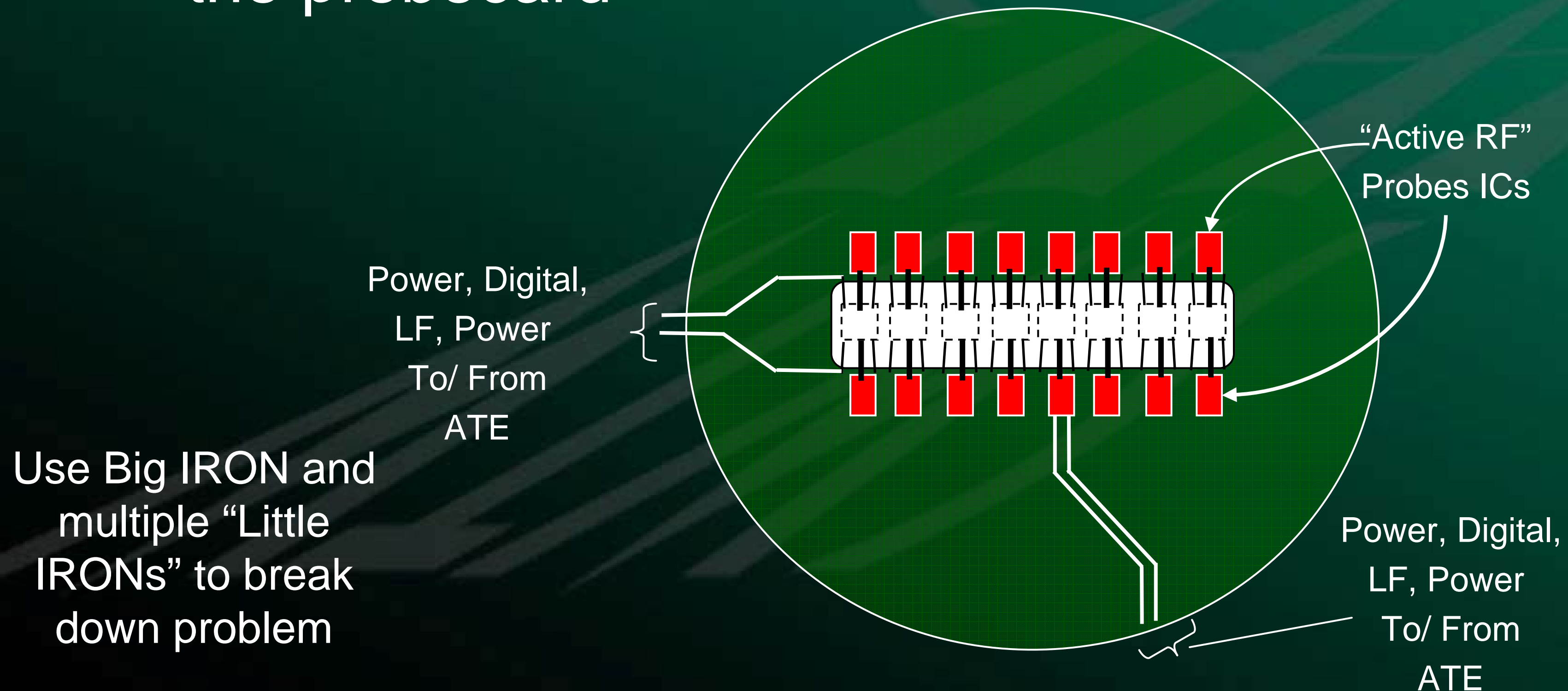
Test Cost per device as much as x10 less

The RF Multi-site Challenge

- ATE
  - Limited RF ports – generally 2 to 8
  - Cost of RF ports - $100K to $500K
- Probecard
  - Probes
  - Controlled impedance traces, SMA connectors
  - Cross-talk, interference

The Multi-site Solution

- Keep all the RF signals close to the DUT
  - Bring the RF measure / source resources to the probecard



Signal Integrity

- If RF signals don’t leave the probecard most of the issues “Go Away”
  - Load Board, Probe Card Traces, Pogo Tower signals are now Low Frequency.
- Probe Pins are all that is left in the RF path.

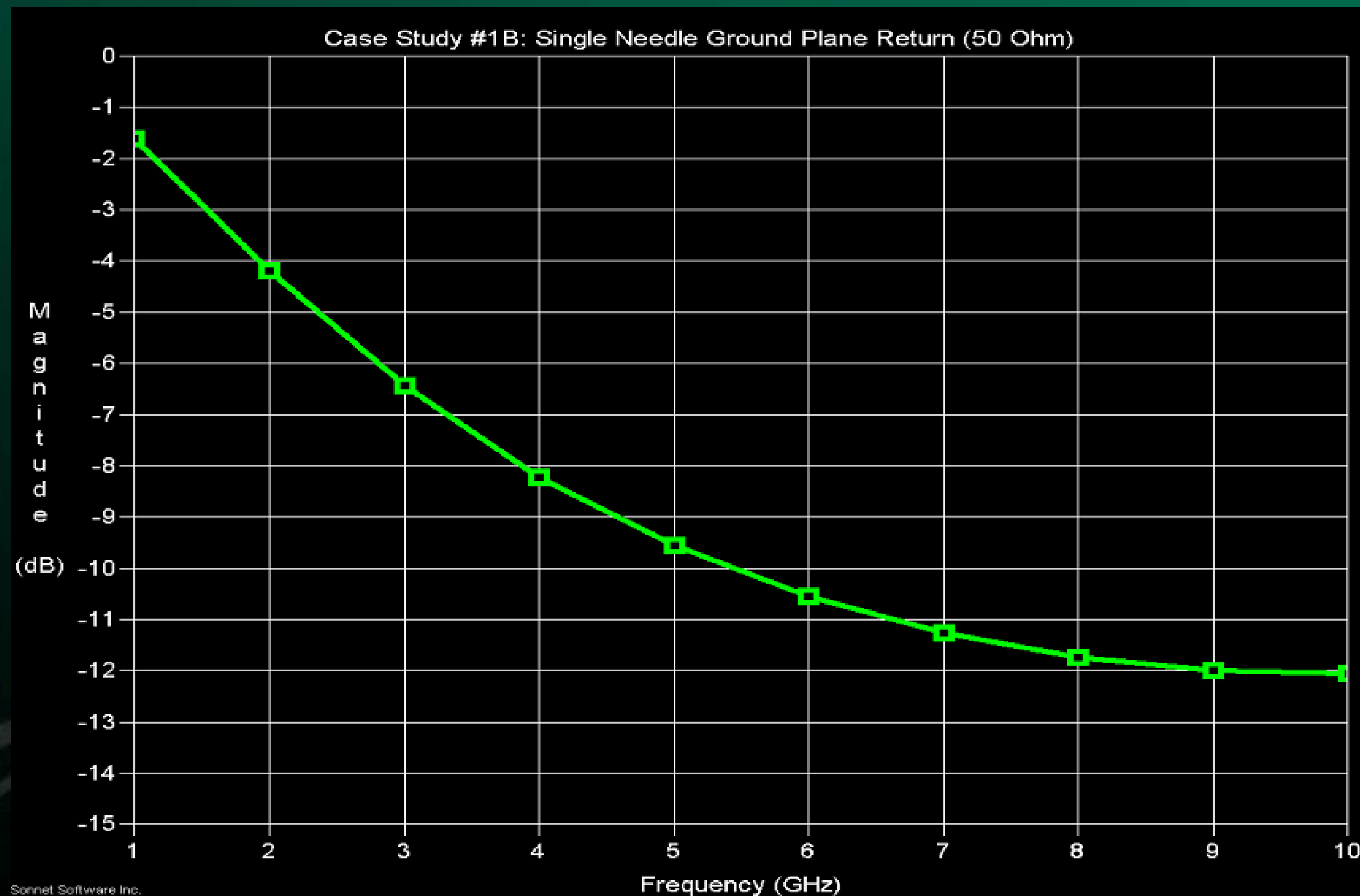
So what about the Needles?

- Model Needles with Sonnet (3D planar EM) solver
- Interested in bandwidth and effect of guard (GND) needles used to emulate (coplanar) RF probes.
- Why try?   Standard RF probecards are too expensive, complex and have too much plumbing.
  - If Standard needle (or Cobra) can work (even badly) then Active RF probe can overcome initial loss.
- Using standard Cantilever or Cobra enables multi-site testing.

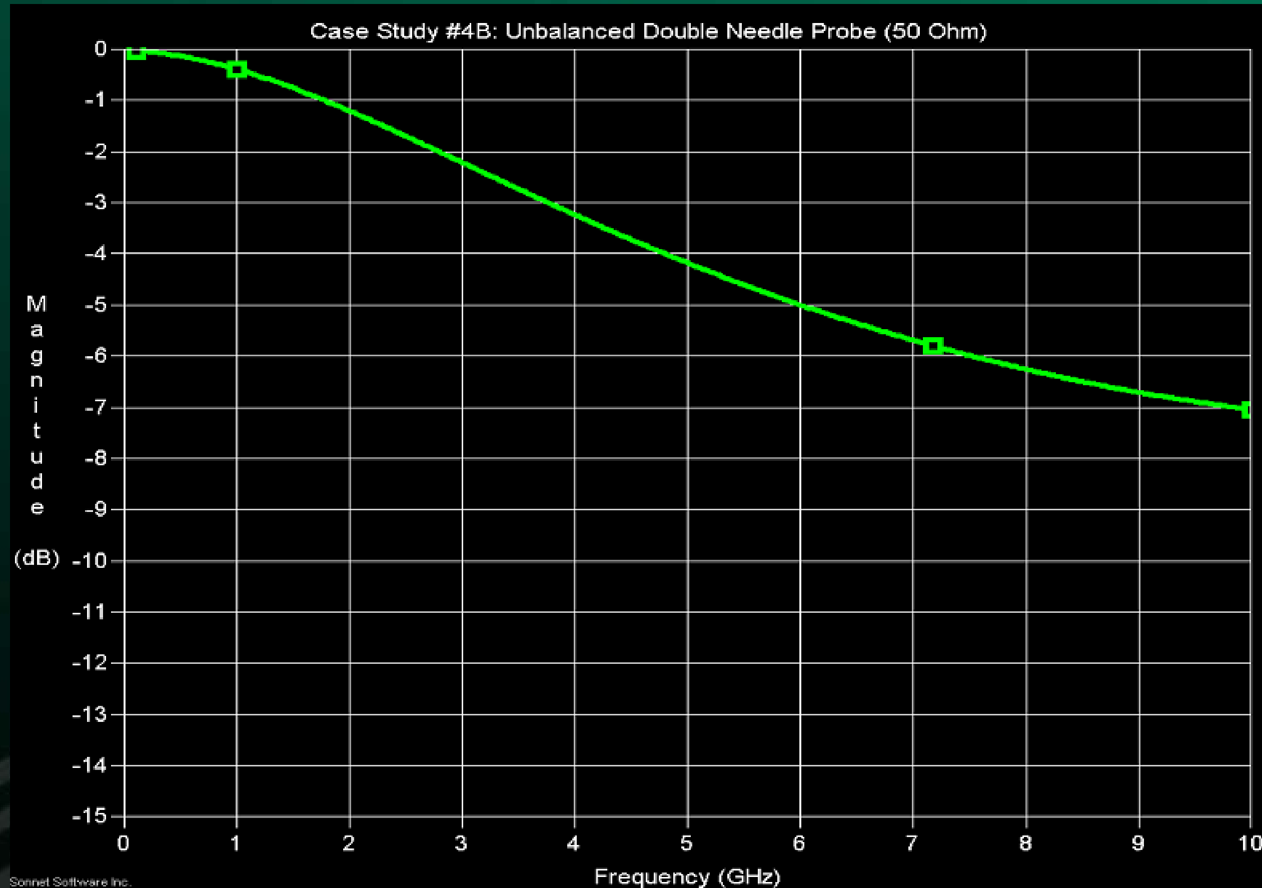
- See other modeling work by
  - R. Rincon ..(TI/Ansoft)…………… SWTW 1998.
  - R. Robertazzi..micro-coax(IBM)………SWTW 2002.

Cantilever Needle

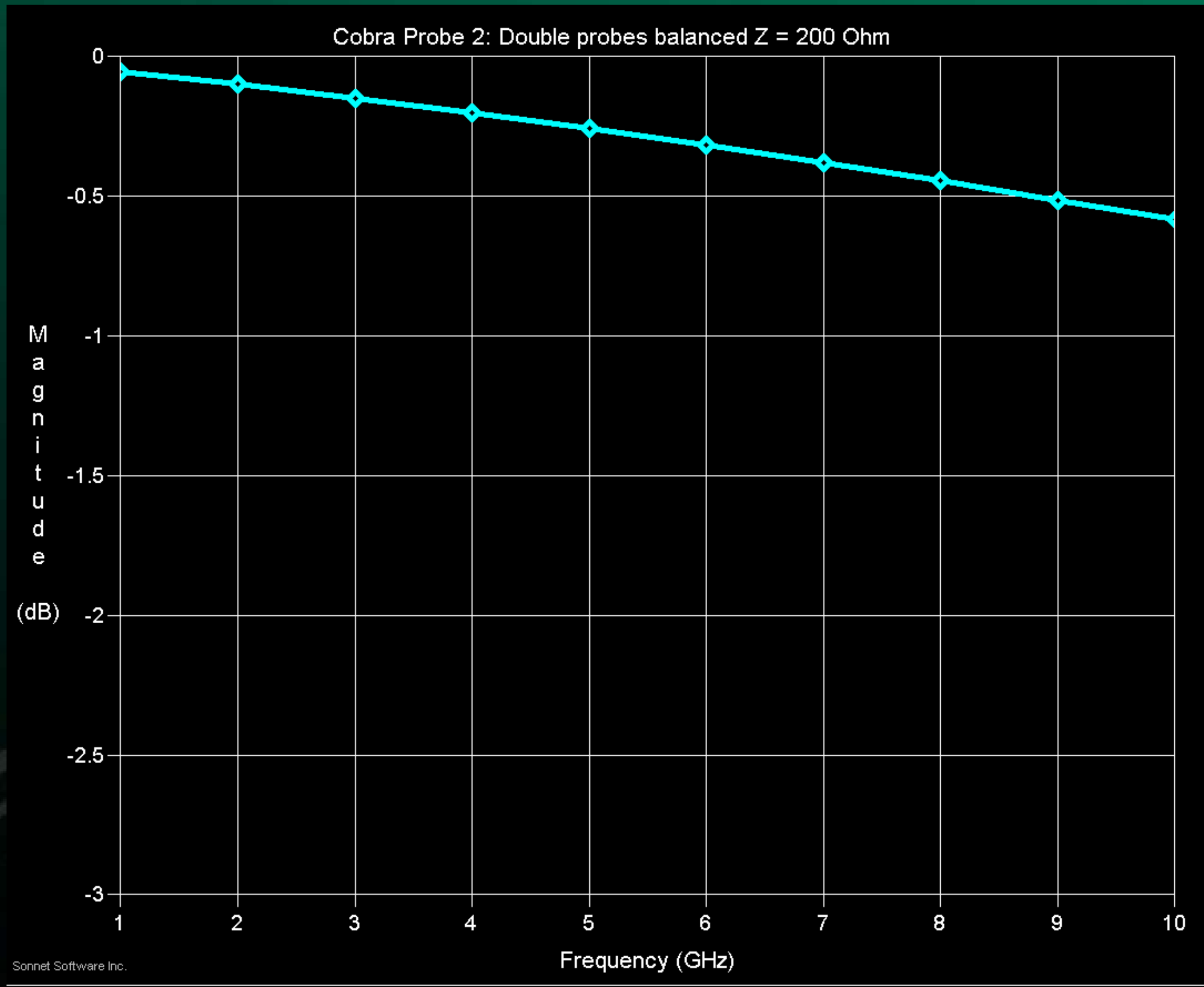
3D planar EM simulation



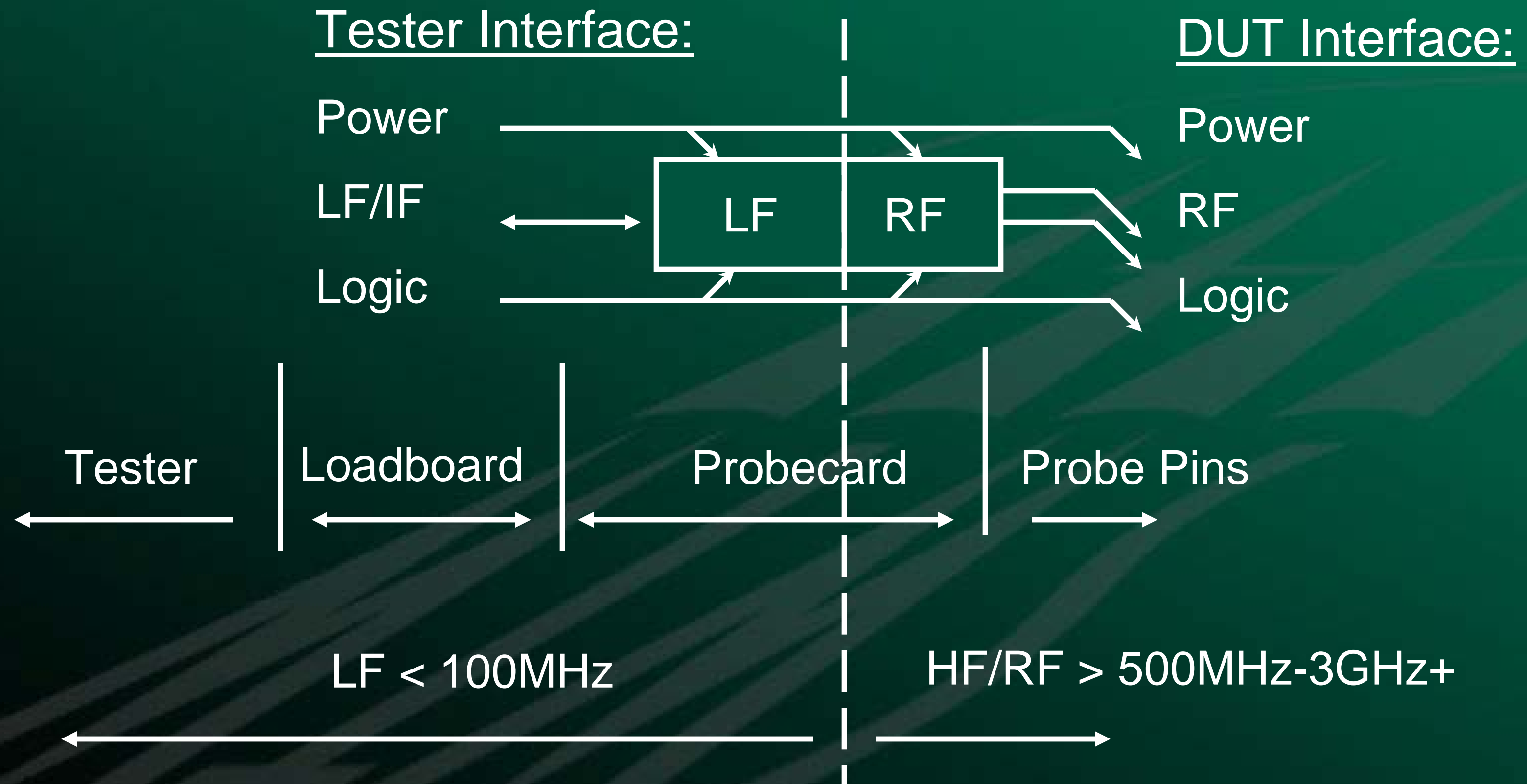
Cantilever Double Needle



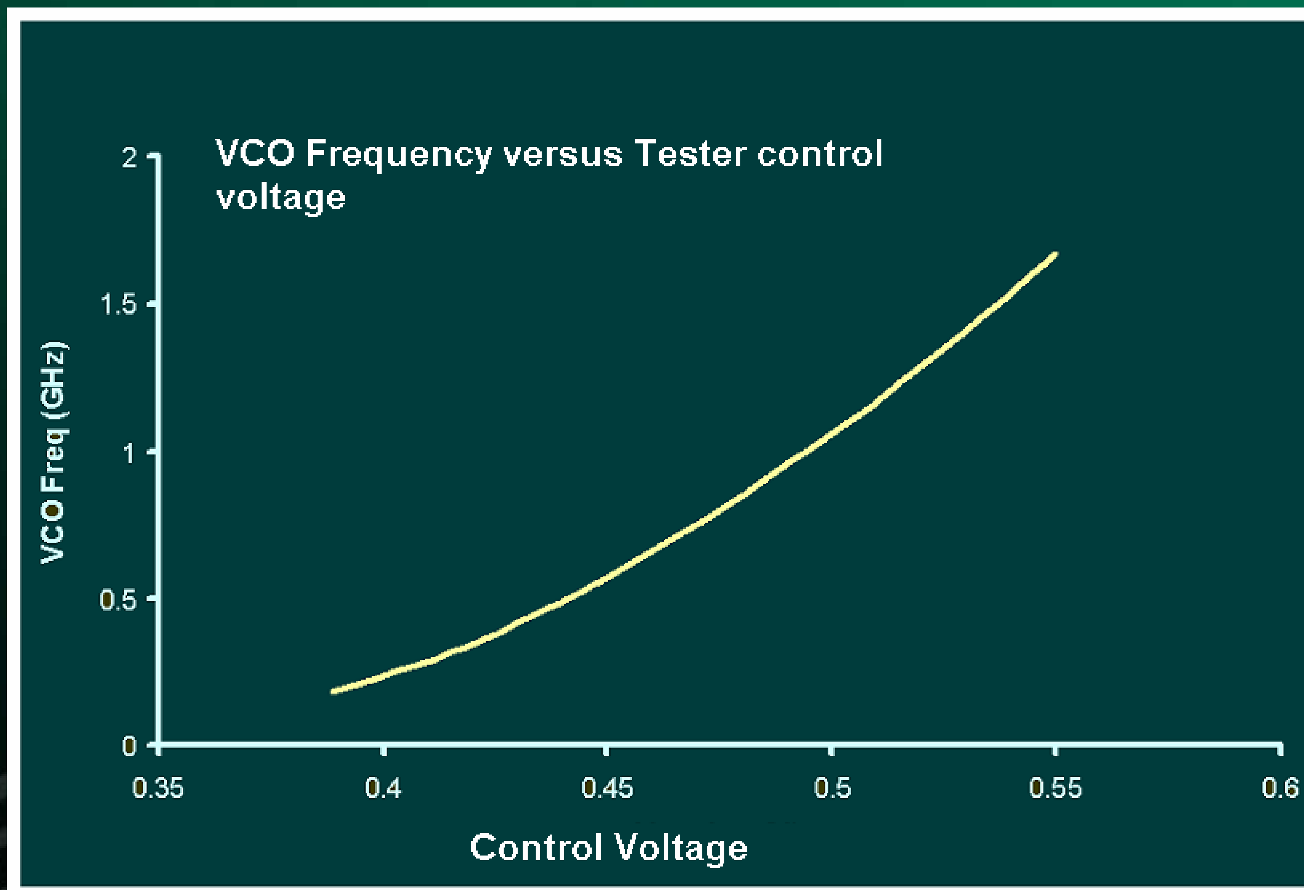
Cantilever Double Needle, Matched Impedance
<u><0.25dB at 5 GHz !</u>



Active RF Probe IC

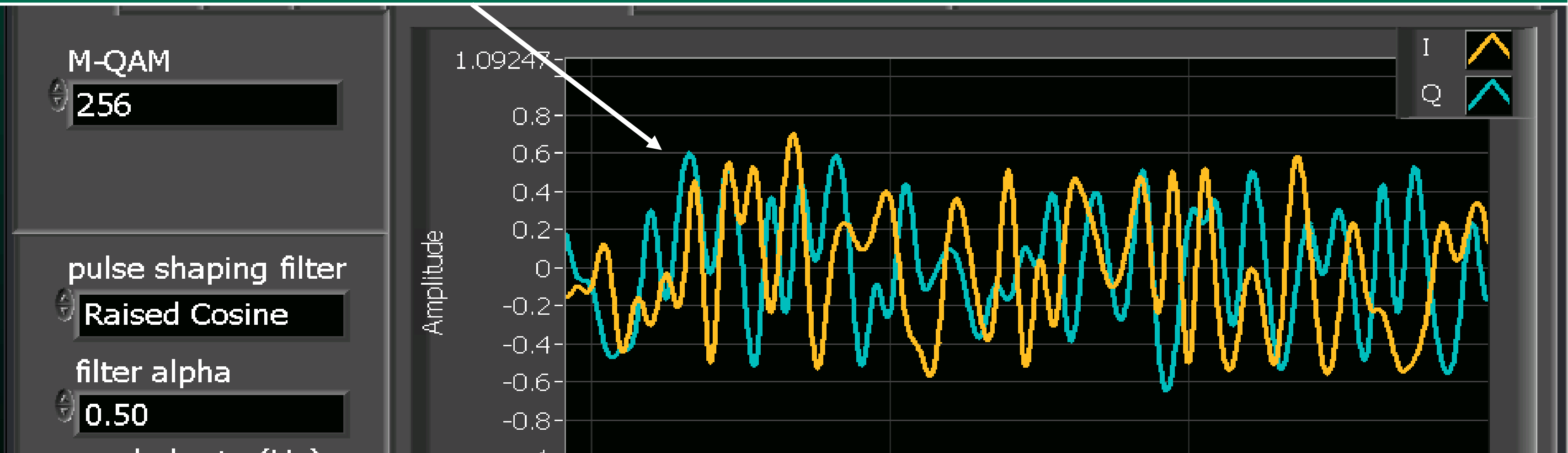


Example - Simple RF Source IC



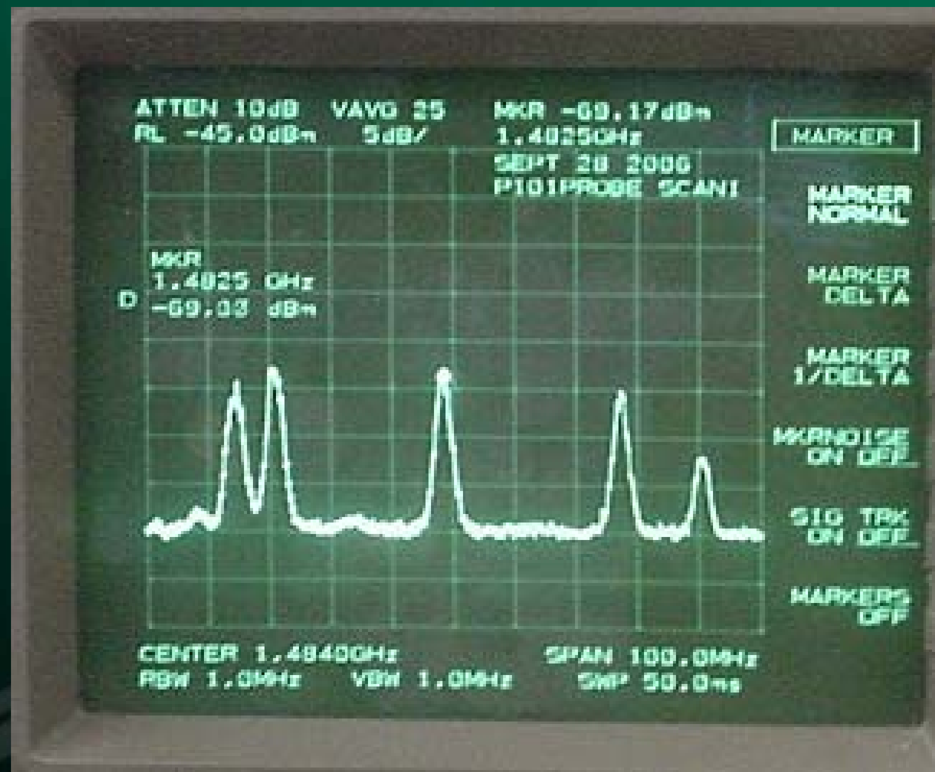
What about Complex Signals ?

- Yes e.g. QAM 256 via Baseband AWG on Tester



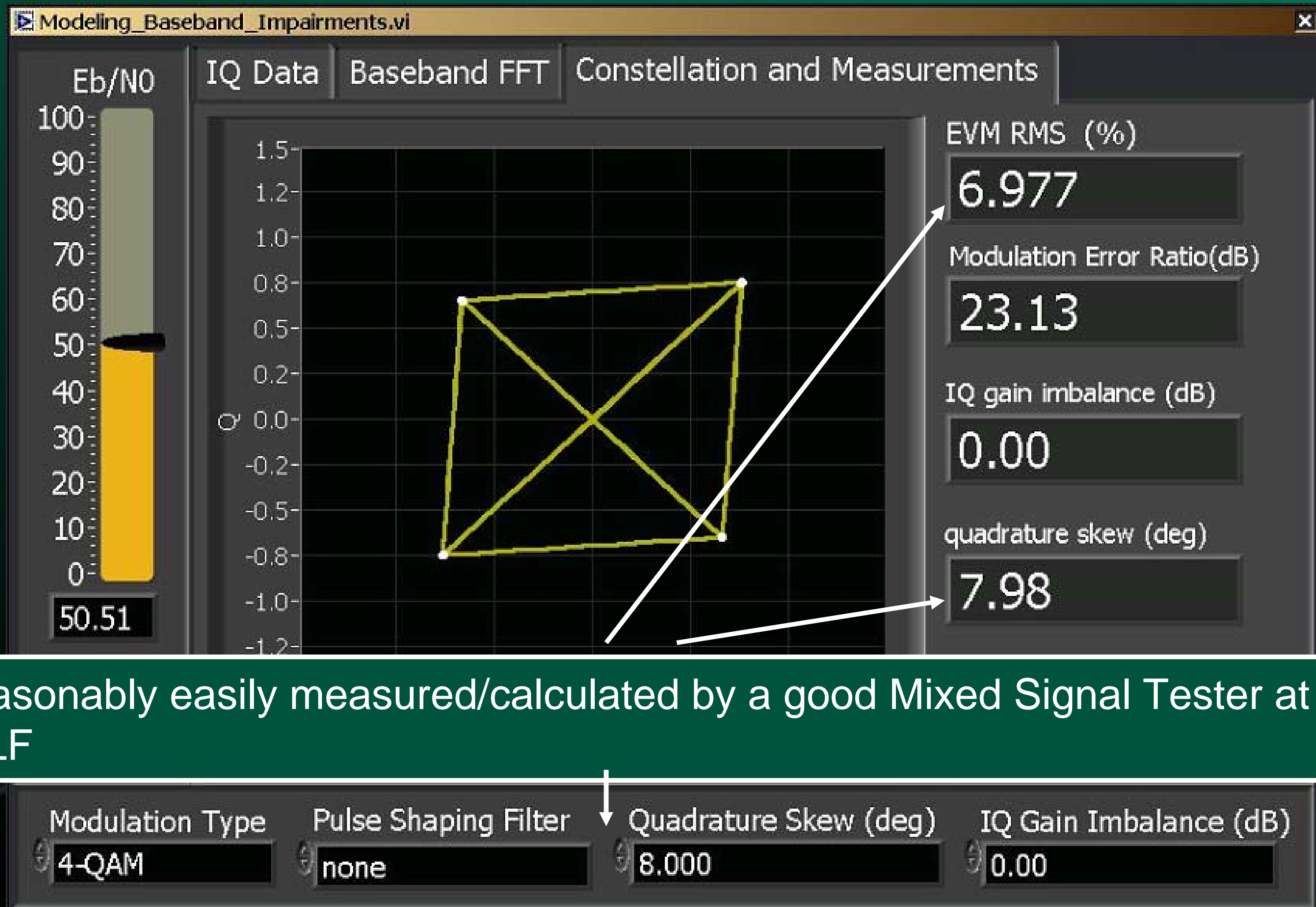
Tester AWG → Upconversion IC → Complex RF

Five - 1.5GHz Tx sources on one Die



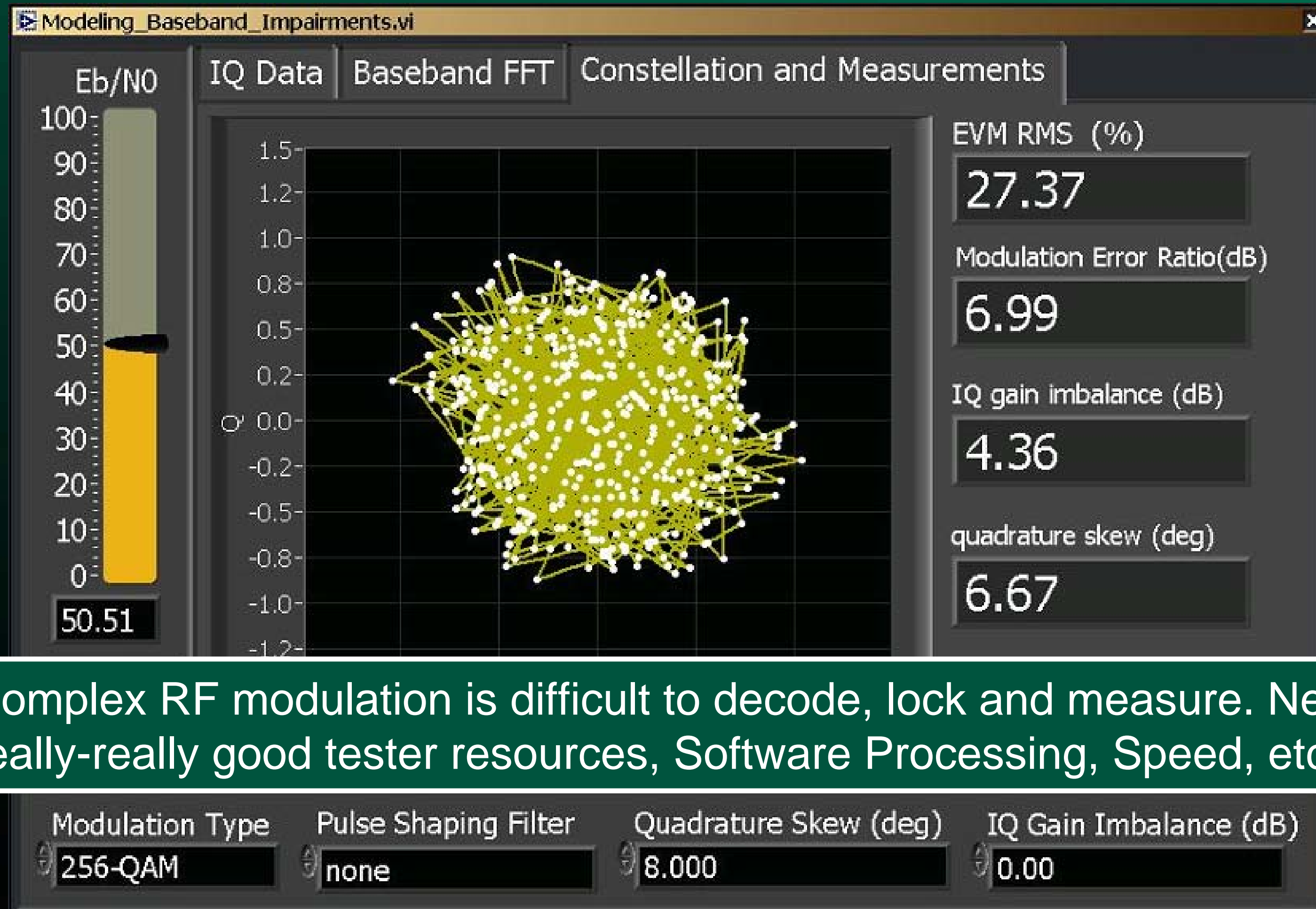
- Wide range source IC covers 0.5-1.8GHz (180nm CMOS)
  - Use AWG tester channel for modulation on RF.

Rx Testing of Simple Modulation At IQ (baseband) - added impairments



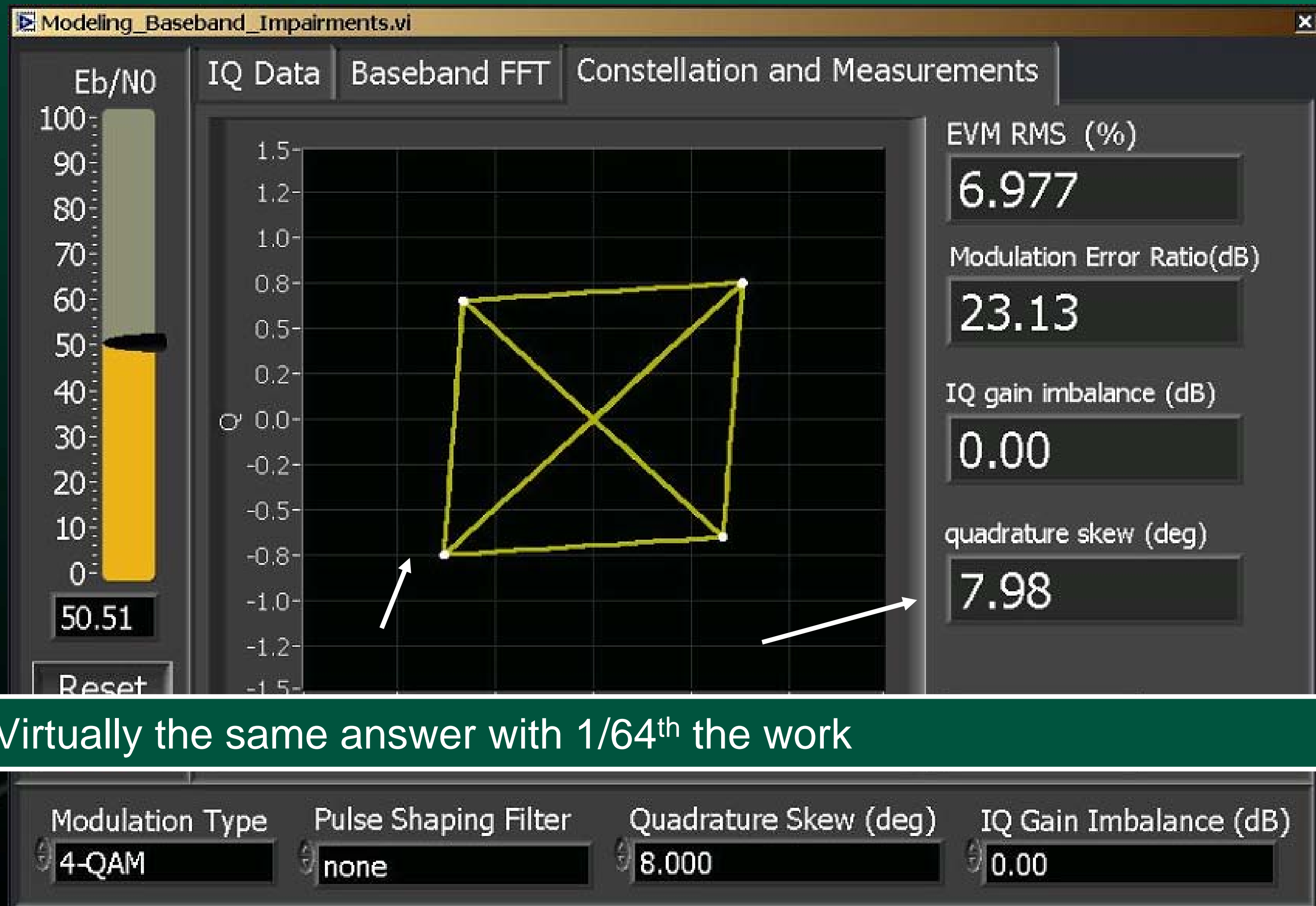
Reasonably easily measured/calculated by a good Mixed Signal Tester at IF/LF

Rx Testing Complex Modulation QAM-256 At IQ (baseband) Complex data and receiver (non-lock)



Complex RF modulation is difficult to decode, lock and measure. Need really-really good tester resources, Software Processing, Speed, etc.

Rx Testing Simple Modulation At IQ (baseband) added impairments



Virtually the same answer with 1/64th the work

The RF Testing Wall Conquered

Big IRON Tester

Helps “Little IRON” RF active probes to Achieve:

- Parallel testing
- Complex signal Analysis

While maintaining parallel Power, Logic, housekeeping, etc.

Multi-site Cost Advantage

Case Study	GSM Transceiver 1 RF input, 1 RF Output 500K devices / month	
	Traditional	"Active RF Probes"
Parallelism	x2	x16
ATE RF Ports	4	0
LF Source	0	8
LF Measure	0	8
ATE Cost	$925K	$800K
Test Time/Touchdown	5 Sec.	5 Sec.
Test Cost / Device	2.3 cents	0.37 Cents

Conclusions

- Bring RF processing resources close to RF signals
- Use standard (modified) cantilever/cobra probe card to enable Multisite testing
- Use Mixed signal tester (LF+logic) resources appropriately
- Simplify tests, if possible (e.g. CW or EVM vs. IIP3 or ACLR) to achieve test coverage parity

Thank You

- Acknowledgements

Chris Sellathamby, Ph.D.
VP Engineering
csellathamby@scanimetrics.com

Jeff Hintzke
Dir. of Marketing
jhintzke@scanimetrics.com

Clayton Householder
Dir. of Sales
chouseholder@scanimetrics.com

Brian Moore
Dir. of R&D
bmoore@scanimetrics.com