IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

Jack Courtney – IBM
Oliver Nagler – Infineon
Jens Kober – AMD
Stu Crippen – Intel

ISMI Probe Council Probe Specification Guidelines and Cost of Ownership

June 5, 2007
San Diego, CA USA

INTERNATIONAL SEMATECH
ISMI
MANUFACTURING INITIATIVE

Overview

- ISMI Update
- CCC Standard
- COO Model Release
- RFID Format Guidelines
- Summary

ISMI Update

- New Members in Probe Council
  - Panasonic & Micron
- Work on Standards
  - Current Carrying Capacity
  - RFID
  - Probe head
  - Qualification
- ITRS Update
  - 2007 Update – simplified the tables

ISMI Members	Probe Council
AMD	M Egloff/J Kober
HP	D Gardner
IBM	J Courtney (Chair)
Infineon	O Nagler
Intel	S Crippen/R Rose
Micron	W Fister/J McBride
NEC	-
NXP	G Koch
Panasonic	T Kawamura/K Hirae
Renesas	-
Samsung	-
Spansion	A Romriell
TI	Daniels/Armendariz
TSMC	YF Jeng

Council Projects – General Principles

Objective **Provide a forum for ISMT members to share best practices in MM&P**

Approach

- Benchmark Metrics
- Share Best Practices
- Site Visits (Fab Tours)
- Networking
- Validate Industry Roadmap Direction
- Communicate Consensus Requirements to Suppliers
- Sub-teams/Focus Groups on Specific Topics of Interest
- Organize and Sponsor Workshops

Deliverables / Milestones

- Two to four council meetings/year
- Benchmarking Surveys

MC Benefit / Comp. Adv.

- Participants see best-in-class performance levels and ways to achieve them
- Accelerated productivity improvement
- Faster problem solving

CCC Measurement

- Background
  - Discussion in the Literature – "Hot" topic
    - EIA 364-70 -Current .vs. Temperature Rise - Connectors
    - Papers at SWTW
      - Kirby,Yan (Intel) – CCC characterization – SWTW 2004
      - Others in 2002, 2003, 2004, 2005
    - Bits Papers
      - Qifang Qiao – Current Rating for Contacts – Bits-2004
    - Prior research
      - Armendariz – 1997 – Characterization of Various Probe Technologies…NMSU Thesis.
  - Important Measurement with huge variability

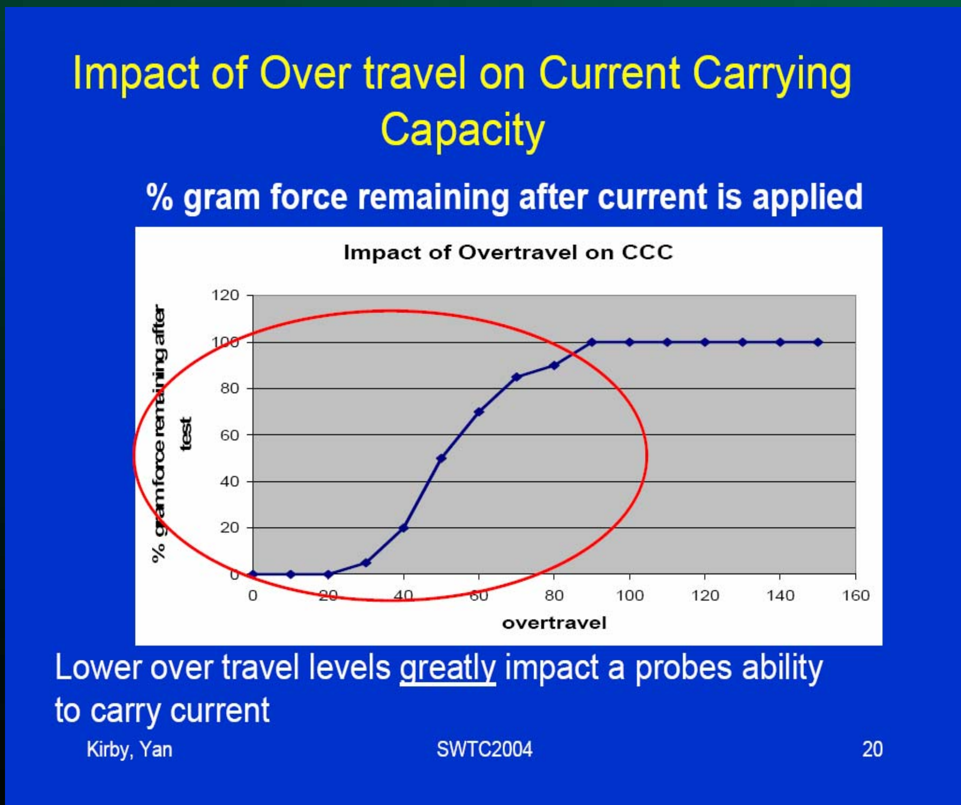
What's the issue with CCC

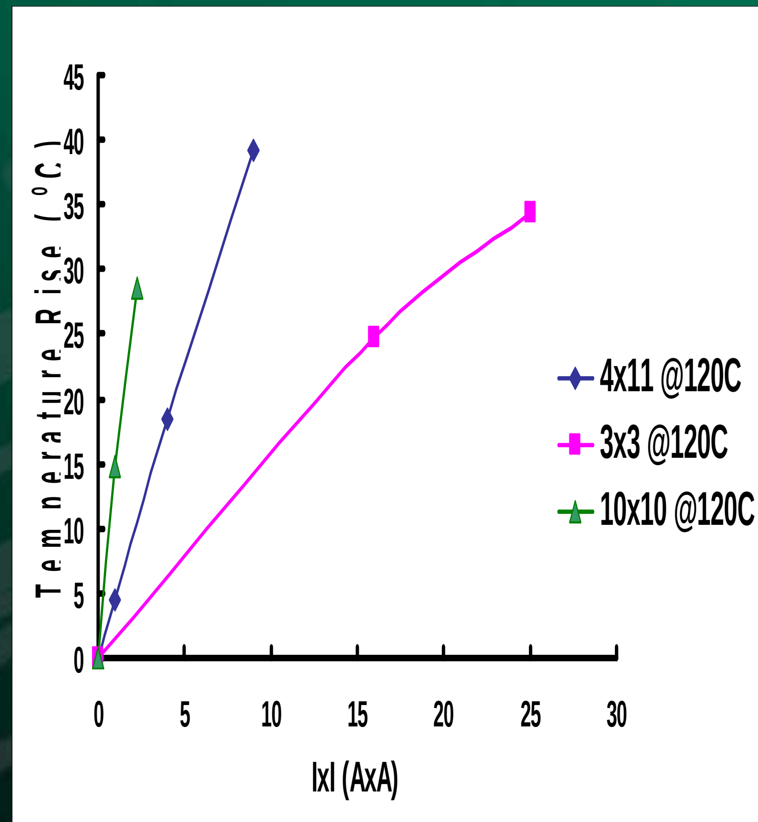
- Probe Protection - $$$
  - Significant cause of hardware failure
    - Usually power & ground
    - Many products can loose a couple power pins but..
    - Adds up eventually plus collateral damage
  - Defects – Robust CCC is always a good thing
    - Current concentration -> Defeats clamps
  - Hi Corner Testing – general trend upward
  - Hi Power Testing – > 10 amps / probe
  - ITRS – Currents continue to climb

Amps, Joules and Apples

- Sources of Variability
  - Fixturing
  - Over-travel
  - Environmental
  - Materials for contact
  - Batch
- **Translation to Production**
  - Every product is unique

Variable Data



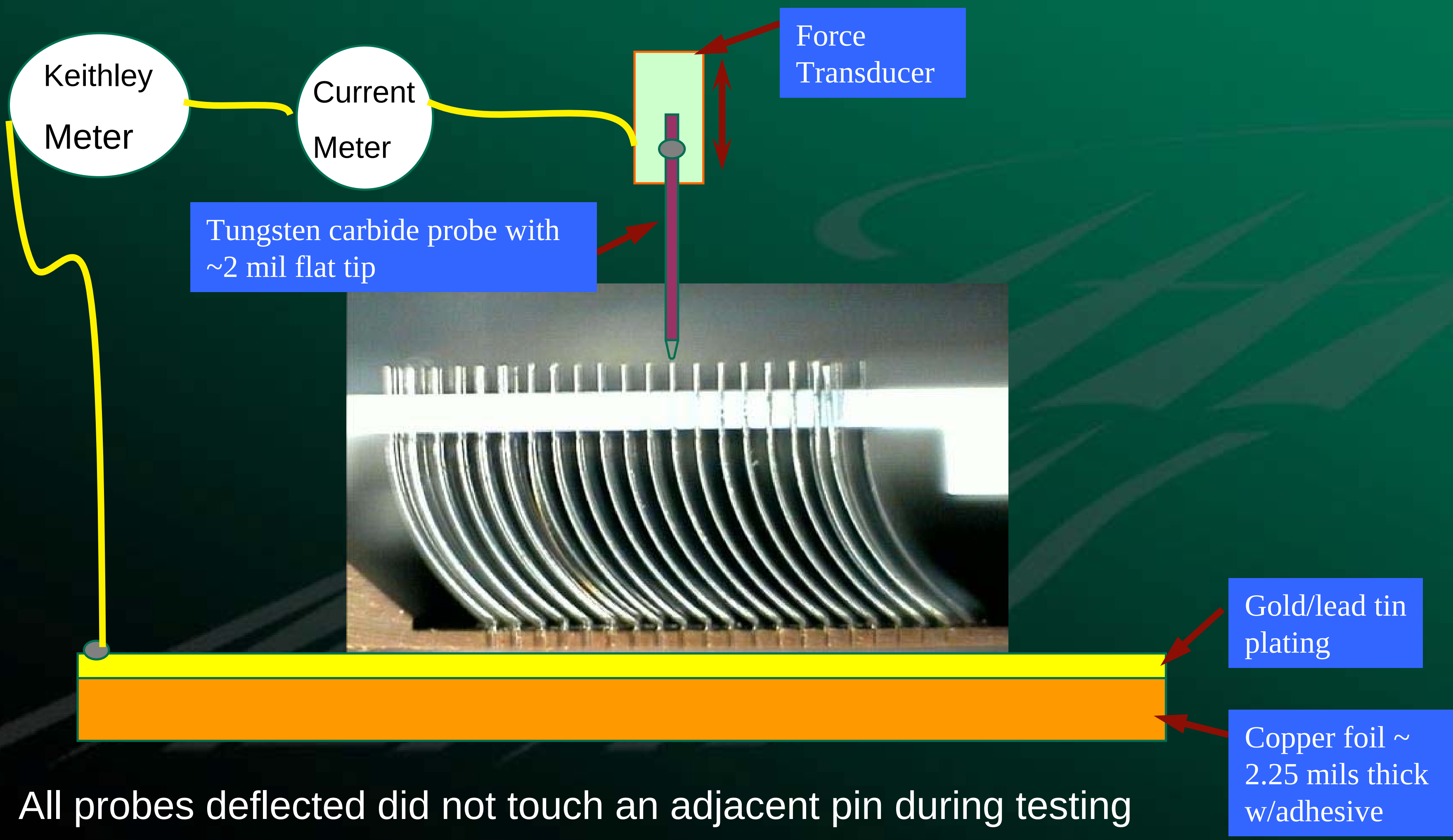


(Q Qiao, IBM, BITs 2004)

KIS

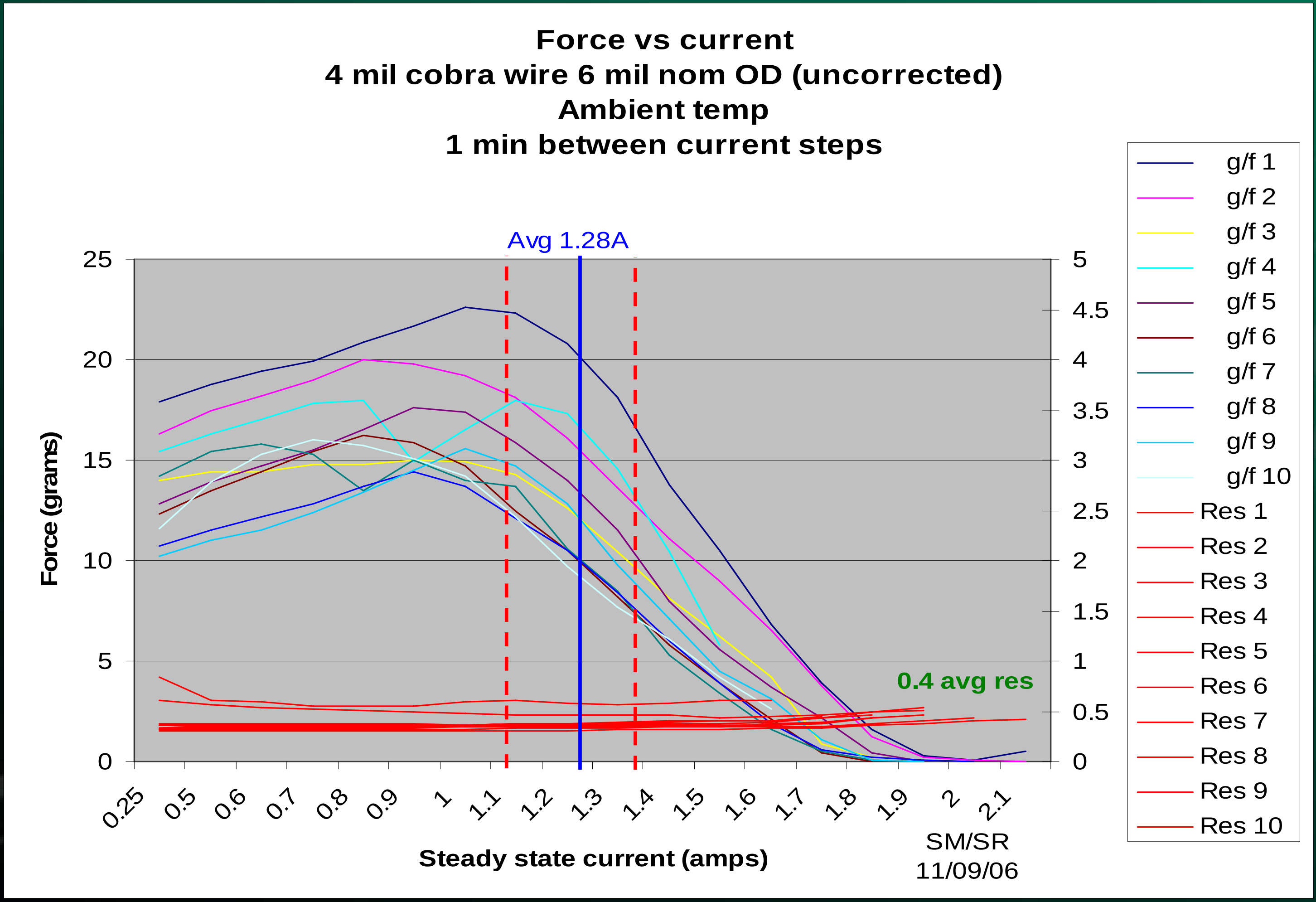
- Methodology – Keep it simple
  - One wire or needle
  - Gold interface
  - Nominal defection
  - Room temperature
  - Apply current, stop, measure force, repeat
  - Good sample size
  - 20% Reduction in force is fail signature

Setup



All probes deflected did not touch an adjacent pin during testing

Example Data



How to use this CCC

- Translation is Product specific
  - Current concentration
  - Test methodology
  - Defect mechanisms
  - Pitch and Population and geometry
- Rules of thumb – examples
  - Reduce CCC by 25 to 50% in most cases
  - All else equal, use the higher CCC probe

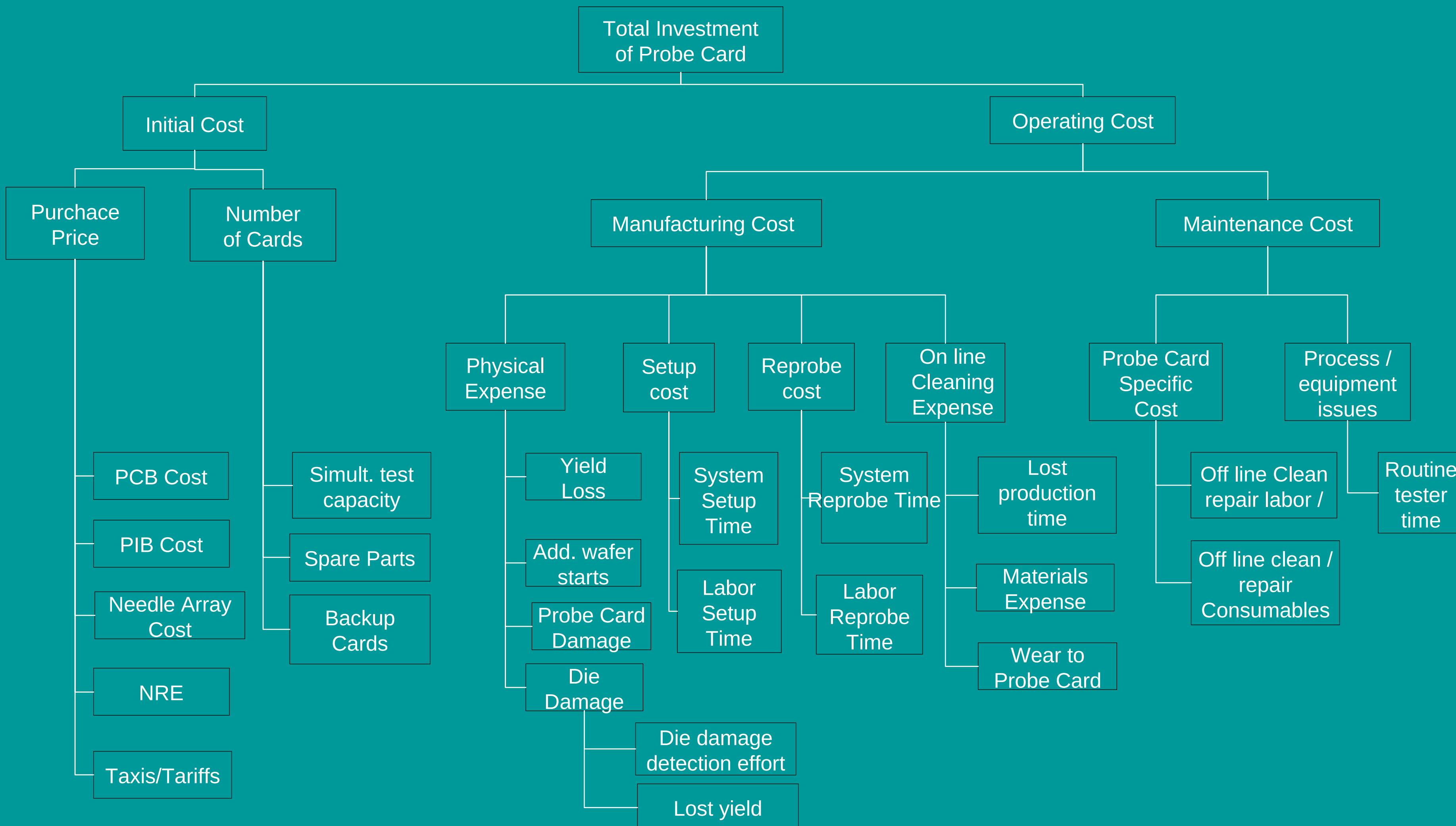
COO Model

- Background
  - Earlier Presentation at SWTW 2003
    - Oliver Nagler
  - Feedback – Public Access needed
- Iterations of model
  - Infineon – pre-loaded with specific vendors & methodologies
  - Probe Council – removed probe specific data
  - Public release – updated and user friendly

COO Description

- COO is used to support decisions involving computing systems, laboratory, testers and manufacturing equipment, for instance.
- Calculates total costs over a specific time period
- Includes the 'hidden' costs, e.g. maintenance, cleaning, yield, and installation
- Provides the tool to assess and manage the cost impact of changes in technology, sourcing and support strategies

COO Flowchart



Elements of COO

Version 15

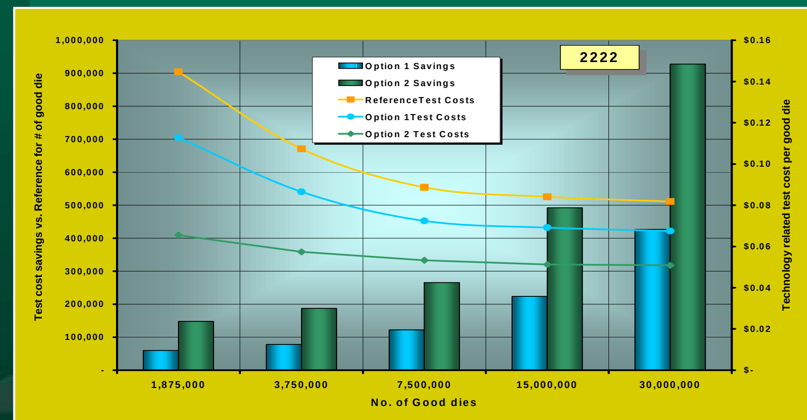
Parameter	Unit	Value
Product Specification		
Internal Product Name	-	2222
Dies per wafer	-	600
Die length	mm	5.00
Die width	mm	5.00
Min. Pad pitch	µm	80
Die contact	-	WB
Pad thickness / Bump height	µm	1000
Bump Diameter	µm	-
Pad / Bump material	-	Al
Pad layout	-	peripheral
Pad length	µm	70
Pad width	µm	70
Probing Parameters		
# of pads contacted	-	200
Test temperature (Max)	°C	25
No. of low speed RF lines (<3Ghz)	-	0
No. of high speed RF lines (3 - 10 GHz)	-	0
Maximum current (continuous)	mA	100
Maximum current (peak)	mA	200
Bandwidth	MHz	100
No. of components req'd on the PC	-	0
Operating Data		
Tester model	-	J750
Prober model	-	UF200
Test Category	-	digital
# of DUT's	-	4
Test time per die	s	6.0
# of wafers per lot	-	25
Productive Data		
Product life cycle	weeks	90
Total # of good die	-	30,000,000
Expected yield	%	95%
Cost of wafer (processing)	$	2000
Ave. # of probers per operator	-	5
Prober operator cost per hour	$	20.00
Pcard technician cost per hour	$	40.00
Ave. cost of tester time per second	$	0.03
Wafer inspection,points per wafer	-	3
Wafer inspection,time per point (seconds)	s	30.00
Tester working time per week (hours)	h	120

Notes:

Mandatory Input Field
Optional input field

Probing Technology	Unit	Reference
Preferred Vendor	-	**Supplier A**
Typical probe card life	# of TD's	1,000,000
Cleaning frequency	# of TD's	200
Cleaning cycle duration	s	20
Maint. cycle	# of TD's	10,000
Maint. exp. (mat'ls, equip., ...)	$	$200.00
Maint. time	min.	90
Pcard rebuild frequence	# of TD's	500,000
Probe card mishandling loss	%	2.00%
Retest Rate	%	3.00%
Yield loss - pad damage	%	0.20%
Yield loss - Cres	%	0.0%
Ave. pcard setup time	min.	30.0
Wfr inspect. freq	n wafers	10

Input Sheet



Cost Element	Reference	Option 1	Option 2	Comments
# of DUTS (w x 1,2,4 etc)	4	4	4	
Number of lots per setup	3	13	53	
Average cost per die		3.52		
Ave # of testers per week		2		
Ave. Weekly run rate (die ek)		333.34		
Total die probed	31,642,232	31,610,558	31,585,264	total good die required / elect yield per card technology / mech yield per card technology
Run rate per week	351,580	351,228	350,947	total die probed / product life cycle
Ave # of probe cards utilized per week	2.00	2.00	2.00	weekly run rate * test time per die) / # of DUTS per card per week
Add. # of probe cards required over life time	6.00	6.00	2.00	= total die probed / typical probe card life rounded up # of DUTS per card
Percentage of cards underutilized	1.49%	1.62%	-194.82%	= % of probe cards (or probe heads) used for less than full life
% usage of underutilized card	291%	290%	295%	= for card underutilized, %age (if life in touchdowns) it is used
Probe card purchase price	$29,759	$23,226	$0	Pcard: Initial purchase price for vertical this is replaceable "core" cost
Probe card board price	$5,000	$5,000	$9,000	For Pyramid the PCB board is reuseable, cores are replaceable
NRE Charge, one time	$0	$2,419	$12,545	Any NRE for the current or alternative probe technology should be input above
Cost of pcard mishandling	$ 595	$ 232	$ -	Design/robustness of "Alternatives" prevents damage by most simple handling errors
Total initial probe card costs	$ 282,834	$ 230,084	$ 48,545	(Card price(assembled) or vert.core+pcb cost * Qty req'd + one time NRE
# of backup cards or replaceable heads	1	1	1	
Cost of backup capability	$ 34,759	$ 23,226	$ -	
Initial purchase cost	$ 317,593	$ 253,310	$ 48,545	Complete card for cantilever,probe head only for other
Probe card rebuilds required	1	1	1	"Current" requires total rebuild - "alts 1&2" eg vertical require core replacement only
Probe card rebuild cost	$ 34,759	$ 23,226	$ -	
Maintenance cycles	790	157	38	= probe life (touchdowns) / maintenance cycle (touchdowns) - 1
Probe card maint. - material cost	$ 158,011	$ 15,705	$ 385	= ext charge or exp. for internal supplies, space, equip, depreciation, etc. per maint. cycle
Probe card maint. - labor cost	$ 47,403	$ 9,423	$ 257	= Internal labor cost: maintenance time * probe card technician cost per hour
Offline maint. cost	$ 240,174	$ 48,354	$ 641	
Number of wafers	52,737	52,684	52,642	
Required total setups	791	158	39	total # of lots / setup per # lots (per pcard type)
Probe set-up - labor cost	$ 7,911	$ 1,581	$ 395	= no. of required setups * Setup time in hours * labor cost per hour
Probe set-up - tester time cost	$ 42,717	$ 8,535	$ 2,132	= Average cost of tester time * Setup time (sec) * no. of setups
Tester set-up cost	$ 50,628	$ 10,115	$ 2,527	
Online Probe cleaning cycles	39,553	15,805	1,579	= probe life (touchdowns) / touchdowns between cleanings / # of DUTS per card
Probe tip cleaning - labor cost	$ 879	$ 351	$ 35	= # of cleaning cycles * cleaning cycle time * operator cost / # of probers per operator
Probe tip cleaning - tester time cost	$ 23,732	$ 9,483	$ 948	= # of cleaning cycles*cleaning cycle time* avg. cost of tester time per sec
Online cleaning cost	$ 24,611	$ 9,834	$ 983	
# of reprobed die	949,267	632,211	157,926	= reprobe % * total number of die probed with single-DUT probe card
Reprobe - labor cost	$ 6,328	$ 4,215	$ 1,053	= no. of die reprobed * test time per die * prober operator cost / # of probers per operator
Reprobe - tester cost	$ 170,868	$ 113,798	$ 28,427	= no. of die reprobed * test time per die * tester cost
Reprobe(selective retest)	$ 177,196	$ 118,013	$ 29,480	
Wafer inspection - labor	$ 2,637	$ 1,054	$ 263	= no. of wafers inspected * time per inspection * labor cost
Wafer inspection - tester time	$ 4,746	$ 1,897	$ 474	= no. of wafers inspected * time per inspection * cost of tester time
Mech. yield loss (pad damage)	$ 211,371	$ 105,580	$ 21,099	good die rejected with Cantilever versus with alternatives
Cost of test time	$ 1,423,900	$ 1,422,475	$ 1,421,337	= no. of die * test time per die * tester cost / # of DUTS per card
Relative elect. yield loss	$ 2,564	$ 1,138	$ -	relative to most cost effective option
Total tester hours used	15426	14409	13457	
Probe Card Related Costs	$ 1,028,955	$ 548,156	$ 104,011	
Total Probe Cost of GOOD die required	$ 2,452,855	$ 1,970,632	$ 1,525,348	
Cost savings	$ -	$ 482,224	$ 927,507	
Total Probe Cost Per Million Good Die	$ 81,762	$ 65,688	$ 50,845	
Cost savings per Million Good Die	$ -	$ 16,074	$ 30,917	
Total TEST Cost Per Good Die	$0.08	$0.07	$0.05	

Calculation

Cost Calculation

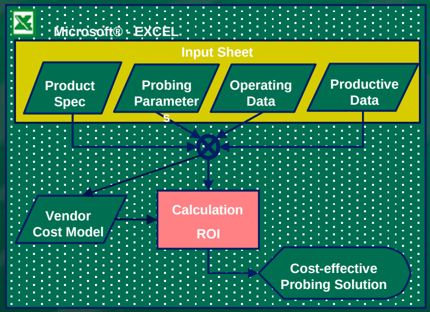
- Initial probe card costs +
- Total purchase cost +
- Probe card rebuild cost +
- Offline maint. Cost +
- Tester set-up cost +
- Online cleaning cost +
- Reprobe cost +
- Mechanical yield loss +
- Relative electrical yield loss

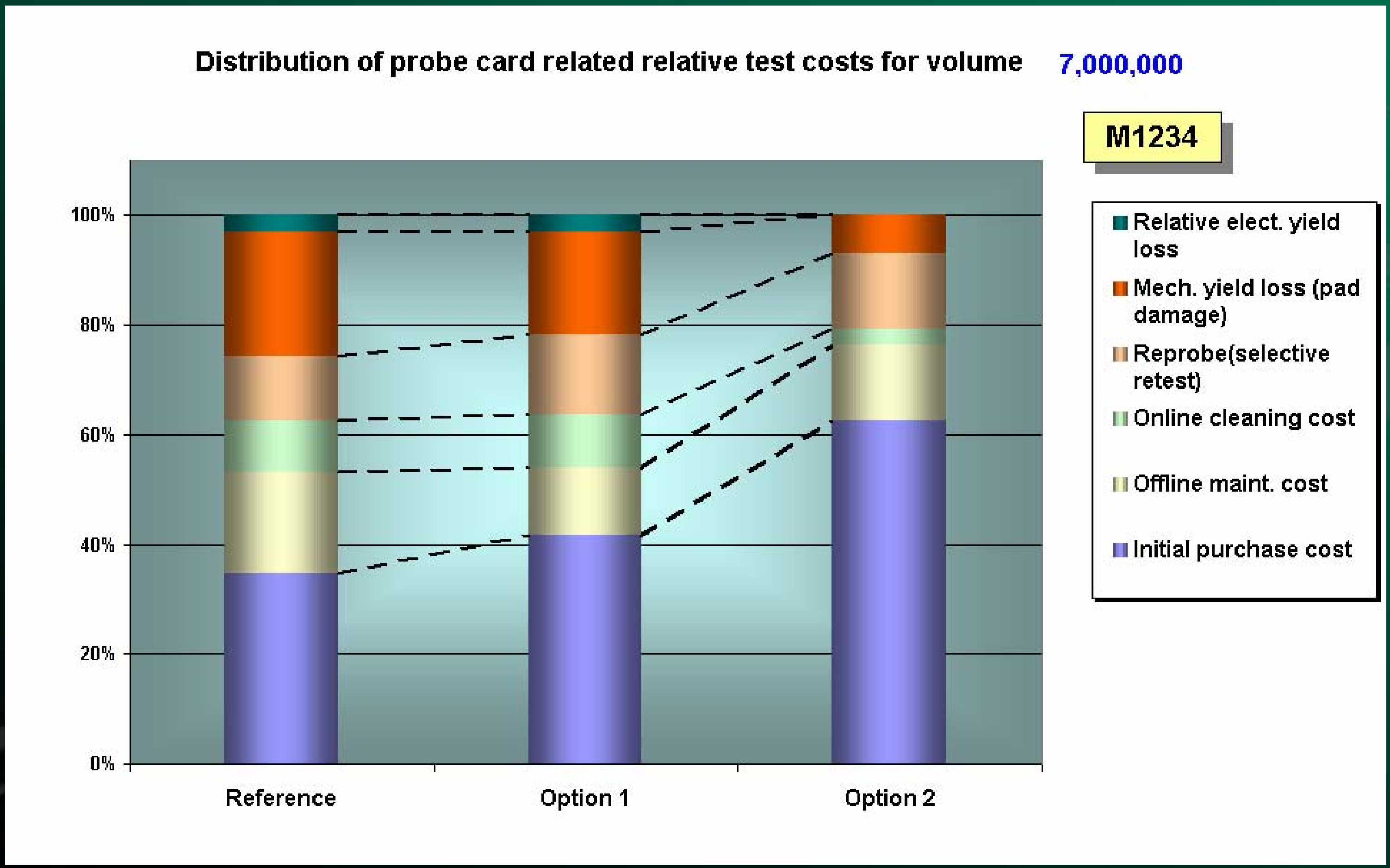
=

- Probe related Costs +
- Cost of test time

=

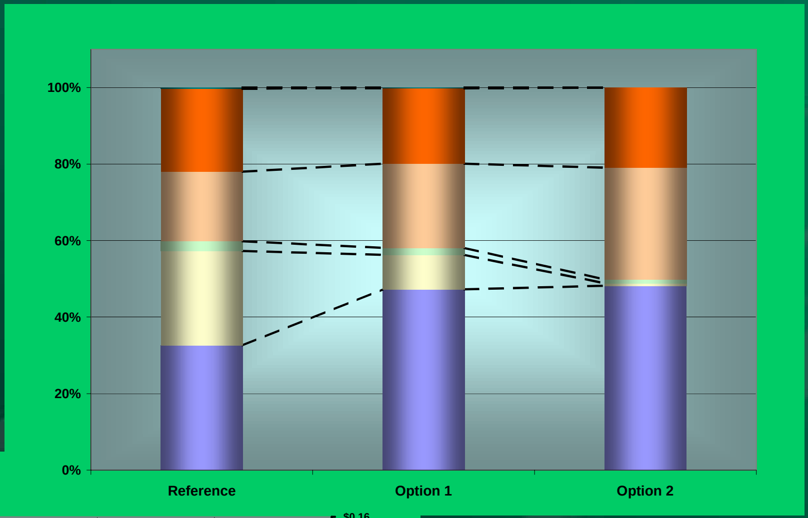
- Total Probe Costs

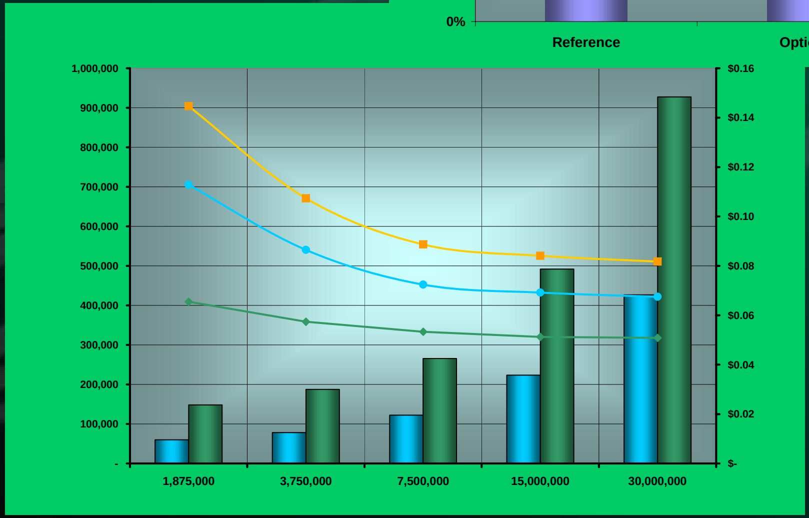



Distribution of probe card related relative test costs for volume 7,000,000
M1234
100%
80%
60%
40%
20%
0%
Reference
Option 1
Option 2
Relative elect. yield loss
Mech. yield loss (pad damage)
Reprobe(selective retest)
Online cleaning cost
Offline maint. cost
Initial purchase cost

Example

- High pin count (200)
- High volume (>10 Mio.)
- 4-DUT
- Target Yield 95%
- No RF-pins
- Long test time (6sec.)
- No Cres-related Yield loss
- Max. Retest rate 3%





Access to COO & CCC

- Contact Tom.Wear@ismi.sematech.org
- Package includes direction
- Available starting 7/1/2007
- CCC Guideline available through ISMI webpage
  – www.ismi.sematech.org

RFID

- **Motivation**
  - Error free, automatic probe tracking
    - Location and configuration
    - Touchdowns and repairs
- **Scope**
  - Guideline for data standard
  - System architecture discussion
  - Not an implementation guide

Data Standard

- **Description**
  - 16 data fields or “pages” – 8 characters each
  - Page 1 – Read only serial number
  - Pages 2 – 16 – Read & write
    - Part numbers and serial numbers
    - Probe head or spider numbers
    - Polish and cleaning cycles
    - Touchdowns

Use

- **Qualification** - Initialize id and cycle count info
- **Setup** – Verify correct probe card at tester
- **Production** – Touchdown and cleaning cycles automatically updated & Inventory control
- **Maintenance** –
  - Update spider/head id
  - Update maintenance cycle count
  - Verify ID for metrology files

Access

- Go to the ISMI homepage
- www.ismi.sematech.org
  - Publications
  - ISMI Publications
  - White papers
- Feedback welcome
  - Contact Tom Wear
    - Tom.Wear@ismi.sematech.org

Future Work

- Probe Head Standard
- Probe Qualification Guidelines
- Technology Dev

Thanks for your Support !

- IBM – Sam McKnight
- TI – Boyd Daniels, Norm Armendariz
- ISMI Member Companies