IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

Azul Systems Inc
Wentworth Laboratories Inc

Challenges of Vertical Probing for the 48 Core 11,700 Bump Count Vega2 Processor

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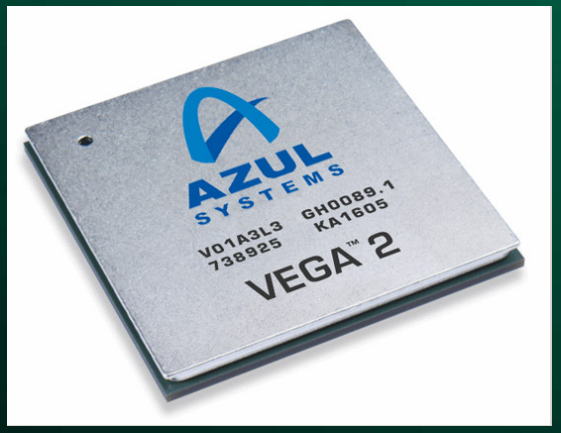
Outline

- Describe Vega2 Multi-Core processor
- Probe Interface Board and Probe Card design
- Probing challenges of the Vega2 processor
  - PC Board Flexing due to probing 11,700 bumps
  - Prober considerations
  - High Power Challenges
  - Hardware Bring-up challenges
  - Maintenance challenges
- Techniques to reduce impact of high power
  - Fully populated probe card
  - Test Pattern Partitioning
- What challenges lie ahead?
- Summary

Vega2 Processor



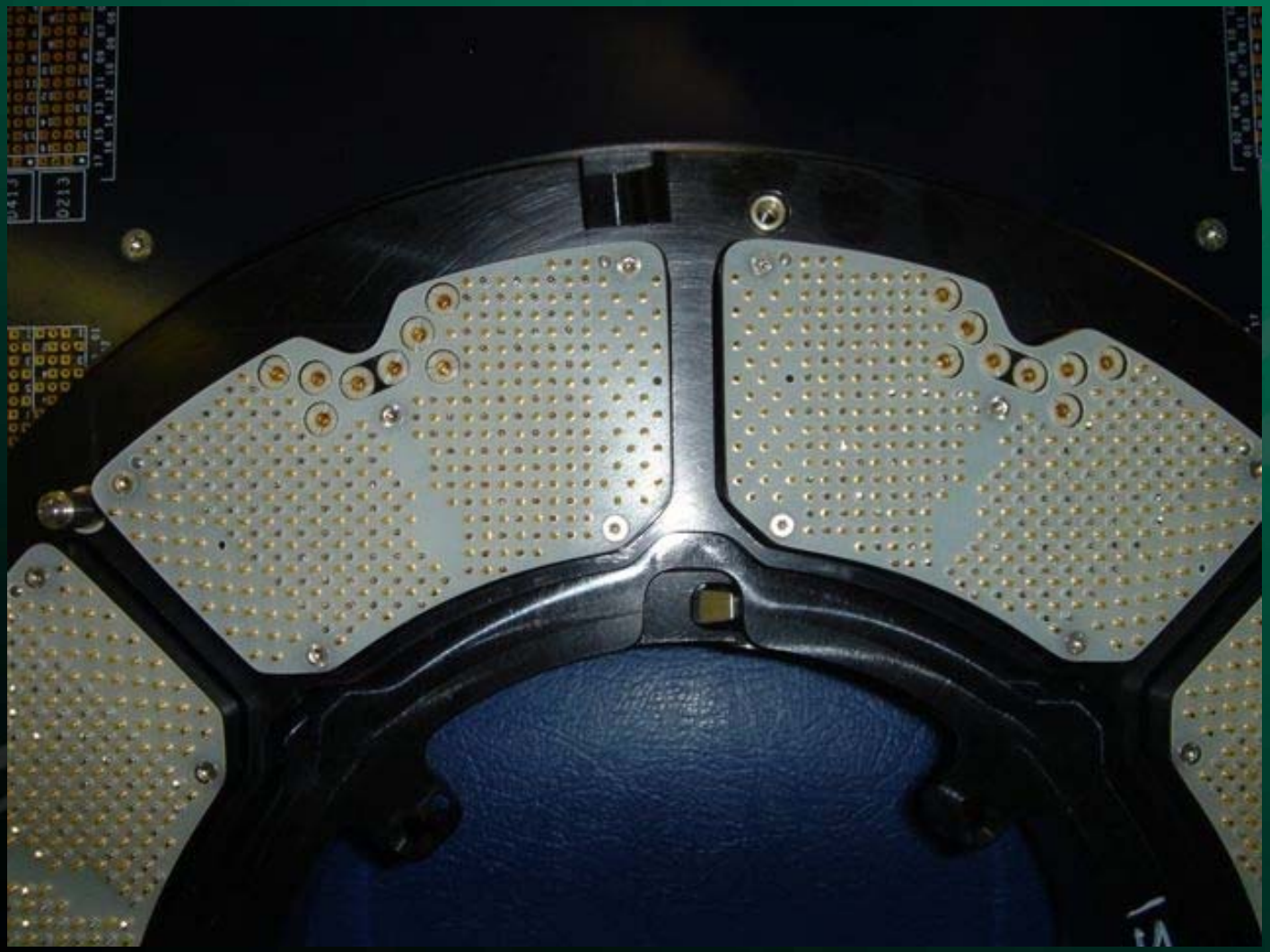
The Multi-core Vega2 processor designed by Azul Systems consists of following:

- 48 Cores
- 812 Million Transistors
- 90nm LowK technology
- 11,700 bumps, 175um bump pitch
- 976 IO + 10,700 Power and Ground bumps
- Die Size of ~20mm on each side.
- Max Power Design Requirement in excess of 120A

Hardware Interface Design

- Complete redesign of the hardware interface
  - Probe Interface Board Design
  - Probe Card Design
- The new interface can handle up to 200A current.
  - Power supply interface modified to high current capable plugs.
  - Beefed up power planes on all PCB's
  - Two 100A High current DPS ganged to supply upto 200A current
- Multi-Company project to redesign the existing Verigy P1000 Wafer-Sort Interface to handle high current demand
  - Azul Systems, Wentworth, Verigy and ISE worked together

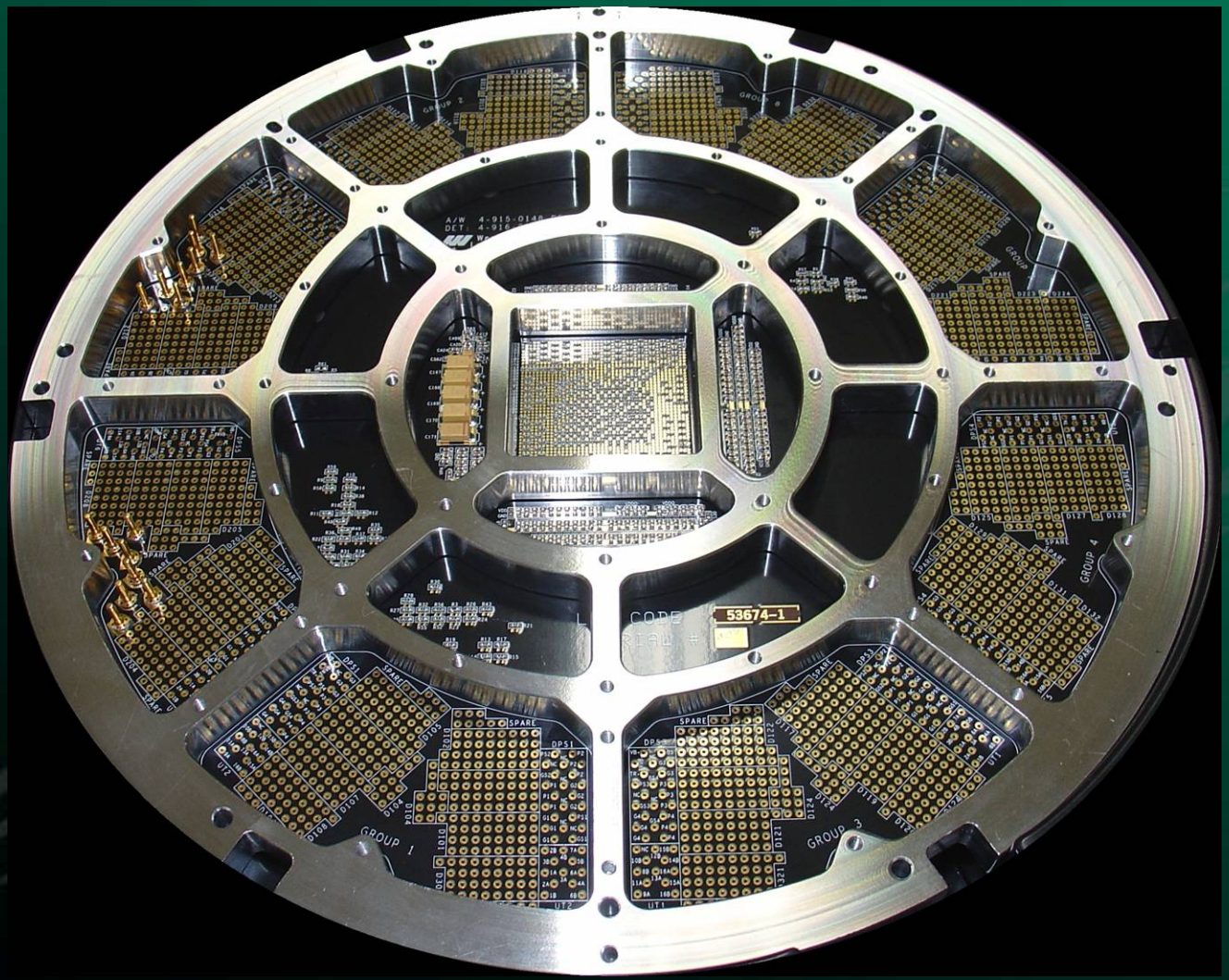
High Current Pogo Tower



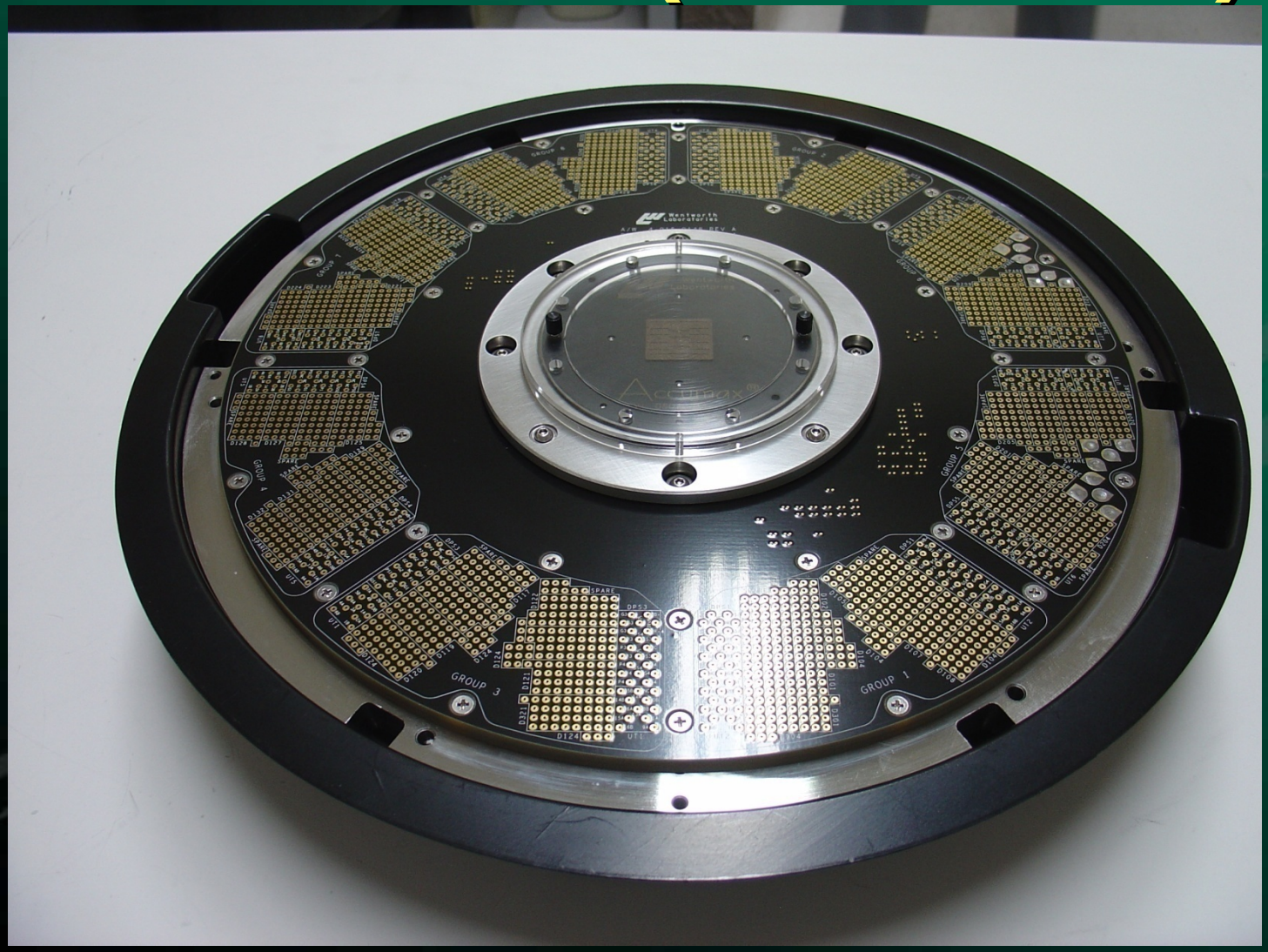
Probe Card Design

- Fully populated probe card with 11,700 probe tips using patented Wentworth Accumax probe technology.
- Probe Card PCB Stiffener redesigned to ensure proper vertical deflection is achieved under high load conditions of close to 85kg of force.

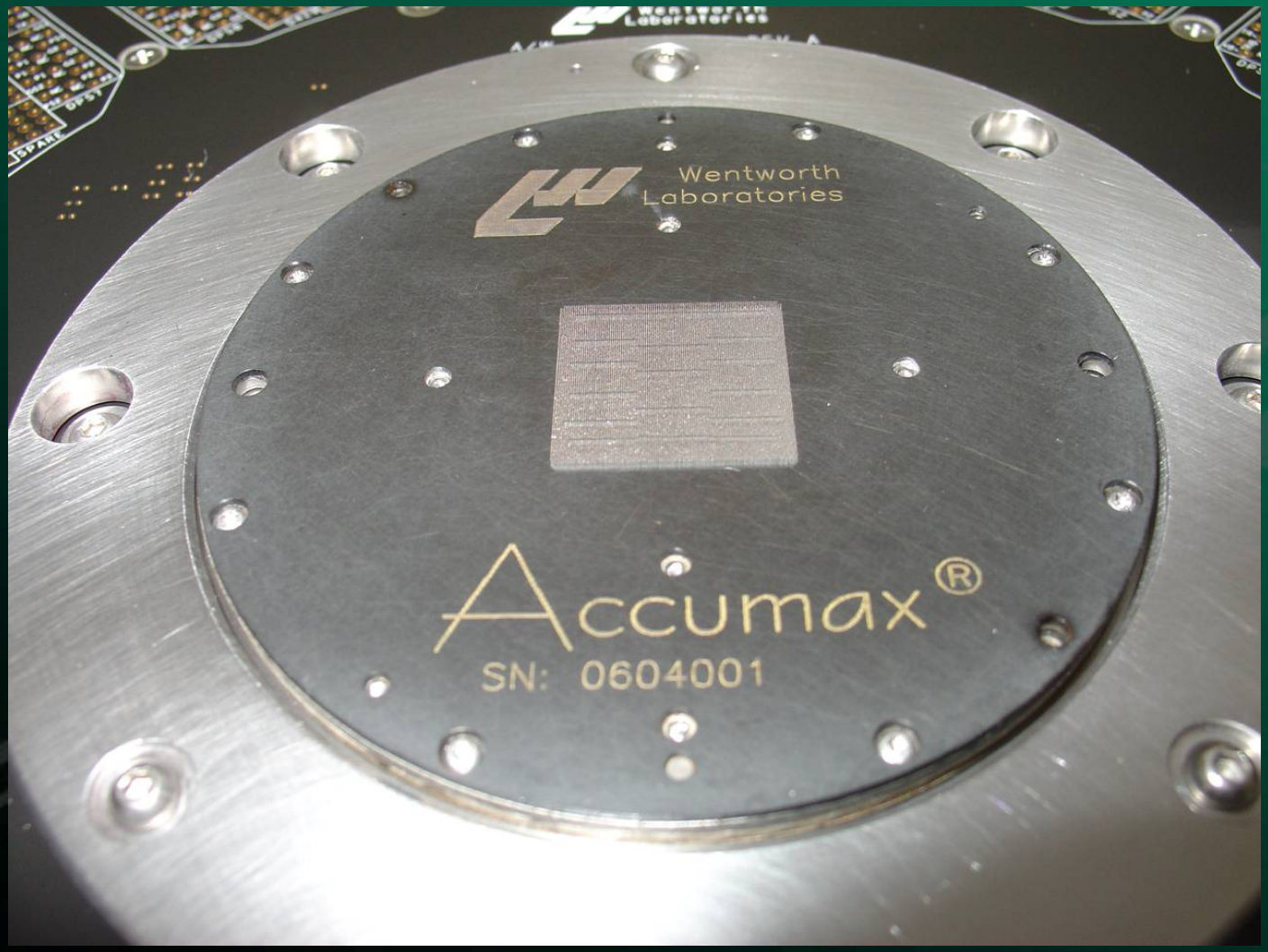
Probe Card Stiffener



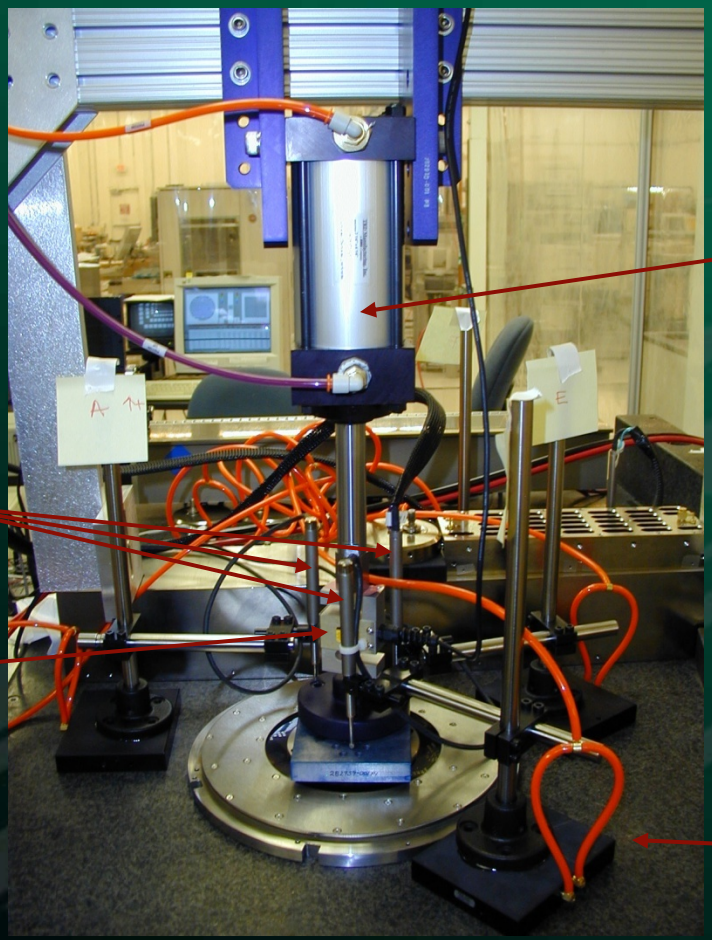
Probe Card (Probe Side)



Probe Card Head



Force vs. distance setup



Pneumatic Piston

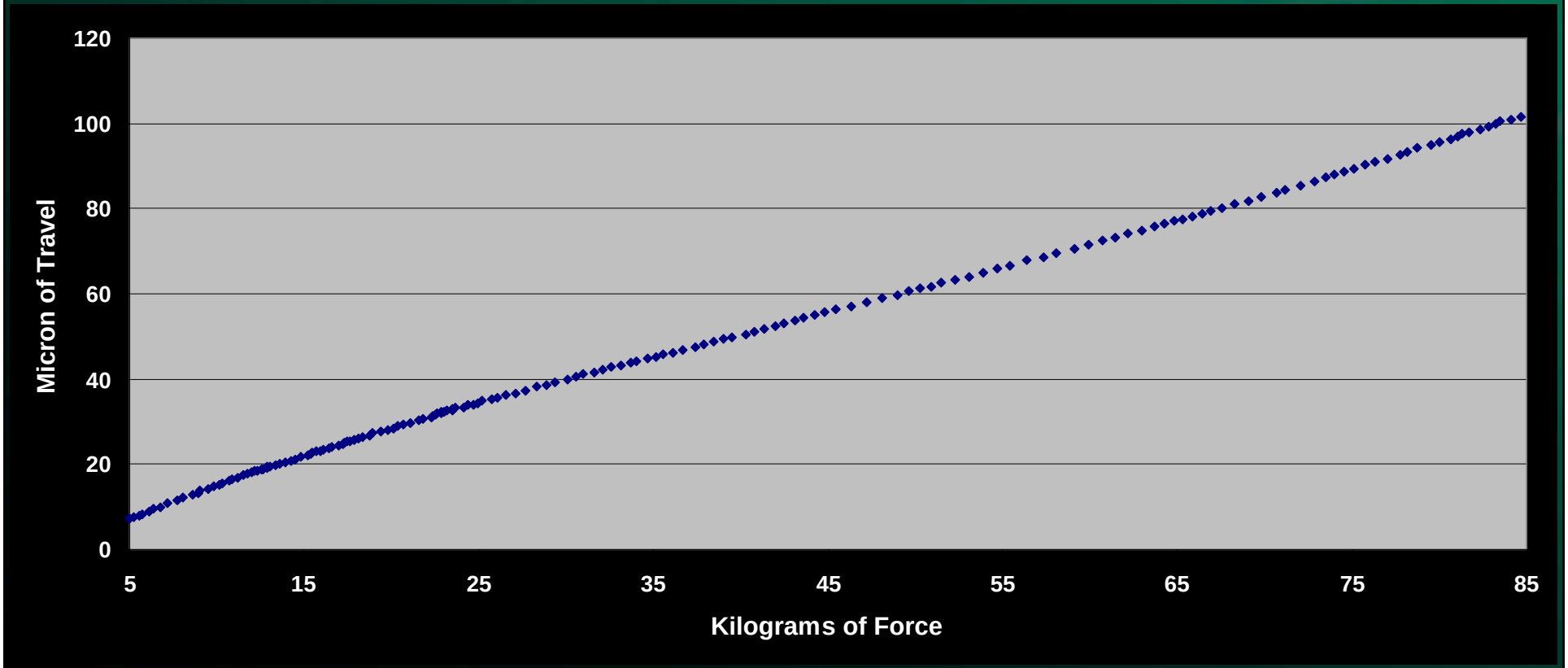
50nm resolution scales

4.536g resolution force gauge

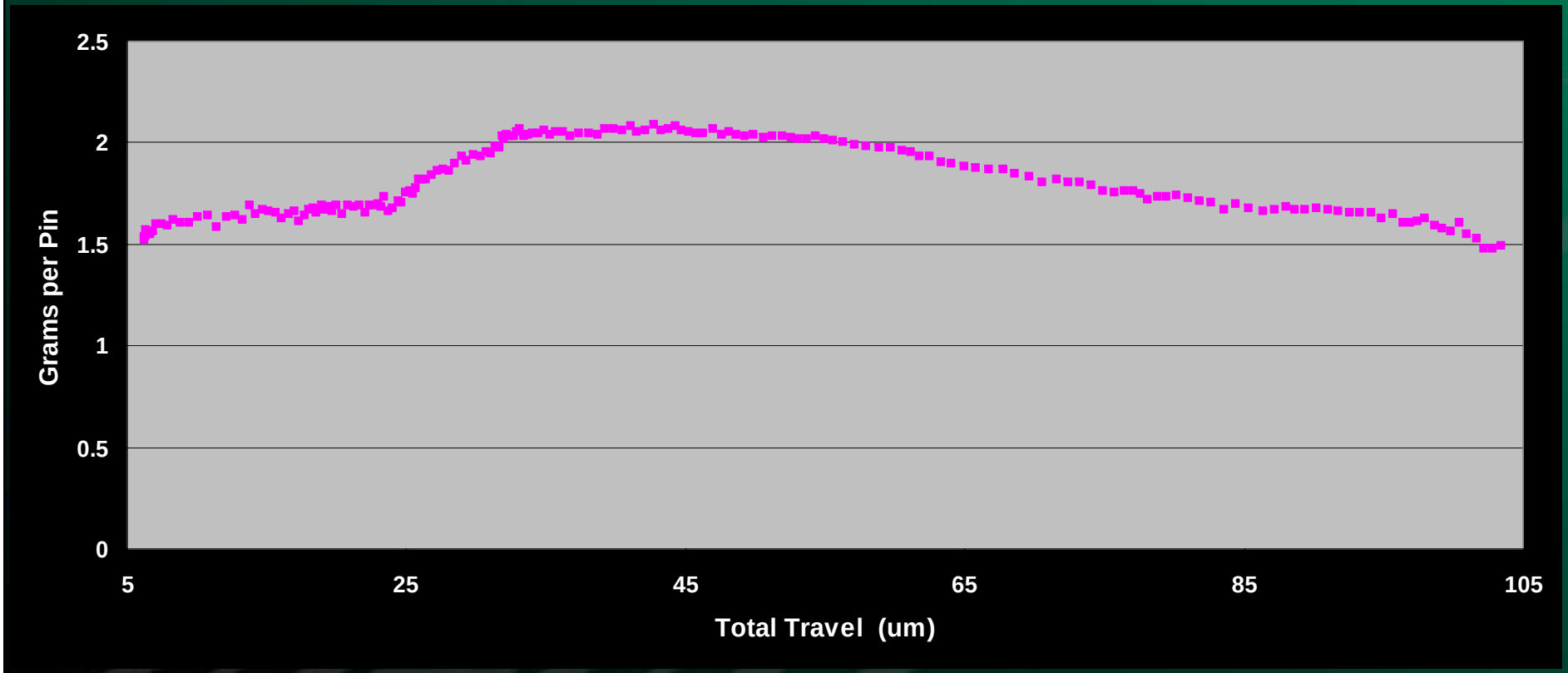
Vacuum Bases

Total Probecard Force

Azul Vega2 Card



Grams per pin vs. Travel



Prober considerations – high pin count probing

- Azul card present a load of 85 kg @ 100um OT in a 400mm/sq area.
  - – Assumes 75um of overdrive after last touch + 25um to overcome planarity with 1.5 gm/mil of probe force.
  - – Future cards can have as much as 135 kg of force required to probe using the above conditions.
  - – Cards with less compliant pins or probes (assume 3.5 gm/mil) with this pin count can exert 164 kg to 237 kg.

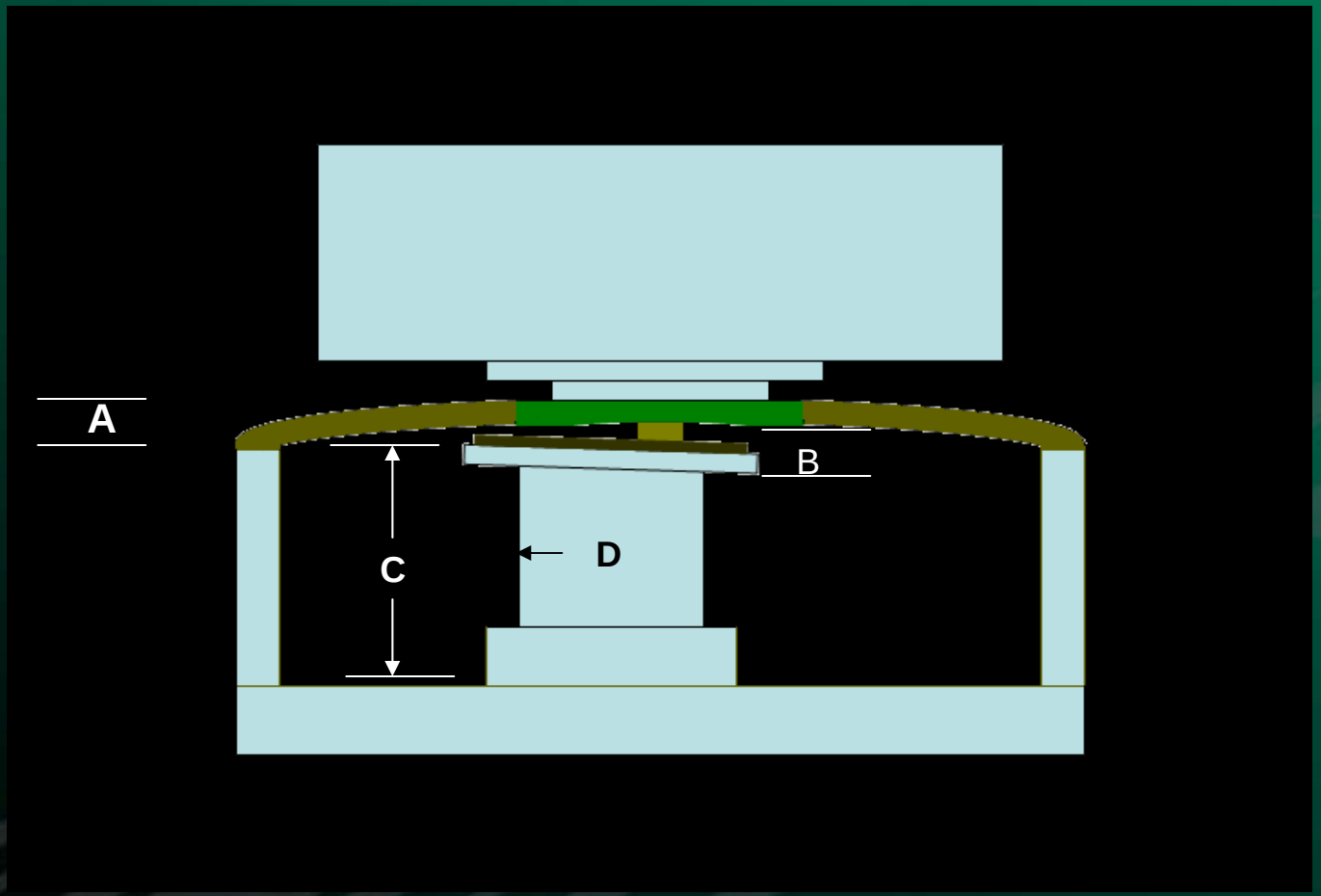
Prober considerations – high pin count probing

- Risks in not obtaining desired overtravel after electrical contact. (especially for high current probing)
  - Burnt pins
  - Decrease in yield
  - Increased repair costs
  - PCB and substrate damage
  - Less cleaning than one expects or calculated

Sources of Mechanical Compliance

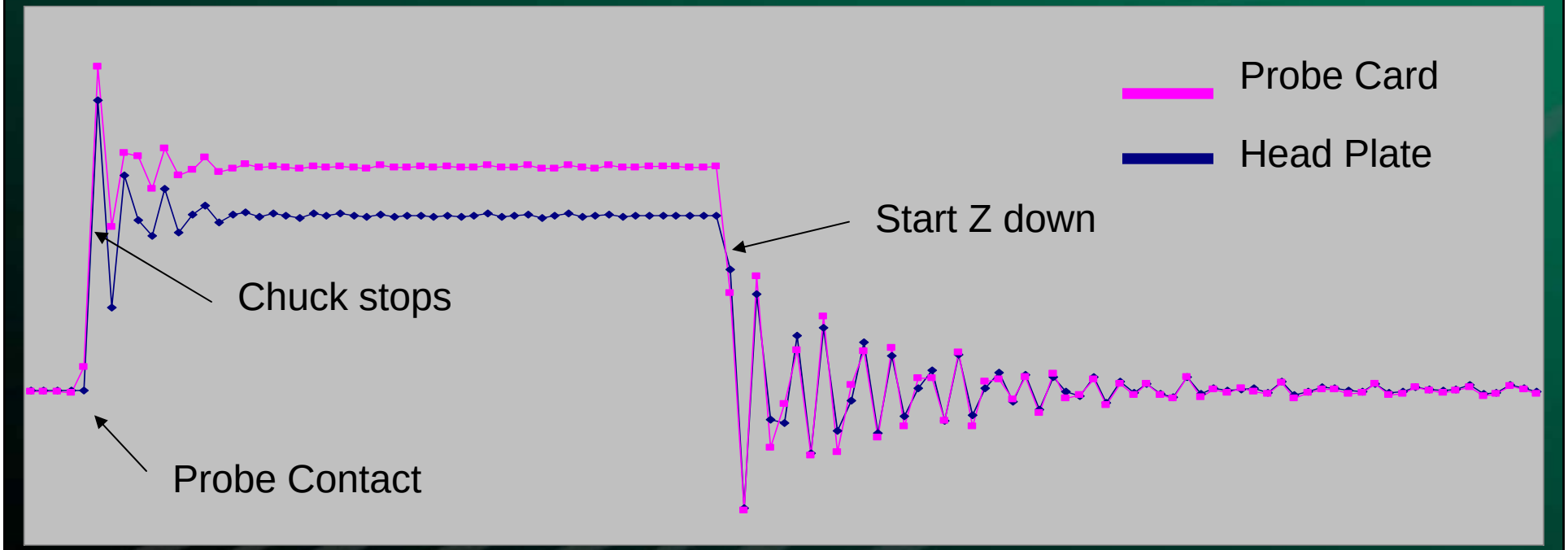
- Tester Interface
- Head Plate
- Probecard
- Chuck deflection
- Chuck and Stage compression
- Horizontal Stage Displacement

Mechanical compliance in Probing

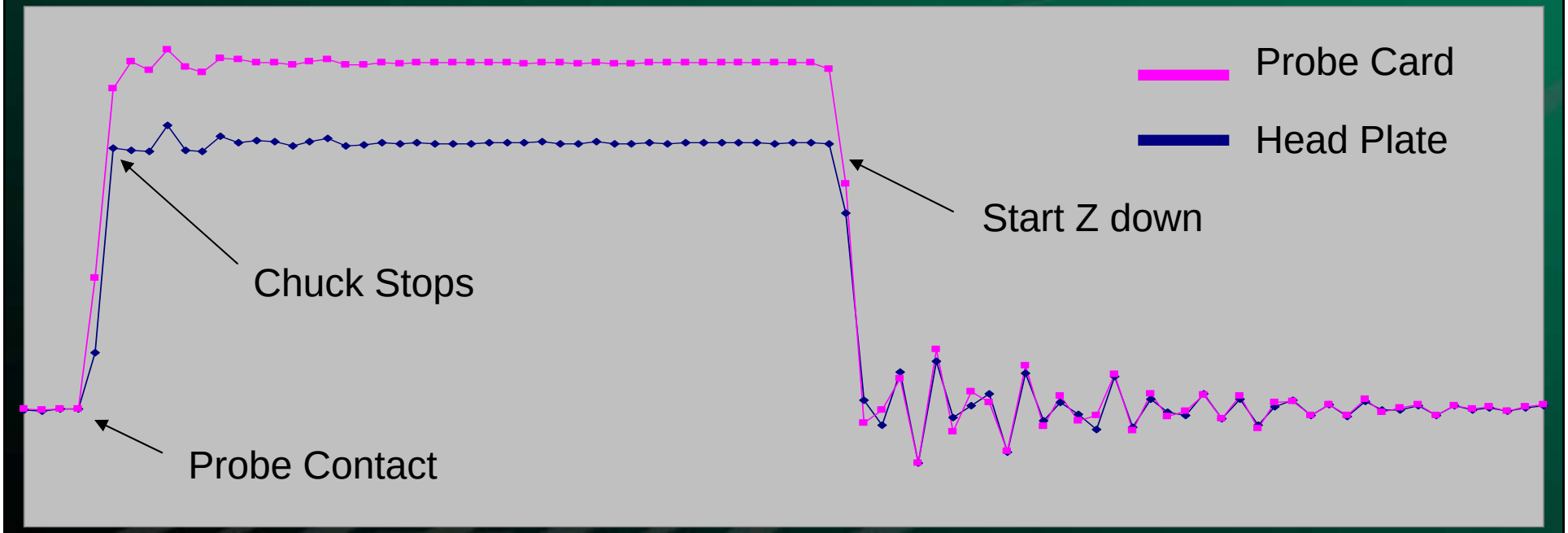


A. Head plate and probe card **B. Chuck deflection**
C. Stage compression **D. Horizontal displacement**

Head Plate and Probe Card motion with normal Z contact



Head Plate and Probe Card motion with MicroTouch ™



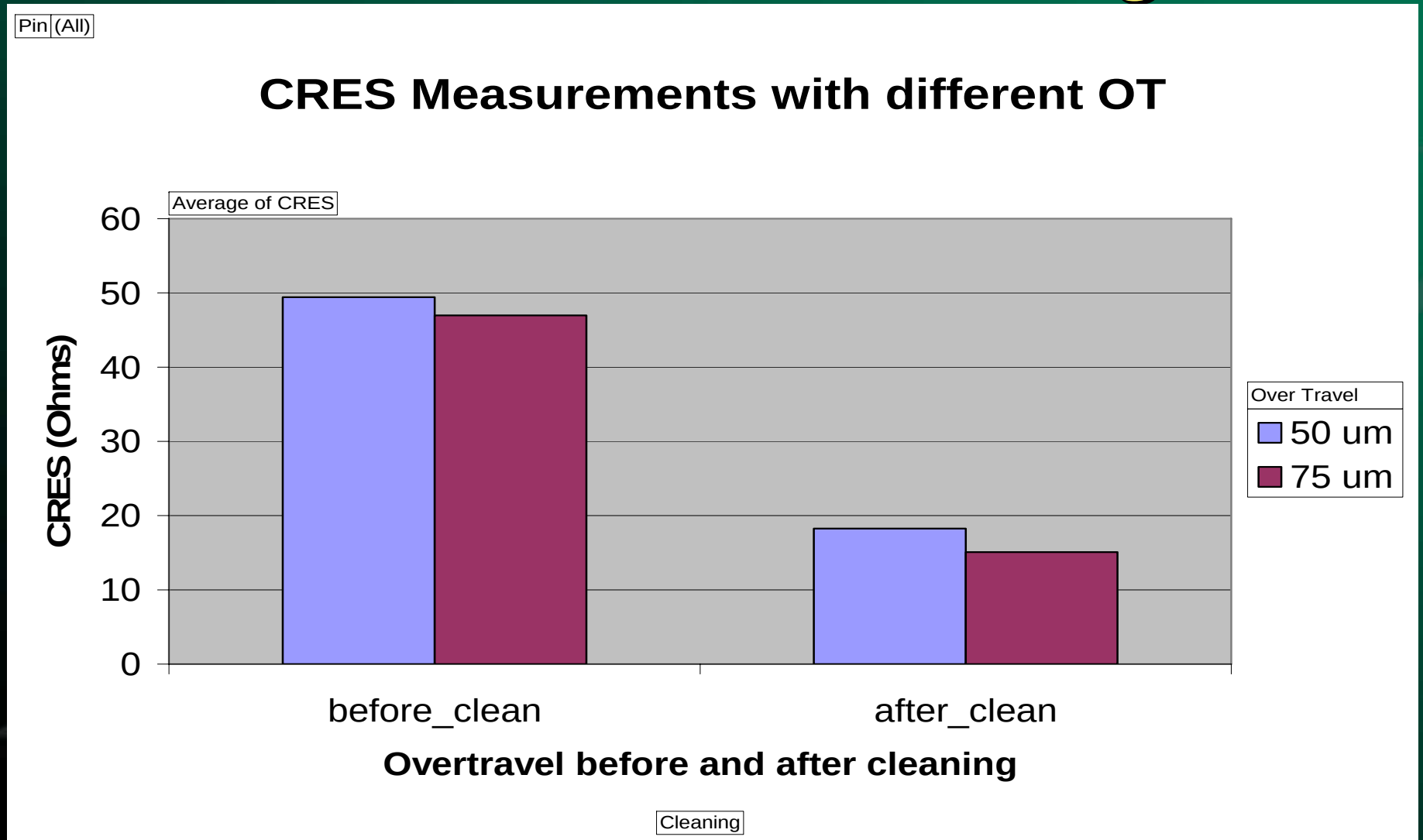
Choice of prober becomes critical

- Choose a manufacturer who will share their data with respect to chuck performance (compression, deflection, Z performance as Z approaches the point of contact – deceleration).
- Choose one that will support the amount of force of the probe card with margin (i.e. If the force after all overdrive is applied will be 130 kg, consider choosing a prober with a 200 kg spec).
- Choose one that has a good temperature control

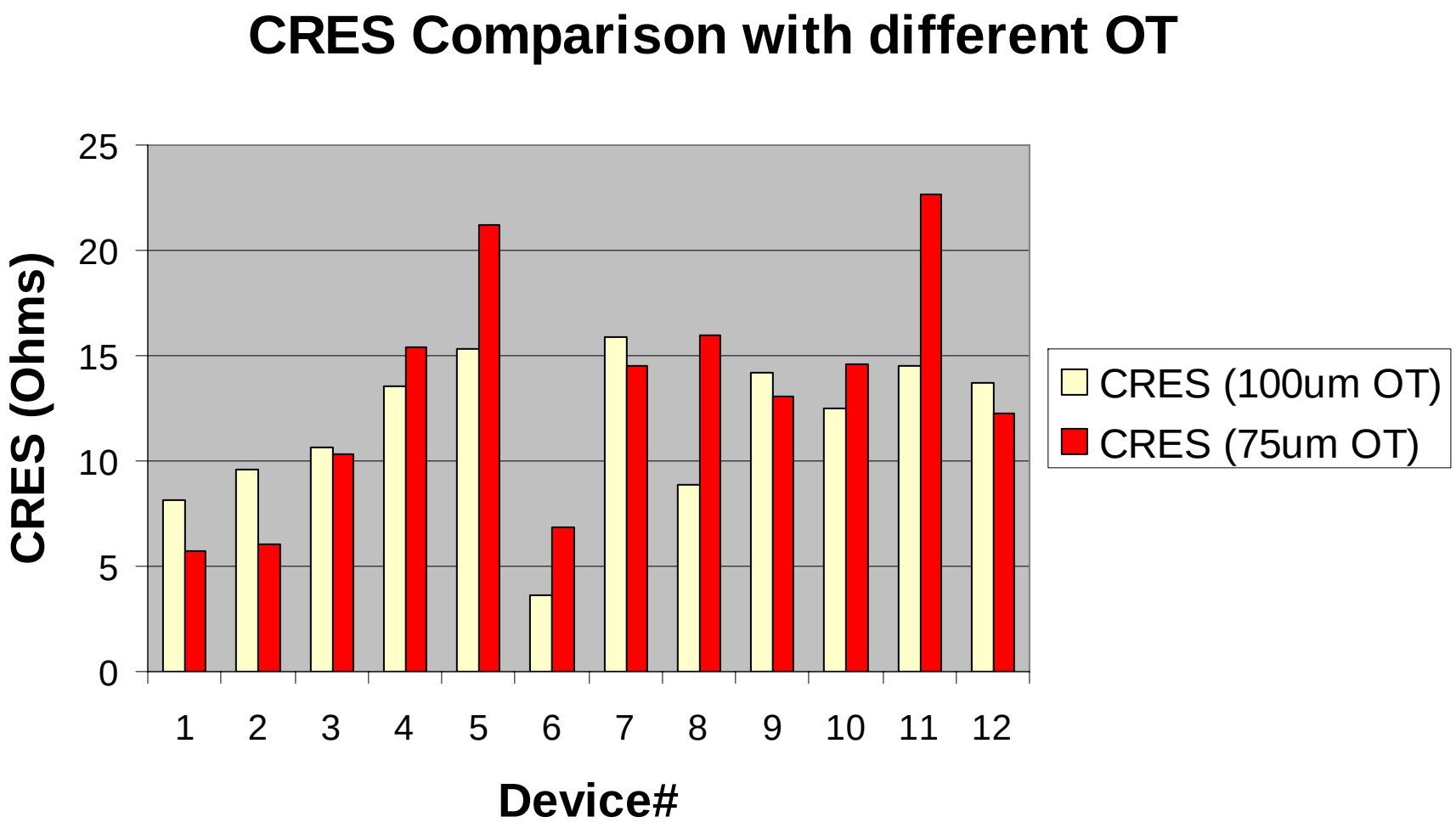
Probe Card Cleaning

- How often do we need to clean?
  - Collected online boundary scan data
  - Boundary scan patterns to measure VOL
  - Total Cres = Vol/Iol – Buffer Impedance
  - Probes cleaned at the start of each wafer
    - Got rid of oxide build-up on the probe tips.
  - Over-travel increased to reduce Cres.

Probe Card Cleaning



Over-travel Analysis



Test Pattern Partitioning to Reduce Power

- Testing all sections of the chip in parallel has issues:
  - Higher current demand on the supplies
  - Higher heat generation due to simultaneous switching
- Our patterns were divided to test subsections of the chip
  - Clocks to rest of the chip shutoff while testing subsections
- Pattern partitioning significantly reduced dynamic power
- Static Power still remains an issue
  - The effect is reduced by testing at colder temperatures

High Power Challenges

- Fully populated card improves the IR drop
  - Previous generation card depopulated power and ground probes
  - Sort yield stability improved by fully populating all probes
  - Less prober downtime as compared to depopulated card
- Maintenance issues
  - Higher chance of probe burn out
  - Easy replacement of probes needed for reduced down time
- Temperature controlled chuck
  - Required to minimize probe card damage
- Accumax probe tips to improve current carrying capacity
  - 2x improvement from previous generation.
  - Probe can carry 1 amp for 2 minutes.
- Redesign of the hardware interface
  - Existing hardware did not support high current power supplies

Hardware Debug Challenges

- Probe Card
  - Jumper options to support switching to lower pin count tester
- Prober
  - Setting cleaning parameters for the prober
  - Setting up prober/probecard for cold chuck testing
- Probe Interface Board
  - New design not backwards compatible with existing template
  - Incorrect Power supply control signal assignments
    - Caused the PS board shutdown
    - Removing the pogo pins from the interface board fixed the issue.
  - Wrong resistors used between power and ground.

What Challenges Lie Ahead

- Pushing the boundaries of force vs. deflection of the state of the art probers of our time.
  - Our next generation product will have ~17,000 bumps.
  - We are already close to the limits imposed by the prober
  - Power feasibility study underway for the existing hardware
- Static Power consumption is increasing with each product generation
  - As process technology shrinks transistor count goes up
  - Transistors are also getting leakier.
  - Static power as a percentage of total power is increasing.

Summary

- Designed a new hardware interface for high power, high bump count wafer probing
  - Capable of handling multiple generations of products
- Overcame challenges to enable stable yields
- Impact of fully populating the probe card
  - Less downtime, better yield stability, improved IR drop
  - Need to watch out for prober force limitations.
- Wentworth's latest probing technology enabled
  - High pin count, higher current carry capacity,
  - Ease of maintenance with low probe card down time.

Thanks

- We would like to thank the following people who contributed to our presentation.
  - Chuck Heebner, Wentworth
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