IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

SWTW

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Low Yield Response (LYR) in High Volume Production

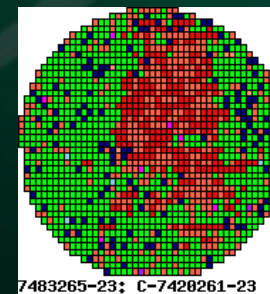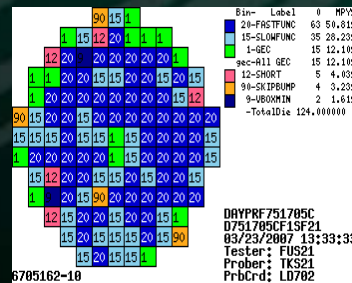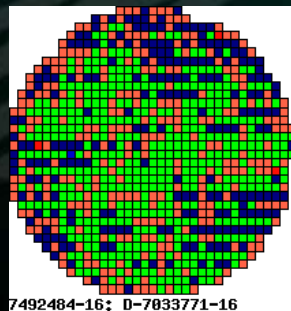TEXAS INSTRUMENTS
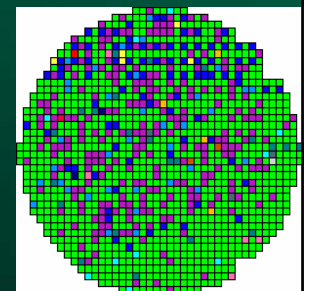
June 3-6, 2007

San Diego, CA USA

Agenda

- Background
- Problem Statement
- Objective
- Methodology
- Results
- Conclusions
- Acknowledgments

Background

Probe operations have to battle with yield related Issues on a daily basis – how do you minimize lost time?
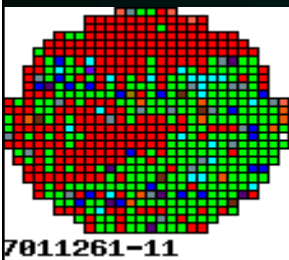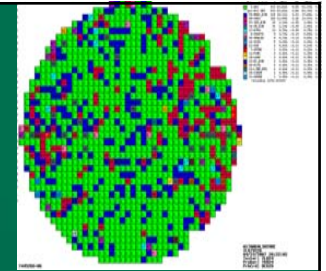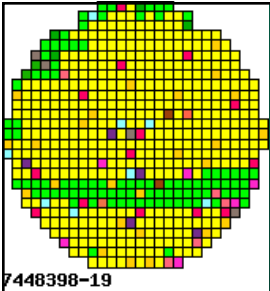
Problem Statement

How do you effectively diagnose, evaluate and recover from yield related problems?
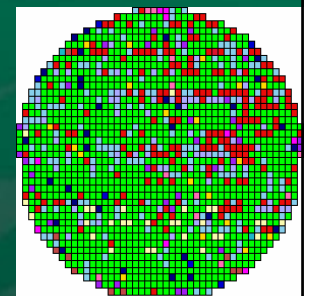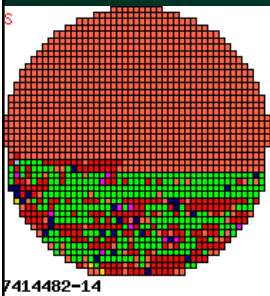
– No standard troubleshooting procedures –replace boards, pc, - shotgun approach

– Communication gaps/delays between different parties involved (Mfg – Engineering - Business)

– No problem traceability to close process and system gaps.

Objective

   To provide a process flow that allows for effective evaluation and troubleshooting of yield related problems driving to root cause solutions. Low Yield Response or LYR methodology creation provides these decisions .
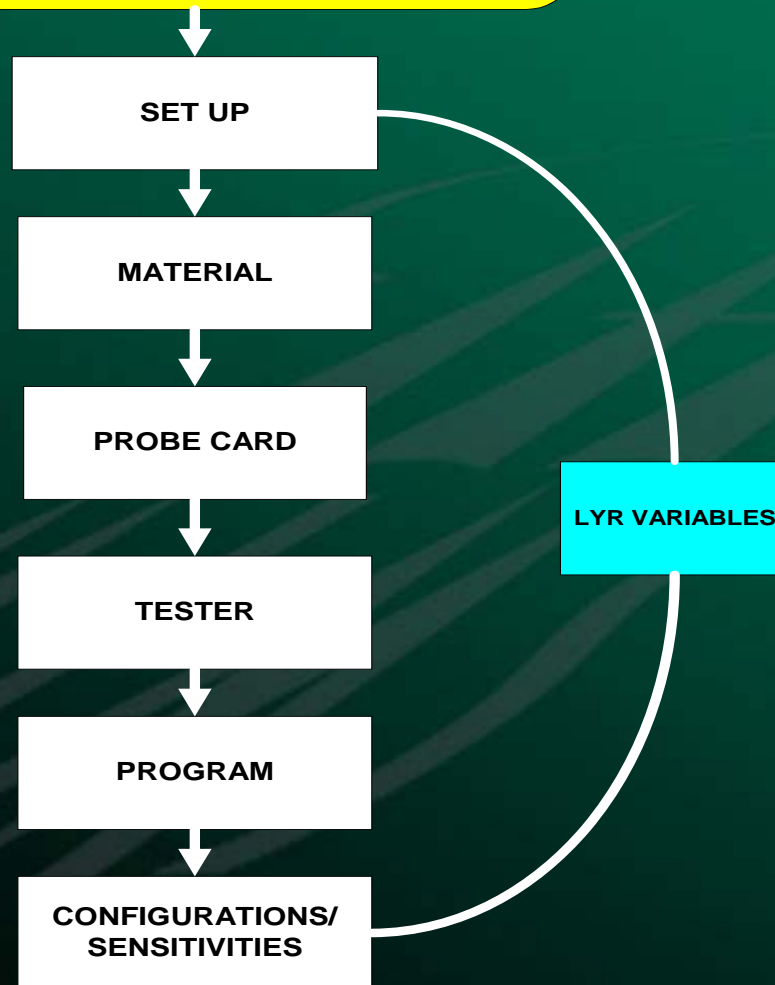
Methodology

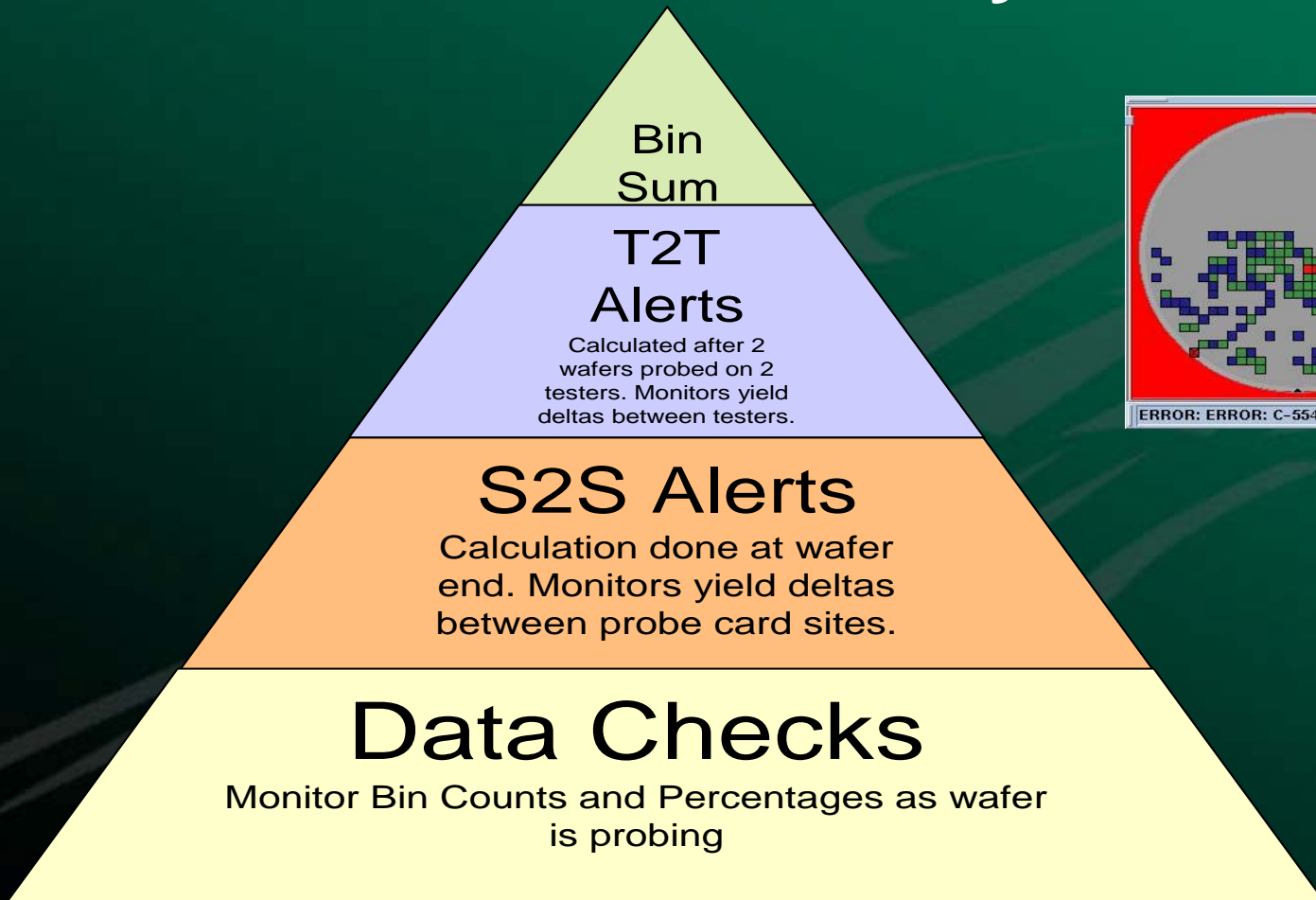DATA CHECK = Troubleshooting Trigger

LYR General Procedure:

A data check stops the testers to evaluate potential test issues. This triggers a LYR which uses a variable process elimination to find root cause which includes the escalation procedure between the different groups involved: mfg, EE, PE, and Apps.

SET UP

MATERIAL

PROBE CARD

TESTER

PROGRAM

CONFIGURATIONS/ SENSITIVITIES

LYR VARIABLES

Methodology
Yield Data Hierarchy

Bin Sum

T2T Alerts
Calculated after 2 wafers probed on 2 testers. Monitors yield deltas between testers.

S2S Alerts
Calculation done at wafer end. Monitors yield deltas between probe card sites.

Data Checks
Monitor Bin Counts and Percentages as wafer is probing

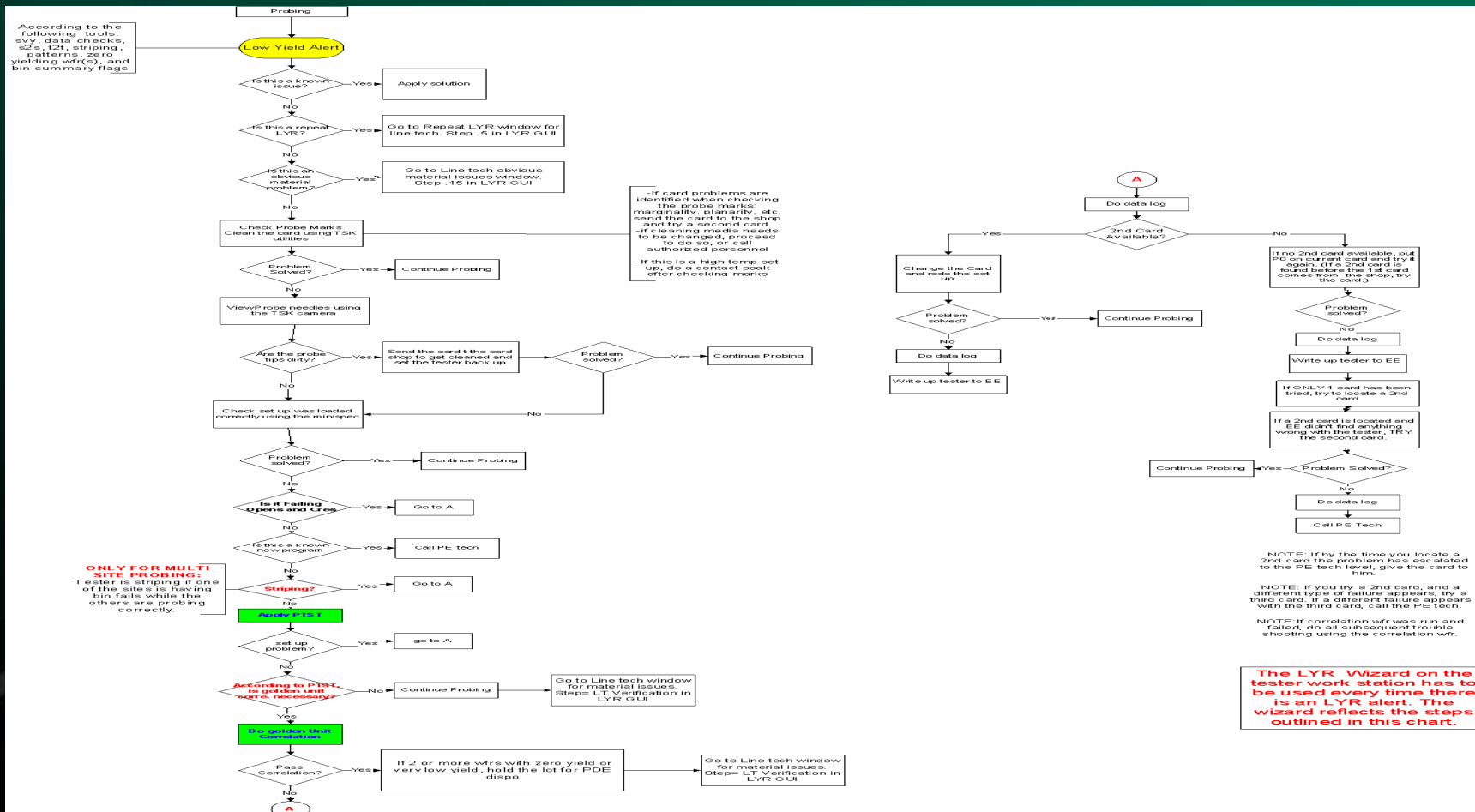ERROR: ERROR: C-5544402-18: OPENS > 1%

Methodology
LYR process Flow

- Each group involved has an automated troubleshooting flow. The different flows interact with each other.

- There is an LYR GUI access from the tester that guides the user through the troubleshooting decision process and escalations.

Methodology

Mfg Flow Example

Methodology

The LYR GUI

Methodology
The Known Issues Data Base

- This is used in the LYR when we do not want to go through the normal troubleshooting process, some examples are:
    - Lot(s) affected by a fab excursion.
    - Known program issues, awaiting fix.
    - Engineer wants to be called to work on the tool for a specific problem.
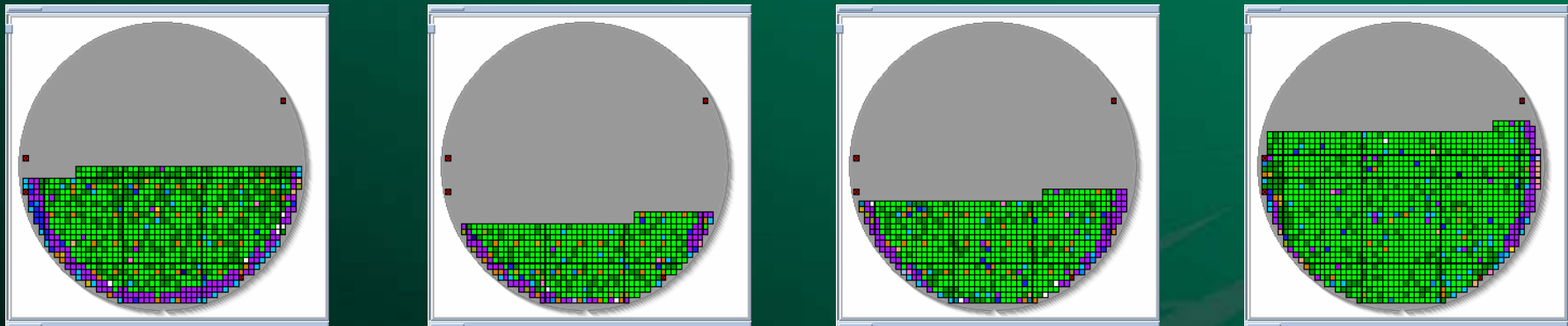
Methodology

The Known Issues Data Base

Example

Known issues can be entered using different combinations: lots, probe cards, programs, testers, log points, etc.

Methodology
Known Issue Example

Example of known issue settings.

Automated Banner Response

Problem:
Are you doing LYR for Bin 27 >8 in a row data check, and you have a bin 27 ring around the wafer?

Example of known issue pop-up window.

Solution:
Per DM6 PDE this is a known issue. Contact Line Tech to verify fail pattern and to disable data check for 1st wafer. If more than 1 wafer has same issue have PE Tech disable data check for lot.

Methodology

LYR Verification Process

After Mfg, EE or PE finish the troubleshooting process. The LYR performs an automated check to verify that the yield issue has been resolved. If the failing bin percentage increases or there are further data checks, then it reopens to continue with the next troubleshooting steps.

Methodology
LYR Verification Process

File Edit Options   **Help**

> ### Verifing LYR is complete

> LYR is now monitoring BIN48 . If this bin is not a GEC the LYR will monitor this bin to see if it increases. If it increases it will fail or if the tester data checks it will fail.
>
> Processing...
>
> Start percent '79', current percent '81'. Verification process will be complete when wafer reaches '89'

> << BACK Save/Quit NEXT >> Cancel

File Edit Options   **Help**

> ### Verification Failed, LYR is not complete

> Please hit 'NEXT' LYR is not complete

> << BACK Save/Quit NEXT >> Cancel

Methodology
LYR Lot History Documentation

```
SMW20DE3                    SMS/370 LOT/MACHINE COMMENT LIST              SDL01

REQUEST:   LST            <LST,DEL>          LOGPT:        9450
FACILITY:  DMOS6                             OPN:          _____
LOT:       5140903

SEL  LP  OPN
     9450 8760   DATE:WED SEP  7 090050 CDT 2005
                 LYR VERSION:2.0
                 ----------------------------------------------------------------
                 LYR NUMBER:050907090012
                 TESTER NAME:VLB235
                 FACILITY:DMOS6
                 TESTAREA:MULTIPROBE
                 PROGRAM NAME:A751501EP1ST15
                 LOT NUMBER:5140903
                 FIRST WAFER:4-5140903-14
                 USER NAME:OPERATOR
                 INITIAL DESCRIPTION:FAILING HIGH BIN 46 AND BIN 13...

NEXT TRAN                                                DEST= _____
SMWA0015 PRESS <ENTER> KEY FOR CONTINUATION              05/09/07 15:59:32
F6:RETURN TO MENU  F10:M13 MACH STATUS   F11:M17 START WORK    F12:M22 MISTI MENU

TCW 735 03 12                    A ADLIMA
```

Methodology
LYR Documentation- Search Utility

LYR troubleshooting Example

```
UserID=a0869436 - Operator
Shift=D
Date=Wed May 16 23:25:24 CDT 2007
LYR_Version=3.0
-----------------------------------------------------------
LYR_Number=070516232421
Tester_Name=vlb10
Facility=DMOS6
Testarea=MULTIPROBE
Program_Name=A751799EP1DT19
Lot_Number=7075838
Chuck_Temp=30
First_Wafer=4-7075838-05
User_Name=Operator
Initial_Description=stripping_bin_16_on_site_1
Automatic_Description=OTHER
First_Card=LB120
Card_Type=STANDARD
Number_Of_Sites=2
Status=EEcomplete
Is_This_Flash_Material=NO
Was_The_LYR_Filled_Out_Correctly=New_LYR
MFG_Obvious_Material_Problem=NO
Did_Cleaning_Card_Checking_Marks_Fixed_Problem=NO
Did_Probe_Tips_Look_Dirty=NO
Did_Matching_The_Setup_To_The_Minispec_Fixed_Problem=NO
Is_Tester_Probing_Opens_Or_CRES=NO
Is_This_a_New_Program=NO
Number_Of_Lots_Under_Program=64
Is_Tester_Striping=YES
Is_There_A_Second_Card_Available=YES
Did_Second_Card_Fix_Problem=NO
Second_Card_Name=LB112
Was_Second_Card_Failing_The_Same_Way_As_The_First=YES
Escalated_To=EE,Two_Cards_Failed_The_Same_Way
-----------------------------------------------------------
UserID=a0215297 - EE
-----------------------------------------------------------
Two_Cards_Used=YES
Is_This_Problem_A_Known_Issue_EE=NO
Verified_Failing_Same_On_Both_Attempts=YES
What_Is_The_Tester_Failing=solid_bin____16_fallout_after_having_run_good
What_Site_Is_Failing=single_site
Did_Probe_Card_Have_History_Failing_The_Same_Fail=NO
Any_Problems_Found_During_Visual_Check=NO
Is_There_Any_Tester_Trends=NO
Verified_Tester_Is_Failing_Opens_Or_Cres=NO
Are_Power_Supplies_OK=NO
Are_Power_Supplies_OK_Comment=-86_v_psa_was_reading_out_of_tolerance_at_1.8v_adjsuted_to_.9v_
Pwr_Supplies_Failed=-86v_reading_1.8v_over_tolerance..adjusted_to_.9v_well_withing_tolerance^
Did_Diags_Pass=NO
Did_Diags_Pass_Comment=failed_sys32io,sys32ioplus_for_quad1_pincrd_5_
Diags_Failed=replaced_32io++_in_slot5_with_new_and_now_passes_failed_diags..recald_system_also_failed_to
-----------------------------------------------------------
UserID=x0039937 - EE
-----------------------------------------------------------
Redo_Setup_Is_Problem_Fixed=YES
Solution_Found=Diags_Failed
```
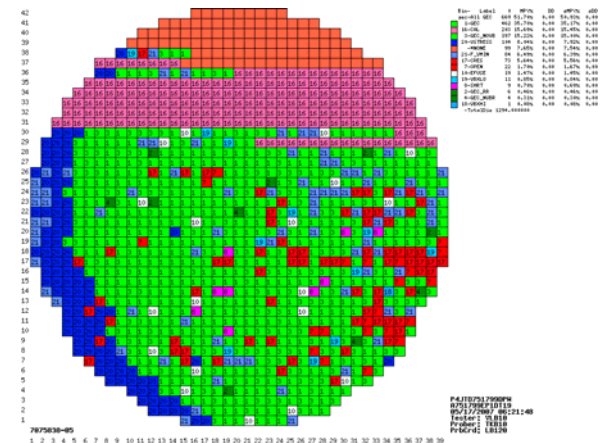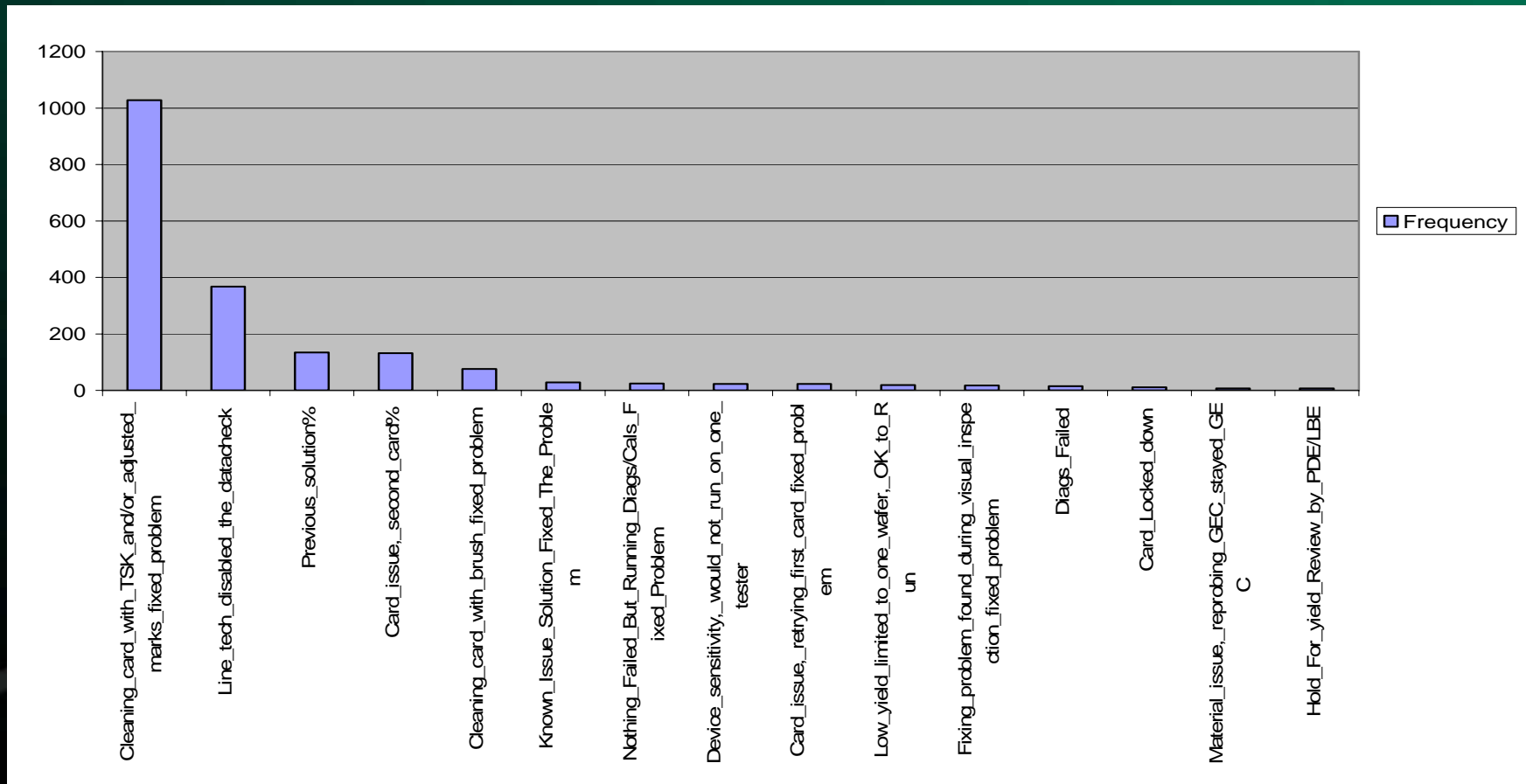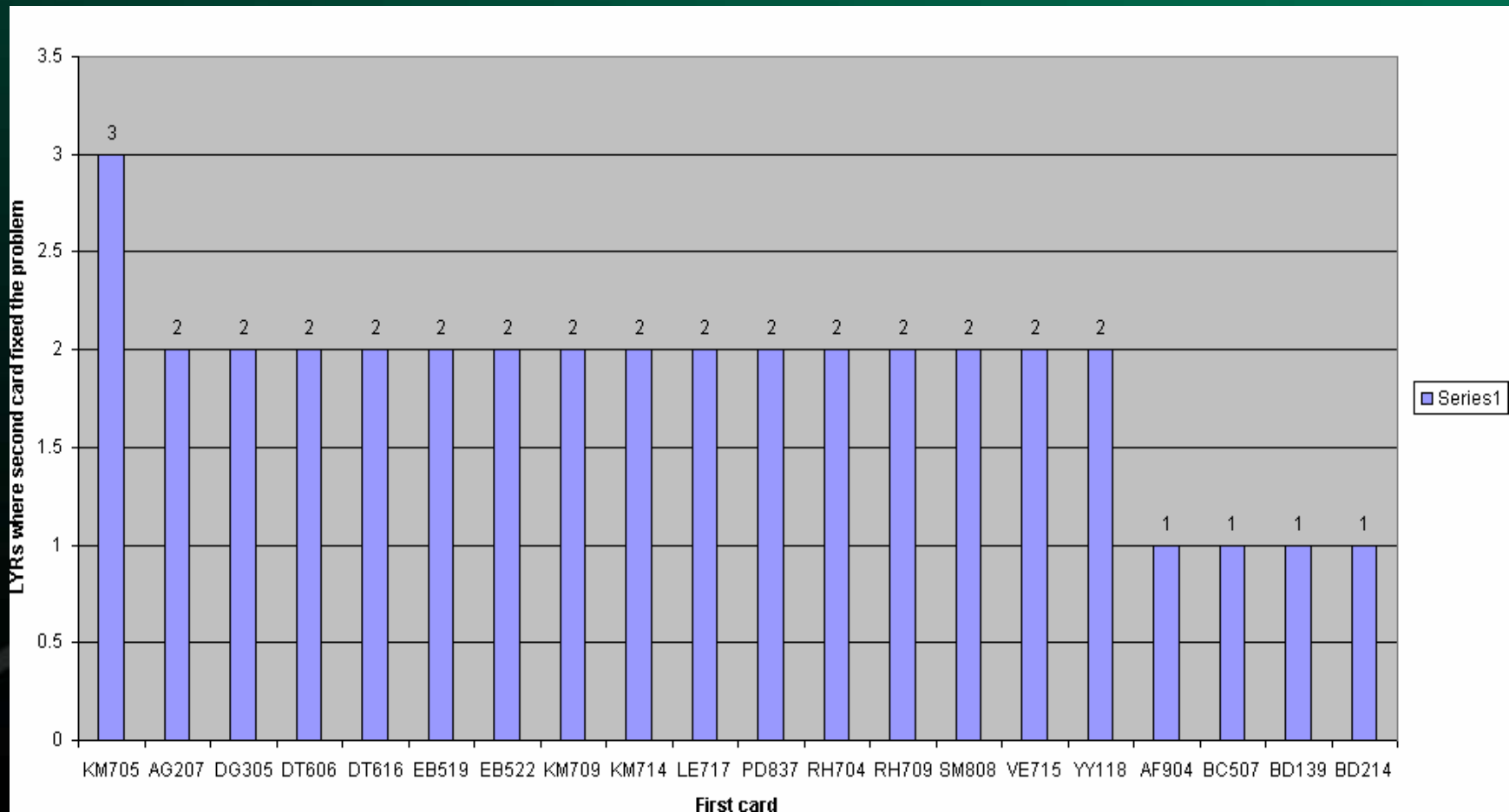
Results

Using LYR Solutions to Drive Process Changes
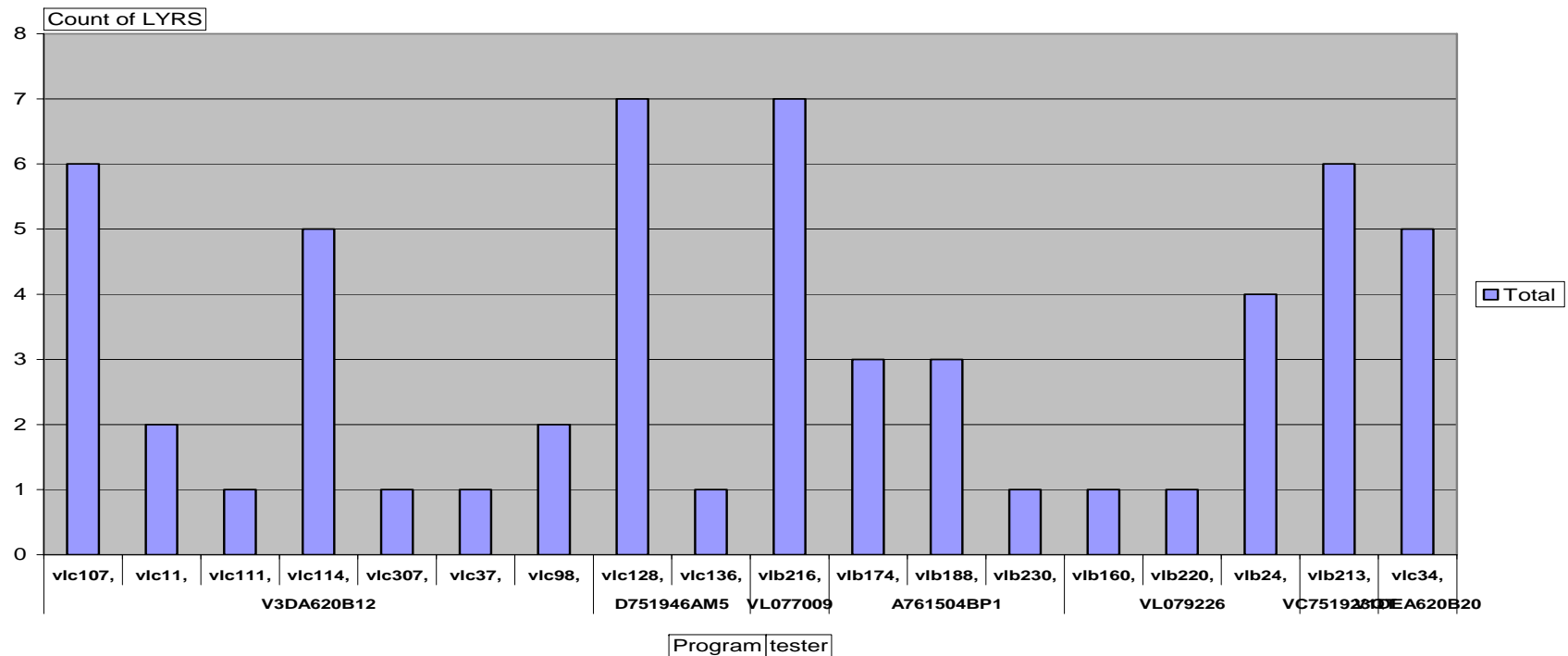
Results

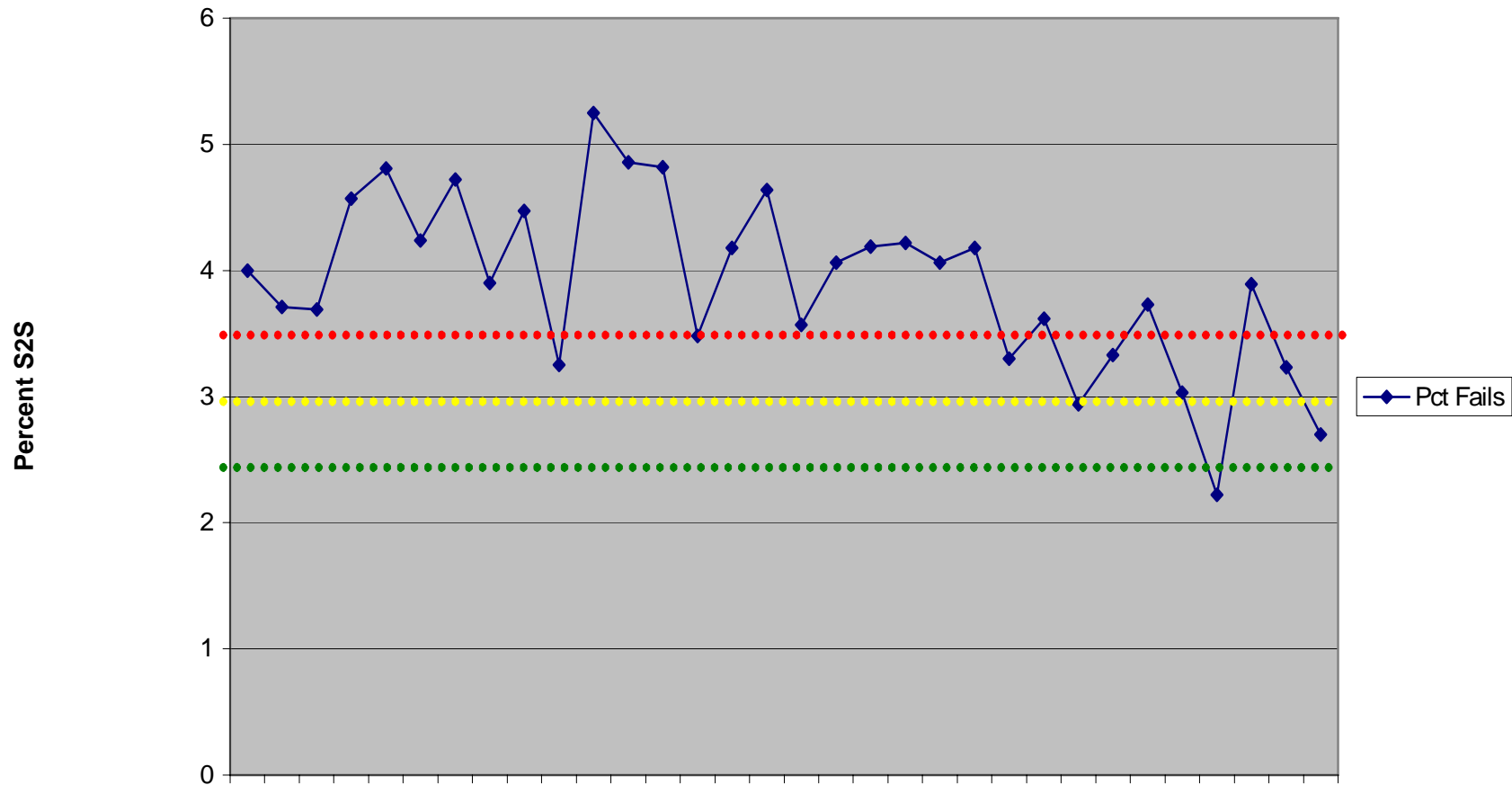## Using LYR to Identify Problematic Cards

Results

Using LYR to Resolve Program Issues

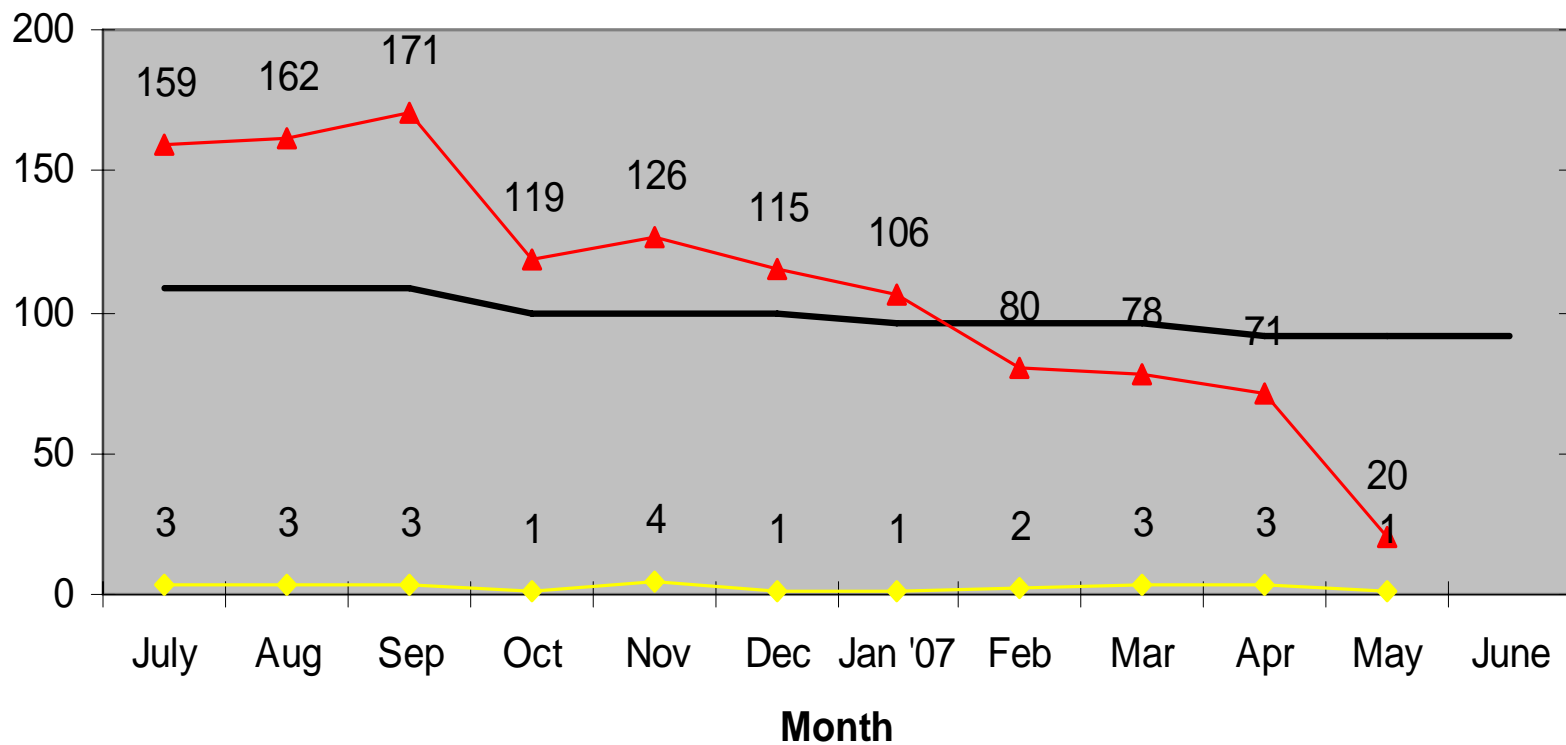

Excessive LYR by Program April 18 to May 4

Site to Site Results

Running Percent S2S Fails
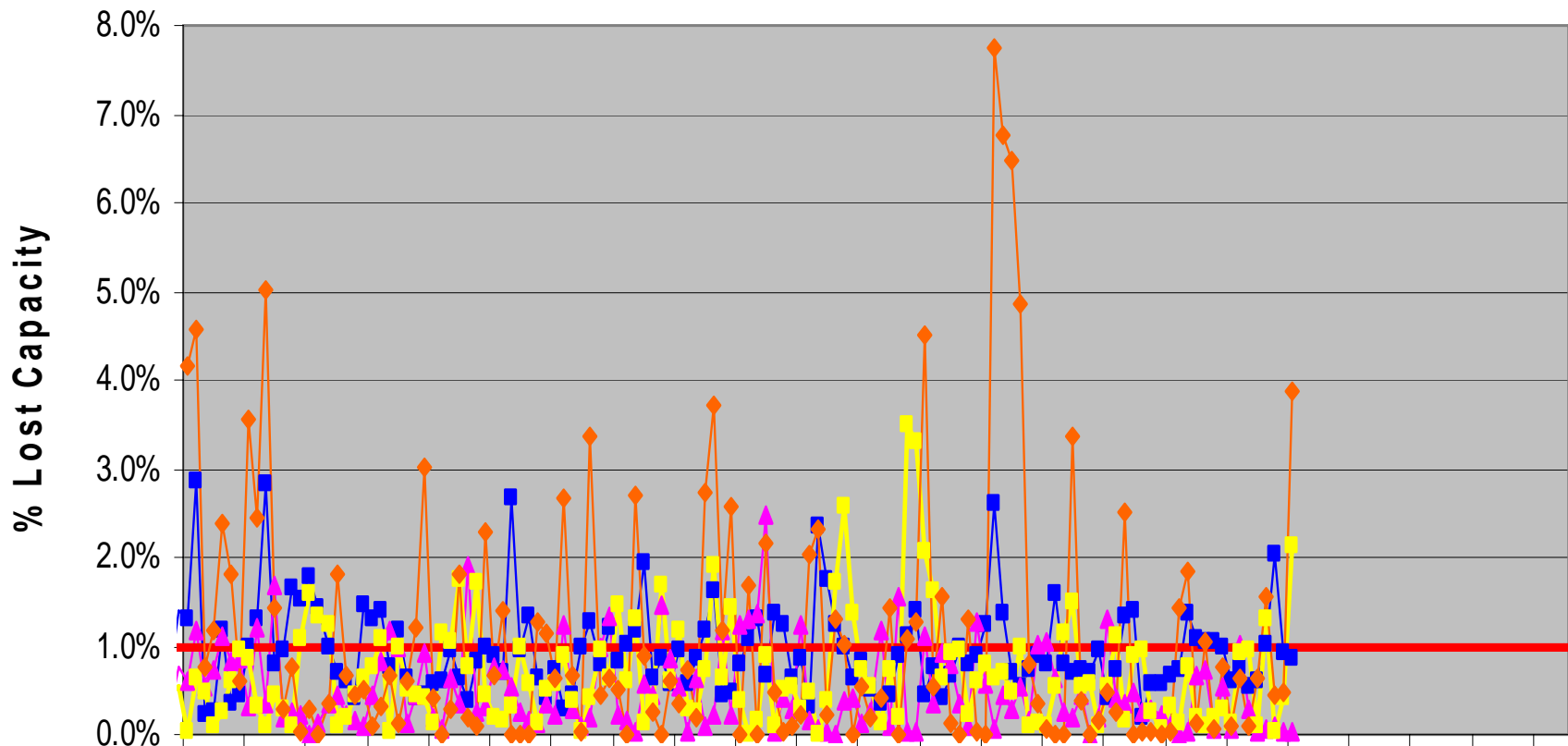
Tester to Tester Results

EBT T2T Monthly Alerts & Responses 3Q 06 - 2007 YTD

Retest Results

East Building Test
Reprobe Due to Production Issues 2007 YTD

Conclusions

– The Low Yield Response provides a standardized process to troubleshoot yield related issues that deals with the interaction between the different parties involved.

– LYR analysis results provide the basis to drive process/system changes that help the factory run better.

Acknowledgments

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- Francisco Tort
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- Shelbron Barnes
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Thanks For Listening

Questions?

Contact a-wegleitner@ti.com