IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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IBM Systems & Technology Group
Essex Junction, Vermont

Thin Film Interposer (TFI™) Probes in Production

Challenges, Experiences, and Lessons Learned

June 6, 2007

Overview

- ***Background***
- **Benefits**
  - Why does IBM use TFI?
- **Challenges**
  - Parallelism and Co-Planarity
  - Vacuum
  - Handling and Cleaning
  - Thermal Constraints
  - Retest Constraints
- **Experiences**
  - “Channel 119 - The Crushed Pin Issue”
  - “Channel 113 - The Hotspot Issue”
  - “When Processors Attack”
- **Summary**

Background

- TFI probes were developed by IBM team members in Endicott, Yorktown Heights, Fishkill, and Burlington in the early 1990s
- Pedestal substrates were developed by IBM Ceramic Packaging in Fishkill

[51] **Int. Cl.**^{5} **H01R 9/09**
[52] **U.S. Cl.** **439/66**; 439/67; 439/77; 439/591
[58] **Field of Search** 439/66, 67, 77, 91, 439/591, 908

[56] **References Cited**

U.S. PATENT DOCUMENTS

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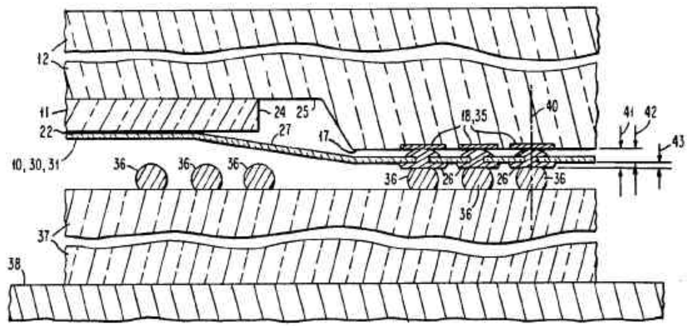
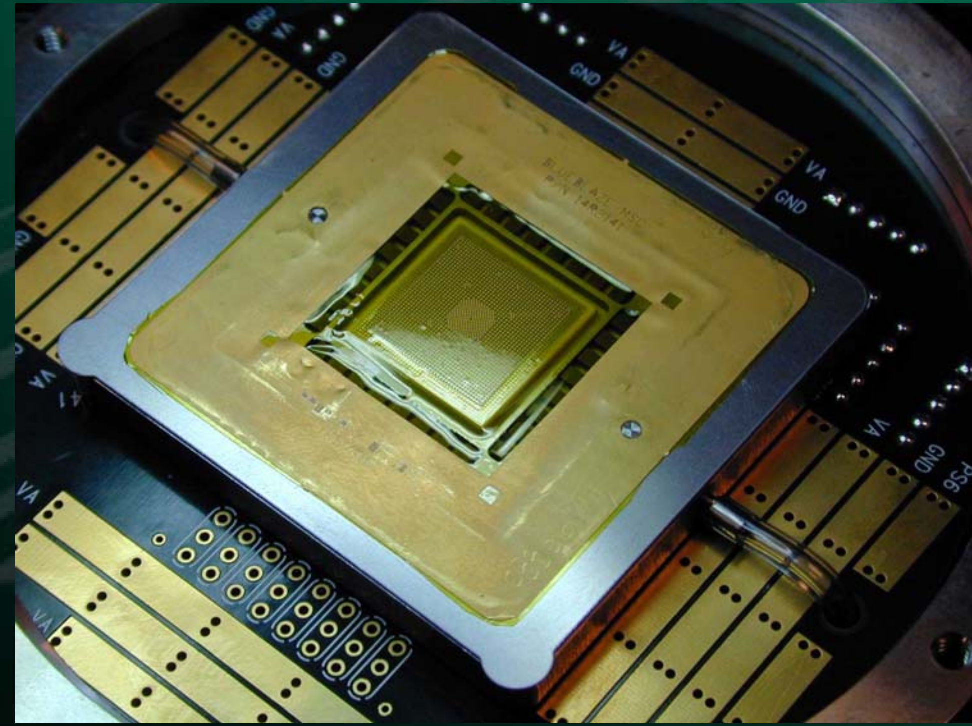
[57] **ABSTRACT**

A thin interface pellicle probe for making temporary or permanent interconnections to pads or bumps on a semiconductor device wherein the pads or bumps may be arranged in high density patterns is described incorporating an electrode for each pad or bump wherein the electrode has a raised portion thereon for penetrating the surface of the pad or bump to create sidewalls to provide a clean contact surface and the electrode has a recessed surface to limit the penetration of the raised portion. The electrodes may be affixed to a thin flexible membrane to permit each contact to have independent movement over a limited distance and of a limited rotation. The invention overcomes the problem of making easily breakable electrical interconnections to high density arrays of pads or bumps on integrated circuit structures for testing, burn-in or package interconnect and testing applications.

12 Claims, 16 Drawing Sheets





Background

- Production use of TFI and pedestal probecards began in 1998 on MCM chips for the S/390 G5 mainframe, on the IBM-designed LLCC wafer tester using Electroglas 3001 probers

- *Die Sizes:*
  - 8x8mm thru 17x17mm
- *C4 Pitch:*
  - 318um min
- *Pincount:*
  - ~ 1,600 max
- *Power @ Test:*
  - ~ 40W max

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IBM S/390 Server G5/G6

Vol. 43, No. 5/6, 1999

Order No. G322-0219

This issue contains nineteen papers on the IBM S/390 Server G5 and G6 systems. Included are descriptions of the G5 and G6 multichip modules (MCMs), the S/390 CMOS Cryptographic Coprocessor Facility, the S/390 implementation of the IEEE Floating-Point arithmetic standard, and design innovations such as the binodal cache and the Integrated Cluster Bus.

IBM Journal of Research and Development

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Preface	Kevin Carswell and Cyril Price, *Guest Editors*	p. 619
MCM technology and design for the S/390 G5 system	G. A. Katopis, W. D. Becker, T. R. Mazzawy, H. H. Smith, C. K. Vakirtzis, S. A. Kuppinger, B. Singh, P. C. Lin, J. Bartells, Jr., G. V. Kihlmire, P. N. Venkatachalam, H. I. Stoller, and J. L. Frankel	p. 621

Comments

```
1. Hold low yielding lots for engineering disposition.
> 2. Uses TFI probes.   USE WWW SETUP GUIDE FOR REFERENCE
> 3. CONVERGENCE MUST!! BE FORCED AT LOT INIT
> 4. STEP PLAN = A88H3543
```

Wafer Setup Guide "SYMPHONY CP 14.6MM WAFER":

```
Created  by: rmc    @       .btv.ibm.com on October 27, 1998 at 10:52
Modified by: stg     @ .  .  .    on April 8, 2004 at 07:28
```

General Information:

Wafer Diameter (mm)	200
Notch Orientation	3 o'clock
Handler Set Name	EG3001
Space Transformers	TRL TFI ALL-98 12.75
Probe Ids	PRL TFI 14.6 MM
Misc	Not Applicable
Start Site:	05, 12
Major Periodicity (mm)	16.15 by 15.00

Notes

```
Step Plan = A88H3543
Space Transformer ID = Axx - Jxx
Probe ID = 06702xxx
```

View the Wafer Setup Picture:

1998

IBM introduces in May the IBM S/390 - Generation 5 (G5) server, the most powerful S/390 computing system. Two months later, IBM says the S/390 G5 Parallel Enterprise Server 10-way Turbo model has smashed the 1,000 MIPS barrier, making it the world's most powerful mainframe. The company ships its 1,000th S/390 Parallel Enterprise Server - Generation 5 in November — less than 100 days after G5 manufacturing began, marking the largest ramp-up in S/390 history. In all, 1998 shipments of mainframe computing power, measured in MIPS, increase 60 percent over 1997.

IBM's e-business and network computing announcements during 1998 include the industry's premier system security for conducting business over the Internet encompassing a hardware/software solution integrated with IBM's flagship enterprise operating system, OS/390, and IBM S/390 Parallel Enterprise servers - Generation 3 (G3) and Generation 4 (G4).

Background

- TFI was migrated to the Teradyne J973 / TEL P-8XL platform for testing the POWER4 processor in 2000

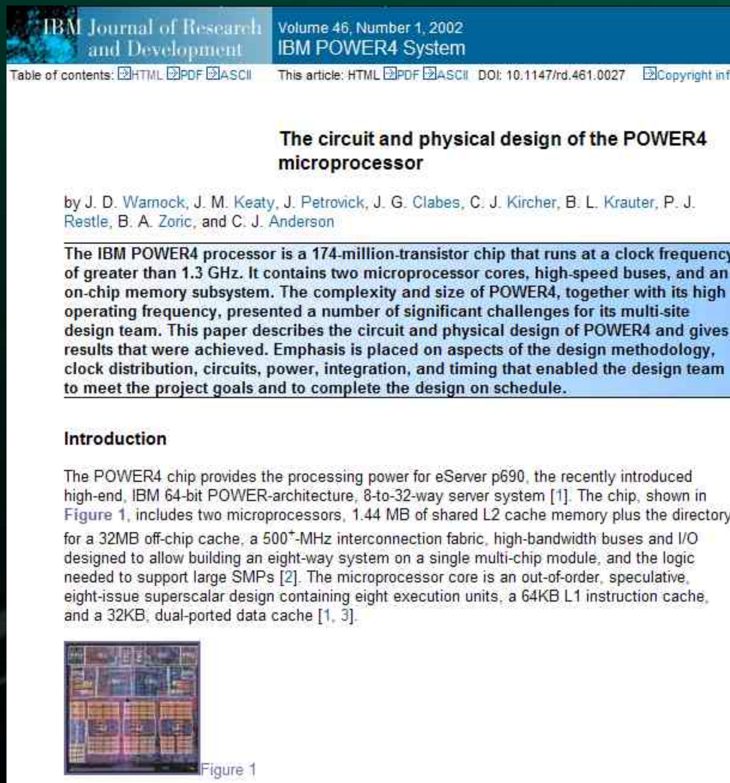

IBM Journal of Research and Development | Volume 46, Number 1, 2002 | IBM POWER4 System

Table of contents: HTML PDF ASCII   This article: HTML PDF ASCII   DOI: 10.1147/rd.461.0027   Copyright info

The circuit and physical design of the POWER4 microprocessor

by J. D. Warnock, J. M. Keaty, J. Petrovick, J. G. Clabes, C. J. Kircher, B. L. Krauter, P. J. Restle, B. A. Zoric, and C. J. Anderson

The IBM POWER4 processor is a 174-million-transistor chip that runs at a clock frequency of greater than 1.3 GHz. It contains two microprocessor cores, high-speed buses, and an on-chip memory subsystem. The complexity and size of POWER4, together with its high operating frequency, presented a number of significant challenges for its multi-site design team. This paper describes the circuit and physical design of POWER4 and gives results that were achieved. Emphasis is placed on aspects of the design methodology, clock distribution, circuits, power, integration, and timing that enabled the design team to meet the project goals and to complete the design on schedule.

Introduction

The POWER4 chip provides the processing power for eServer p690, the recently introduced high-end, IBM 64-bit POWER-architecture, 8-to-32-way server system [1]. The chip, shown in Figure 1, includes two microprocessors, 1.44 MB of shared L2 cache memory plus the directory for a 32MB off-chip cache, a 500+-MHz interconnection fabric, high-bandwidth buses and I/O designed to allow building an eight-way system on a single multi-chip module, and the logic needed to support large SMPs [2]. The microprocessor core is an out-of-order, speculative, eight-issue superscalar design containing eight execution units, a 64KB L1 instruction cache, and a 32KB, dual-ported data cache [1, 3].

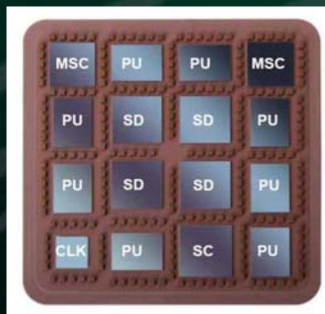
Figure 1

Background

- Since 2000, TFI is being used to test:
  - all zSeries mainframe MCM processors/ASICs
  - all pSeries and iSeries server processors
- TFI is used on 5 tester platforms:
  - LLCC, Teradyne J973, Teradyne UltraFlex, Advantest 66XX, Agilent 93000
- *Die Sizes:*
  - 8x8 - 21x21mm
- *C4 Pitch:*
  - 200um min
- *Pincount:*
  - ~ 7,800 max
- *Power @ Test:*
  - ~ 400W max

System z

Systems i and p



z9 MCM

p5 MCM

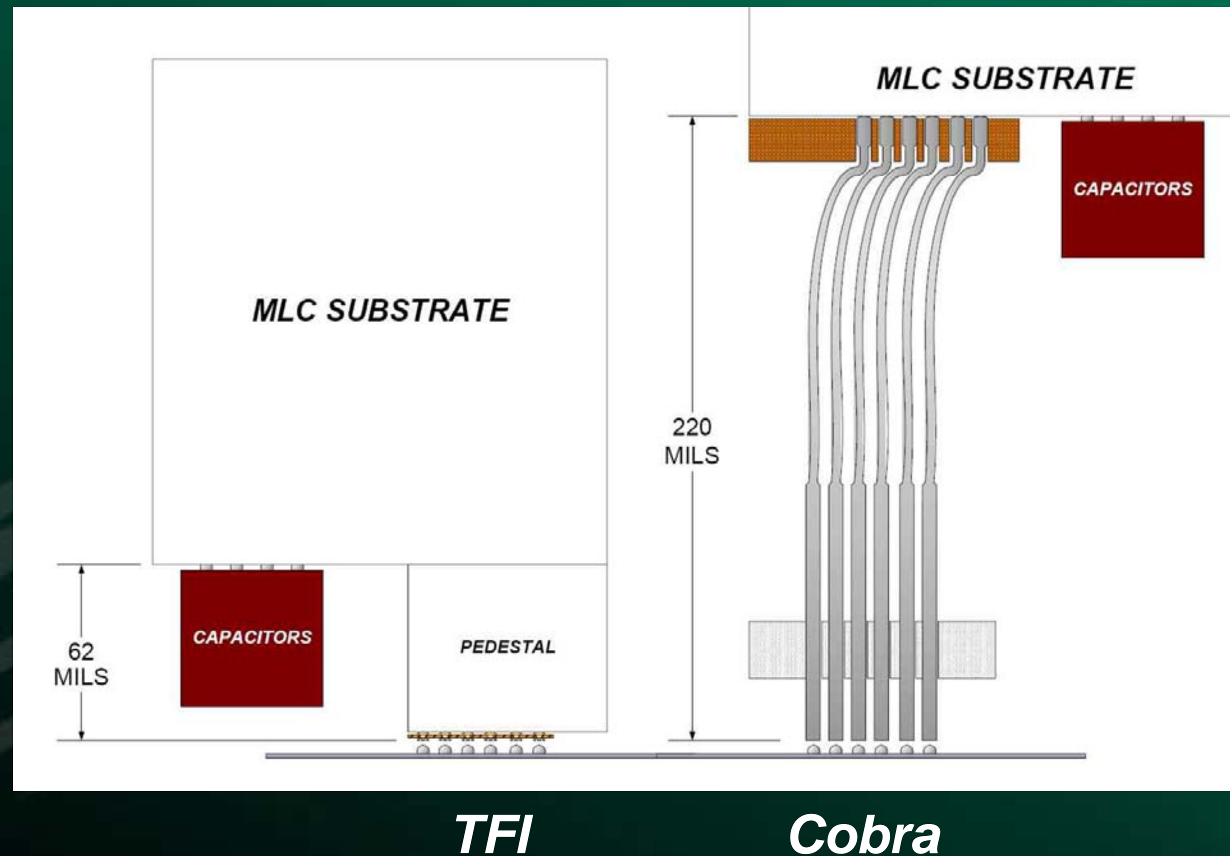
TFI™ Probes in Production

- **Background**
- ***Benefits***
  - *Why does IBM use TFI?*
- **Challenges**
  - Parallelism and Co-Planarity
  - Vacuum
  - Handling and Cleaning
  - Thermal Constraints
  - Retest Constraints
- **Experiences**
  - "Channel 119 - The Crushed Pin Issue"
  - "Channel 113 - The Hotspot Issue"
  - "When Processors Attack"
- **Summary**

Benefits

Why does IBM use TFI?

- Power Delivery
  - *low inductance*
  - *DUT is closer to decoupling*

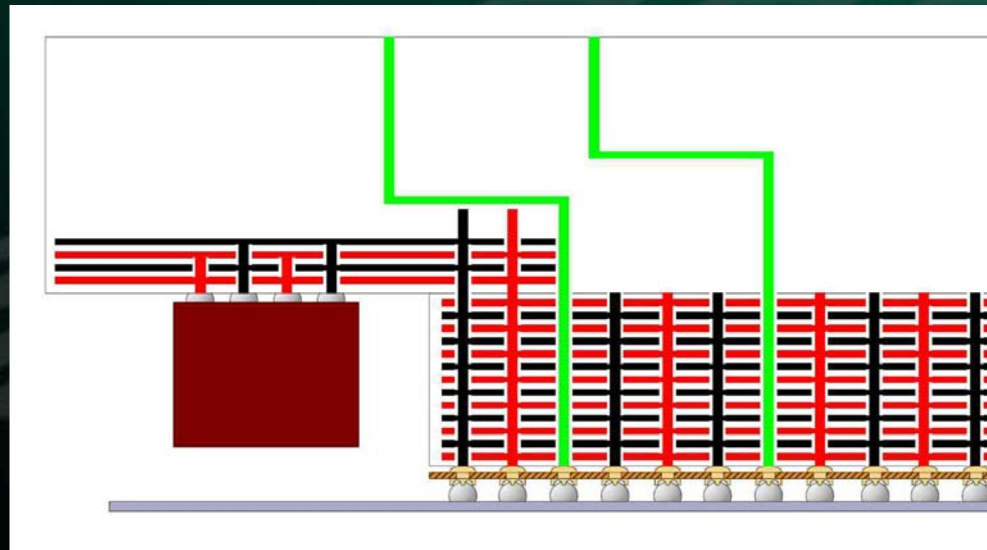


TFI ***Cobra***

Benefits

Why does IBM use TFI?

- Power Delivery
  - Power/Ground planes built into the pedestal allow for lateral current flow right up to the DUT
  - Capacitance of pedestal planes further enhance di/dt performance



Benefits

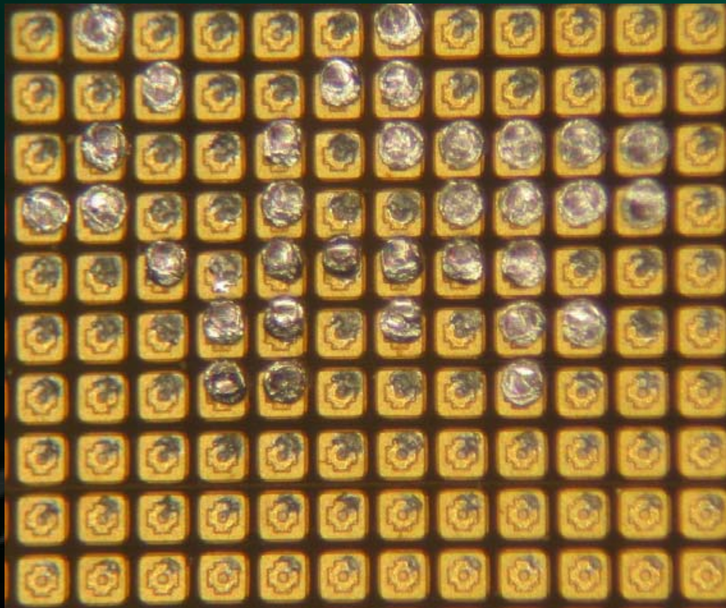
Why does IBM use TFI?

- Thermal Performance
  - The TFI / Pedestal interface is the closest test environment to "package-level" of any C4 wafer probe technology.
    - *If a chip is prone to thermal runaway at package-level, it will behave similarly during TFI test.*

Benefits

Why does IBM use TFI?

- Thermal Performance
  - If an over-current event happens, the C4 is the fuse, not the probe.



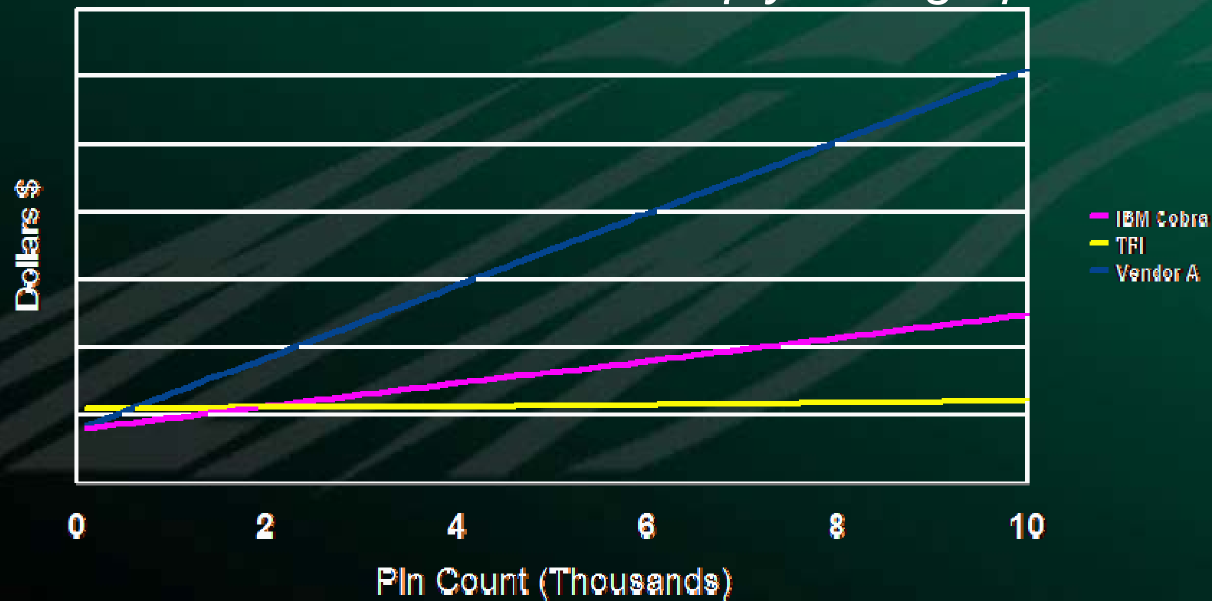
TFI

Cobra

Benefits

Why does IBM use TFI?

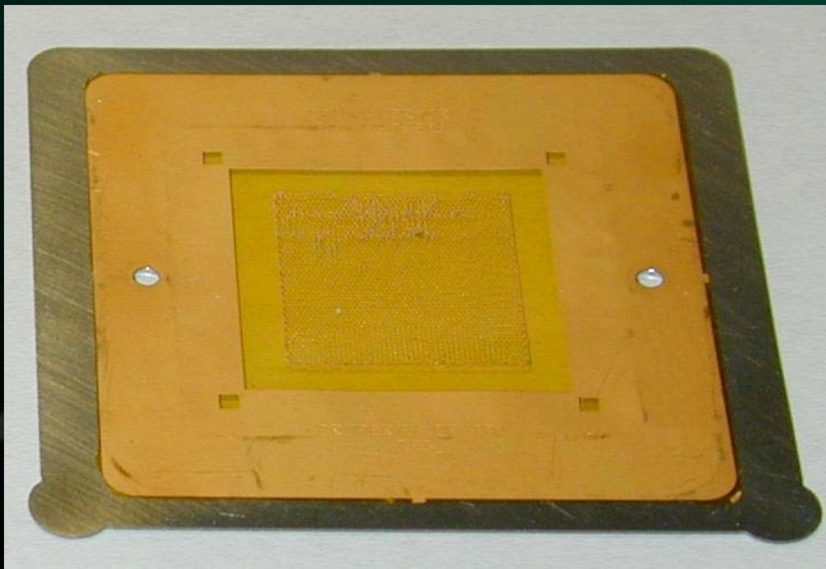
- Scalability
  - TFI probes are produced using photolithography, so:
    - *Pitch, density, and asymmetry are not limited by fab process*
    - *Cost does not increase as steeply for high-pincount probes*



Benefits

Why does IBM use TFI?

- Maintenance
  - Simple design
  - If a pin is damaged, it can be "plucked" easily without removing dies or disturbing other pins (though pins cannot be replaced)



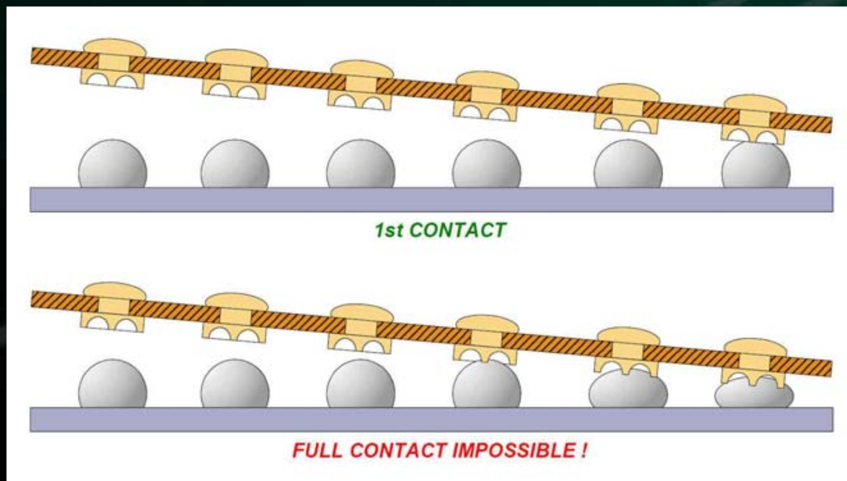
TFI™ Probes in Production

- **Background**
- **Benefits**
  - Why does IBM use TFI?
- ***Challenges***
  - *Parallelism and Co-Planarity*
  - *Vacuum*
  - *Handling and Cleaning*
  - *Thermal Constraints*
  - *Retest Constraints*
- **Experiences**
  - "Channel 119 - The Crushed Pin Issue"
  - "Channel 113 - The Hotspot Issue"
  - "When Processors Attack"
- **Summary**

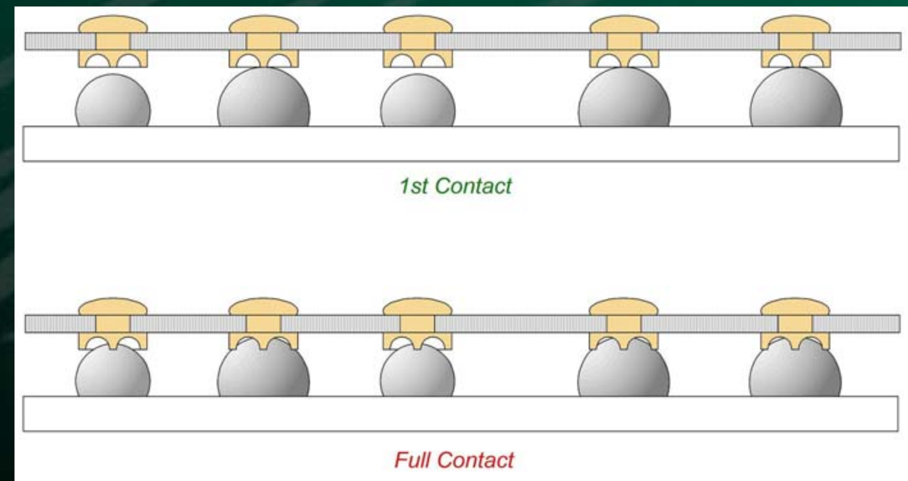
Challenges

- Parallelism and Co-Planarity
  - TFI is a rigid probe array
    - *making contact with wafer is difficult to impossible if the probe array and the wafer C4s are not co-planar, and parallel to each other.*

PARALLELISM

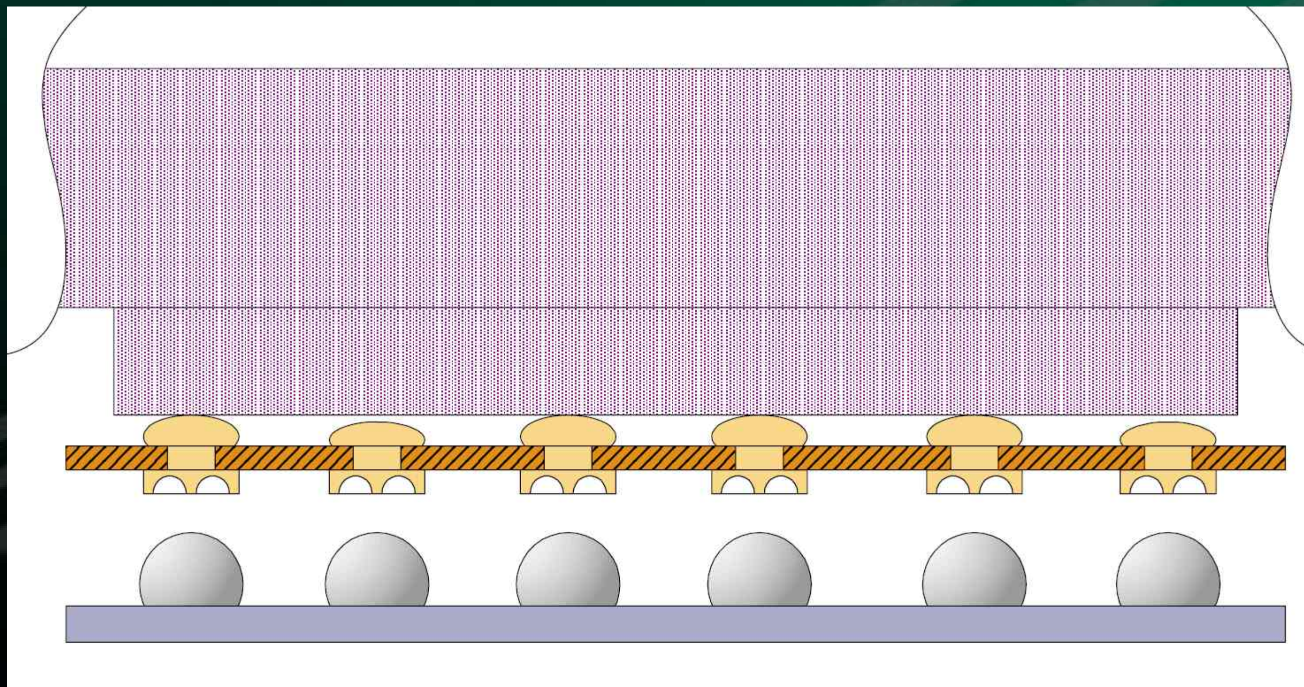


CO-PLANARITY



Challenges

- Parallelism and Co-Planarity
  - Co-Planarity from probe to probe must be within microns
    - *re-discovered the "hard way"; illustrated later in Experiences section*



Challenges

- Parallelism and Co-Planarity
  - In production test, all combinations of probecards and testers need to be interchangeable and parallel

Challenges

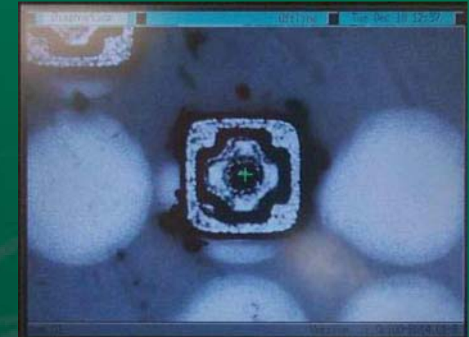
- Parallelism and Co-Planarity
  - Parallelism tolerance windows (z-variation across die):
    - Cobra Probes: 50 - 100um
    - TFI Probes: ***8 - 20um !***
  - Levelling procedure with the J973 testhead fixture was not accurate or repeatable enough to maintain the TFI tolerance window

Challenges

- Parallelism and Co-Planarity
  - IBM developed a procedure using the TEL prober look-up optics to “dial in” the J973 testhead levelling using a “golden” standard probecard
  - The rigid and co-planar nature of the probe array (held in place under vacuum) gave us a very accurate measurement of probe parallelism

Challenges

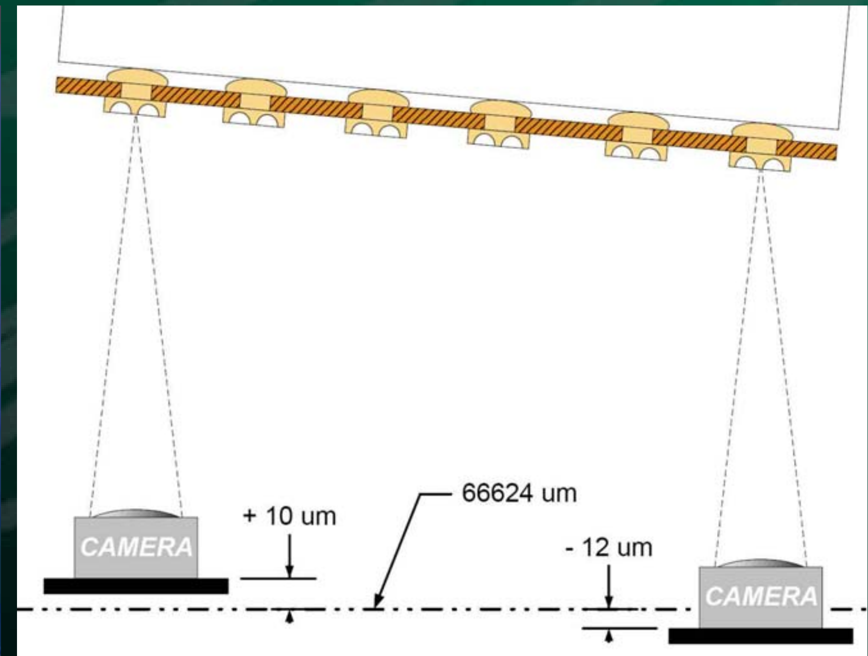
- Parallelism and Co-Planarity
  - Illustration of planarization measurement process



Probe Alignment Results

O K

Probe Center	X Coordinate	103387	µm
Probe Center	Y Coordinate	234134	µm
Probe Center	Z Coordinate	66624	µm
Probe Angle	θ Coordinate	2261	×0.0001°
Reference Pin	Z Coordinate	-12	µm
Pin 1	Z Coordinate	10	µm
Pin 2	Z Coordinate	5	µm
Pin 3	Z Coordinate	-2	µm



Challenges

- Vacuum

Why use vacuum?

- – Probehead needed to be thin to minimize pedestal height
- – Quick installation and removal of probehead
- – Simple probehead design:
  - *TFI foil, adhesive, mounting plate*
  - *No screw-holes or crevices to trap chemical cleaning solution*
- – Probers already need a steady, reliable vacuum supply

Challenges

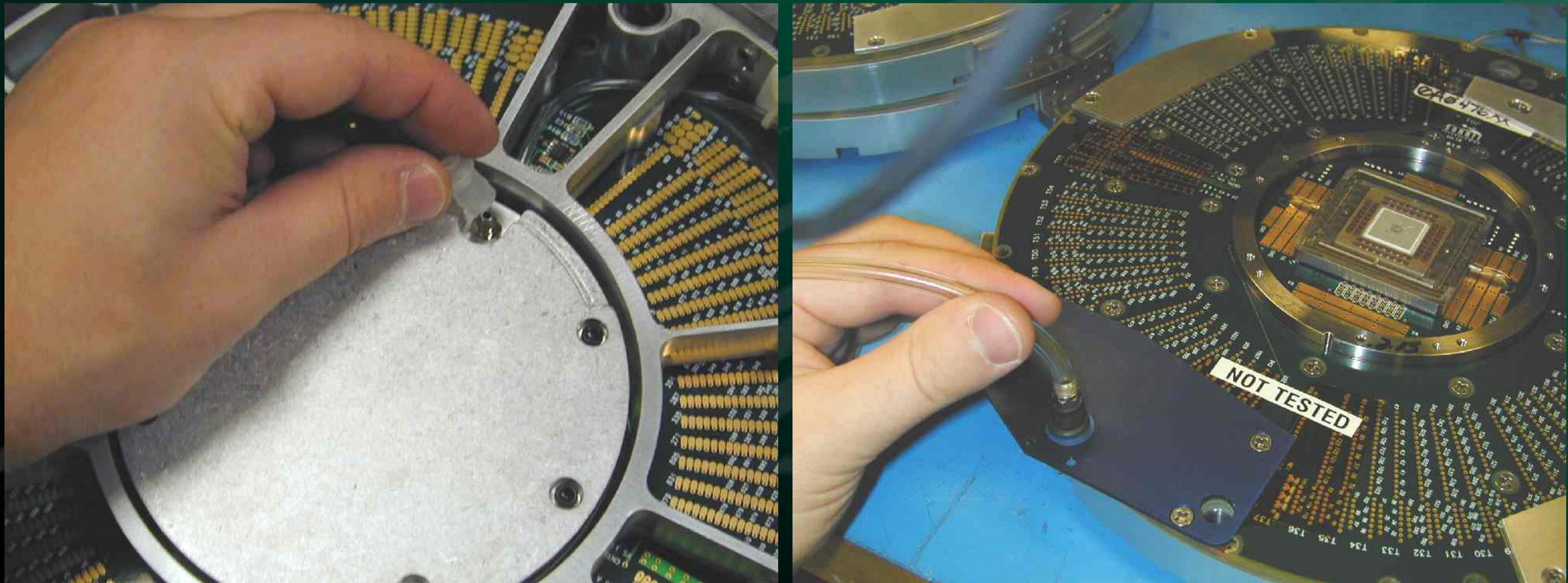
- Vacuum

Why use vacuum?

  - Probes are held tightly against the pedestal, which prevents:
    - *Extra impact force for "sagging" probes in the array center*
    - *Any micro-bonds between probes and C4s from pulling and strecthing the film during separation*

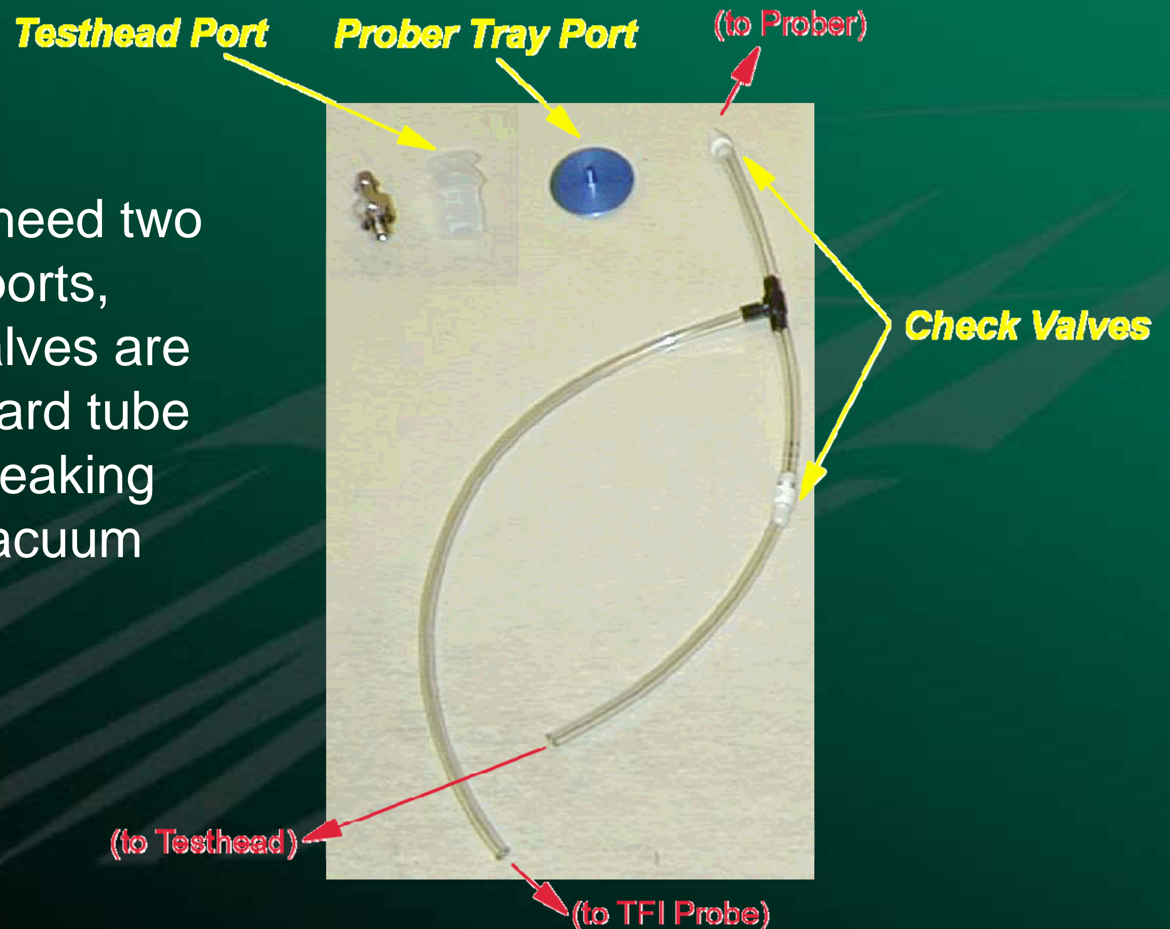
Challenges

- Vacuum
  - Vacuum lines are routed through the prober to two places:
    - *Tester-side of probecard when docked*
    - *Probecard loading tray at front of prober*



Challenges

- Vacuum
  - Since probecards need two vacuum interface ports, miniature check-valves are used in the probecard tube routing to prevent leaking from the unused vacuum port

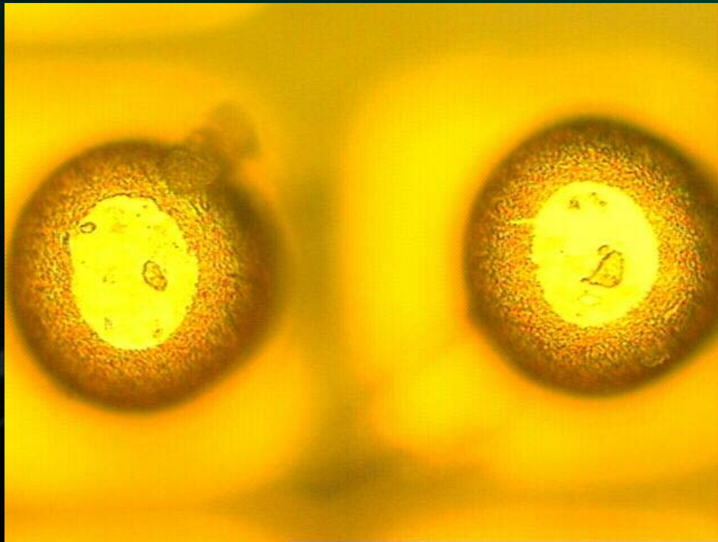


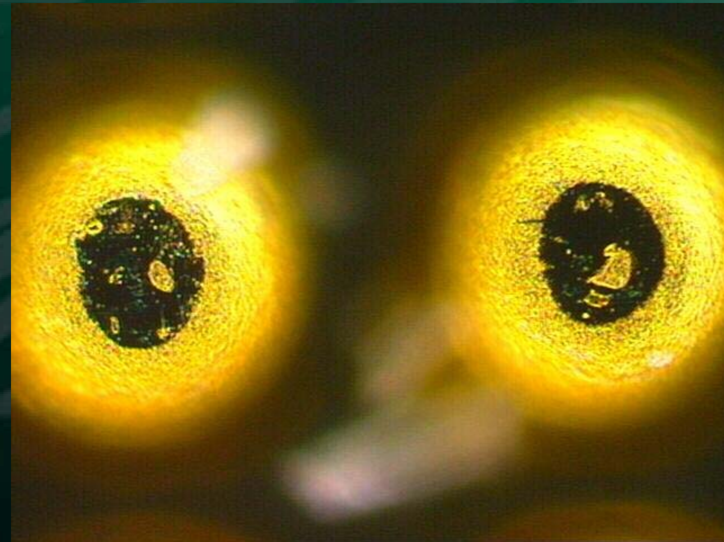
Challenges

- Handling and Cleaning
  - – TFI probe electrical contact is very sensitive to foreign material contamination, especially between the probe and pedestal
  - – The probe has little to no lateral “scrub” during contact to break through any FM

Challenges

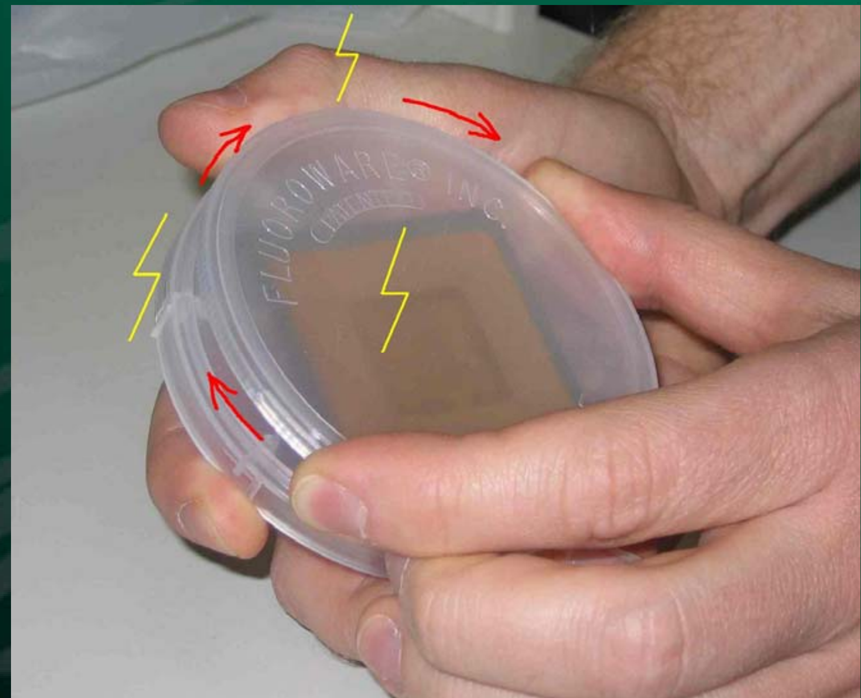
- Handling and Cleaning
  - FM contamination has been and continues to be the biggest source of failed TFI test setups
  - Skin flakes were found to be the primary culprit





Challenges

- Handling and Cleaning
  - The 4-inch plastic wafer containers used to store TFI probes are non-ESD
  - The charge built up from opening the container may be attracting FM to the probes



Challenges

- Handling and Cleaning
  - Options are being evaluated to solution the FM issue:
    - *Ionizers and gloves at probe inspection stations*
    - *Ionizers at testers during probe loading*
    - *ESD containers*
    - *UV microscope inspection*
    - *Auto-loading cartridges (like a CD changer)*

Challenges

- Handling and Cleaning
  - The sculpted shape of the TFI pin does not allow for standard probe polishing techniques used at in-situ cleaning
  - TFI probes must be removed from the tester at each cleaning cycle to be sent for off-line chemical cleaning

Challenges

- Handling and Cleaning
  - Off-line chemical cleaning is effective, but significantly increases tool down-time, and requires at least 1 spare probe per tool
  - Probes are often allowed to run longer than the allowed cleaning cycle to avoid re-setup of a tool, diminishing probe life and risking product damage

Challenges

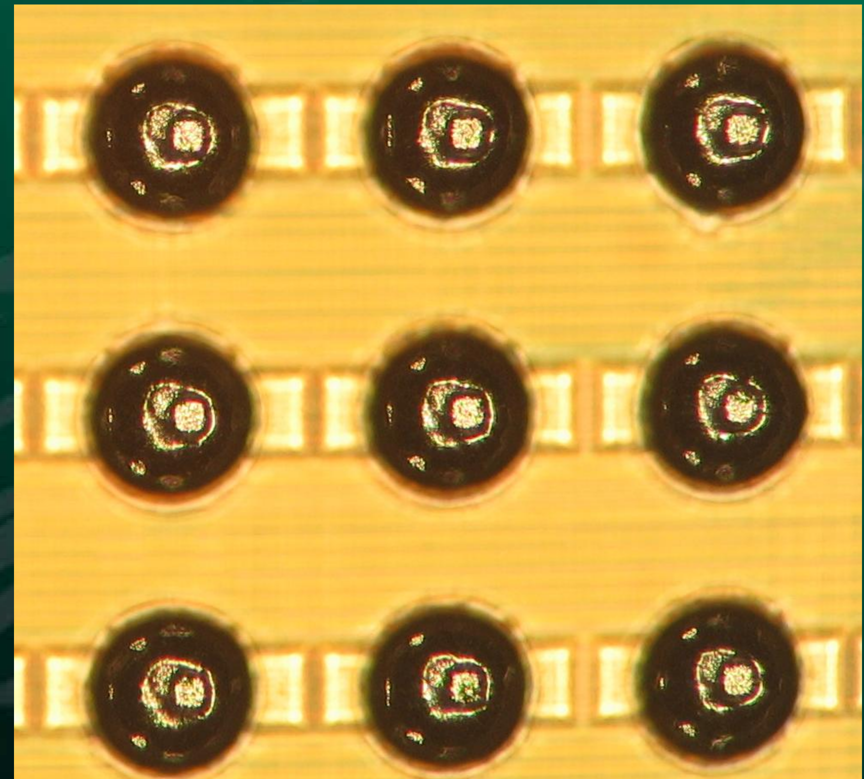
- Handling and Cleaning
  - Options for allowing in-situ TFI cleaning:
    - *Altering metallurgy and tip shape to allow abrasive cleaning*
    - *Chemical cleaning station inside prober*
    - *Auto-loading/unloading cartridge inside prober*

Challenges

- Thermal Constraints
  - TFI probes maintain very stable X-Y position over wide temperature range (-10°C to 75°C production, 90°C lab)
  - However, TFI probes are susceptible to contact failure from drastic thermal gradients within a die through *vertical expansion* *(illustrated in Experiences section)*

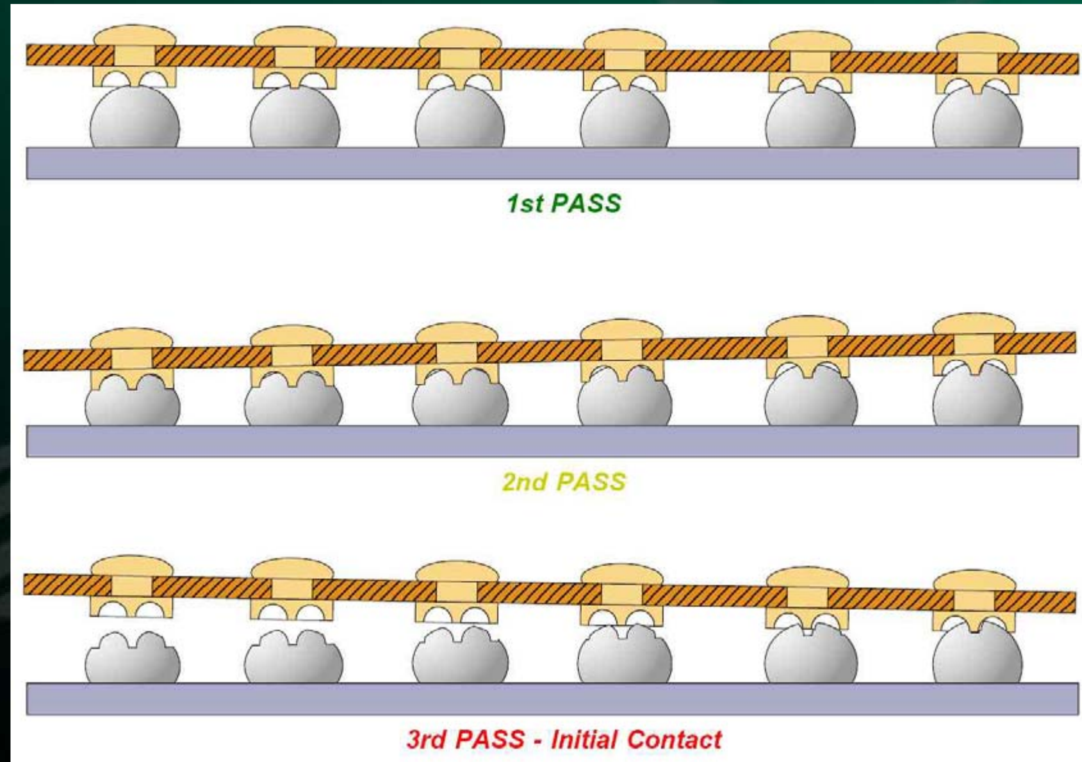
Challenges

- Retest Constraints
  - TFI probe tips are sculpted to puncture through the tin-oxide on a C4 with minimal force
  - After probing, the impression on the C4 is permanent. Each time a die is probed, a new impression is made.



Challenges

- Retest Constraints
  - Though parallelism and co-planarity are held within tight windows, contact becomes more difficult with each re-test.



Challenges

- Retest Constraints
  - It was found that a 3rd test pass yielded too many contact fails and risked permanent deformation of the C4s.
  - Test routing procedures were altered to mandate a reflow step after the 2nd test pass.

TFI™ Probes in Production

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- **Benefits**
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  - Vacuum
  - Handling and Cleaning
  - Thermal Constraints
  - Retest Constraints
- ***Experiences***
  - *"Channel 119 - The Crushed Pin Issue"*
  - "Channel 113 - The Hotspot Issue"
  - "When Processors Attack"
- **Summary**

Experiences

- "Channel 119 – The Crushed Pin Issue"
  - After several weeks of successful testing on POWER5+ early-user hardware (EUH), a rash of contact issues started happening, and worsened over time
  - The contact fails were always with only a few (1-3) signals, and Channel 119 was by far the most common
  - There was no evident pattern isolating specific testers, probecards, or product vintages

Experiences

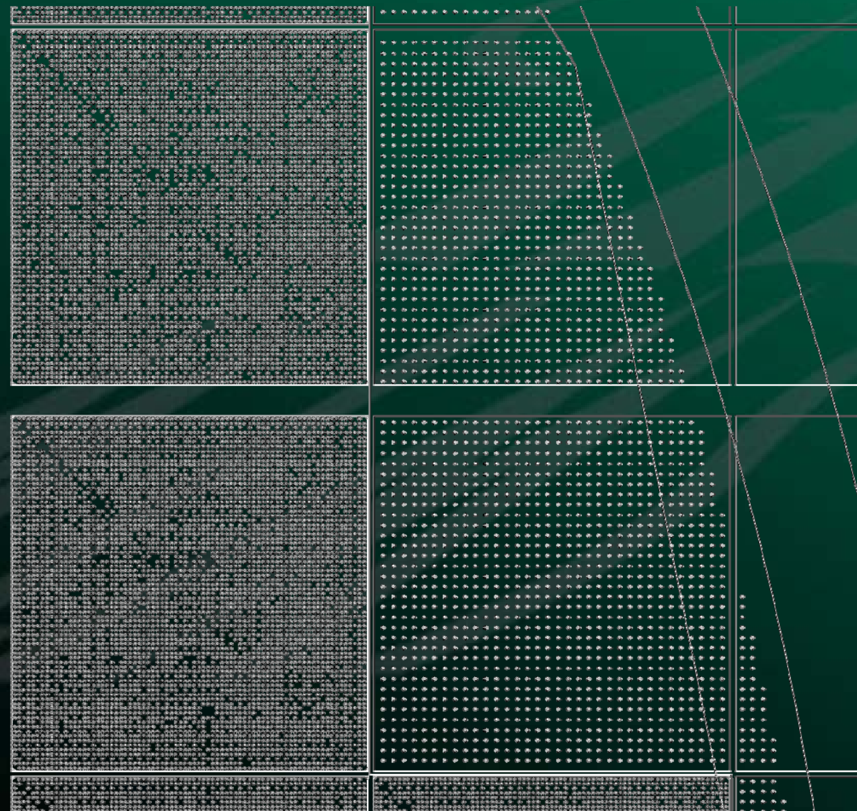
- "Channel 119 – The Crushed Pin Issue"
  - Inspection of impressions on the wafer did not reveal any evidence of light-probing, or on the C4 for Channel 119
  - No evidence of TFI probe damage was observed under standard microscope inspection

Experiences

- "Channel 119 – The Crushed Pin Issue"
  - During further "micro" inspection of the failing C4 hitmark on the wafer, indexing from site to site revealed a deep C4 impression on a *non-functional, partial site*

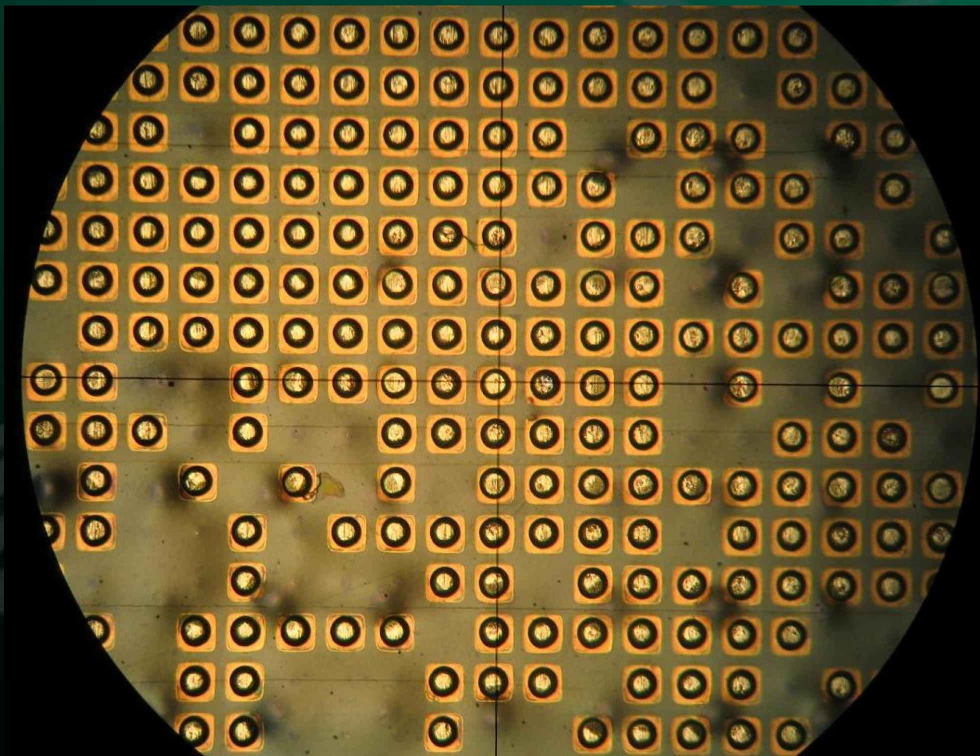
Experiences

- "Channel 119 – The Crushed Pin Issue"
  - IBM does not use the product C4 image for partial sites on the wafer edges



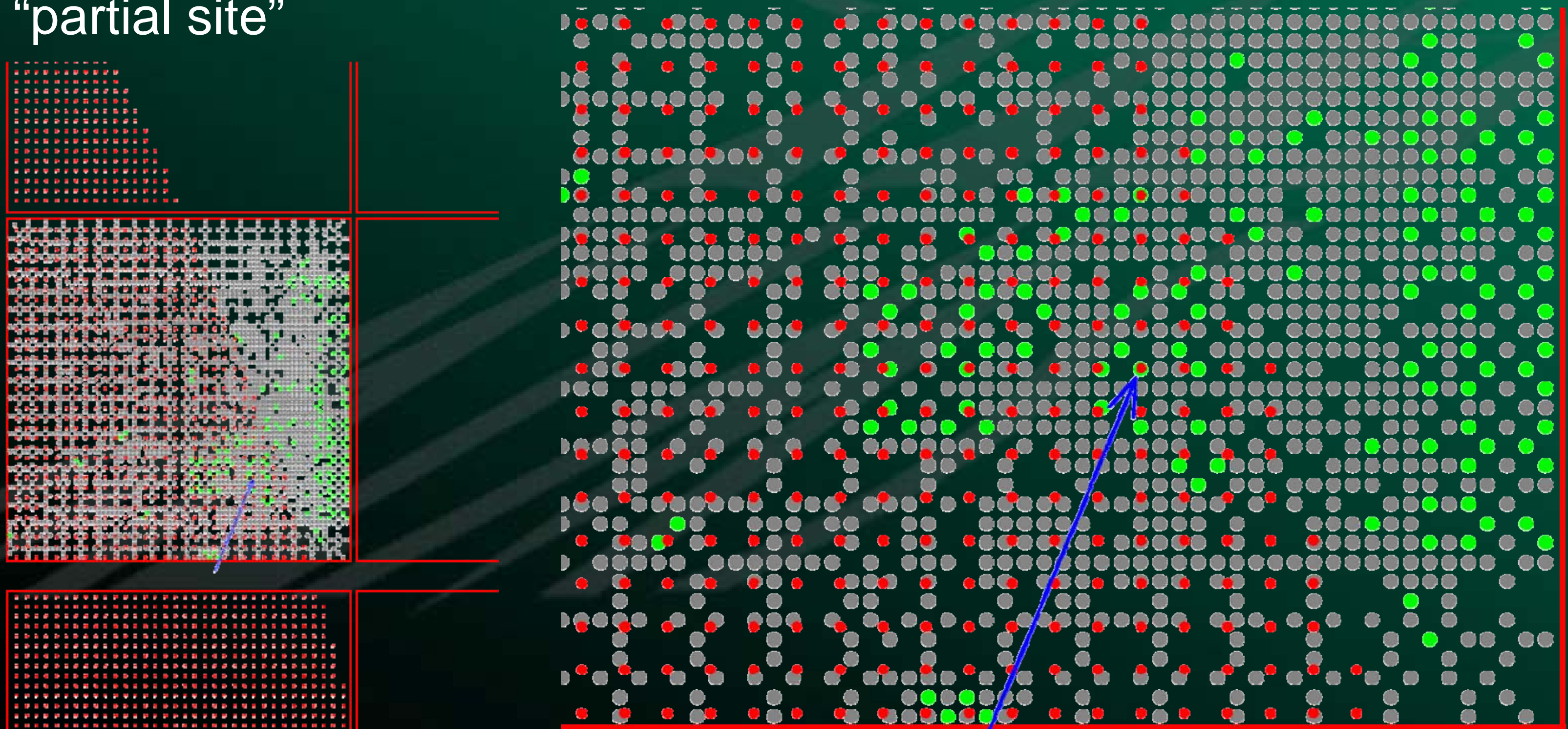
Experiences

- "Channel 119 – The Crushed Pin Issue"
  - Closer inspection of a failing TFI probe revealed uniform impressions in the film



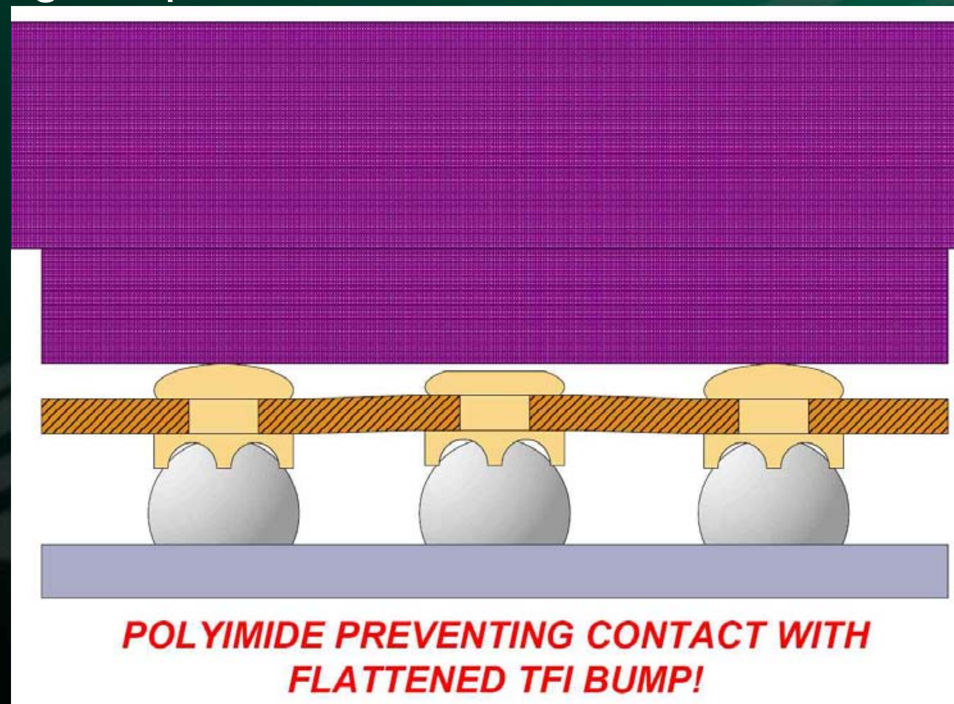
Experiences

- "Channel 119 – The Crushed Pin Issue"
  - An overlay of the probe array on data for the C4 plating mask revealed that only the few failing signals were hitting C4s on the "partial site"



Experiences

- "Channel 119 – The Crushed Pin Issue"
  - The impressions for Ch. 119 did not look lighter because the polyimide film was strong enough keep the flattened probes from contacting the pedestal under load!



Experiences

- "Channel 119 – The Crushed Pin Issue"
  - Lesson Learned:
    - *Use the die mapping feature on the prober!*

TFI™ Probes in Production

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  - Why does IBM use TFI?
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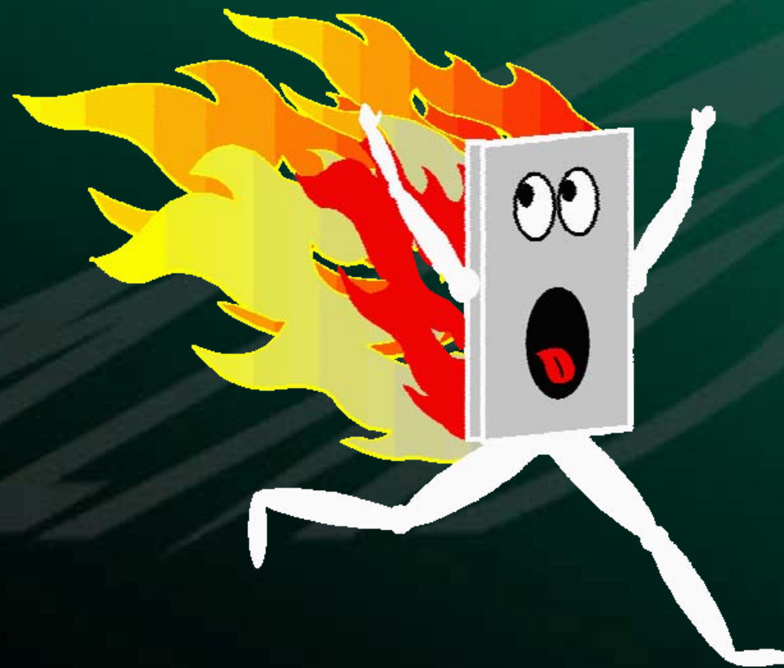
- ***Experiences***
  - "Channel 119 - The Crushed Pin Issue"
  - *"Channel 113 - The Hotspot Issue"*
  - "When Processors Attack"
- **Summary**

Experiences

- "Channel 113 – The Hotspot Issue"
  - Test engineers began noticing high fallout on POWER5+ for faster chips on the 2nd test pass (70°C). An unwelcome effect was revealed during the high-corner voltage screen ….

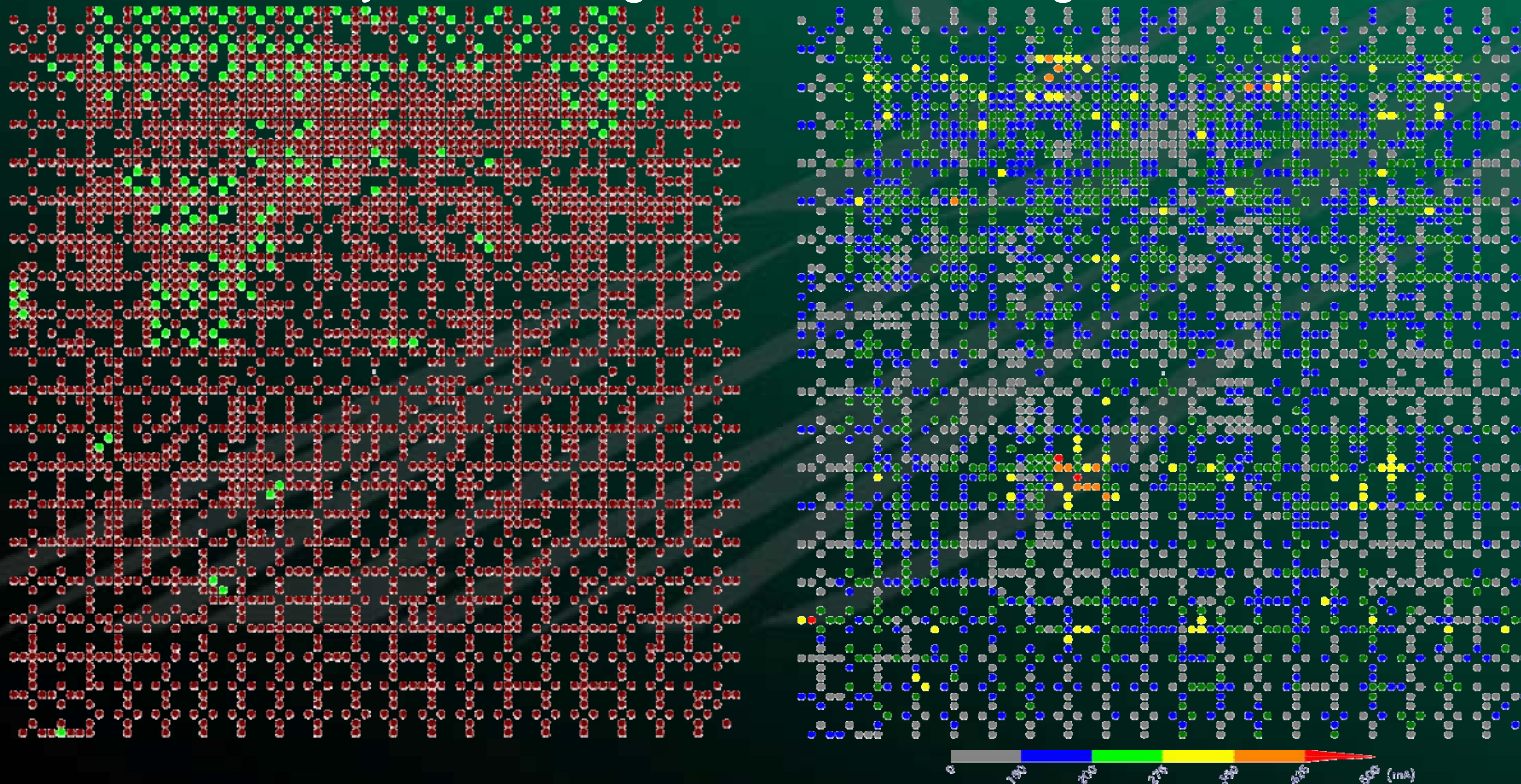


Experiences

- “Channel 113 – The Hotspot Issue”
  - IBM uses Built-In Self Test (BIST) in our test methodology so:
    - *Not all signals need to be probed at wafer*
    - *Testers don’t need as many signal cards*

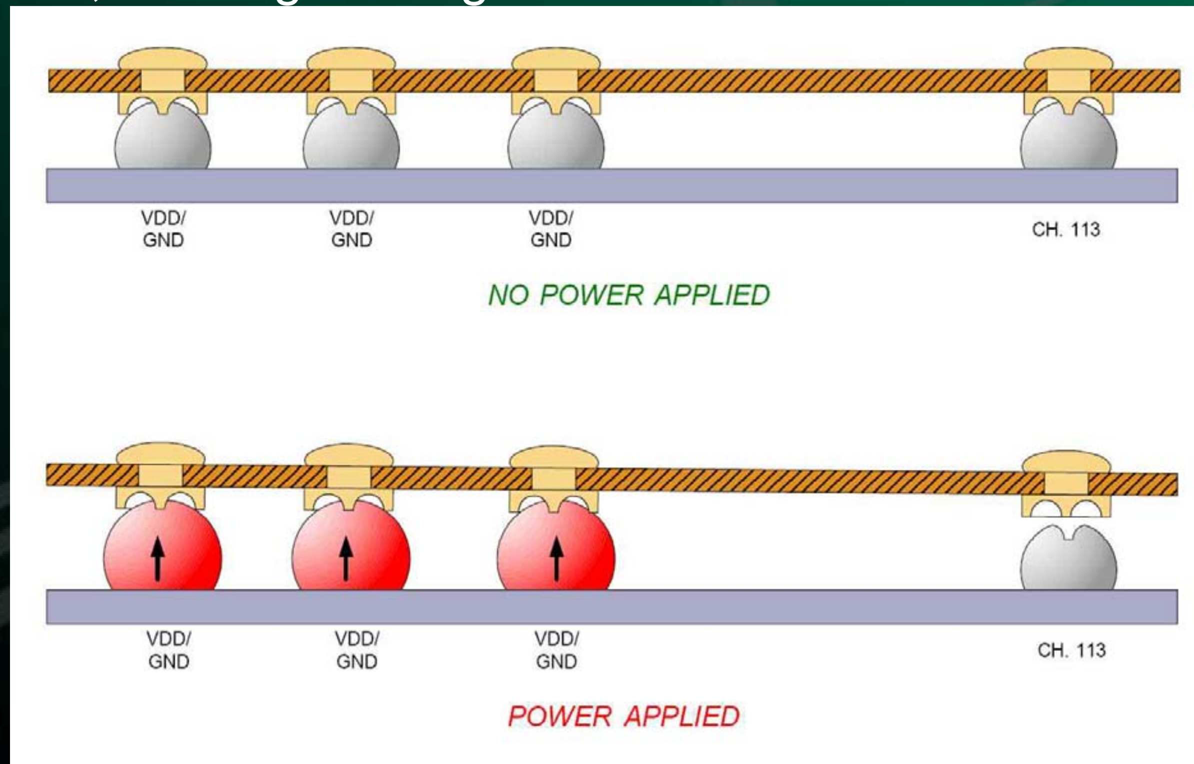
Experiences

- "Channel 113 – The Hotspot Issue"
  - The chip has the two logical cores on the top 3rd of the die, and the L2 arrays on the right and bottom edges



Experiences

- "Channel 113 – The Hotspot Issue"
  - On faster dies, a thermal gradient developed during this voltage screen, causing one signal in the corner to lose contact

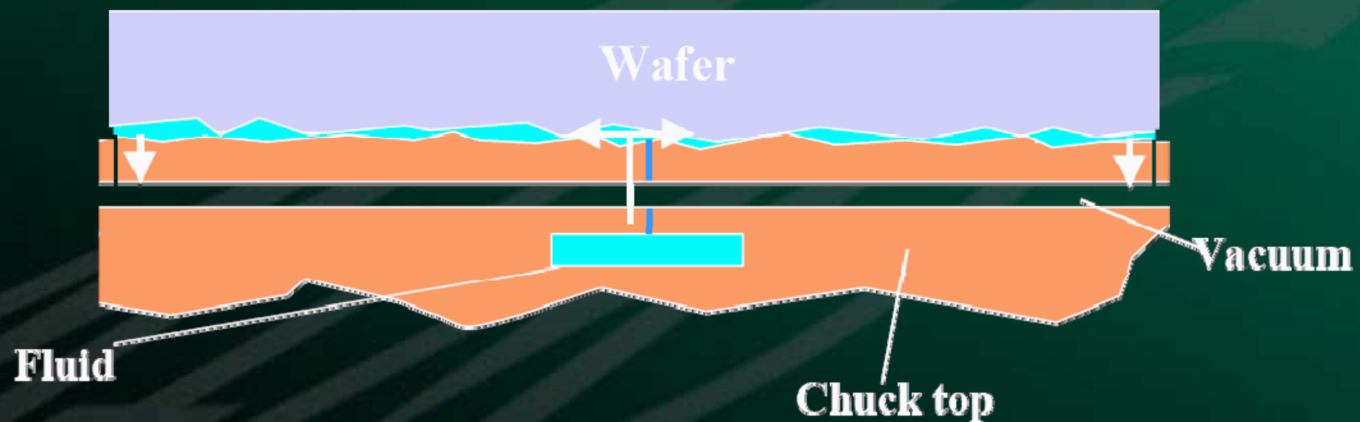


Experiences

- "Channel 113 – The Hotspot Issue"
  - The solution was to build in a pull-up on that signal in the next revision of the chip design, since it only needed to be in a certain state during the screen
  - To test older product, the chuck temperature had to be lowered by 15°C so the cores didn't get as hot

Experiences

- "Channel 113 – The Hotspot Issue"
  - Using a prober with a Liquid Thermal Interface (LTI) chuck would have likely solved this issue, but was not qualified for production at the time



Source: Tokyo Electron

Experiences

- "Channel 113 – The Hotspot Issue"
  - Lesson Learned:
    - *Don't mix with TFI with thermal gradients across a die!*

TFI™ Probes in Production

- **Background**
- **Benefits**
  - Why does IBM use TFI?
- **Challenges**
  - Parallelism and Co-Planarity
  - Vacuum
  - Handling and Cleaning
  - Thermal Constraints
  - Retest Constraints
- ***Experiences***
  - “Channel 119 - The Crushed Pin Issue”
  - “Channel 113 - The Hotspot Issue”
  - *“When Processors Attack”*
- **Summary**

Experiences

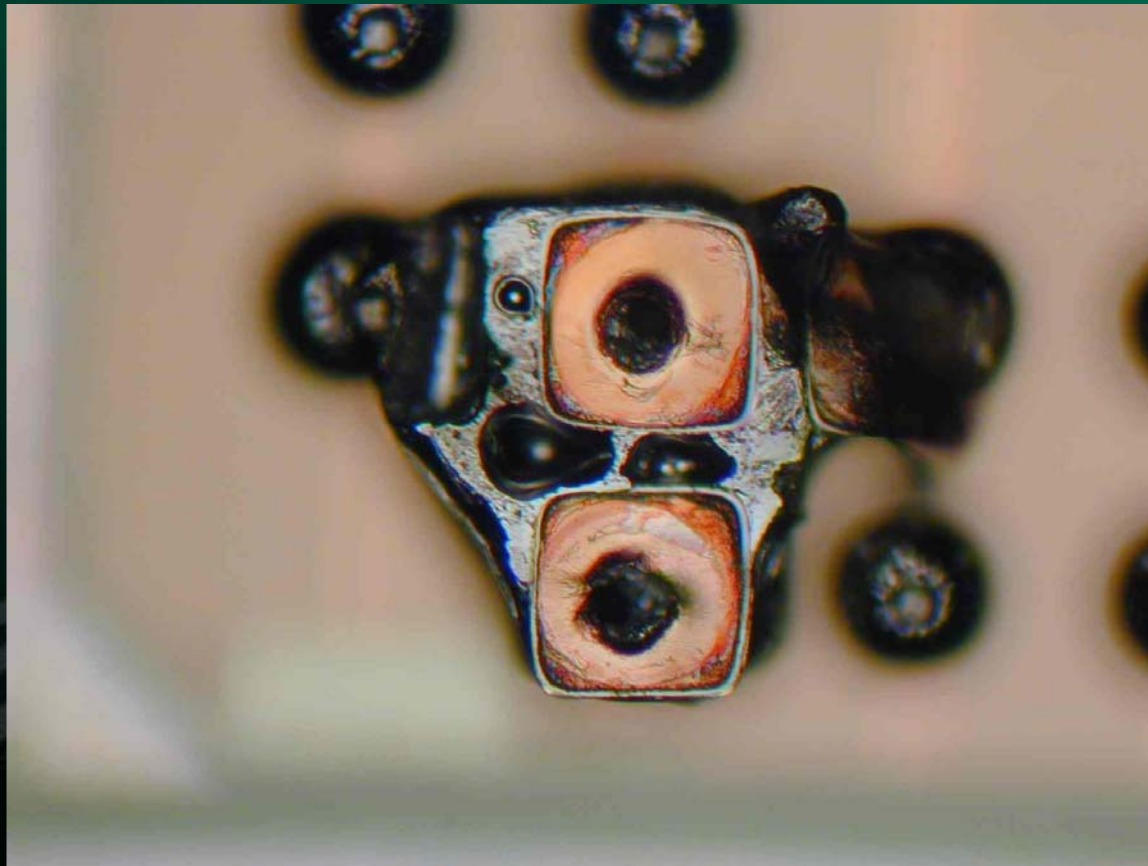
- "When Processors Attack"
  - The Early-User Hardware (EUH) phase of developing a new chip design is usually an "eventful" period on the test floor
  - The following are samples of the sacrifices our probes have made to protect our servers….

Experiences

- "When Processors Attack"
  - Unfortunately, these are all different probes

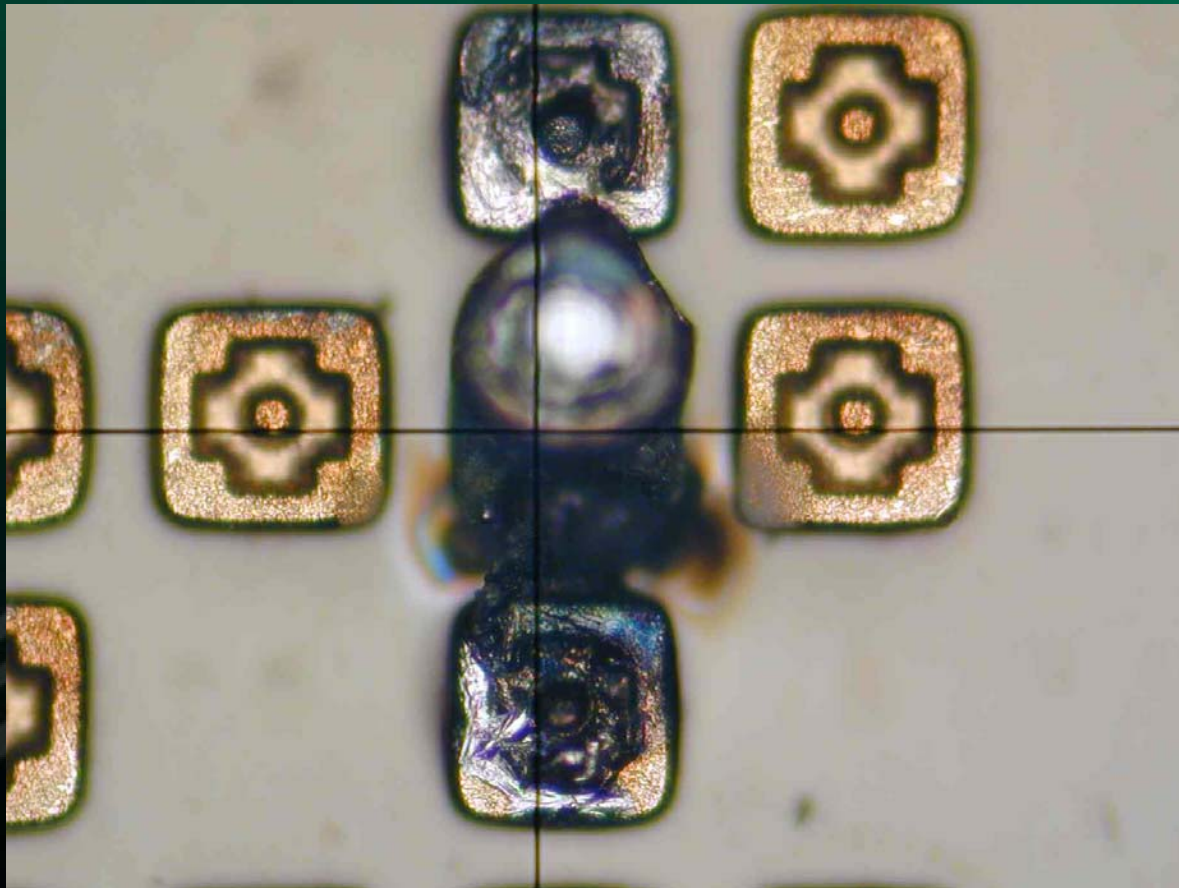
Experiences

- "When Processors Attack"



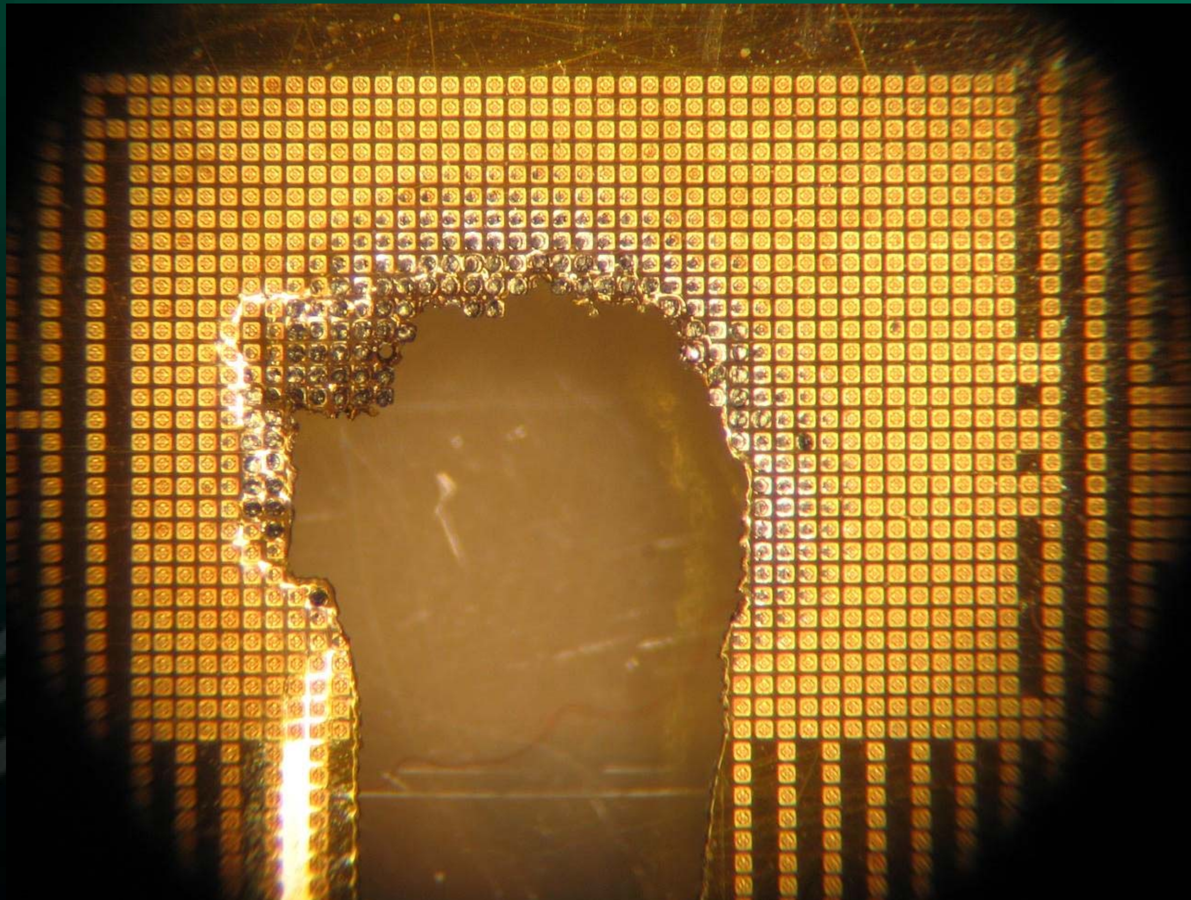
Experiences

- "When Processors Attack"



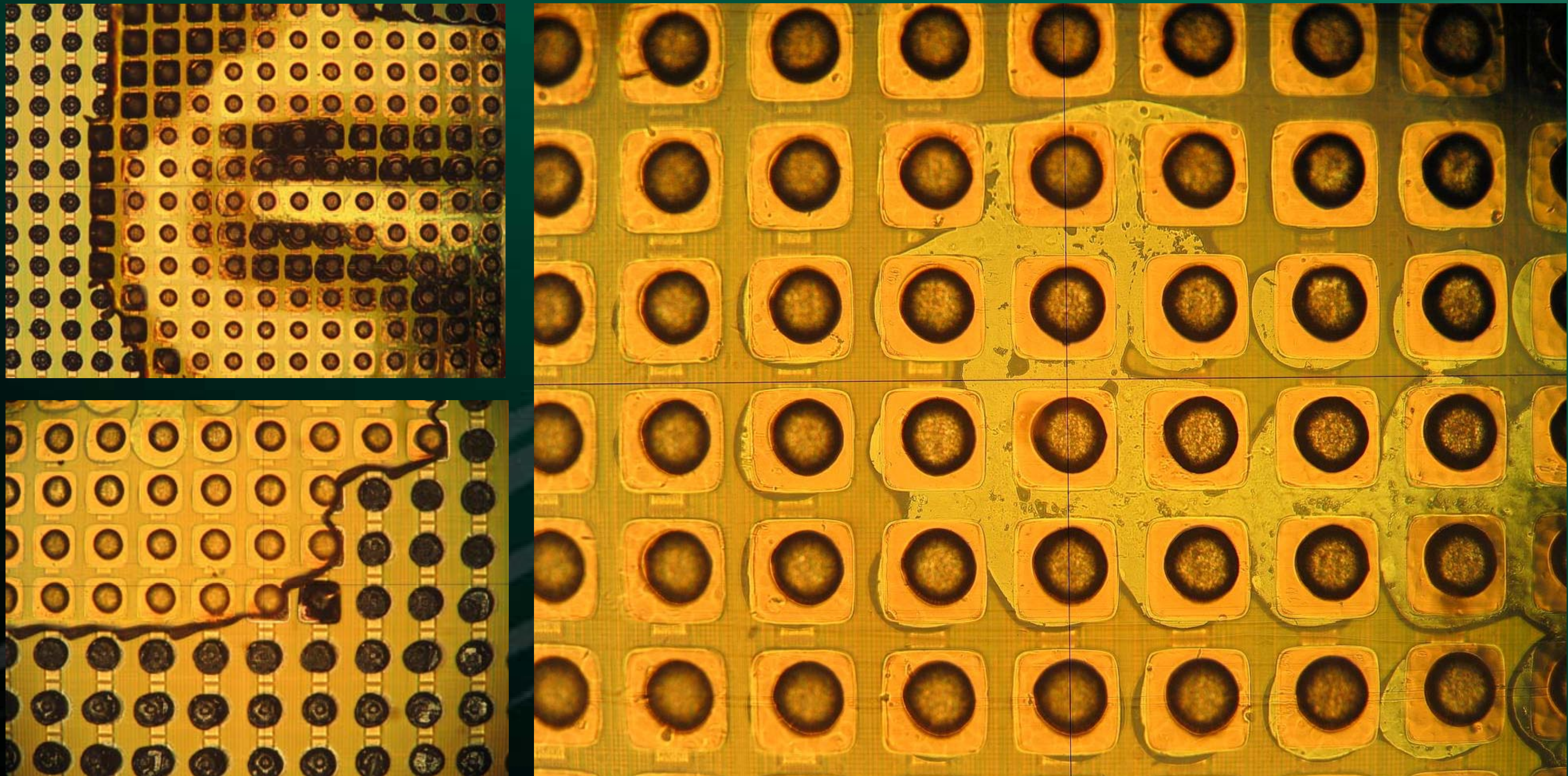
Experiences

- "When Processors Attack"



Experiences

- "When Processors Attack"



TFI™ Probes in Production

- **Background**
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  - Thermal Constraints
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- **Experiences**
  - “Channel 119 - The Crushed Pin Issue”
  - “Channel 113 - The Hotspot Issue”
  - “When Processors Attack”
- ***Summary***

Summary

- TFI is not a very "forgiving" probe technology
- TFI has demanded significant effort and resources make it a production-worthy probing solution
- IBM has developed significant infrastructure around TFI to bring it to the production test floor

but…

- TFI has enabled IBM's test capability to match the increasingly high performance and complexity of its server and mainframe processors
- TFI has enabled IBM to gain and maintain its performance lead in the high-end server market

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