IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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A Cost-Effective Approach for Wafer Level Chip Scale Package Testing

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AGENDA

- The Need
- WSP-Wafer Scale Packages
- WSP- Manufacturing Test Flow
- WSP Probe Card Technologies
- Challenges
- Comparative Summary
- Discussion

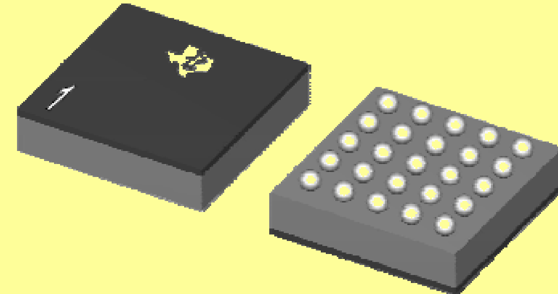
THE NEED

TI has been testing packages at final test after singulation for some time. However, the increasing use of WLCSP- wafer level chip scale package formats require cost-effective RF testing at the wafer-level or before singulation to further reduce test costs and be globally competitive.

TI-WCSP Wafer Chip Scale Packages

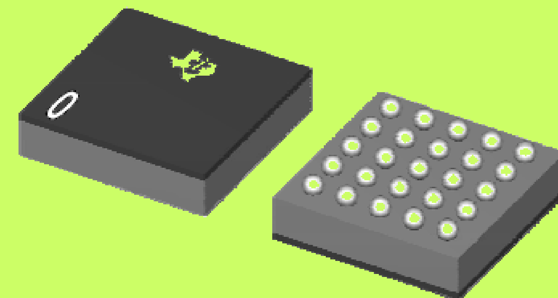
NanoStar™

- WCSP with eutectic SnPb Solder

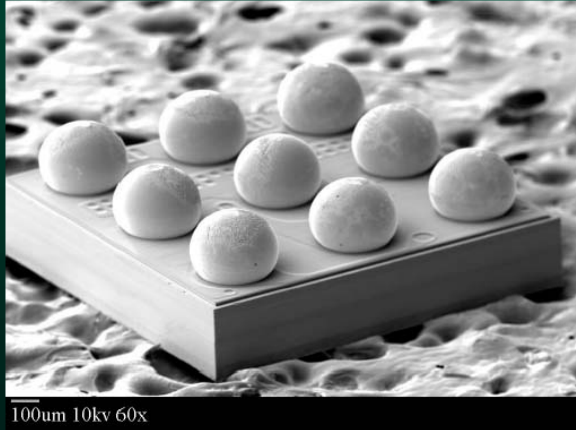


NanoFree™

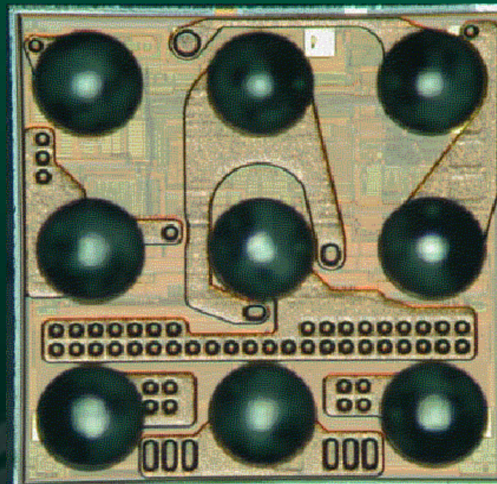
- WCSP with Pb-Free Solder



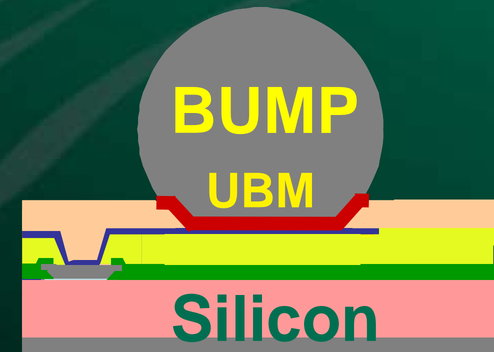
WCSP- Redistribution Layer-RDL



SEM VIEW



OM VIEW

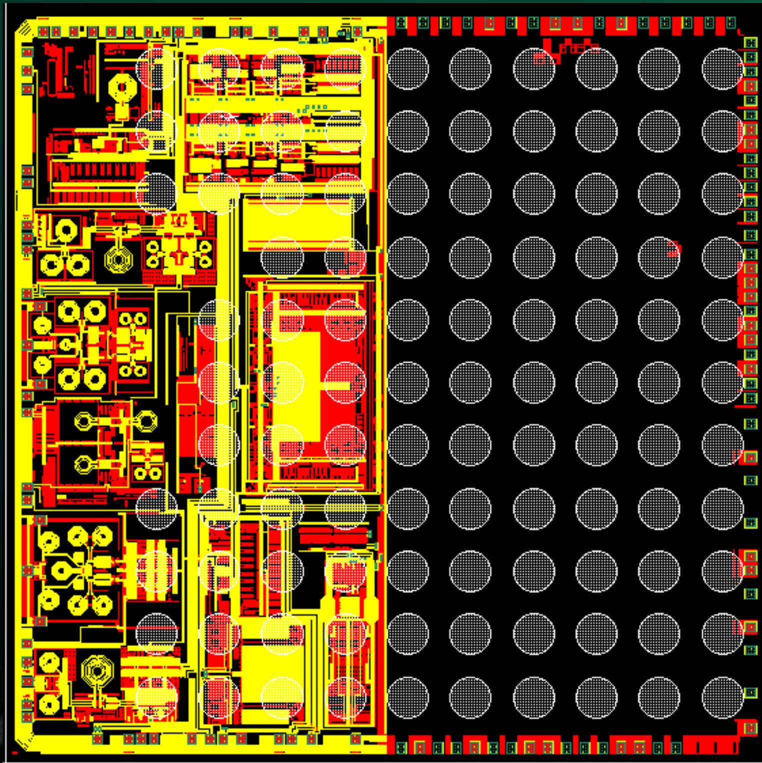


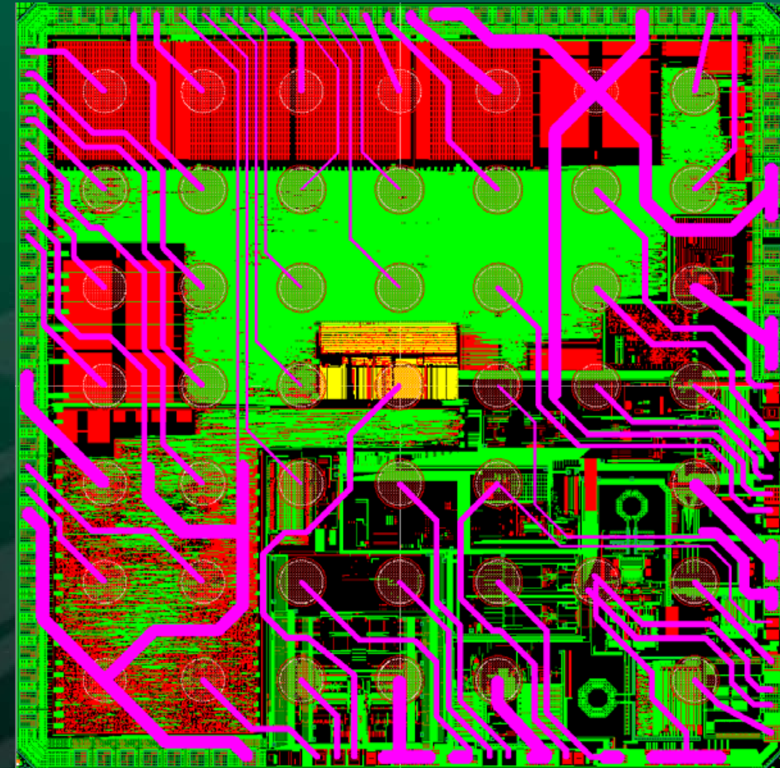
RDL

XS VIEW

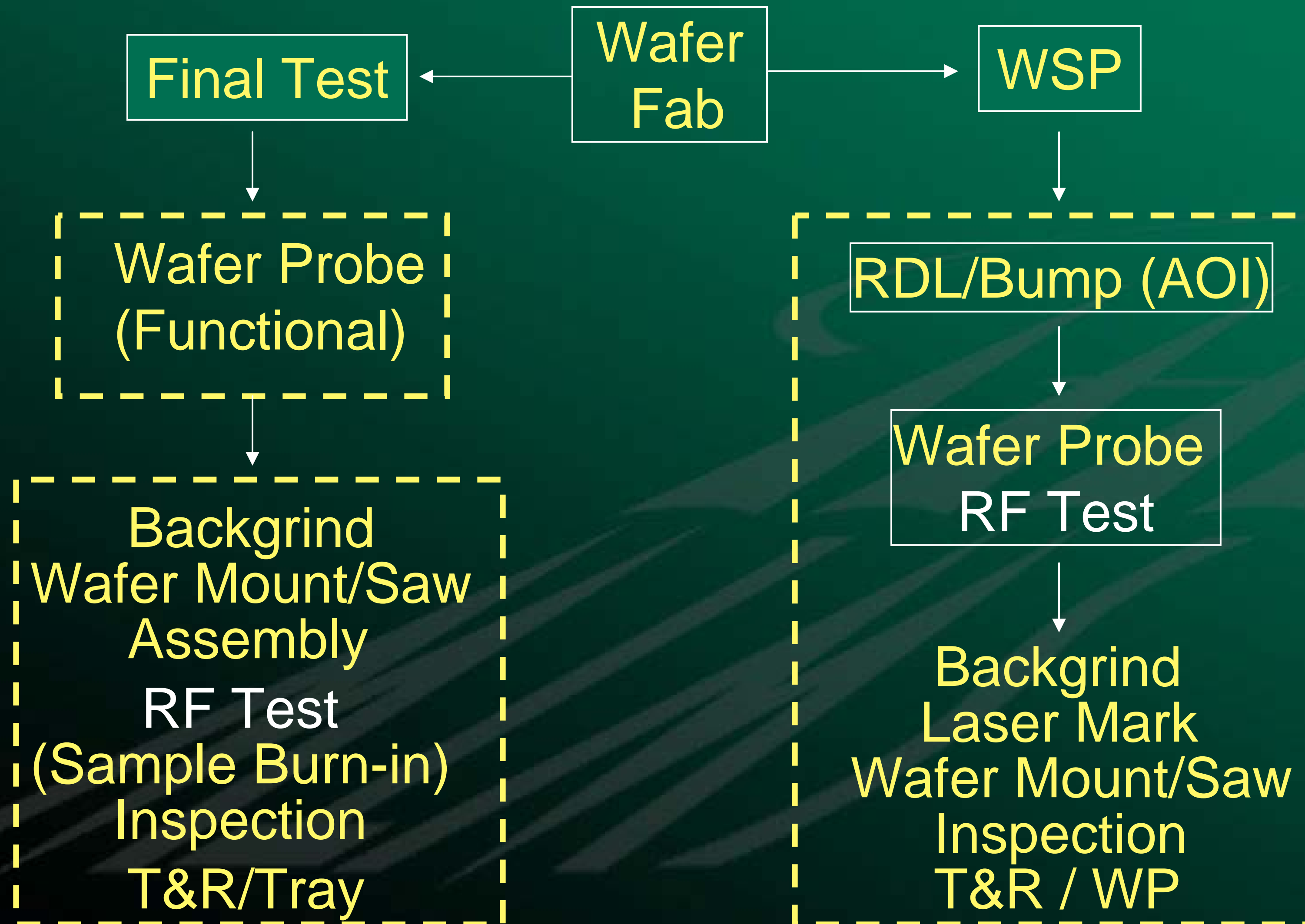
Image Courtesy of the Tucson Reliability Test Lab

WLCSP w/ RDL Examples





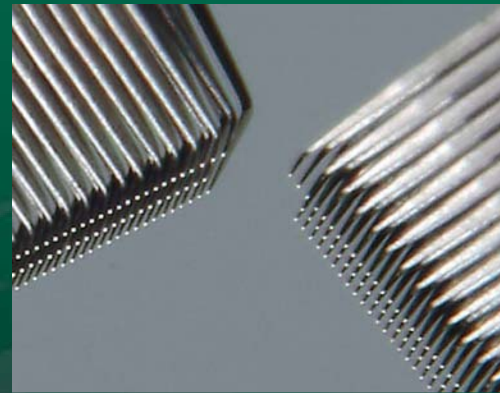
WSP Test Flow -Simplified



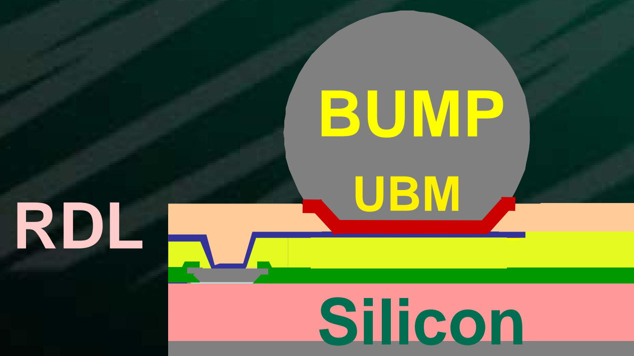
Current Wafer Level Probe Card Technologies

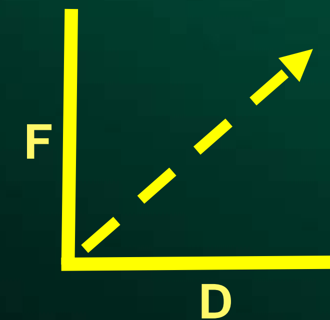
- Cantilever- (Needle Probes)
- Vertical- (Buckling Beam)
- Membrane (Beam Probes) RF

Conventional Cantilever

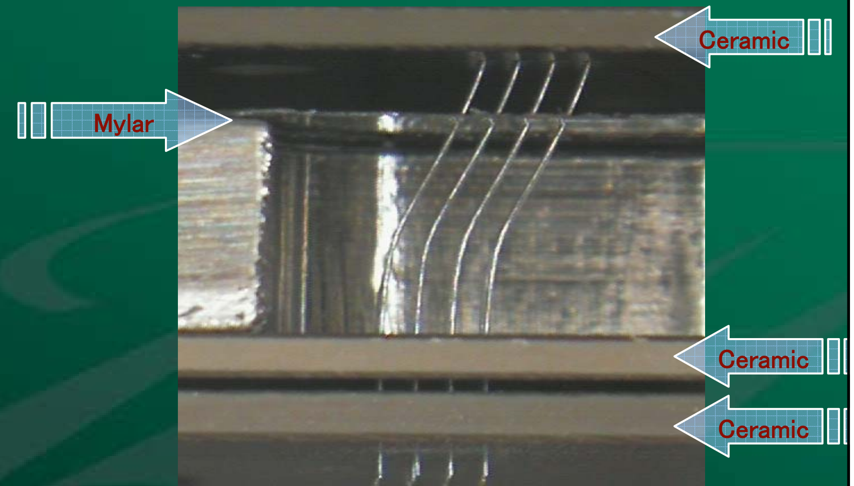


Cantilever Probes

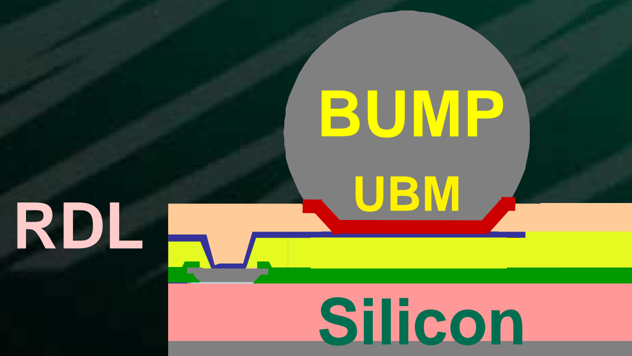


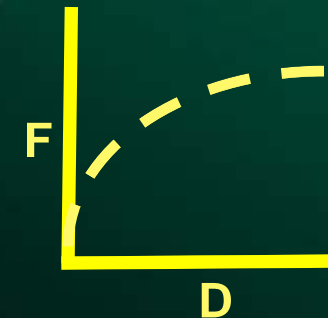


Vertical Buckling Beam

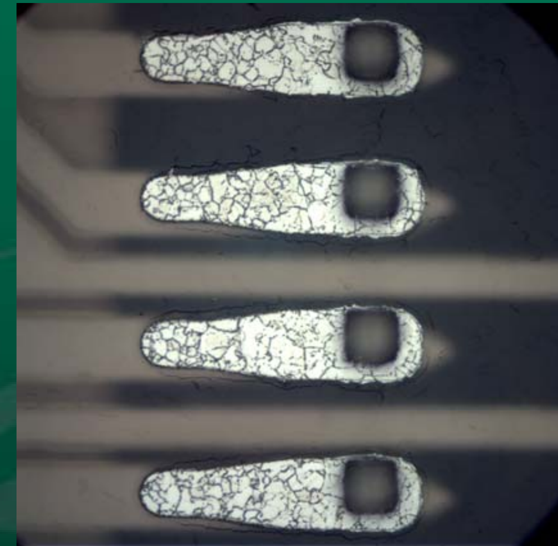


Buckling Beam Probes

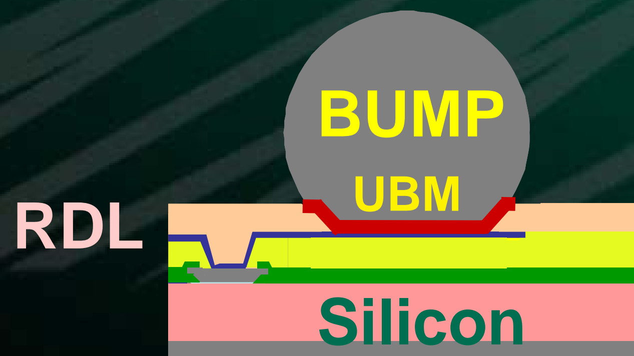


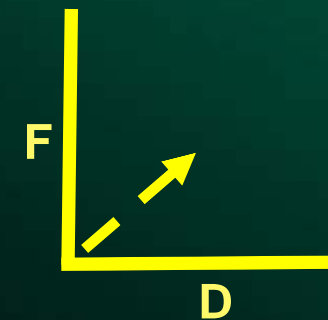


Membrane RF Probe Beams



Probe Beams





WSP Probe Card Tech Applicability

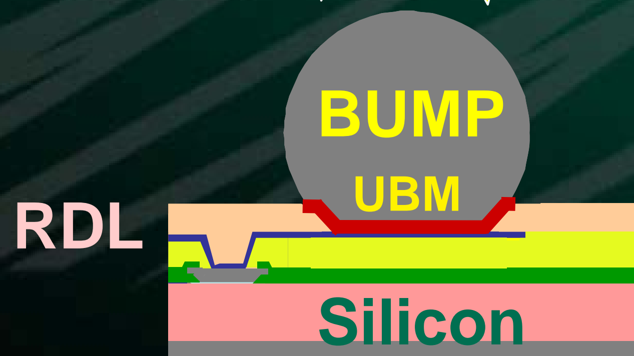
Both cantilever and VPC probe cards exhibited limited electrical properties as well as other physical & operational limitations and can reach 0.3mm but require a space transformer, i.e., MLC/MLO to PCB.

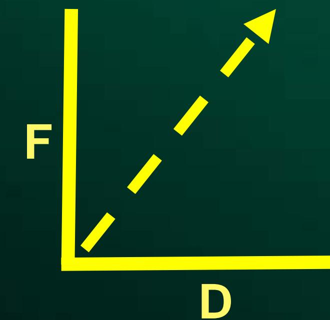
Membrane probe cards have been employed for FC applications that need controlled impedance for RF (radio frequency) testing and can easily reach 0.3mm, but at some cost and also with deflection/ compliance limitations.

Current WLCSP FT-final test contactor technologies, which already use similar sockets and RF pogo pins, so that a similar approach can be also used in wafer level probe card form is the preferred cost-effective approach, to avoid an expensive probe card and skip the RF FT step.

Vertical RF Pogo-Pin

RF Pogo Pins

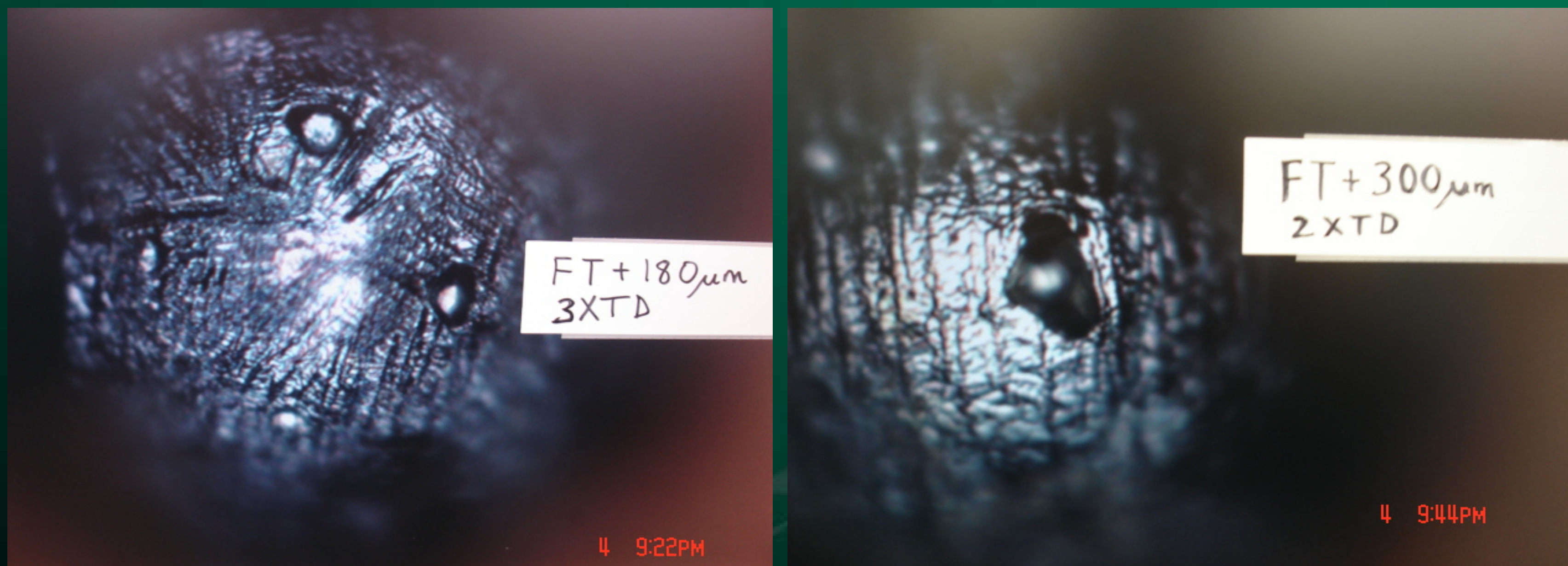




WSP Probe Card Integration Challenges

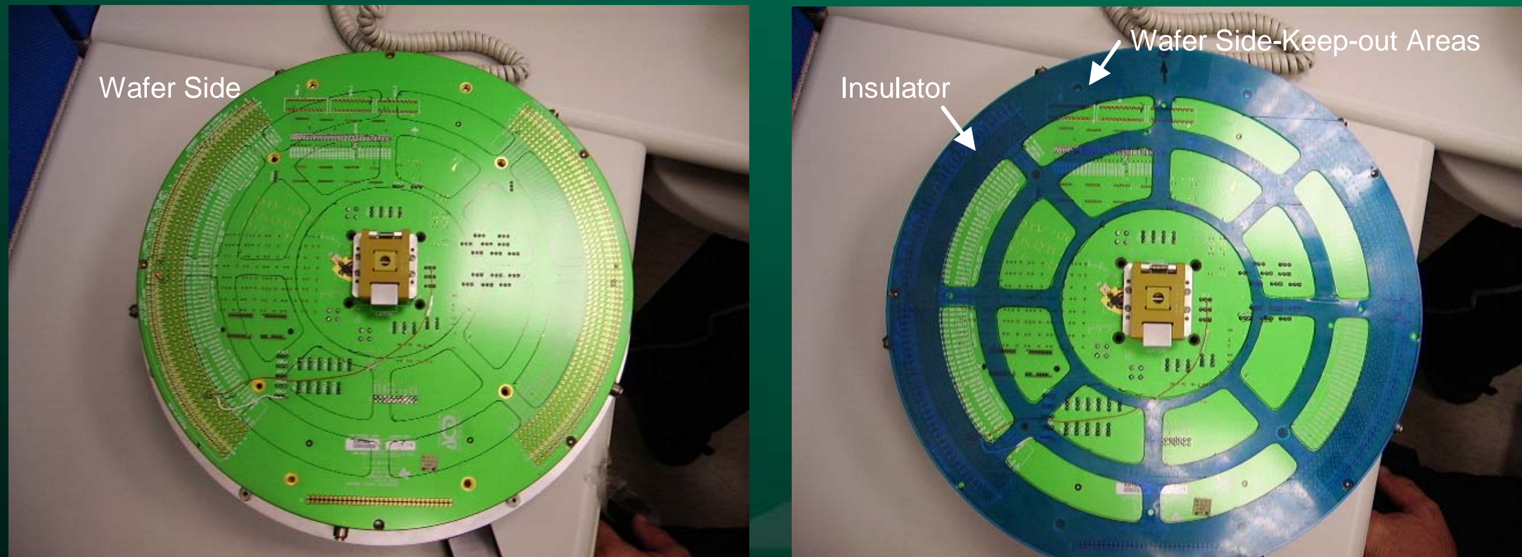
- Probe to Bump Interaction (OT, Alignment)
- Prober/tester Mechanical Interface (Components, Deflection)
- Prober/PCB/Socket/Pogo-Pin and Bump Planarity (Net Compliance, Bump Hts Vary)
- Socket/ Pogo-Pin Design (RF, Tip Shape)
- Alignment Algorithm (Auto Z-Ht Control)
- Cleaning (Media, Stepping, CRes)
- Thermal Requirements (-40 to 129C)
- Industry Maturity (Supplier Base)

Probe to Bump Interaction



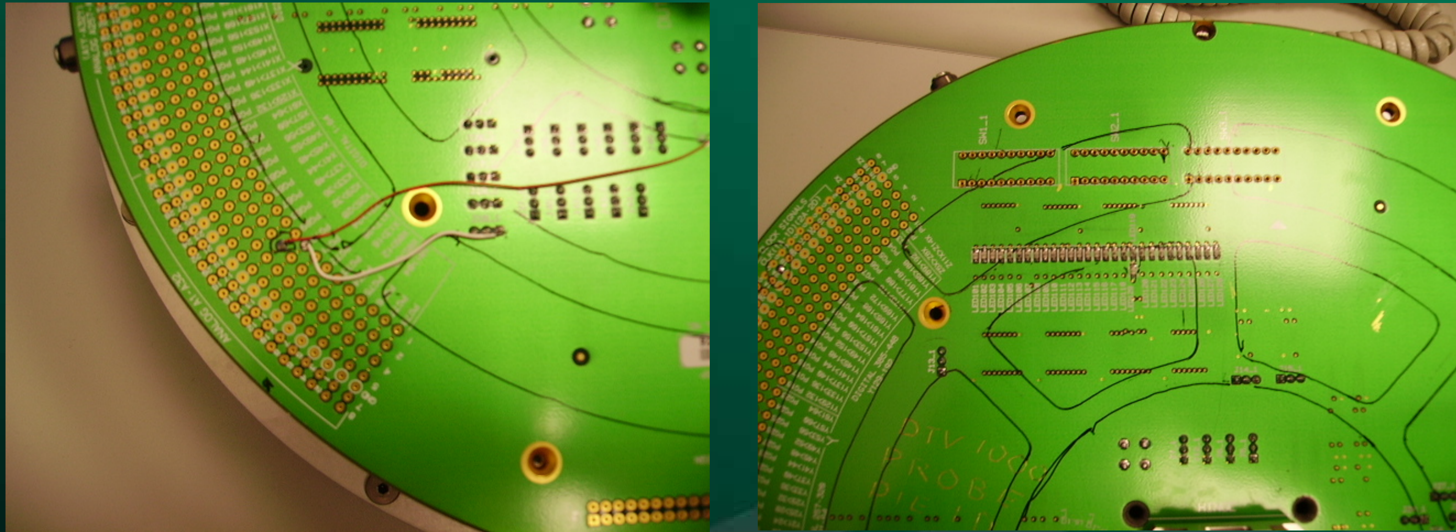
Pogo-pogo tip morphology, planarity and alignment critical to control amount of over-drive. For example, a 4-pt Crown tip uniformly distributes the force (L) as compared to when only 1 of 4 tips contacting, showing more bump deformation "gouging" as a result (R).

WSP Probe Card Design



Wafer side (L) and “blue” insulator (R) overlaid as a template showing exposed areas that are allowed between probe card and probe card support plate for components. With a max height (Z) of 0.040” allowed for this tester interface configuration.

Wafer Side Component Interference

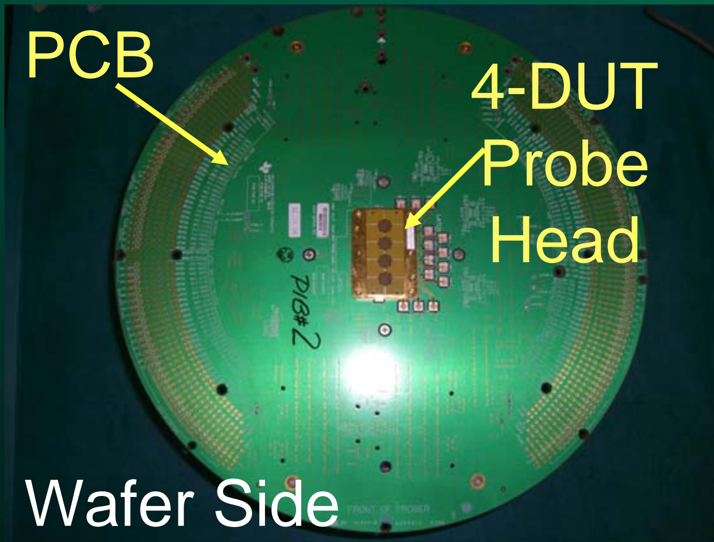


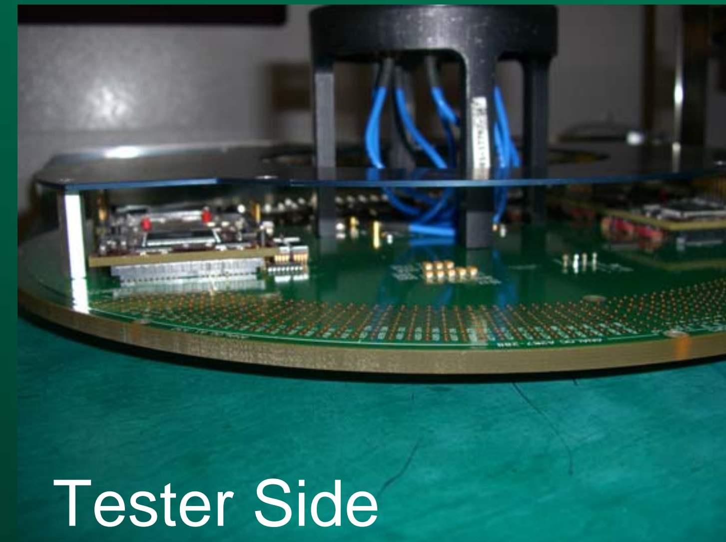
- Jumper “Blue Wires”
- Through-Hole-Mount Solder Joints
- LED Components
- PCB Barrel Vias Protruding
- Sockets and/or Pogo Pins Heights

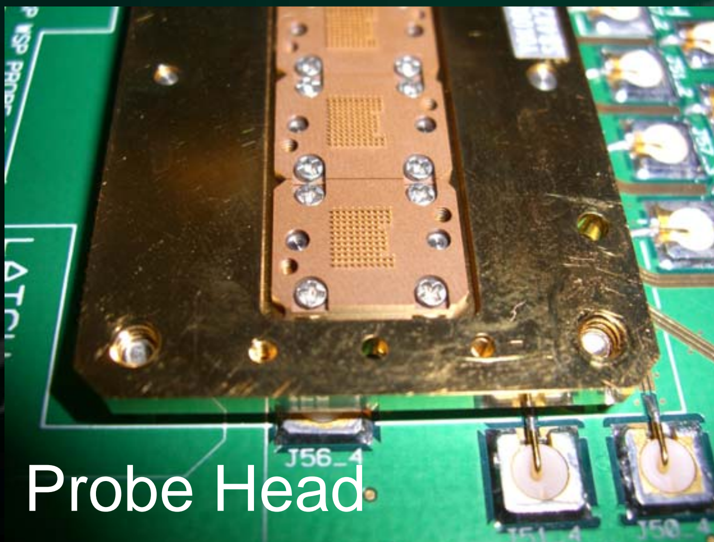
Tester Side Component Interference

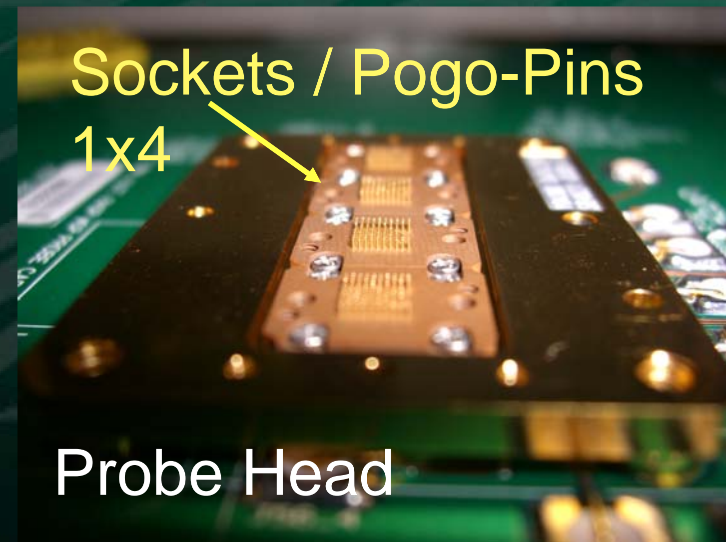
Components as located would interfere with interface tester features such as an "inner" ring (red circle) on PCB tester side (L) to Tester pogo-pin outer ring array on tester tower (R).

WSP Probe Card RF Pogo Pin QS

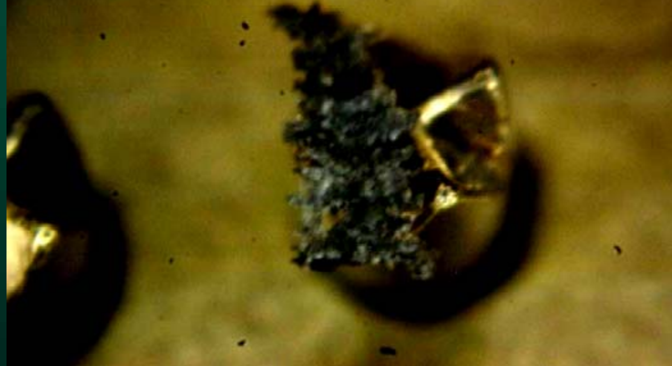




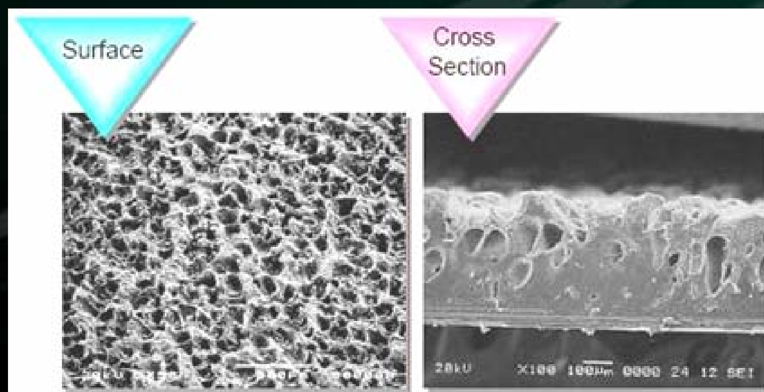


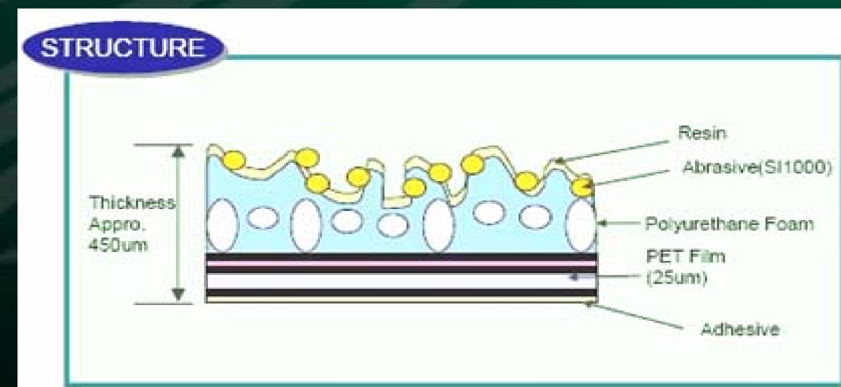


In-Situ (Prober) Pogo Pin Cleaning



Leveraging FT cleaning learning's. Only the 4 tips of this 4-pt. crown pogo pin is cleaned or needs cleaning. Pogo-pin inserted into abrasive and compliant material

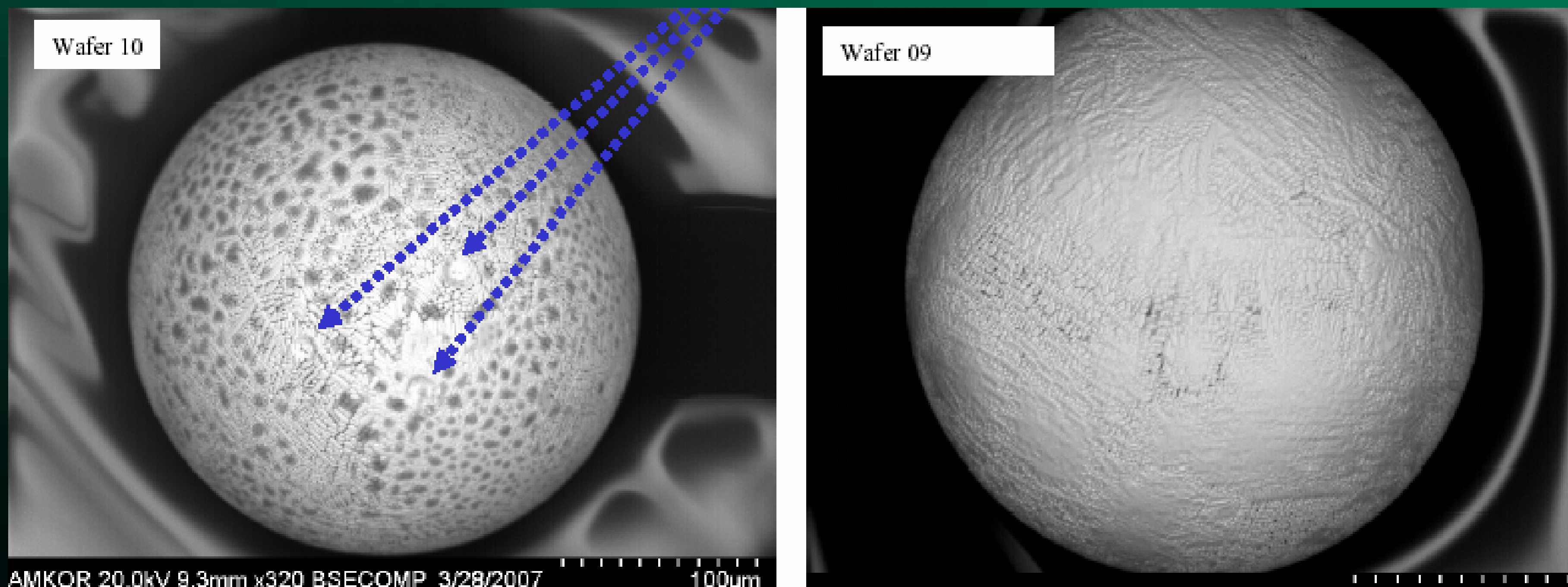




ITS / JEM

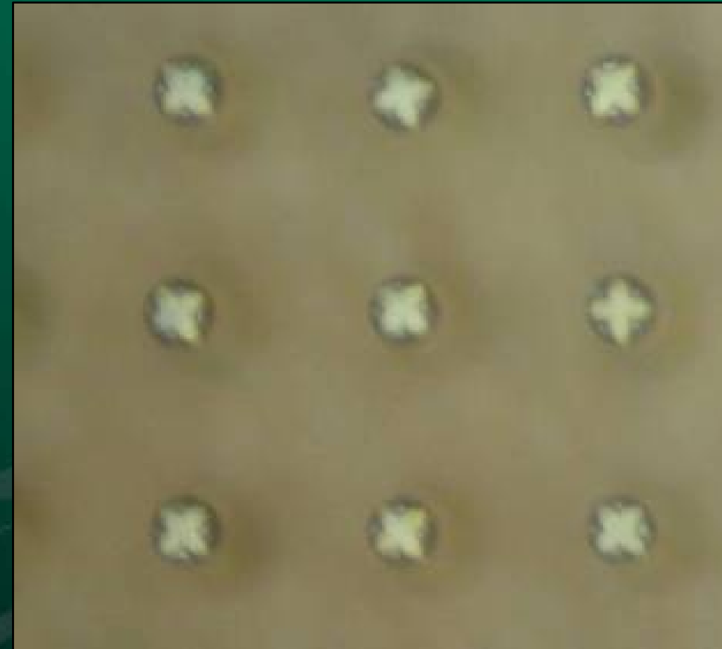
Bump Surface Condition

Carbon-Rich Areas



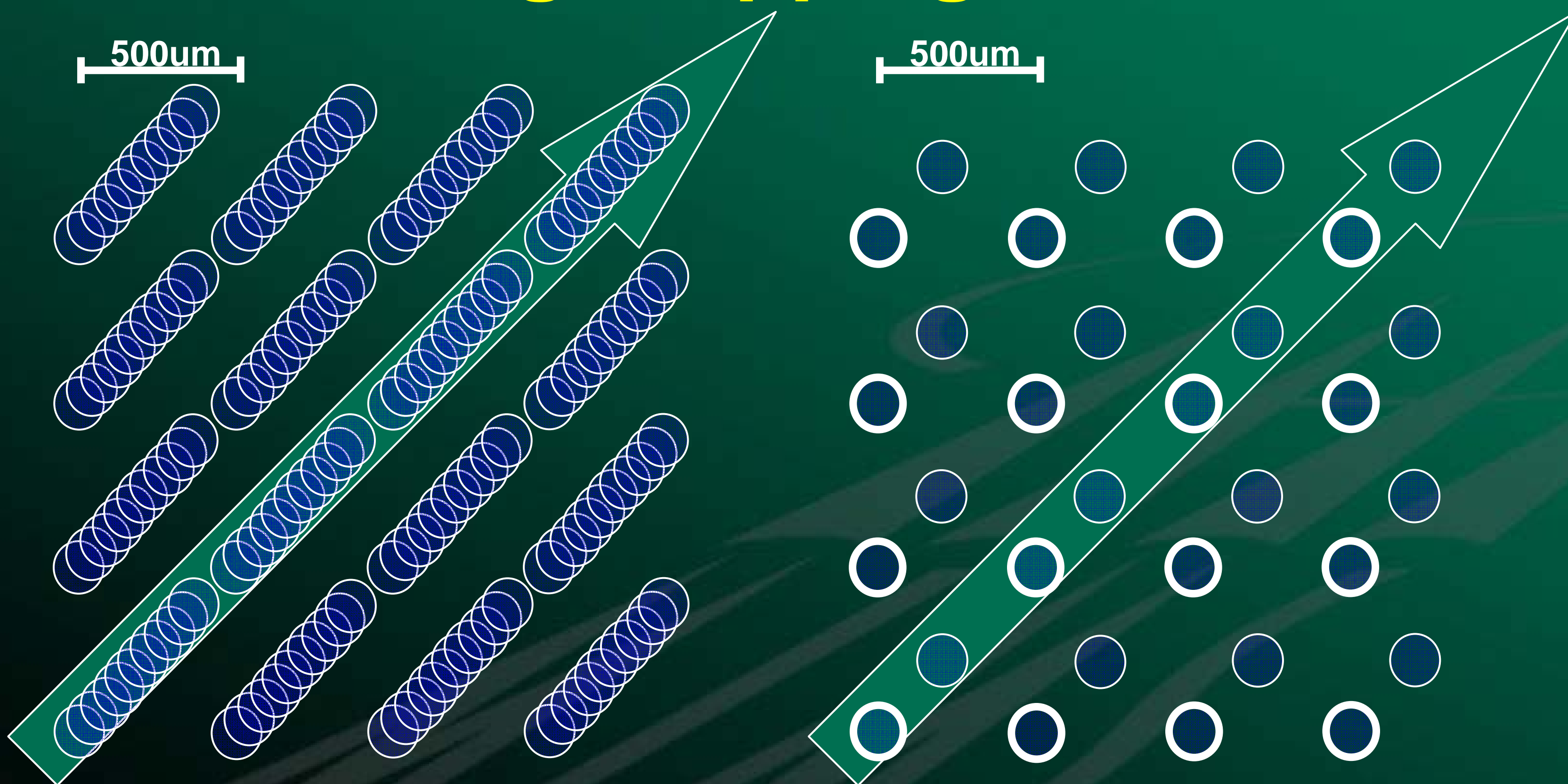
Bump surface condition impacts pogo-pin ability to penetrate bump surface as well as, pogo-pins surface if not cleaned effectively for subsequent bump probing.

Pogo-Pin Condition



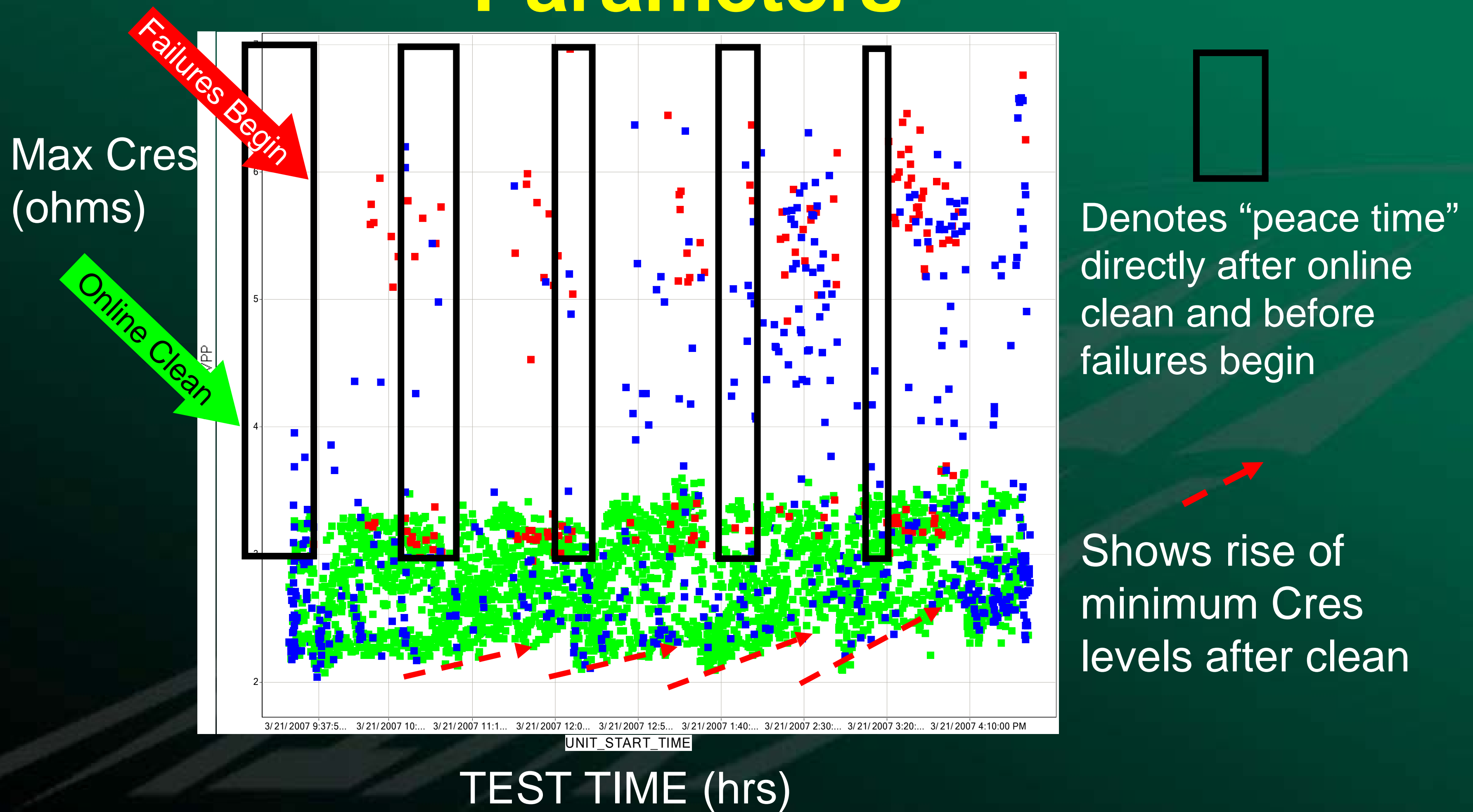
Cleaning media impacts Pogo-pin surface condition and subsequent electrical contact to bump, if cleaning settings not optimized.

Cleaning Stepping Distance

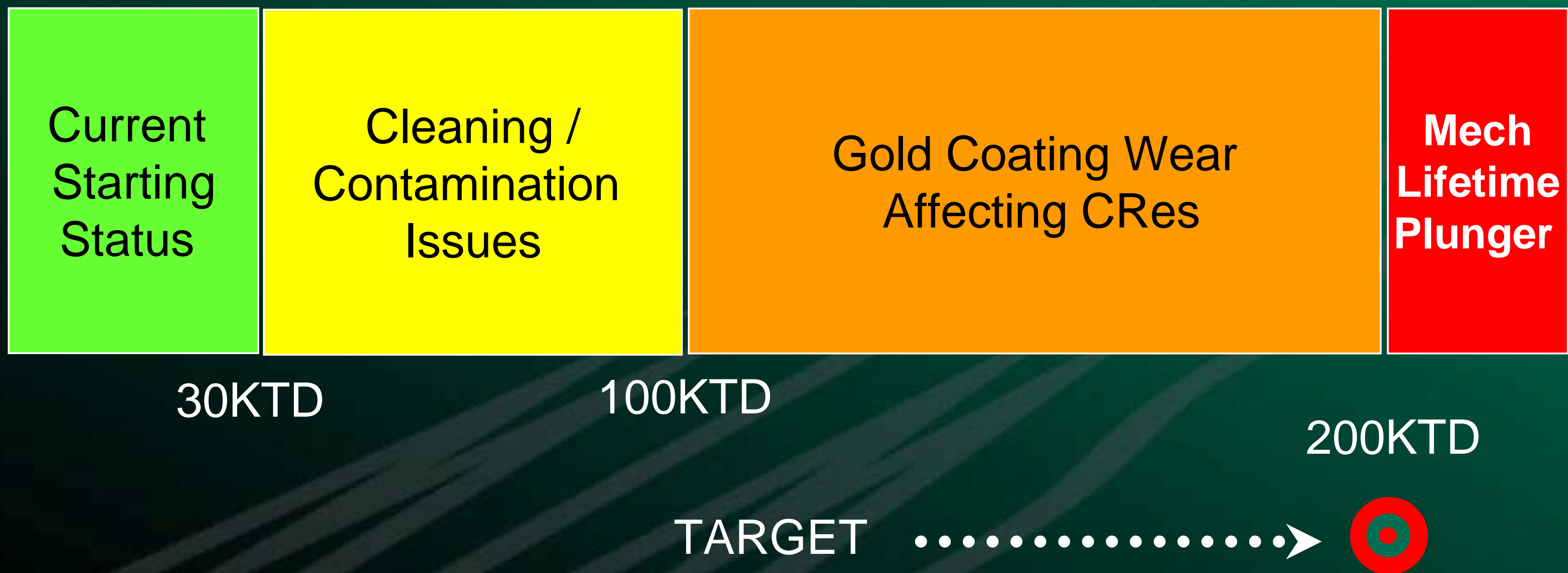


Increasing the stepping distances on cleaning media greatly improves cleaning efficiency. Although, at the expense of using more cleaning media.

Using CRes to Optimize Cleaning Parameters



Key Milestones for WSP Probe Card Lifetime Optimization



WSP PROBE CARD SUMMARY

Technology	PROs	CONs
Cantilever Needles	Low price Short Lead-time for New Designs Repairable Contacts Many Qualified Suppliers	Electrically Limited Area Array limited F / D Linear Bump-Top Damage/ Reflow
VPC Buckling Wires	Dense Multi-site x16 F / D Profile Hi-Temp Stability Many Qualified Suppliers	Electrically Limited Initial Price and Lead Time Bump-Top Damage/ Reflow Probe binding
Membrane Probe Beams	Electrical Properties >40 GHz Pitch <0.3mm Small scrub marks	High Price F/D Limited Range Few Qualified Suppliers Dense multi-site < x4
Socket Pogo-Pins	Low Price Electrical Properties (5GHz) Small Marks on Sides of Bump Multi-site x8, x16	Current Pitch Limited to 0.4mm Prober Integration, cleaning, etc. 0.3mm PCB supplier base Linear F / D

Probe Technology "Gate" for WLCSP Enablement

However, the challenge for a direct 0.3mm socket to PCB connection, is that the PCB technology is not converging to what a socket can be manufactured.

In other words, sockets can be manufactured <0.3mm pitch, but conventional PCB technology "cliff" is currently 0.4mm pitch

Future Work

- Optimize Prober/ Probe Card/ Wafer Settings
  - Planarity vs Pogo-Pin Deflection Optimization
  - Alignment Method / Algorithm
- Optimize Cleaning Settings
  - Media / Tip Design
  - Stepping
- Minimize Probe Card Deflection
  - Tester PCSP Design
  - Mechanical Stiffeners
- Printed Circuit Board Design/ Fab
  - 0.3mm pitch
  - Multi-Site to x16
- Thermal Characterization
  - Cold Temp -40 C
  - High Temp 129 C

Acknowledgements

- Cody Gilleland
- Doyce Ramey
- Kelly Daughtry
- Byron Gibbs