IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Texas Instruments

The Influences of Signal Matching During Multi-site Testing

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San Diego, CA USA

Agenda

- Background
- Problem Statement
- Objective
- Methodology
- Results
- Conclusions
- Acknowledgments

Problem Statement

Approximately 10% of our mutli-site production probe cards are demonstrating signal integrity issues.

- PC's are removed from a production state and put into an engineering issues state -
- Normal diagnostic methods – tester cal, golden unit, PC analyzer – cannot detect failure mechanisms
- Individual die by individual site test as GEC – in parallel sites fail

Objective

To provide a process that allows for effective evaluation and troubleshooting of probe card site related yield problems related to parallel test methods.

PRESENTATION OUTLINE

- Two devices to be discussed in detail
- Issues
  - Yield performance
  - Specific issues.
- Determining cause relationship data analysis
  - Tester
  - Program
  - Probe card
- Performing test
- Analysis results
- Summary

Device A

- Probe parameters
  - Die per wafer - 1533
  - Average Test Time per wafer – 170 min
  - Tester platform – VLCLT UF 3000
  - Probe Card – RASP Cantilever
  - Quad Site
  - Probe Points – 1040
    - 260 points per site
- DUT Parameters
  - Frequency 208 MHZ
  - Six power supplies per site
    - CORE
    - IOs
    - EFUSES
    - ANALOG
    - (2)MEMORY

- **Program Flow**
- **OPEN/SHORTS**
- **OCP**
- **FUSEFARM check**
- **Pre_Tests (scan checker to detect gross failures)**
- **RAM repair**
- **IDDQ Pre-Stress measures**
- **Static Stress (1sec)**
- **VBohHi tests**
- **VNom tests only if VBoxhi is Fail**
- **DieID programmation**
- **VBoxLo tests**
- **VSpeed Tests**
- **Special Cells tests**
- **RAM integrity test**
- **RAM retention test**
- **IDDQ Post-Stress measures**
- **Vddmin searches**
- **PWR-Short tests**
- **End flow.**

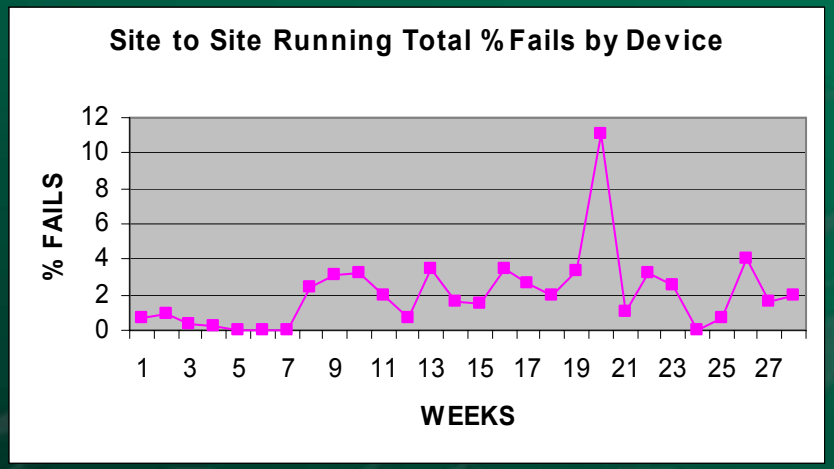
Issues

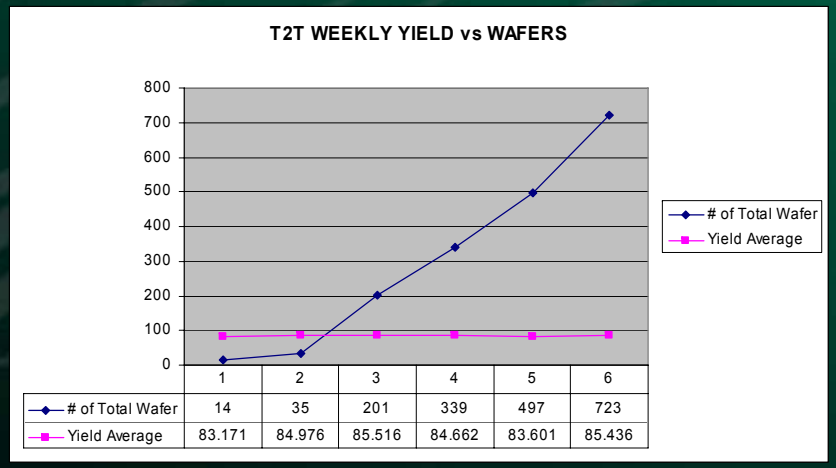
1. Yield Analysis (% variability)
    A. Tester to tester
    B. Site to site.

2. Failure modes
    A. Functional Pattern Response Fails from test
        A. VBoxL
        B. VBoxH

Yield Analysis S2S vs. T2T

- Yield Variability
  - Site to site monitoring of this device indicate an increasing yield delta between sites. Average 2.95 %
  - Tester to tester yield performance data did not identify isolated tester issues but did support site to site failure mode

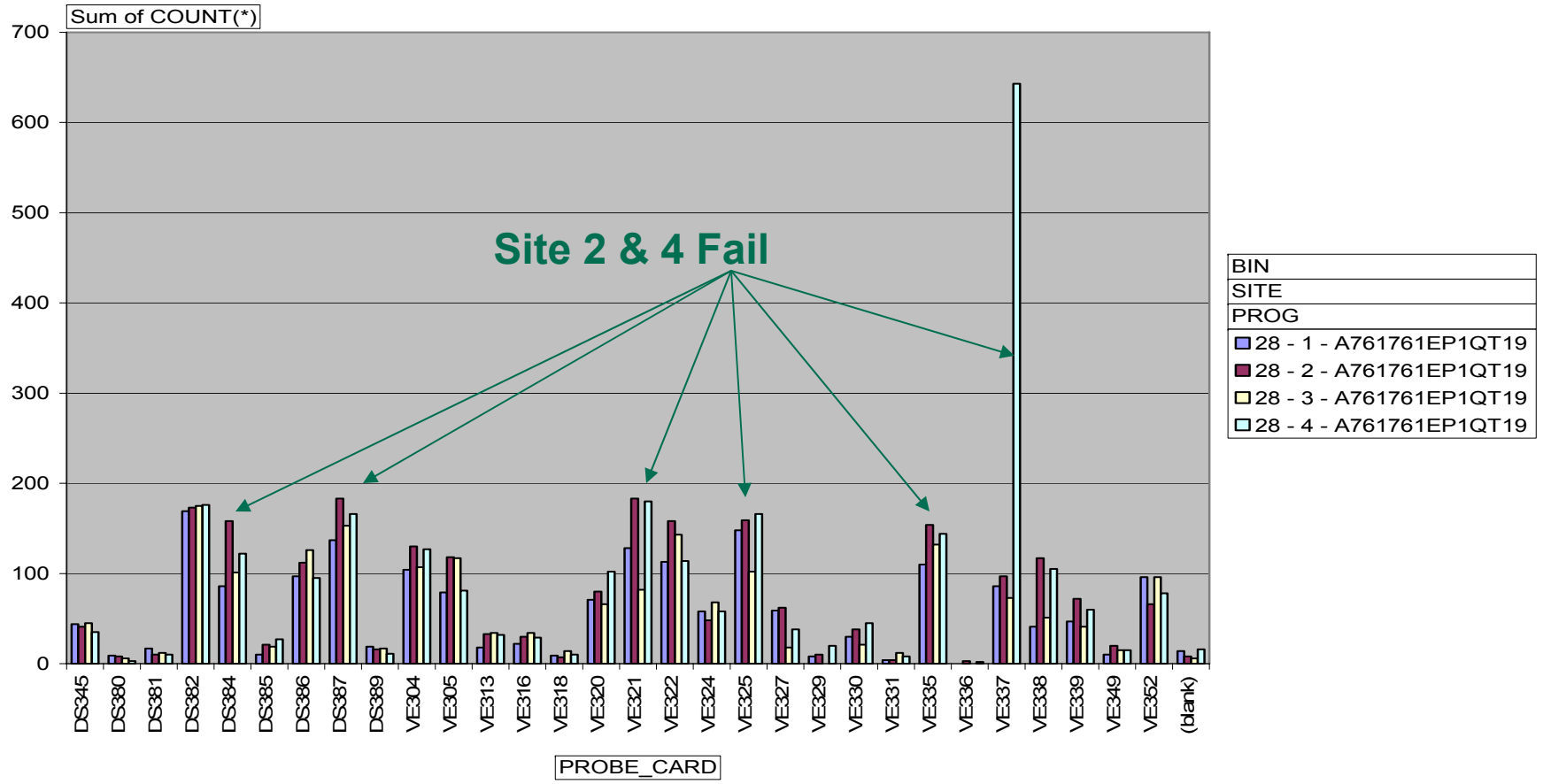




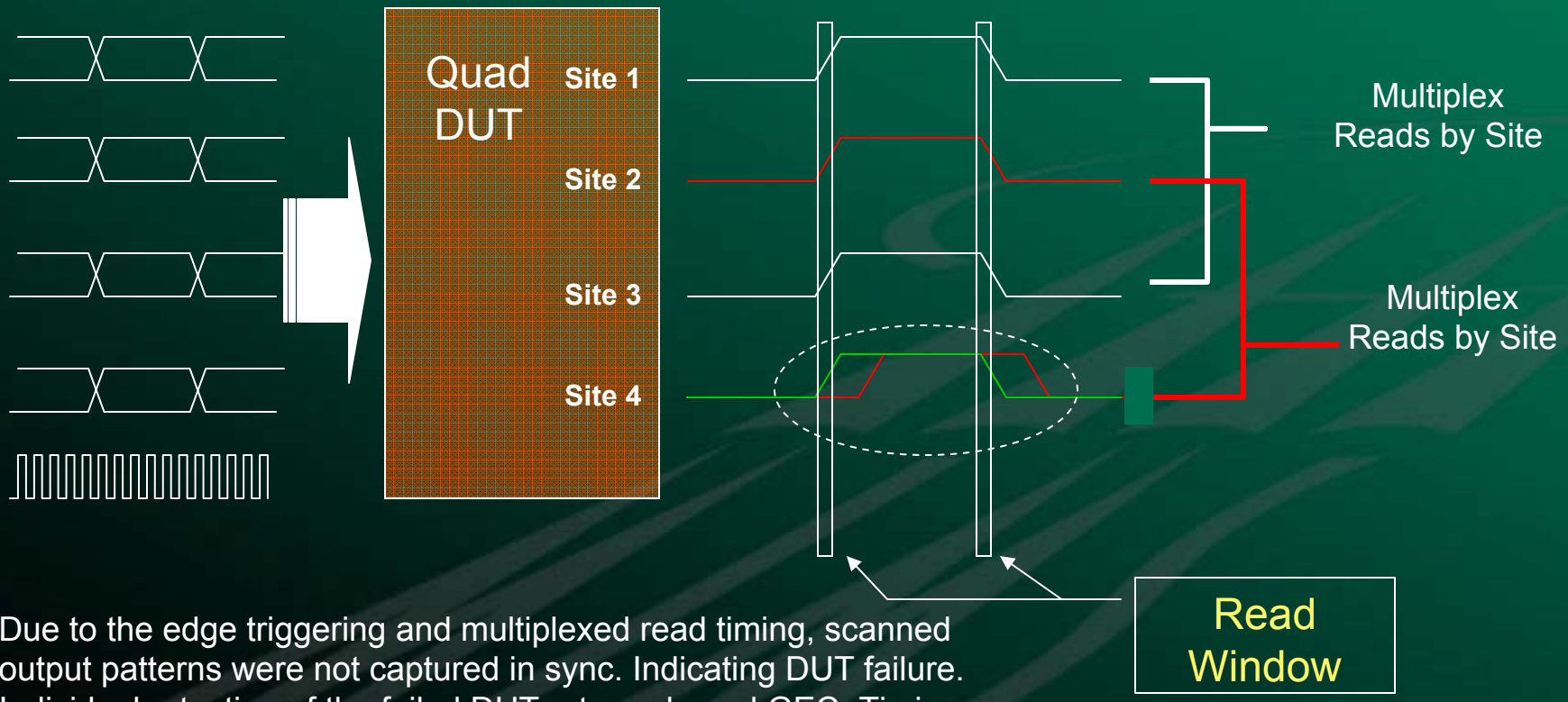
	1	2	3	4	5	6
# of Total Wafer	14	35	201	339	497	723
Yield Average	83.171	84.976	85.516	84.662	83.601	85.436

S2S Yield Analysis

By Probe card

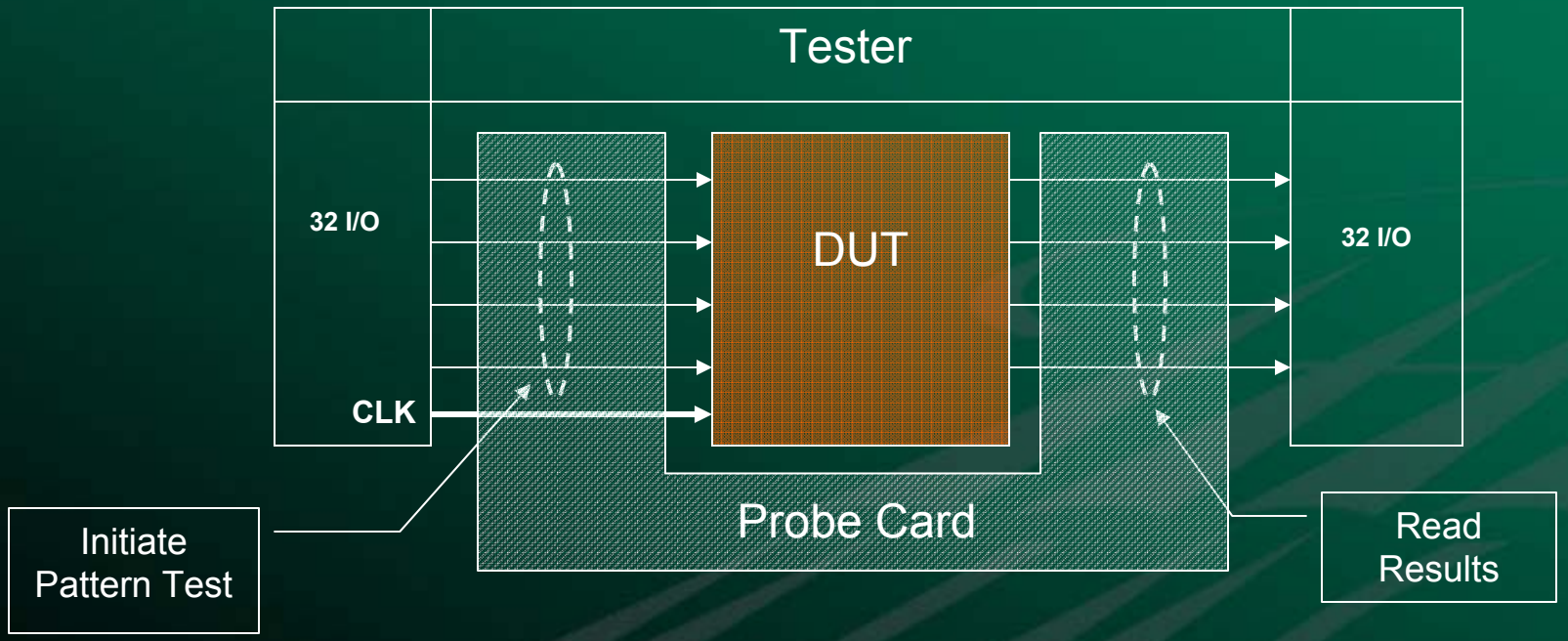


Signal Timing Issue



Due to the edge triggering and multiplexed read timing, scanned output patterns were not captured in sync. Indicating DUT failure. Individual retesting of the failed DUT returned good GEC. Timing adjustment in program resulted in adjacent site function failures which also were recovered on reprobe. Suspect signal trace or timing issues between tester and DUT by site.

Determining Cause Relationship



Critical Signals	
KEYIN4_N	GPIO05
ETX_TCK	GPIO06
TDI	GPIO07
TDO	GPIO43
TCK	PDID03

TDR System
(Time Domain Reflectometery)

Measurement System

- Tektronix TDS8200 oscope
- 20GHz Sampling Module 80E04
- 20GHz Passive 50Ω Probe

Measurement Settings

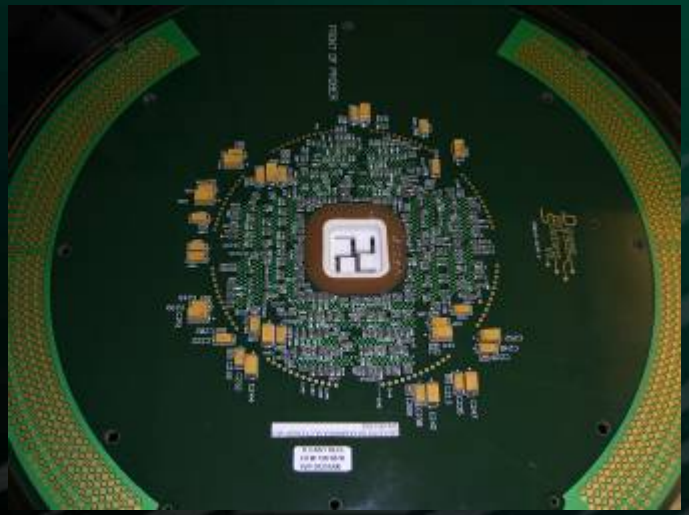
- **20Ω per Div/ Vert**
- **1ns per Div/Horz**

(Equivalent 2.54 cm or 1 inch)

Measurement Details

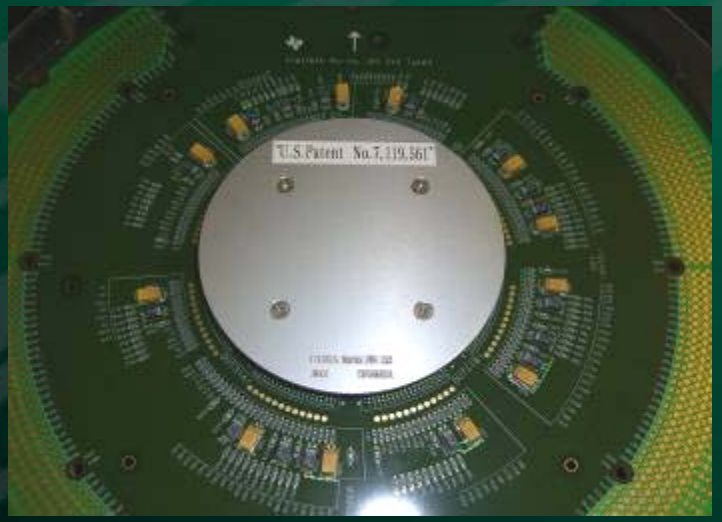
- The following slides are screen captures of comparison TDR measure between probe cards. PC 1 standard build and component lay out, PC 2 build with consideration to maintain site to site trace uniformity.

PC #1

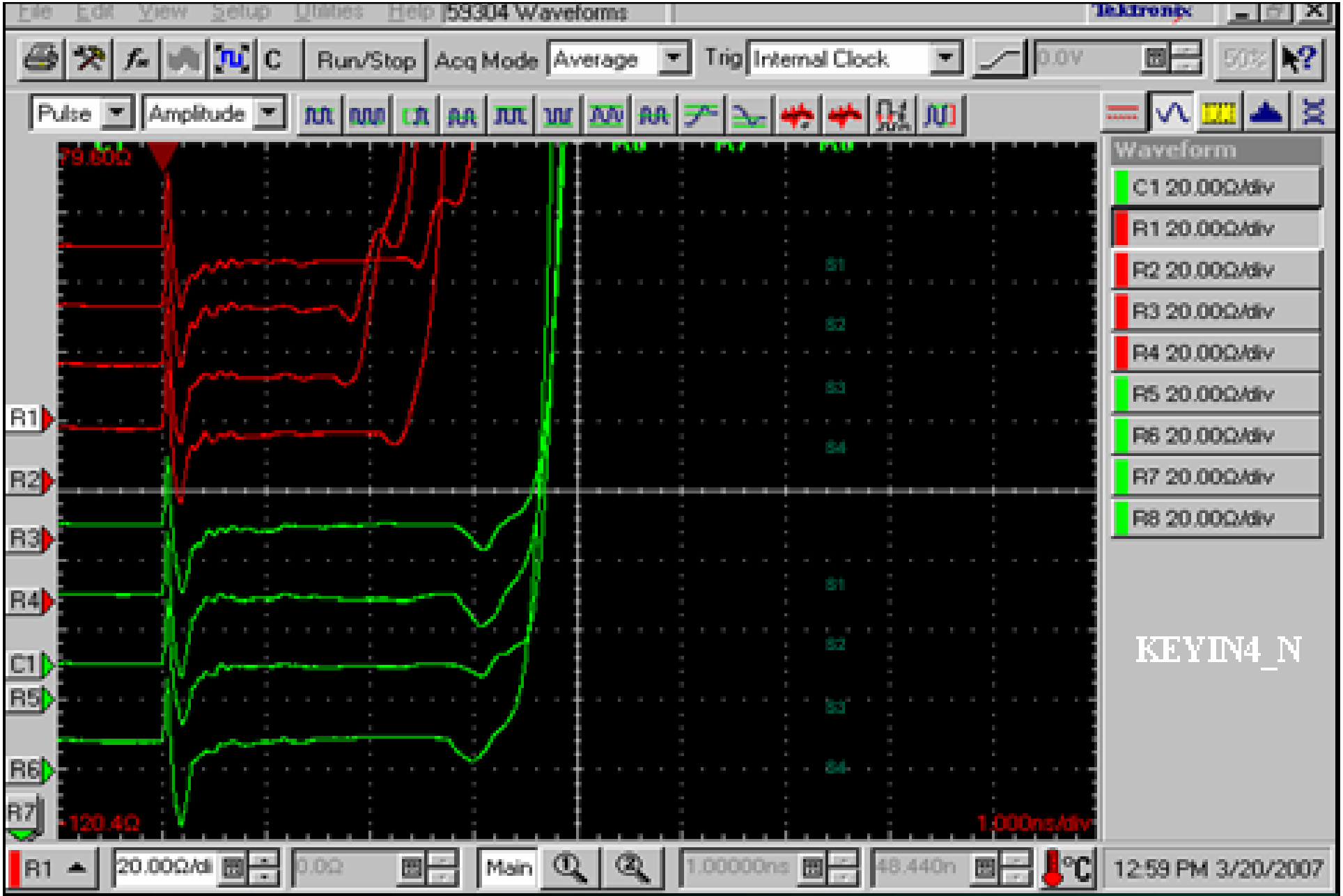


Probe card wo/ Site Matching Considerations

PC #2



Probe card w/ Site Trace Length and Component Layout Matching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R8 20.00Ω/div
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KEYIN4_N
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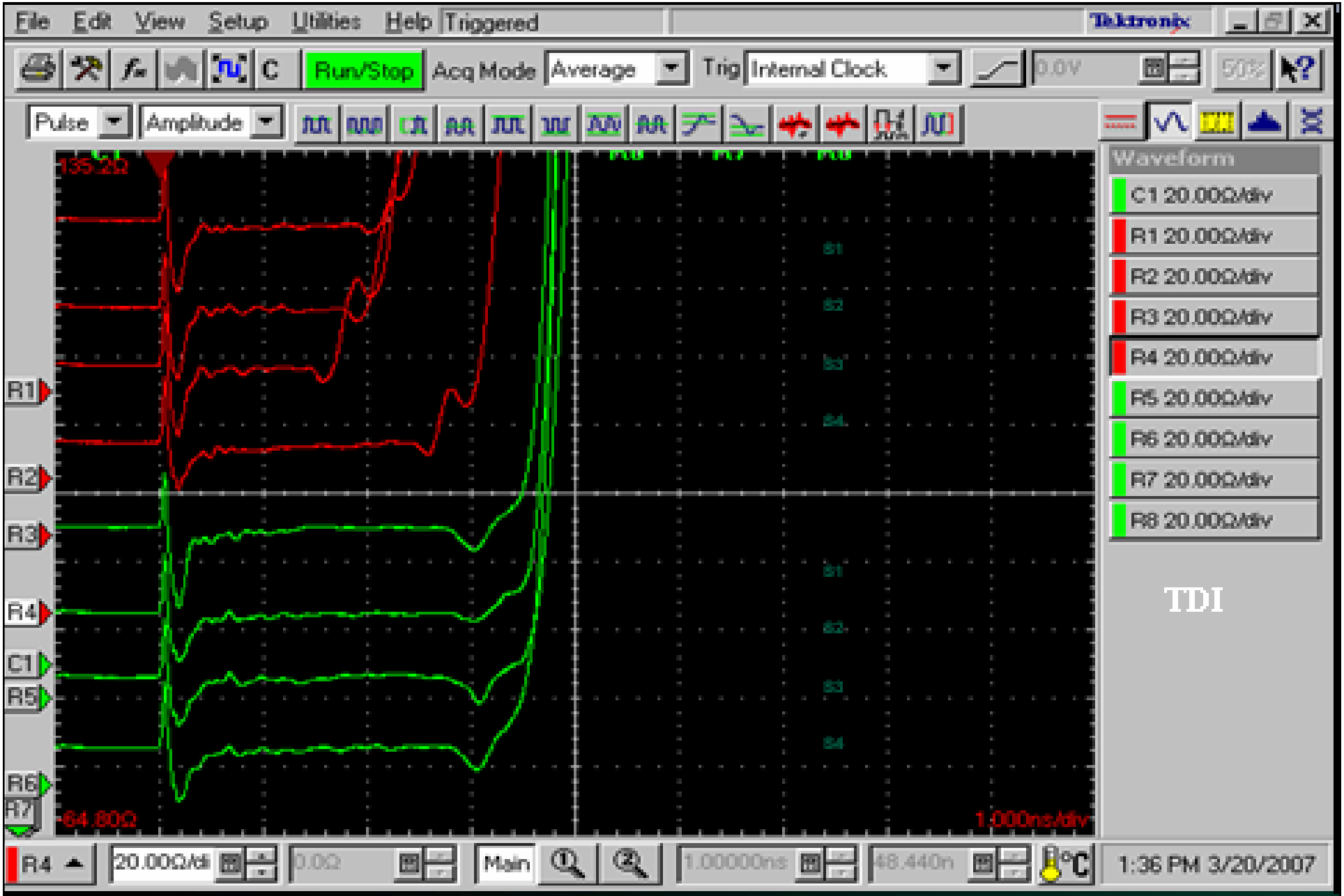
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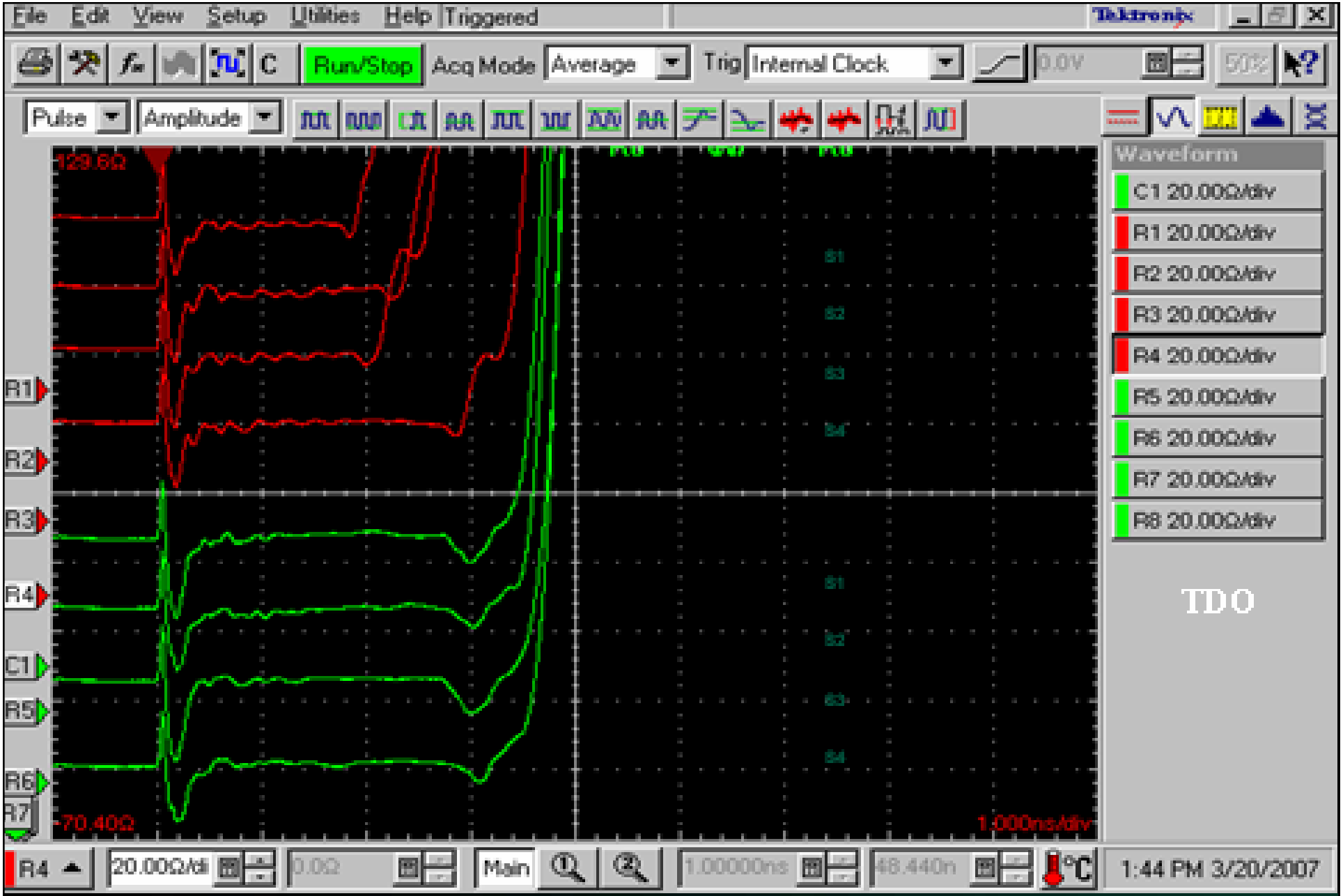
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GPIO05
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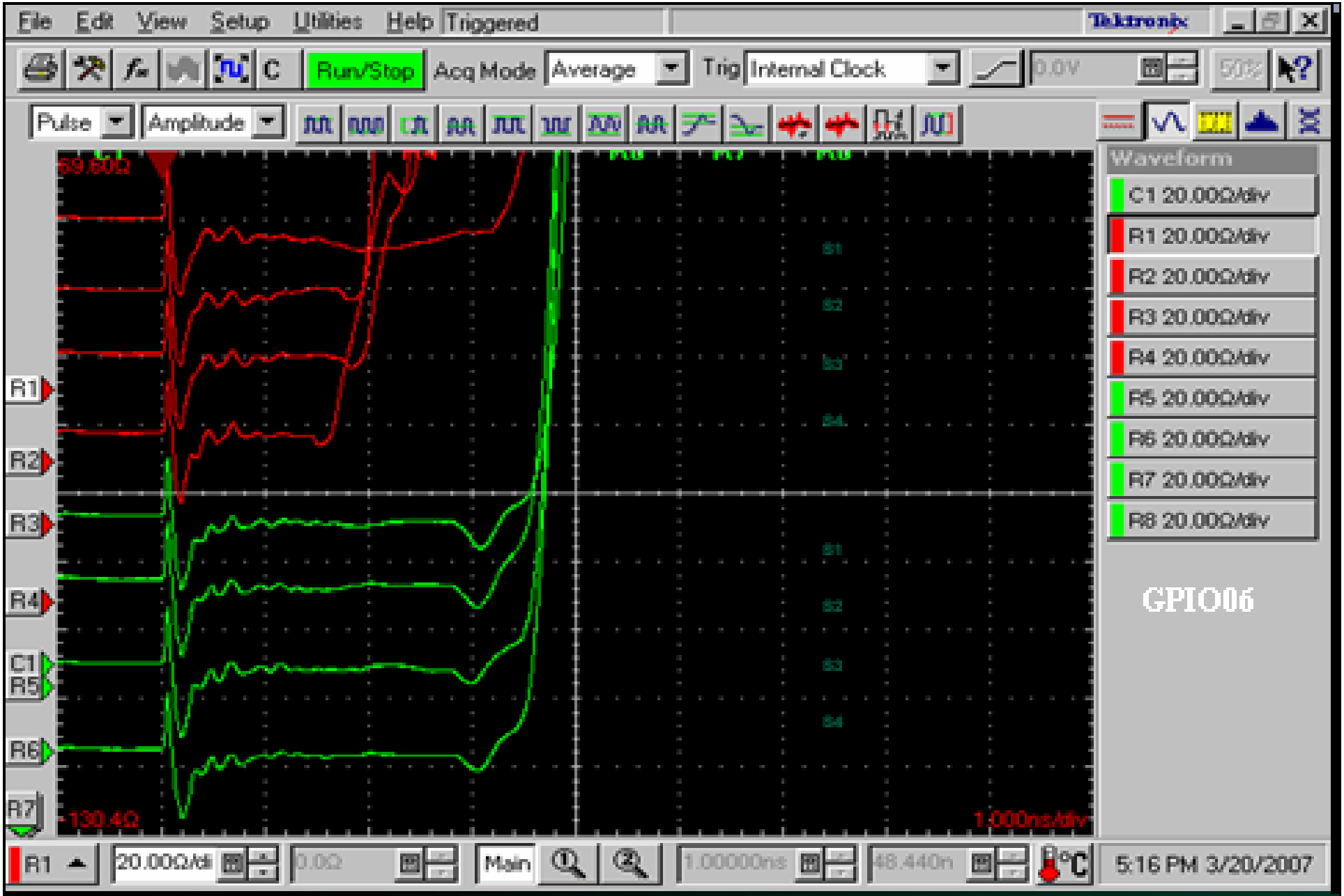
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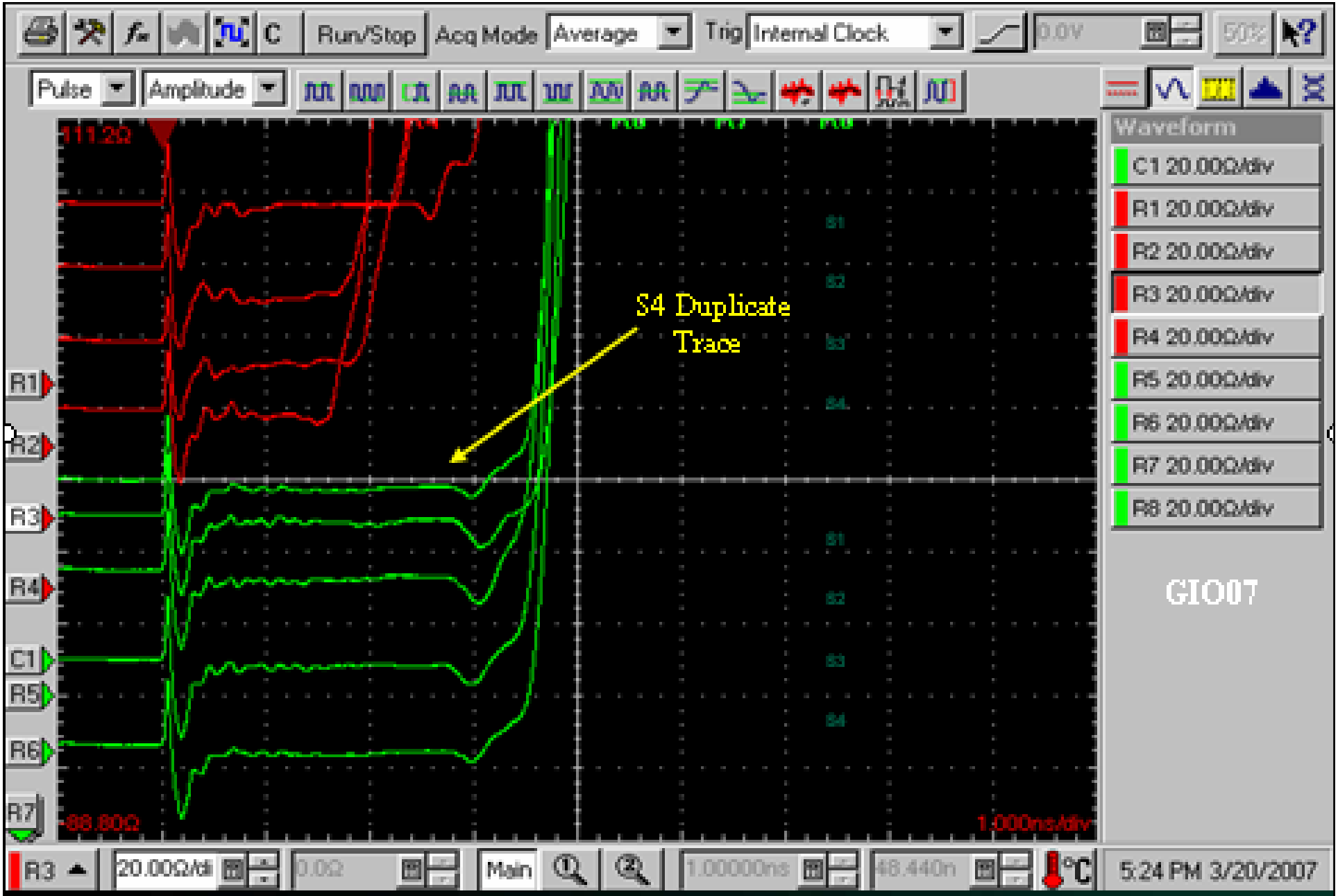
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R5 20.00Ω/div
R6 20.00Ω/div
R7 20.00Ω/div
R8 20.00Ω/div
GIO07
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Main
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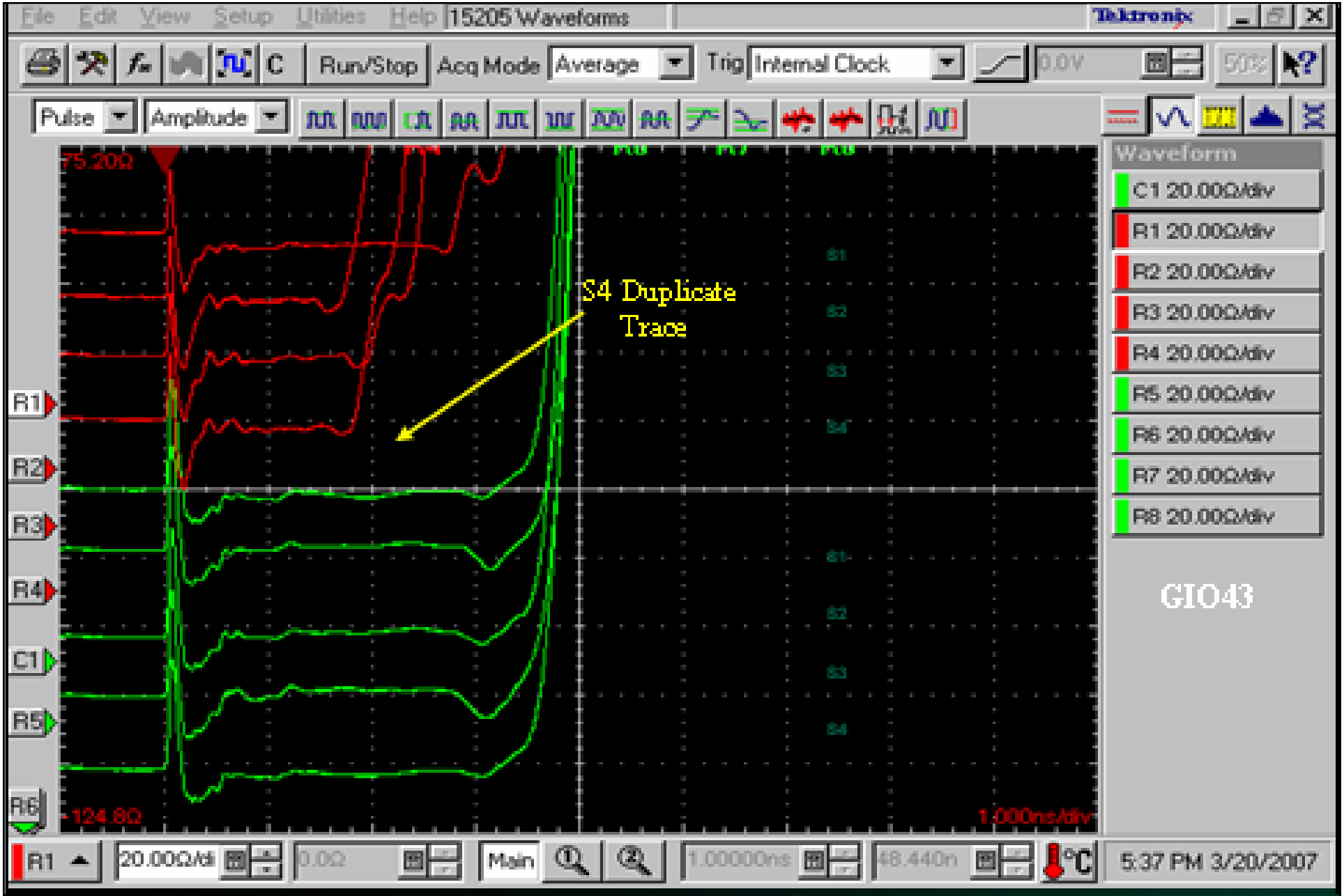
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R5 20.00Ω/div
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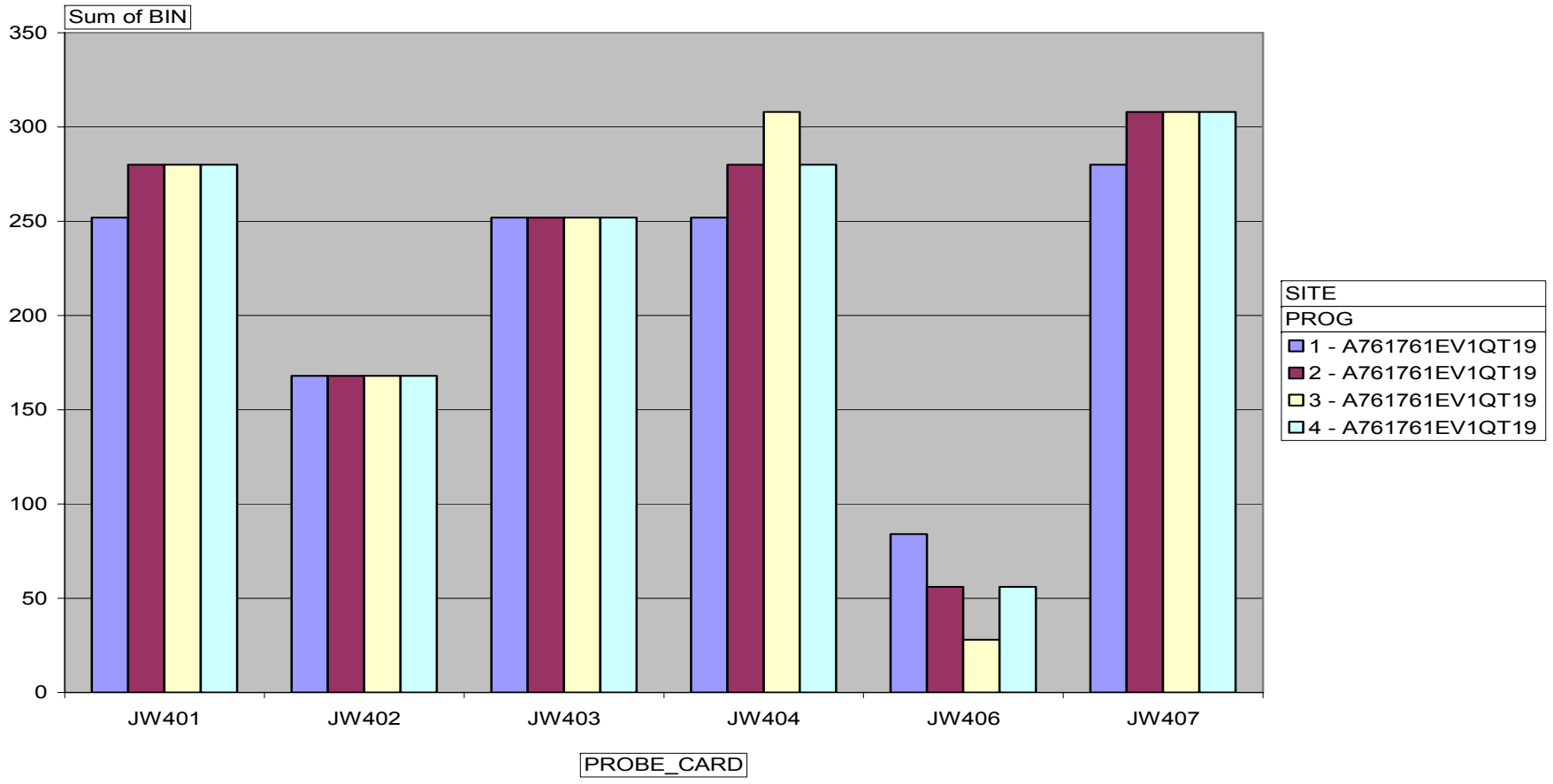
S2S Yield Analysis

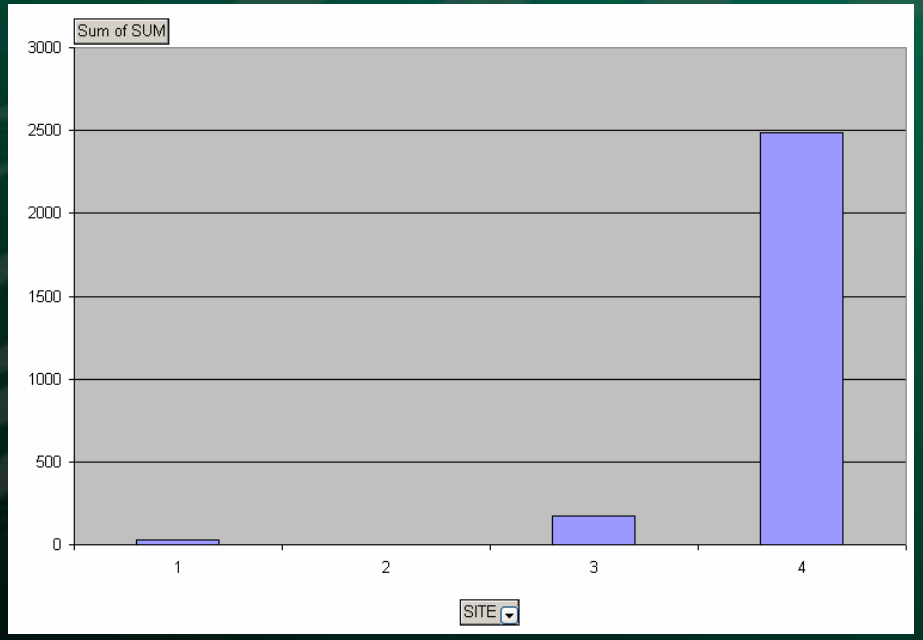
By Probe card W/ site match trace length (PC#2)



Device B

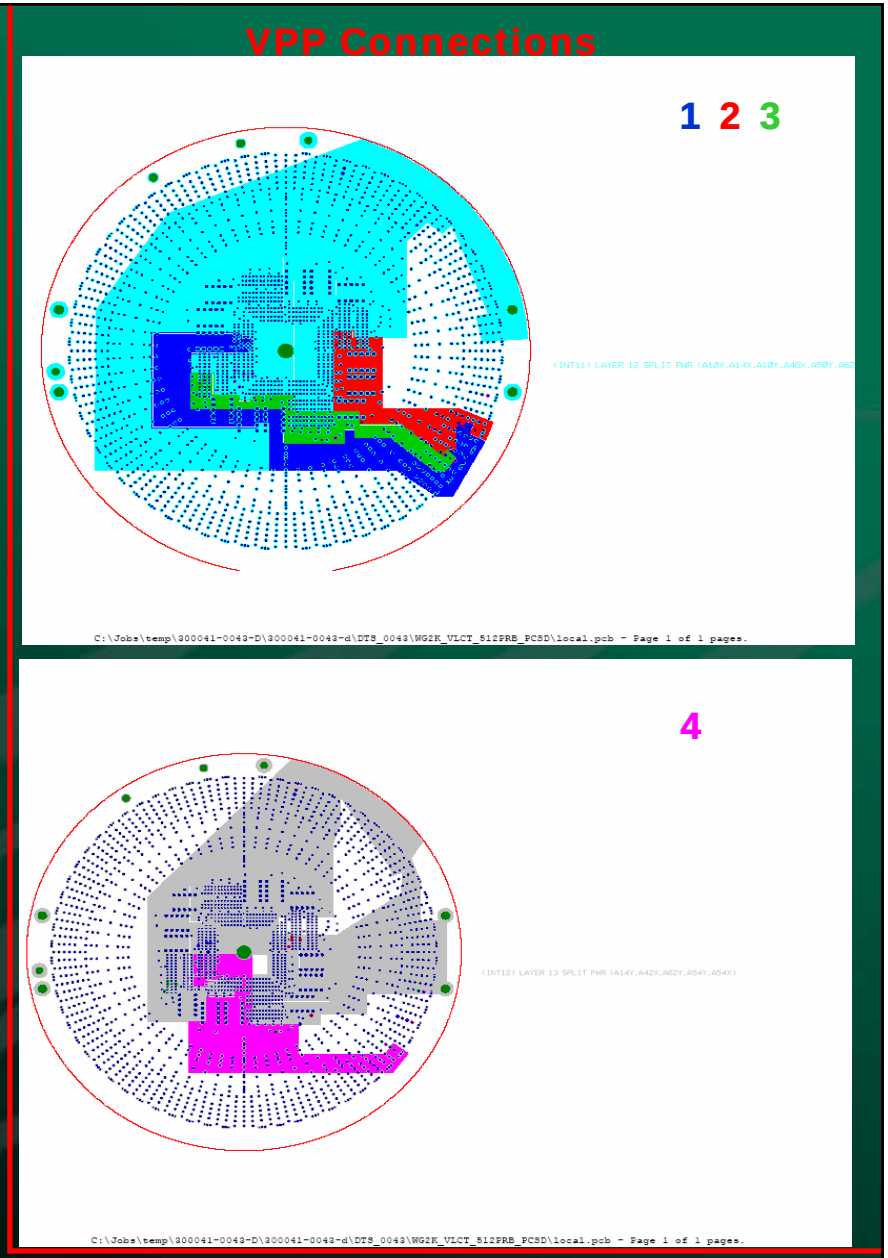
- Probe parameters
  - Tester platform – VLCLT UF 3000
  - Probe Card – Cantilever
  - Quad Site
  - Probe Points – 592
    - 148 points per site
- Issue:
  - Fuse Farm accumulators value and Fuse blown shows different blowing performances across sites
  - Site#4 needs more iterations to blow correct eFuse chain than the other sites

- Critical signal traces:
  - VPP Power
  - VPP Sense

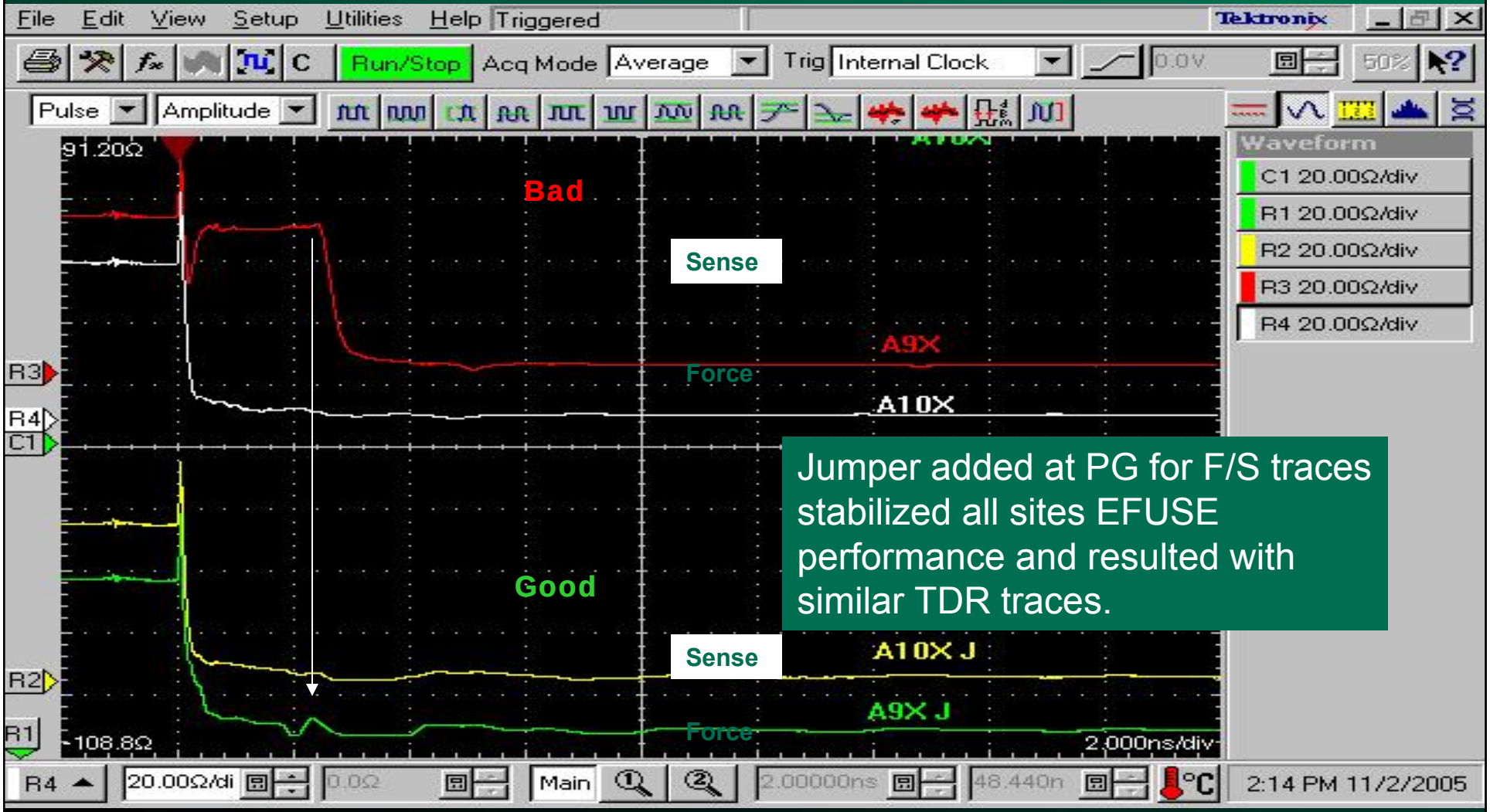


PCB Lay Out

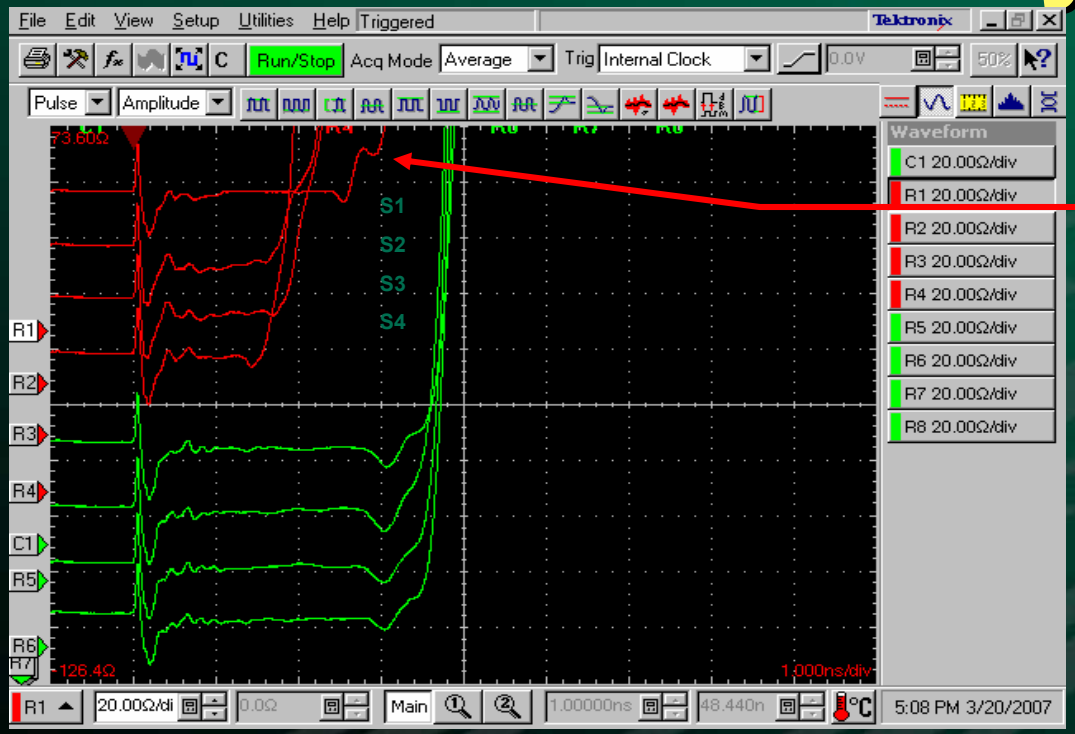
- Suspect contact issue at contact pads or traces resistance and length (capacitive coupling) causing reduced current on fuse blow pulse.
- TDR trace comparisons of both VPP Power and Sense indicated an additional length between sense and power trace different than sites 1 thru 3.
- Fuse blow test performed after adding a jumper between the force and sense traces eliminated issue.

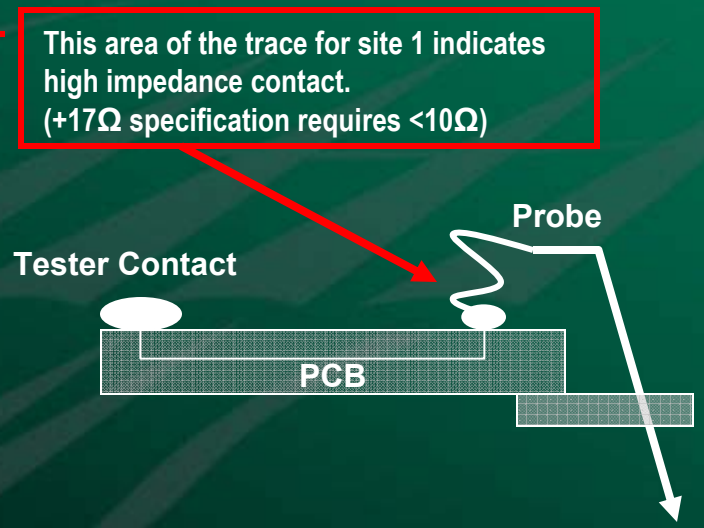


TDR Analysis



Additional Information from TDR Analysis





Further examination of the TDR trace can identify contact issues by indicating impedance measurement changes. In this case, poor probe wire contact to the PCB is indicated.

Summary

As the industry moves toward increasing multisite probing at increased speeds along with post pattern analysis and multiplexed I/O's, additional consideration must be given to insure signal quality not only between tester and DUT but between site to site and DUT.

In order to facilitate implementing improvements in this area, we suggest changing the Test program / Probe card / and Tester – design flow by implementing the following steps:

1. Original designer of the test program and probe card identify critical signal paths. Establish delta length limits as guides for signal types.
2. Probe card vendors implement TDR analysis as part of the standard probe card post build analysis. Trace information as well as analyzer data given as part of standard build specifications. If site / component complexity cause too high delta, the vendor should discuss the issue with the original designer to see if program adjustment can off set the issue.
3. Execute automated TDR analysis on repaired probe cards to eliminate high resistance issues as a result of all repair procedures.

Thanks For Listening

Questions?

Contact a-wegleitner@ti.com