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Semiconductor Wafer Test Workshop

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Vertical Probe Alternative for Cantilever Pad Probing

ANALOG DEVICES
Wentworth Laboratories

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Introduction

This presentation summarizes Analog Devices, Inc.'s evaluation and testing results using an alternative vertical probe card with pointed probes for testing ADI' s mixed signal, multi dut applications on bond pads.

This evaluation is intended to investigate vertical probe card technology as an alternative to traditional cantilever cards used by ADI. The potential benefits of smaller scrub marks, higher frequency, longer card life, easy in house maintenance and potential over-all value when compared to either cantilever or higher cost membrane cards which ADI's uses for higher frequency applications.

Overview

- Analog Devices Inc. testing needs
- Project Objective
- Benefits
- Testing Plan
- Results
- Probe design making this possible
- Next Steps

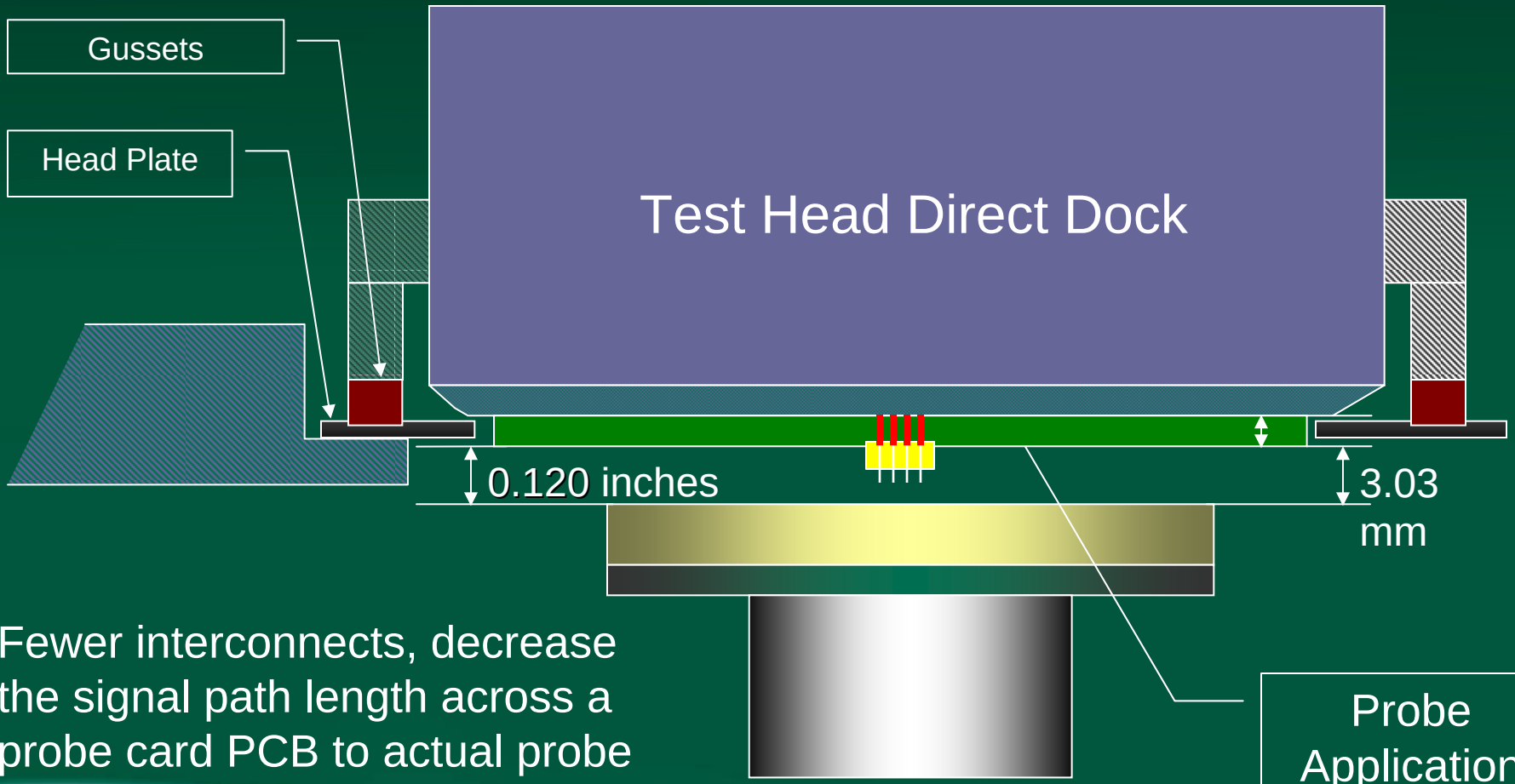
Analog Devices, Inc.
Test Needs

- High performance linear & mixed signal testing
- Lowest cost per touchdown for vertical design
- Low inductance paths for high frequency signals
- Higher frequency than cantilever can provide
- Provide the technical and production test benefits of vertical at a cost closer to cantilever
- Minimize scrub marks for automotive products

Project Objective

- Develop a lower cost vertical probe card capability for lower volume but high performance analog components.
- Develop this vertical probe capability to work on standard bond pad spacing and later for redistributed bump die
- Maintain a price structure which is a cost effective alternative to membrane probe

Design Objective



Fewer interconnects, decrease the signal path length across a probe card PCB to actual probe needle connection.

Vertical Probe Benefits

- Longer touchdown life between rebuilds
- Higher test frequency capability
- Ability to repair in-house
- Reduced scrub mark size with pointed probe, vs. cantilever scrub
- Use on low volume bump applications
  - Cost effective for ADI products

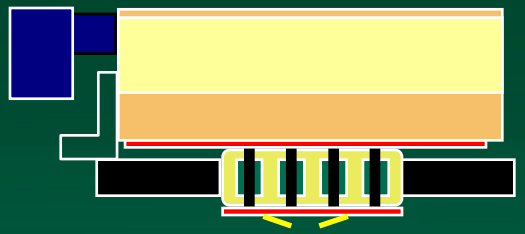
Initial Test Plan

- First design compared CRES on custom test chip designed for bump wafers
  - CRES Values compared to Cantilever
- Data was only used to validate the probe card design concept, early work had stuck pins but did function electrically as desired.

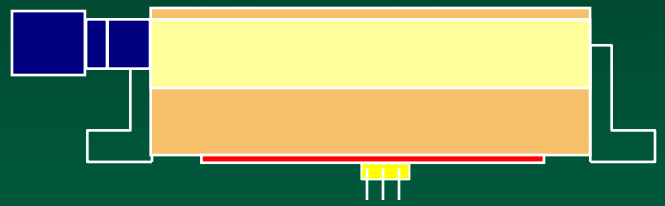
Test Plan

- Test a Power Management chip using both a cantilever ring and new vertical probe card with the same wafers and compare the probe yield and needle performance.
- Optimize the cleaning frequency as required
  - Started at once per wafer
  - later 3-4 times per wafer
  - settled for every 3,000 touchdowns
    - Forced Multi touchdown per DUT to accelerate wear & tear
    - Evaluate any degradation to the PCB and yields

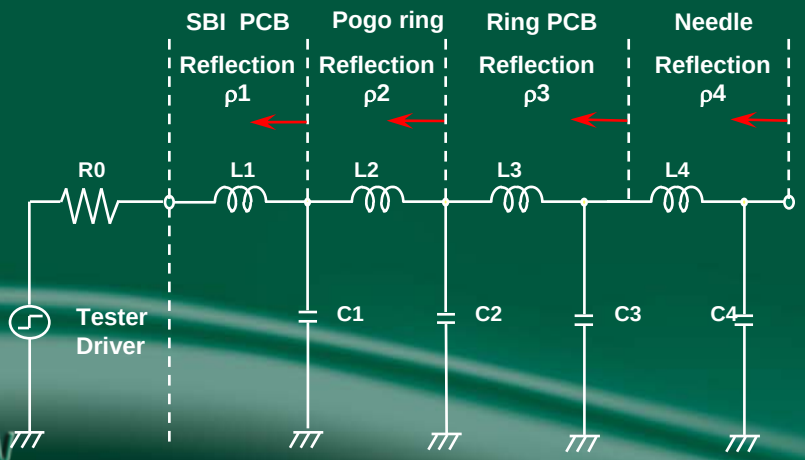
Value of Vertical Direct Docking

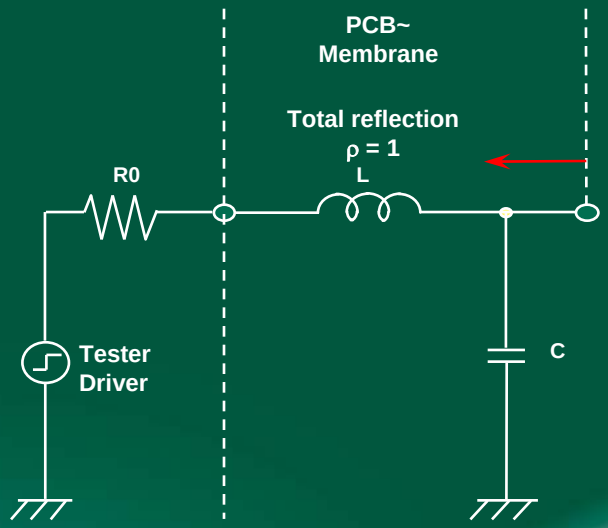


There are several blocks within this interface that can cause a high Z condition.
At each interface there can be a reflection which causes a distortion in DUT input signal. As a result, it can be inadequate for higher speed testing.



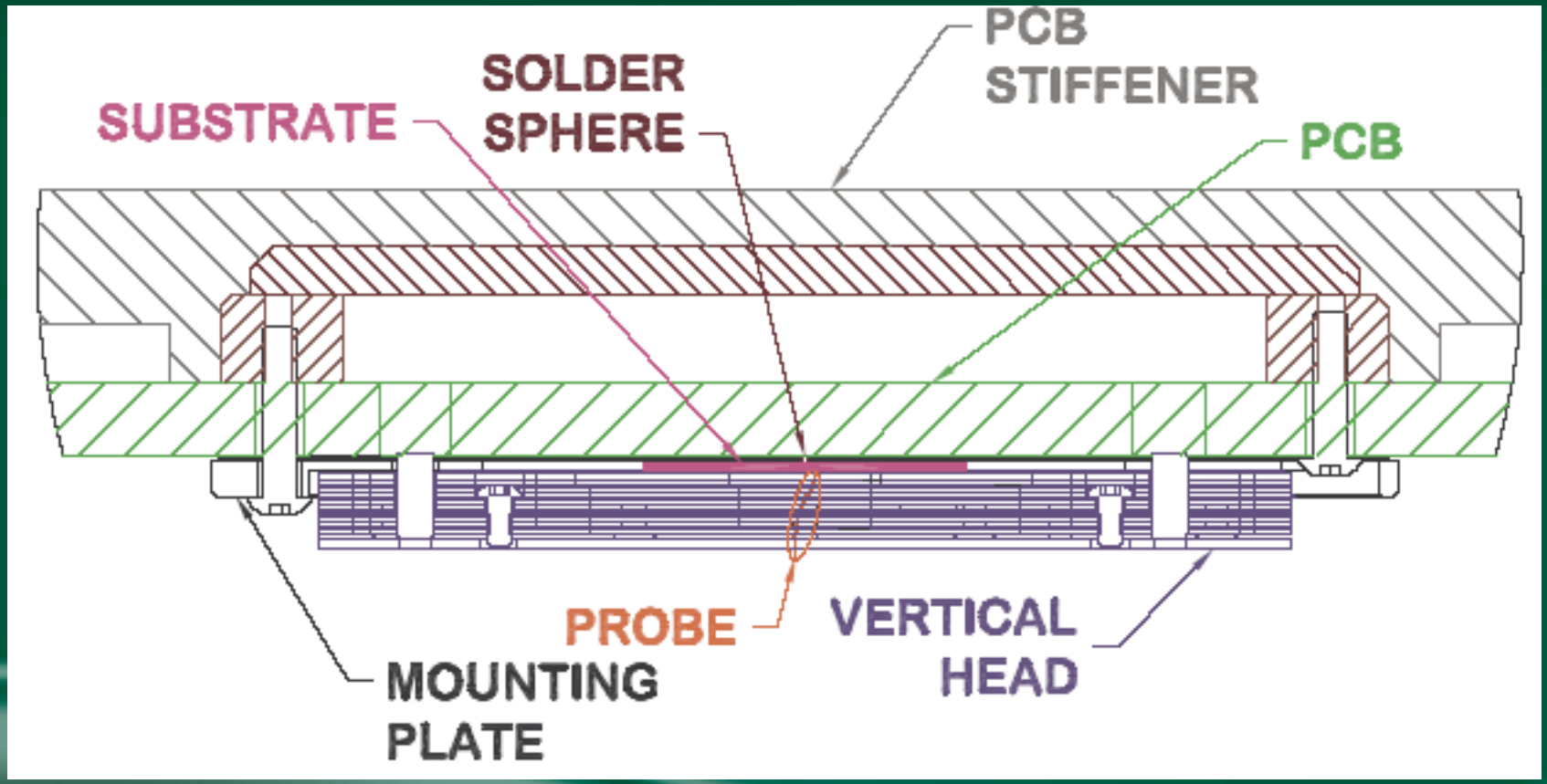
Less reflection with simple Impedance





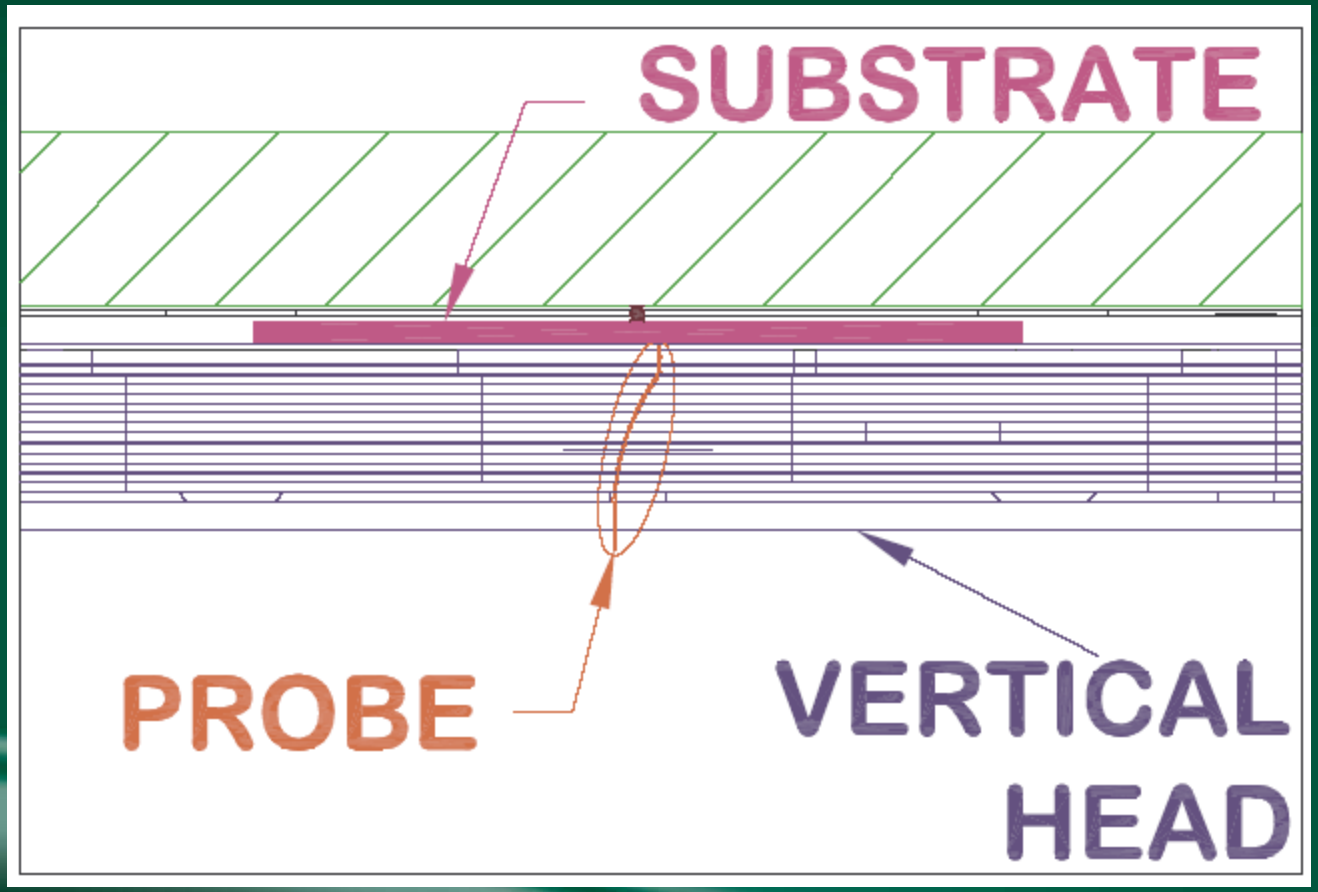
Comparison of Substrate vs Direct Dock Interface

Example: via Substrate Interface



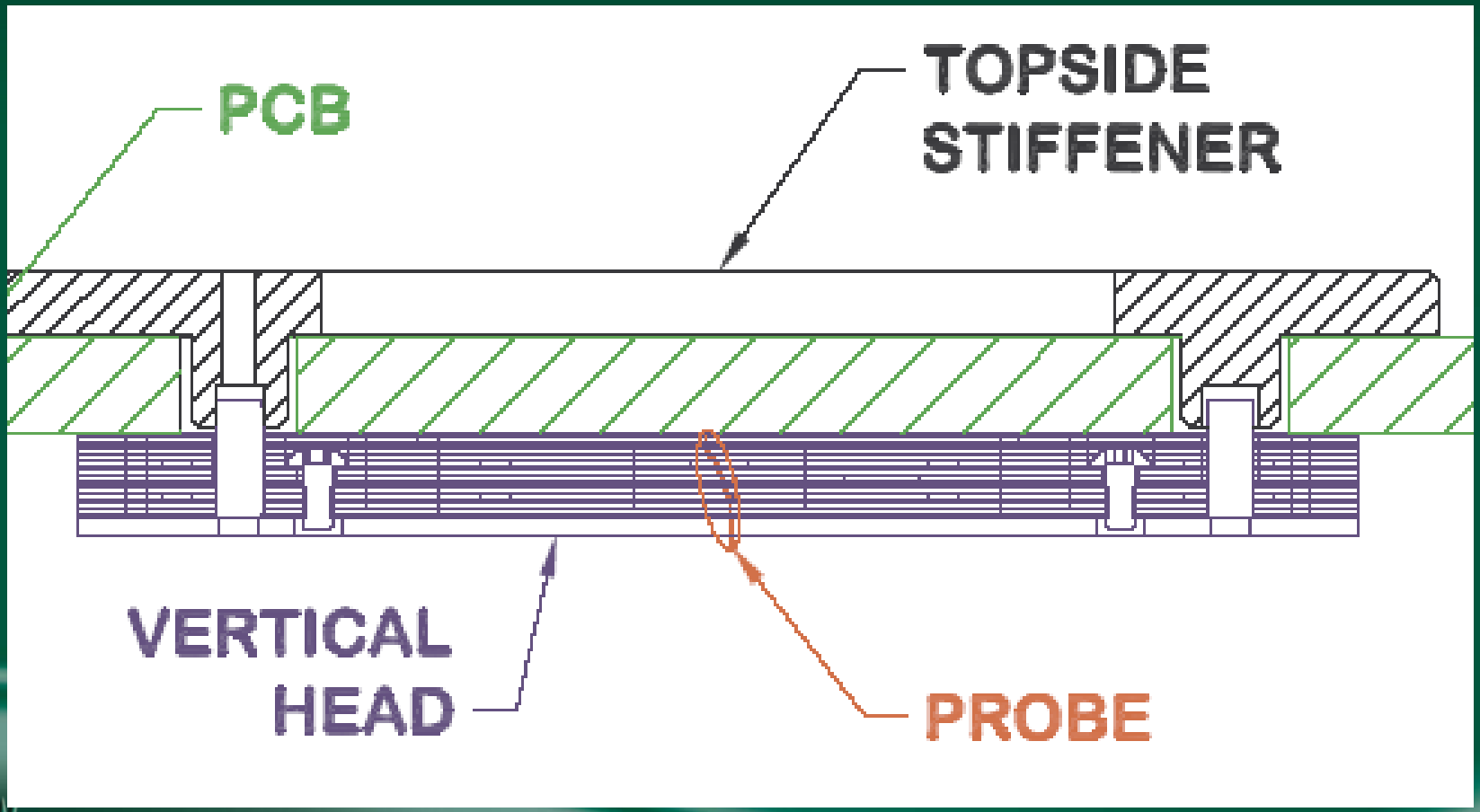
Comparison of Substrate vs Direct Dock Interface

Example : Substrate Interface



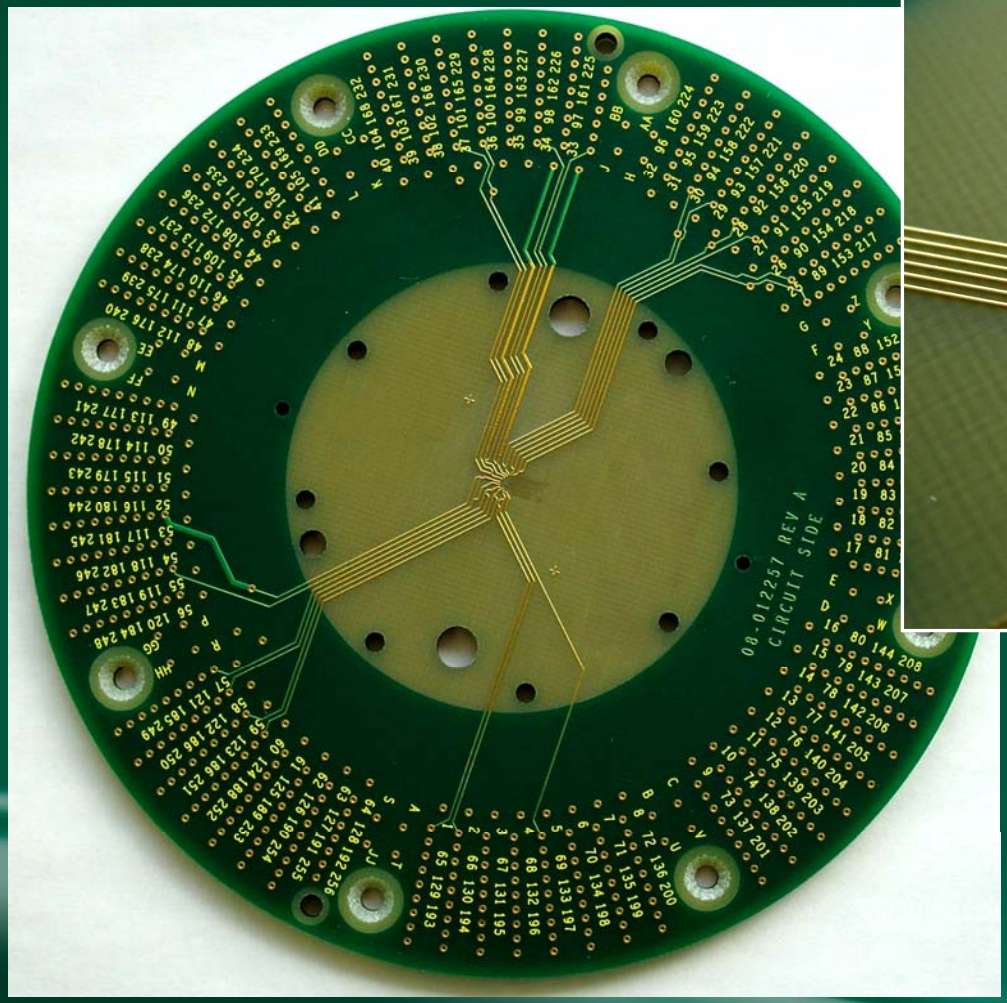
Comparison of Substrate vs Direct Dock Interface

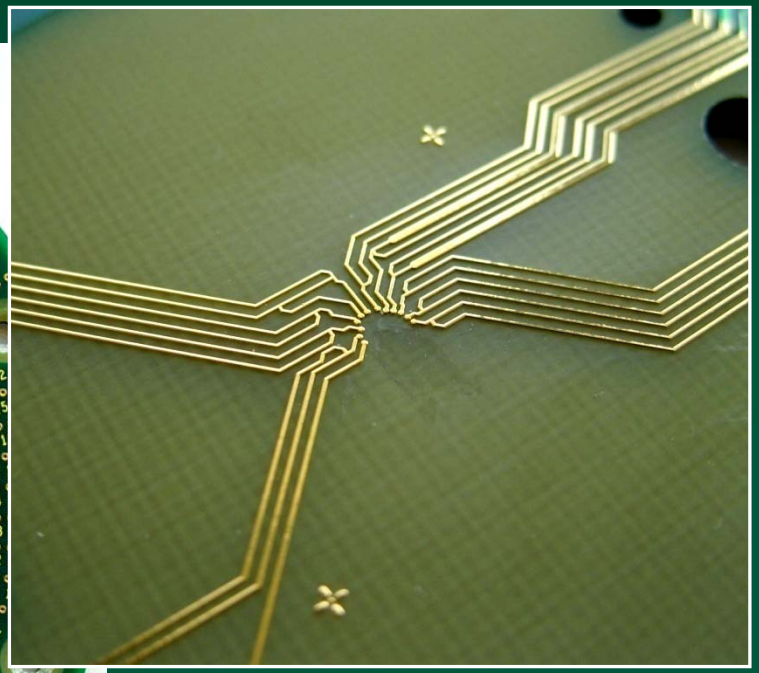
Example : Direct Dock



Direct Dock PCB

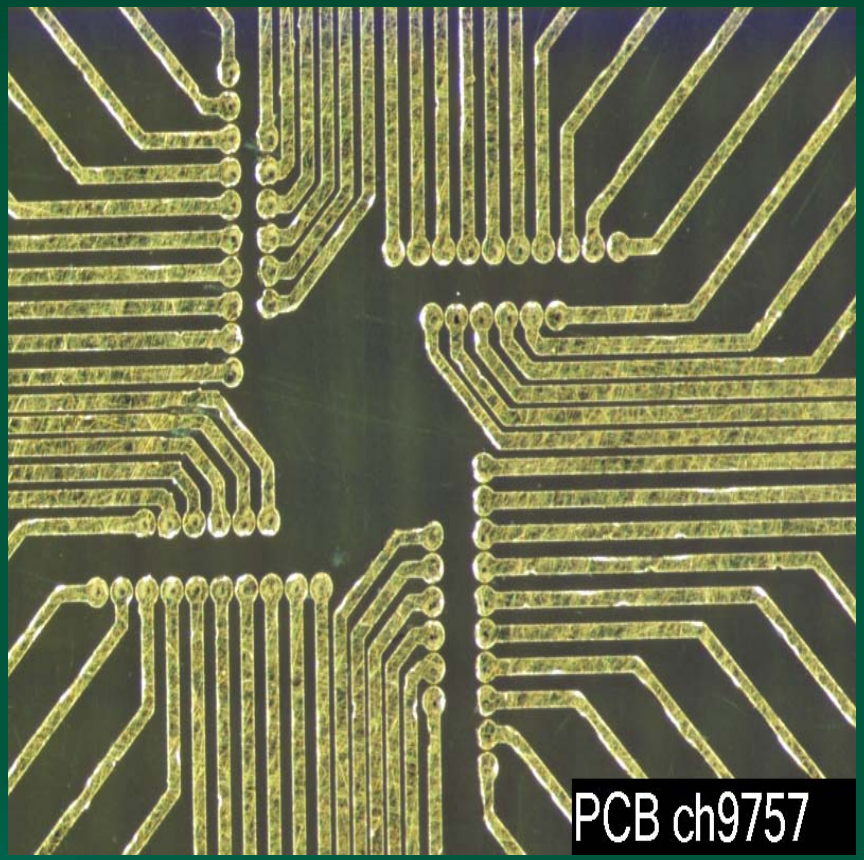
Gap between contacts= 66.6um



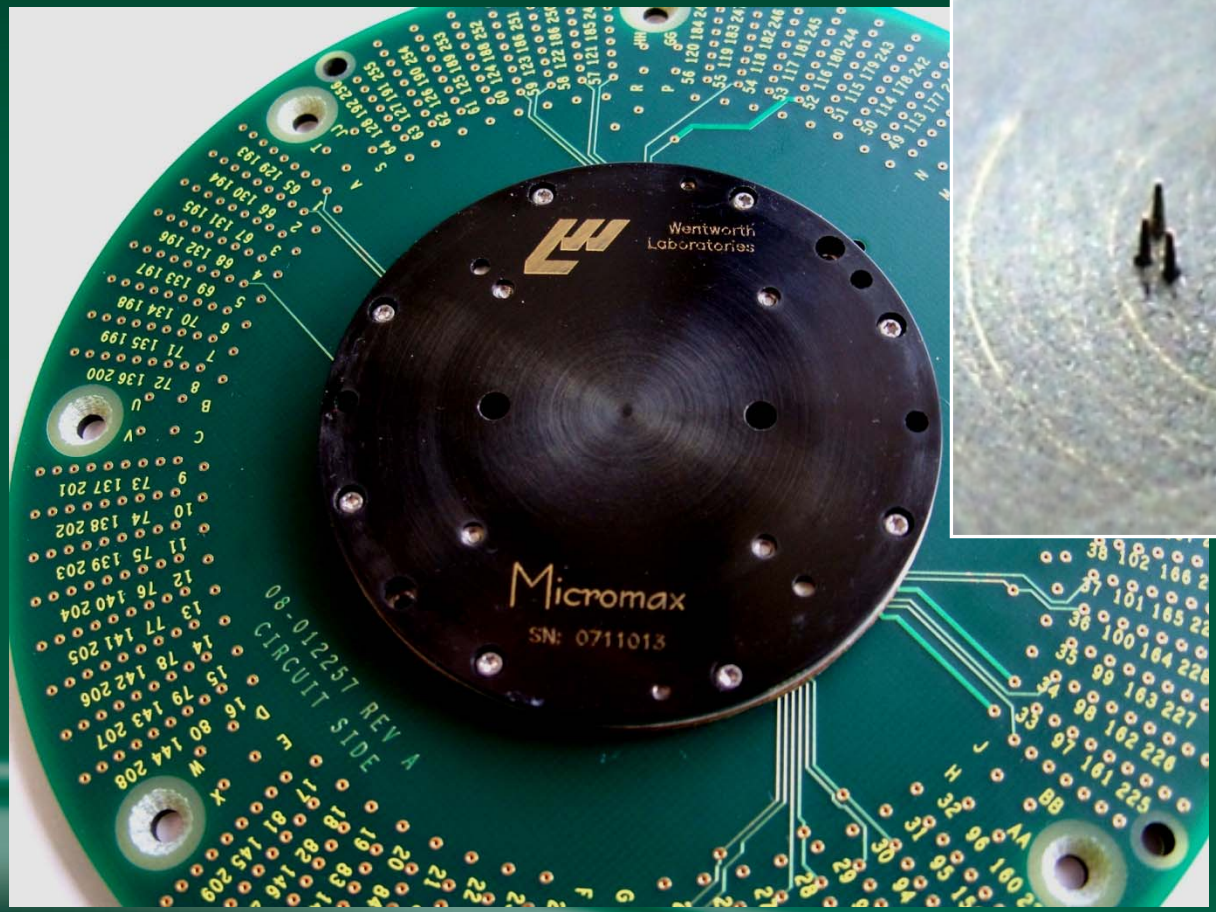


Direct Dock PCB Design

- Eliminates need for substrate (MLO, MLC)
  - Lower cost
  - No lead time for substrate fab
  - Analog in-house PCB design

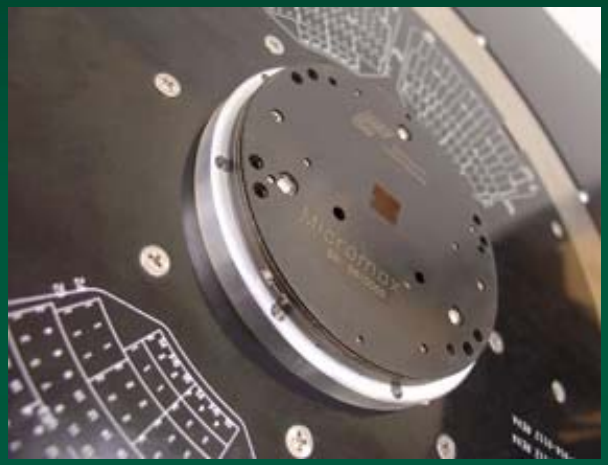


Analog Devices Probe Card

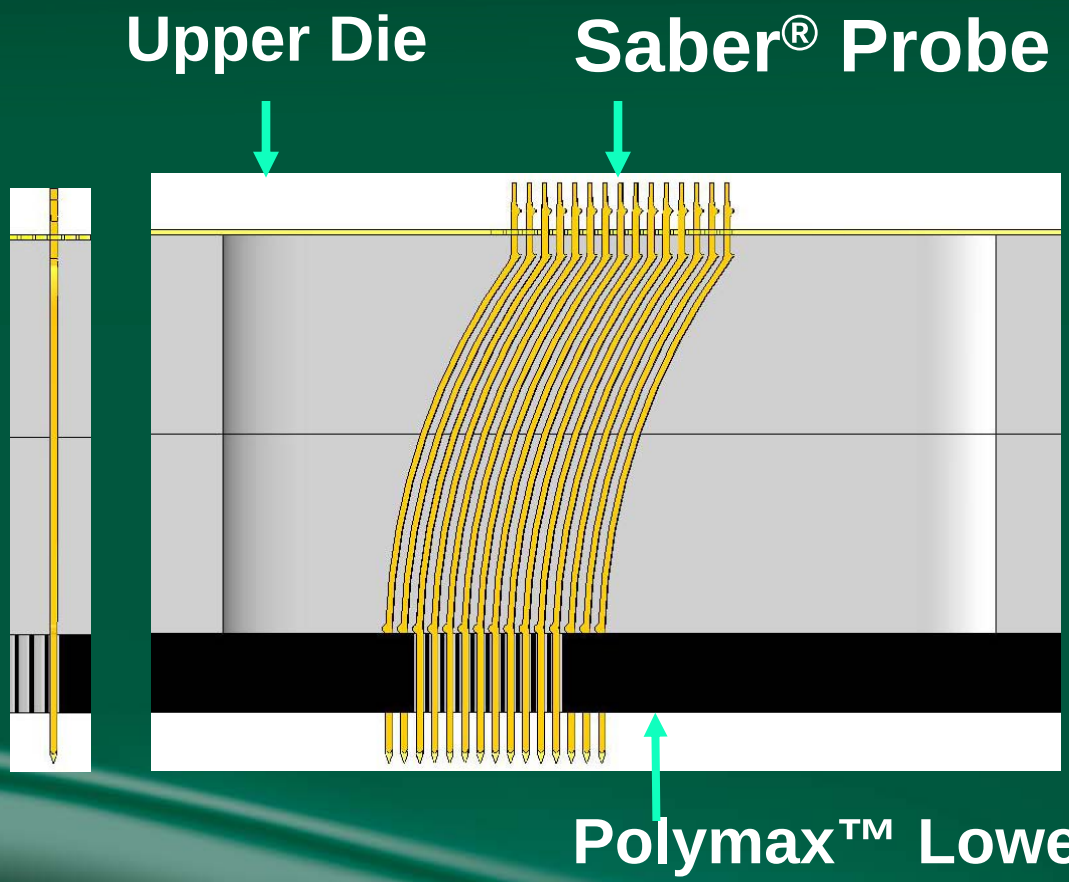


Vertical Direct Dock Probe Card

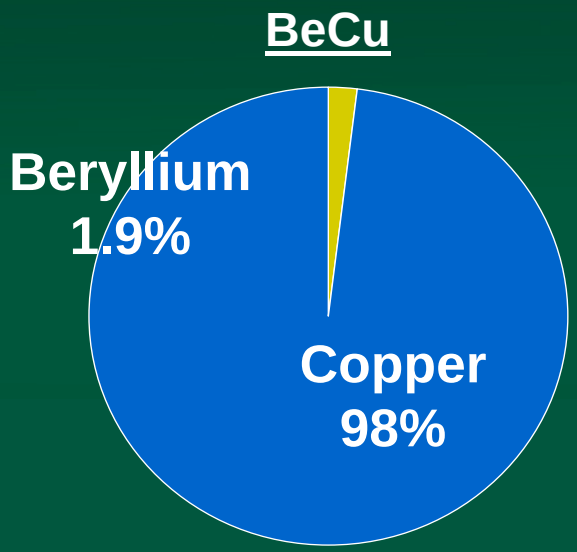
- Uses chemically etched pointed contacts to break through oxides
- Effective alternative to cantilever type probe cards:
  - Does not require planarization or alignment maintenance
  - Easier, faster onsite maintainability
  - Large arrays
  - Test more devices simultaneously
  - Multi-die applications: 1x4, 1x8, 2x2, 2x4
  - Lower cost alternative to low volume high performance



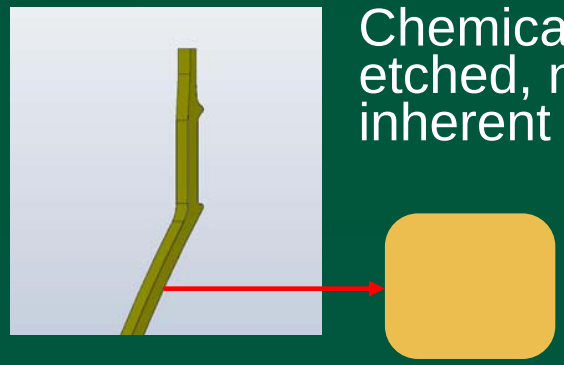
Cross Section of a Vertical Pointed Probe Head Design



BeCu Pointed Saber®Probe Properties



Pointed Probe



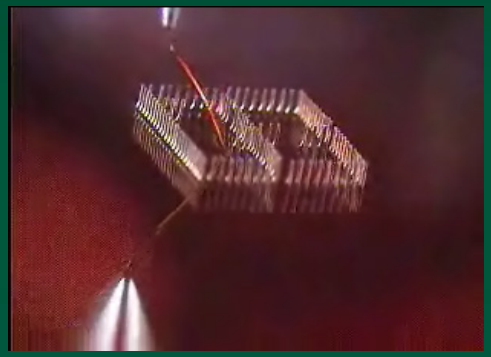
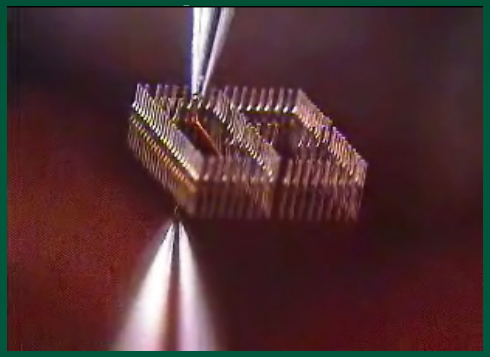
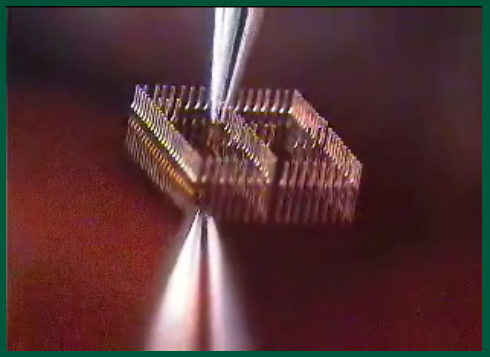
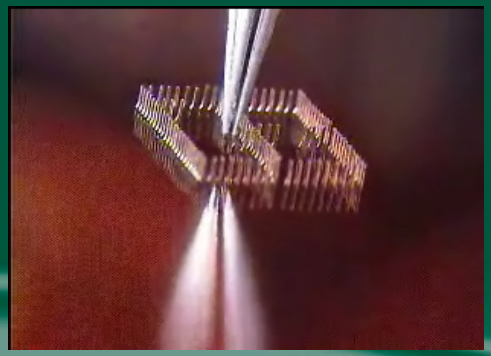
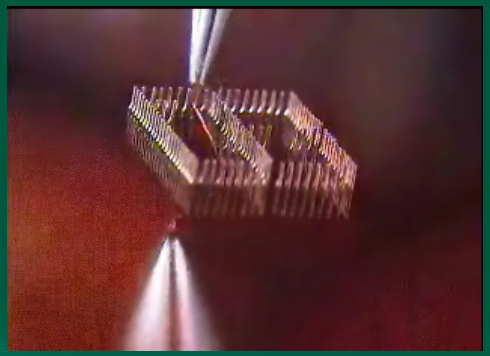
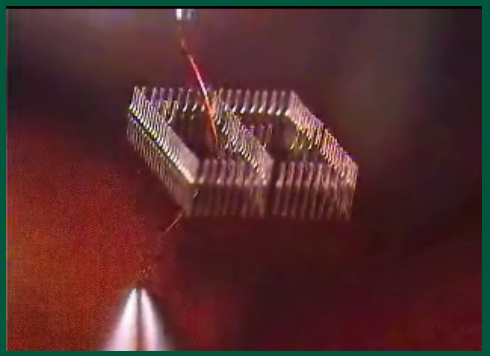
Chemically etched, no inherent stress

Huge cross section

- Current Capacity at 25^{0}C : 600 mA for 2 minutes
- Current Required to “Blow” : 1,300 mA
- Resistivity: 7.0 uohm–cm
- Conductivity @ 20^{0}C : .129 1Mohm–cm

Direct Dock Vertical Probe Maintenance Process

Insert contact thru upper die, lower die and push past

Removal: Grasp contact and pull contact out

Reduced Probe Marks

- Pointed probe design for lower CRES
- Pad sizes shrinking, thus smaller scrub marks are desirable
- Probe and re-probe on same pads are now possible with minimal damage

Results

COMPOSITE BIN SUMMARY 05/20/08 17:39:12

Selected Pass Numbers: 1

Pass:	501254	Machine ID:	plct18
Fail:	20172	Reference X:	24
Total:	521426	Reference Y:	23
Wafers:	62	Average Yield:	96.131%

OVERALL RE-TEST SUMMARY

Re-Tested	0
Recovered	0
Re-Test Rate	0.000%
Re-Test Recovery	0.000%

Testable Die:	537168	Not Tested Die:	92560
Normal:	486700	Skip Die:	0
Sample Test:	50468	Ink Only:	76818
Force Test:	0	No Touch:	0
		Untested:	15742
		Bin Assigned:	0

OVERALL BIN SUMMARY

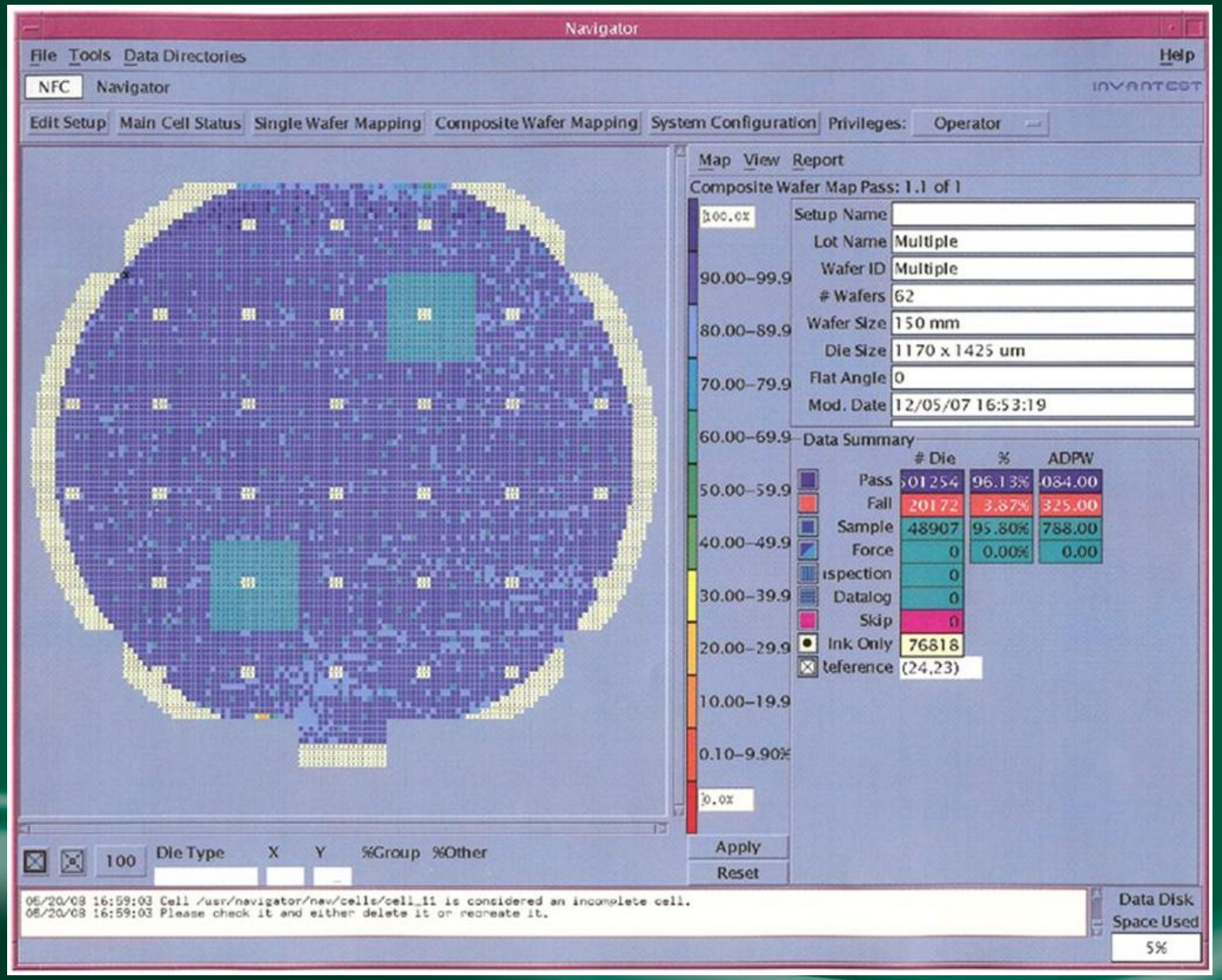
Bin	P/F	Total	Bin %	Sample	Force	Sample Assign
1	Pass	501254	96.131%	0	0	0
7	Fail	929	0.178%	0	0	0
8	Fail	687	0.132%	0	0	0
9	Fail	38	0.007%	0	0	0
10	Fail	1192	0.229%	0	0	0
11	Fail	63	0.012%	0	0	0
12	Fail	15485	2.970%	0	0	0
14	Fail	678	0.130%	0	0	0
16	Fail	1100	0.211%	0	0	0

BIN SUMMARY BY PASS

Pass 1.1 - TEST

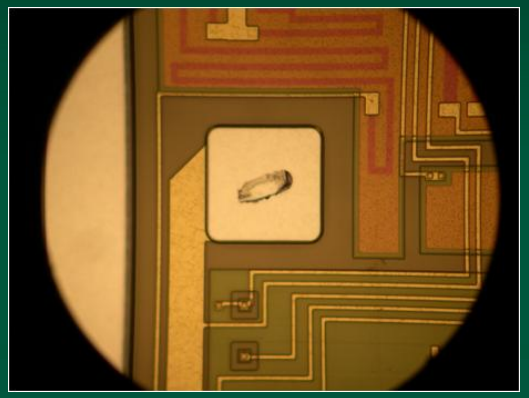
Bin	P/F	Total	Bin %
1	Pass	501254	96.131%
7	Fail	929	0.178%
8	Fail	687	0.132%
9	Fail	38	0.007%
10	Fail	1192	0.229%
11	Fail	63	0.012%
12	Fail	15485	2.970%
14	Fail	678	0.130%
16	Fail	1100	0.211%

Results

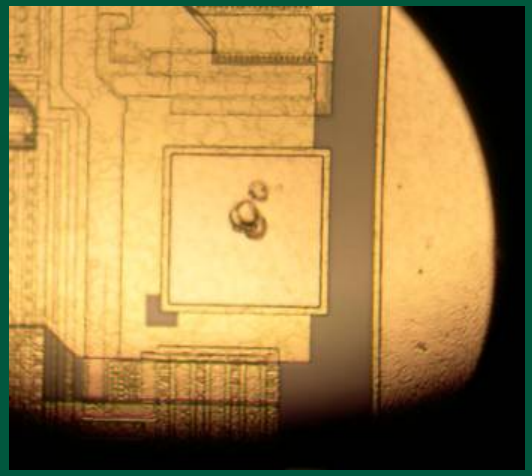

Navigator
File Tools Data Directories
Help
NFC Navigator
Edit Setup
Main Cell Status
Single Wafer Mapping
Composite Wafer Mapping
System Configuration
Privileges: Operator
Map View Report
Composite Wafer Map Pass: 1.1 of 1
100.0%
90.00–99.9
80.00–89.9
70.00–79.9
60.00–69.9
50.00–59.9
40.00–49.9
30.00–39.9
20.00–29.9
10.00–19.9
0.10–9.90%
0.0%
Setup Name
Lot Name Multiple
Wafer ID Multiple
Wafers 62
Wafer Size 150 mm
Die Size 1170 x 1425 um
Flat Angle 0
Mod. Date 12/05/07 16:53:19
Data Summary
Die % ADPW
Pass 501254 96.13% 084.00
Fail 20172 3.87% 325.00
Sample 48907 95.80% 788.00
Force 0 0.00% 0.00
Inspection 0
Datalog 0
Skip 0
Ink Only 76818
Reference (24,23)
100
Die Type X Y %Group %Other
Apply
Reset
06/20/08 16:59:03 Cell /usr/navigator/new/cells/cell_11 is considered an incomplete cell.
06/20/08 16:59:03 Please check it and either delete it or recreate it.
Data Disk Space Used
5%

Various Probe marks

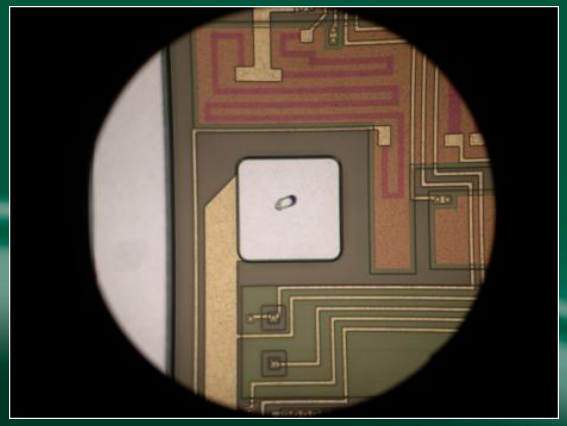
Blade



Vertical probe – 8 times



Epoxy cantilever

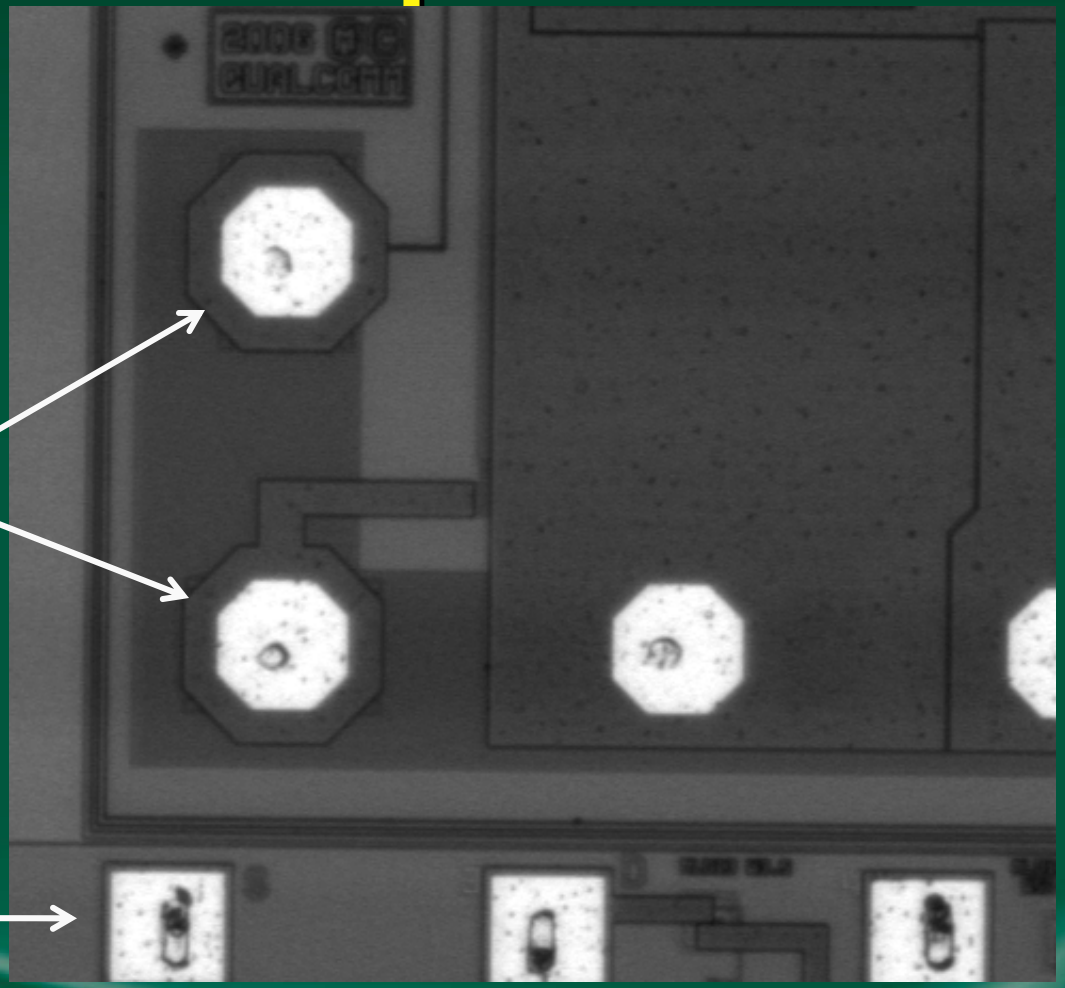


Results: Scrub Mark Comparison

Vertical card gram force applied at 125 um over drive = approx. 6 grams

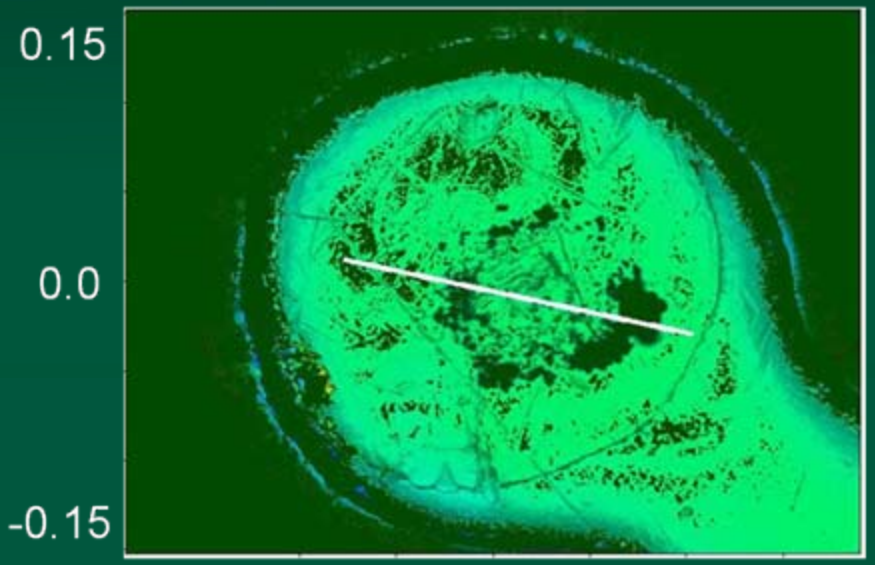
Vertical card scrub marks

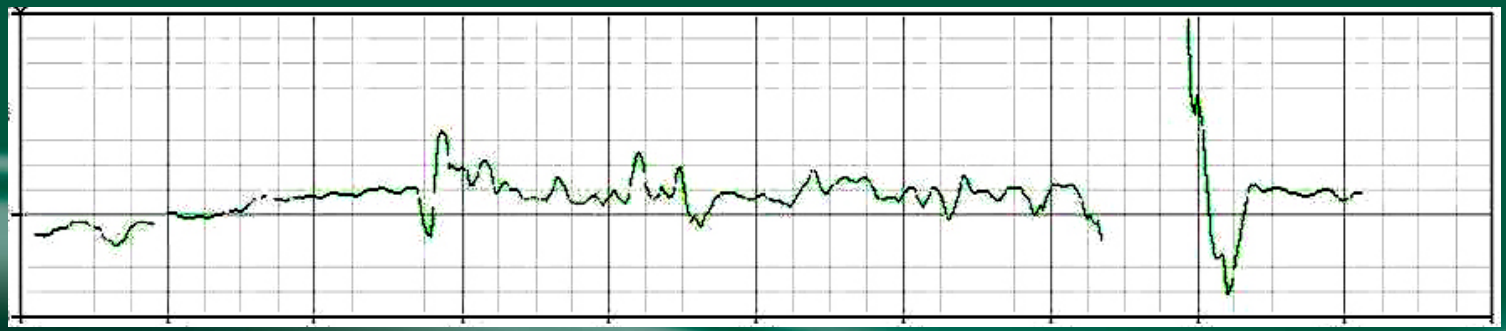
Cantilever scrub marks



Probe Head to PCB Pad Contact

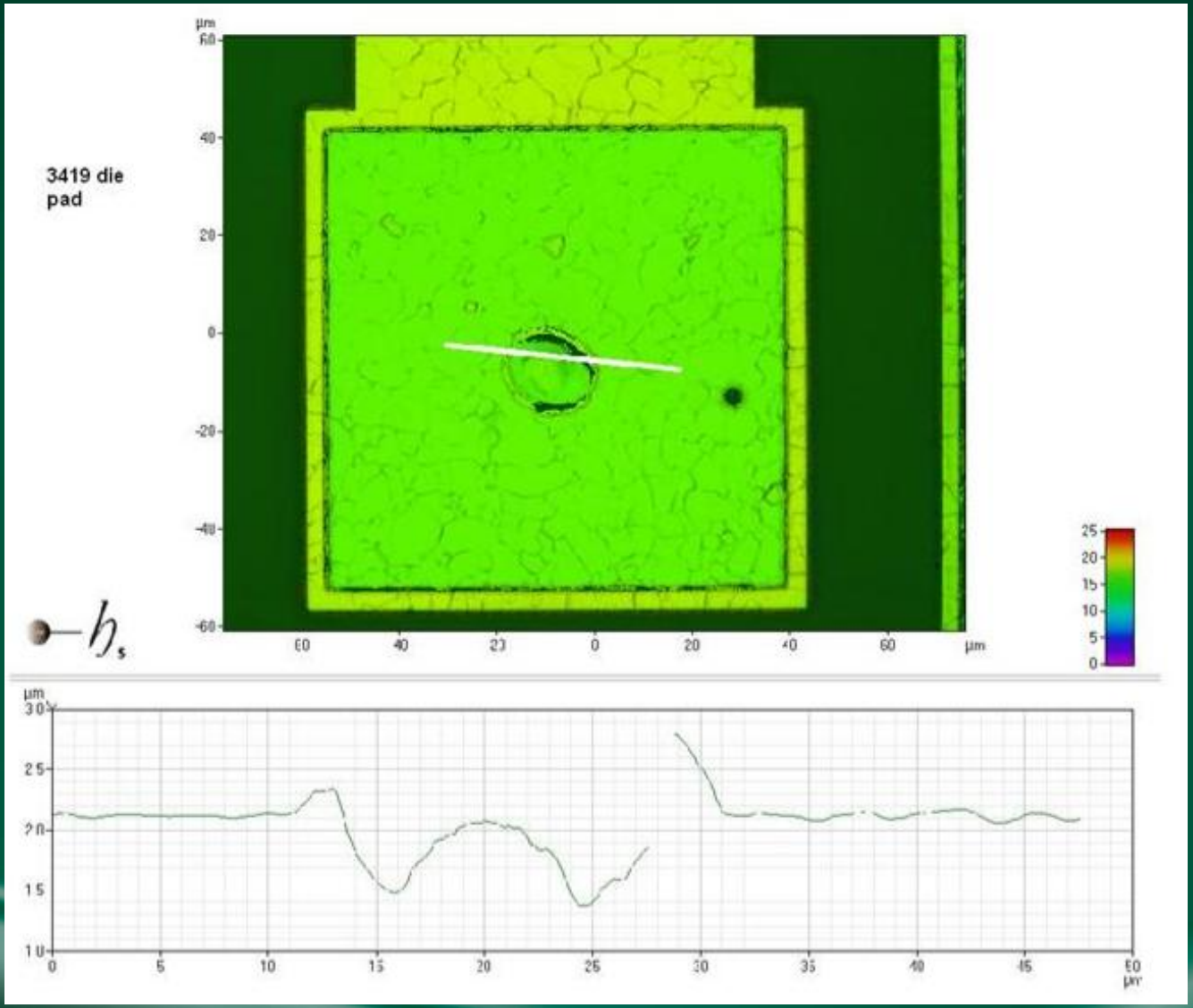
Analysis after 1.1 million touchdowns





Probe Mark Analysis

- 5 um pad penetration
+5 um berm



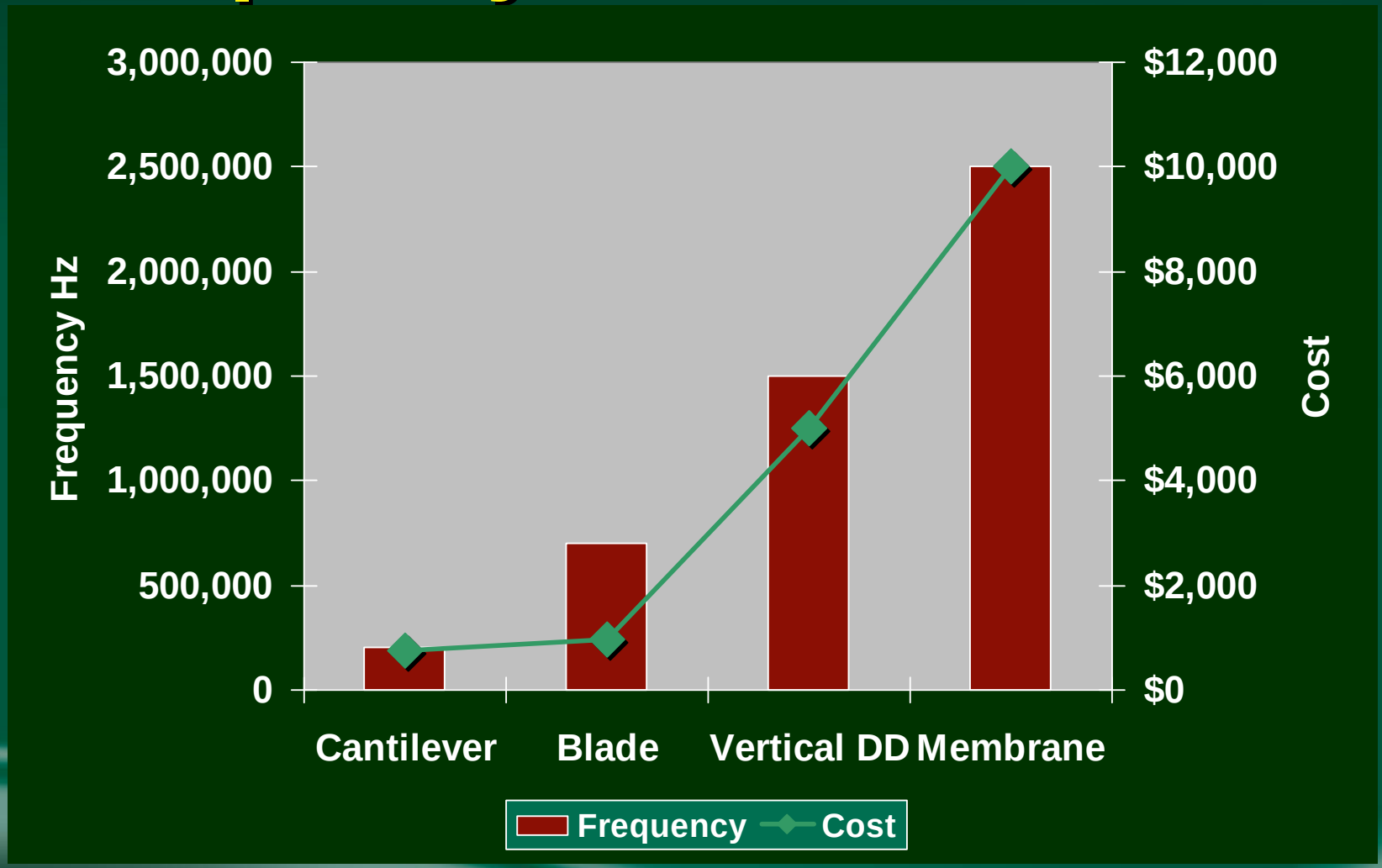
Reduced Probe Marks

- Pointed probes required for lower CRES
- Pad sizes shrinking, thus smaller scrub marks are desirable and required
- Probe and re-probe on same pads were now possible with minimal damage

Cleaning Process Used

- Using International Test Solutions (PL5001-3sh)
- Cleaning determined to be best at 3,000 TD's based on current yield analysis
- Cleaning motion: Z x 10 times for pointed probes
- Using same cleaning material as used for standard cantilever designs

Frequency vs. Cost Chart



Testing Conclusions

- Direct Dock vertical probe card provided a cost effective alternative to cantilever for low volume, high performance products
- Frequency should be much improved over cantilever & may even compete at some level with membrane probes
- This design can meet Analog's test needs at a lower cost than membrane type probe card
- Card life confirmed to 1+ Million touchdowns before offline cleaning is necessary
- Yields were as good as cantilever card designs
- Scrub marks much smaller and preferred

What's Next?

- Evaluate maximum frequency testing
  - Determine if electrical coupling is a limitation
- Optimize in-line cleaning methods
- Review CTE of upper core materials
- Evaluate temperature testing capability
  - Initial data shows promising result at hot
  - Probes sticking at cold (32F, 0C)
- Release this design to more mainstream high performance linear devices
  - Use this direct dock design on high frequency products
  - Take advantage of the short probe and reduced inductance vs. cantilever

Acknowledgements

- John McHatton – Analog Devices, Inc.
- Craig Ventola – Analog Devices, Inc.
- Brian Cannazaro – Analog Devices, Inc.
- Don Hicks – Wentworth Laboratories, Inc.
- Keyur Desai – Wentworth Laboratories, Inc.