

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop



Real-World Avalanche Testing Of Single-Die, Wafers, Hybrid Modules, and Packaged Devices

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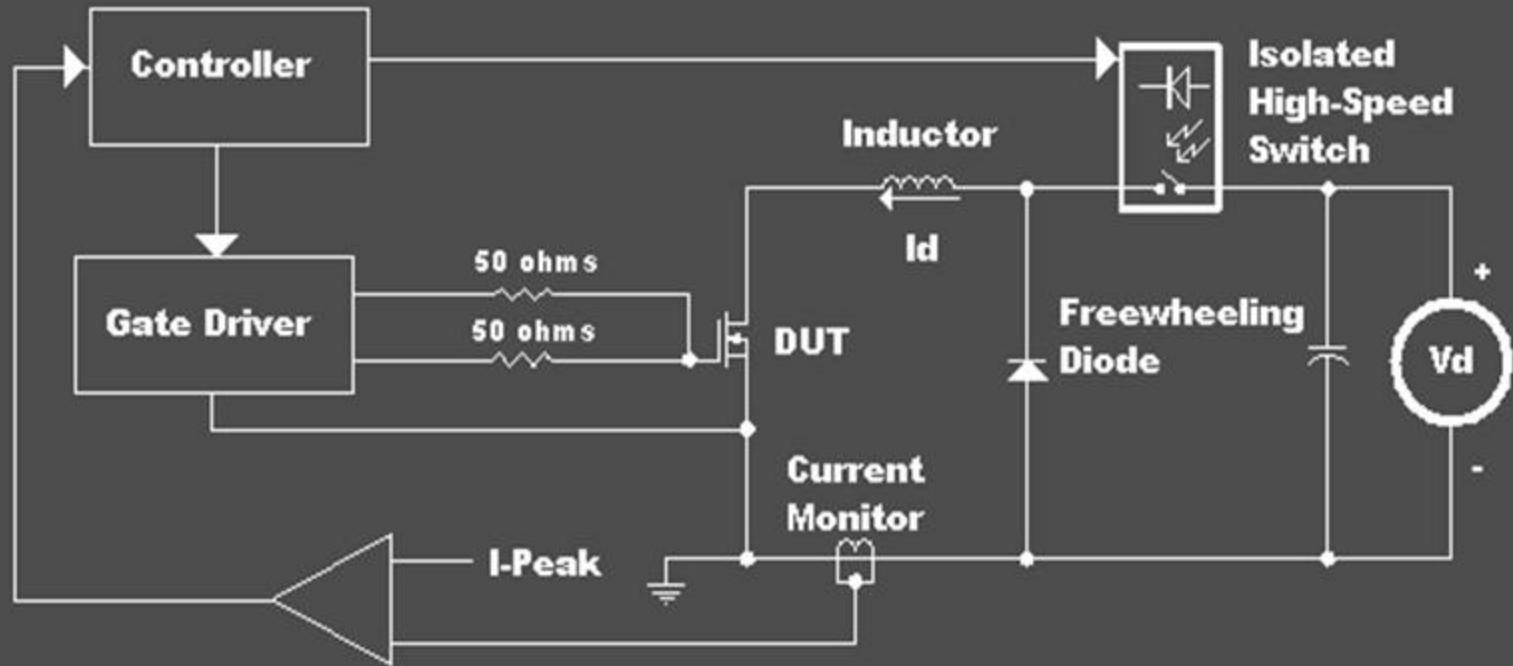
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Avalanche Testing Background

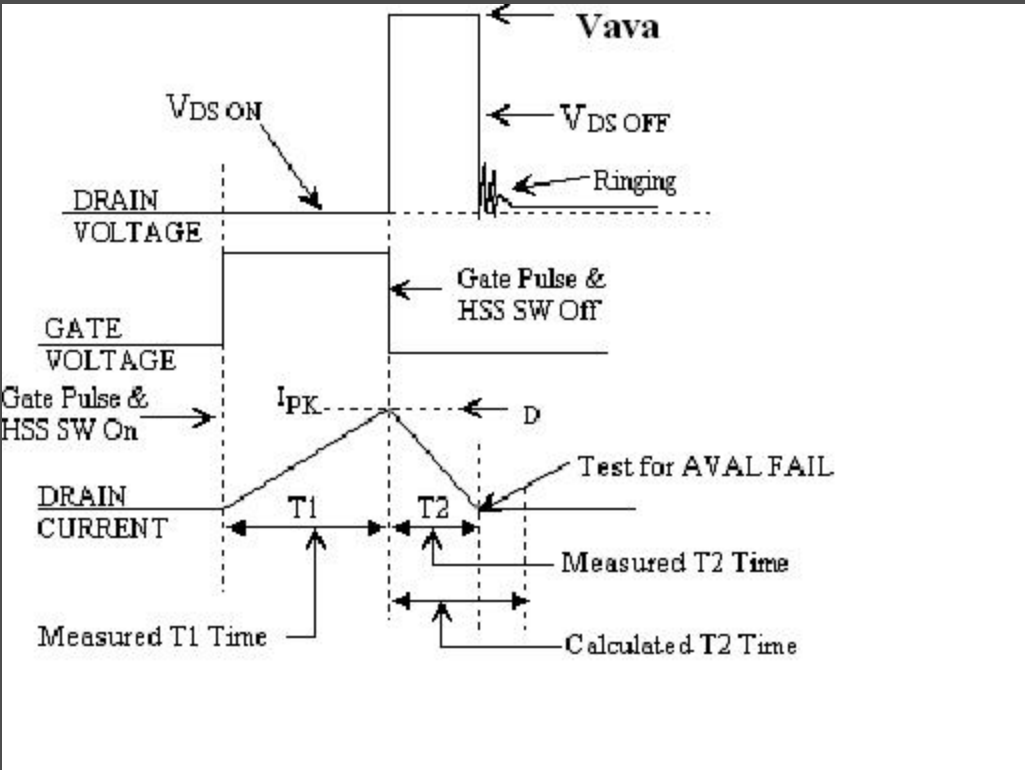
- MOSFET Avalanche Testing - 1985
- Manufactures Disagreed On Usefulness
- Major Manufactures Now Provide Energy Ratings
- What Is Avalanche Mode?
- What Is Ruggedness?
- Avalanche Test Methods
- Industrial Avalanche Test Standards
 - MIL-STD-750 METHOD 3470.2
 - JEDEC STANDARD JESD24-5

Ideal Avalanche Test Circuit



$$E_{AVA} = \frac{1}{2}L \times I_D^2$$

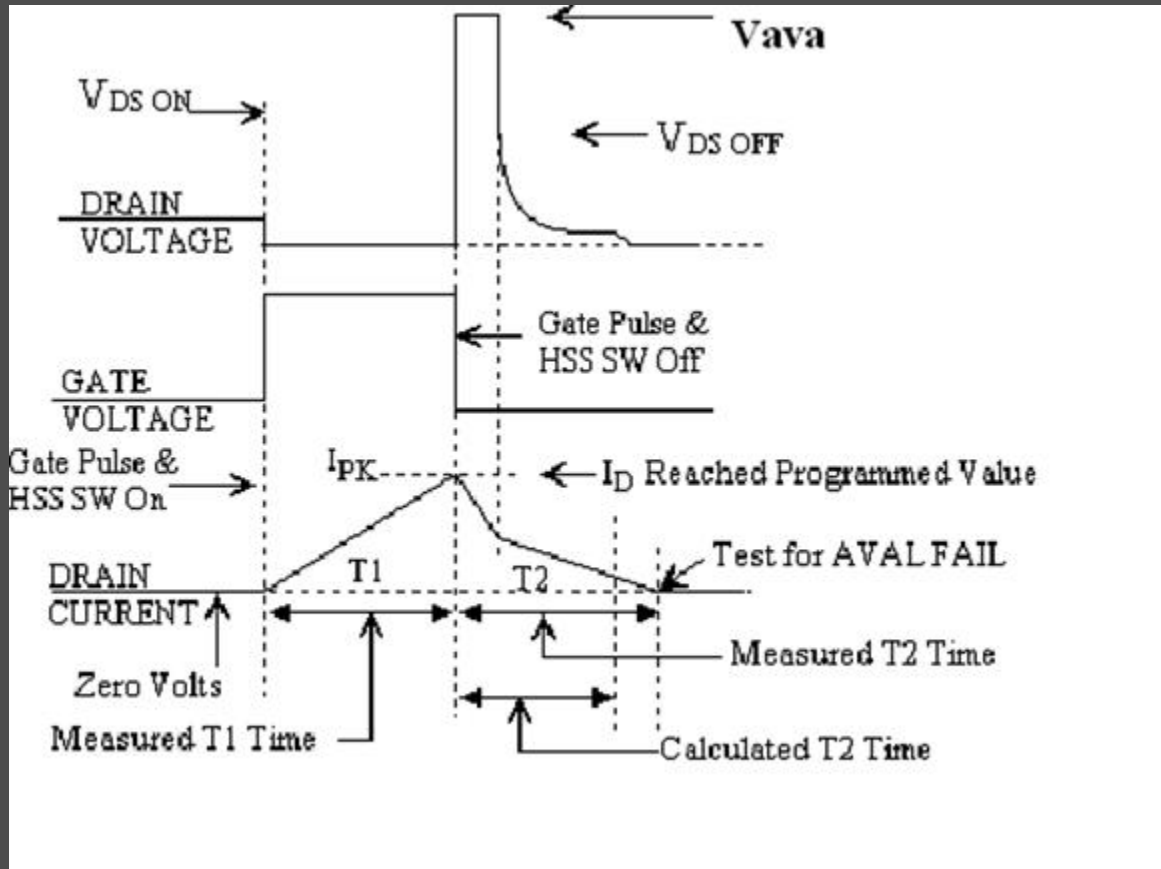
Good Avalanche Test Waveform



T1 and T2 Times
Calculated From:
Inductance Value
I Peak
Rated Drain Voltage

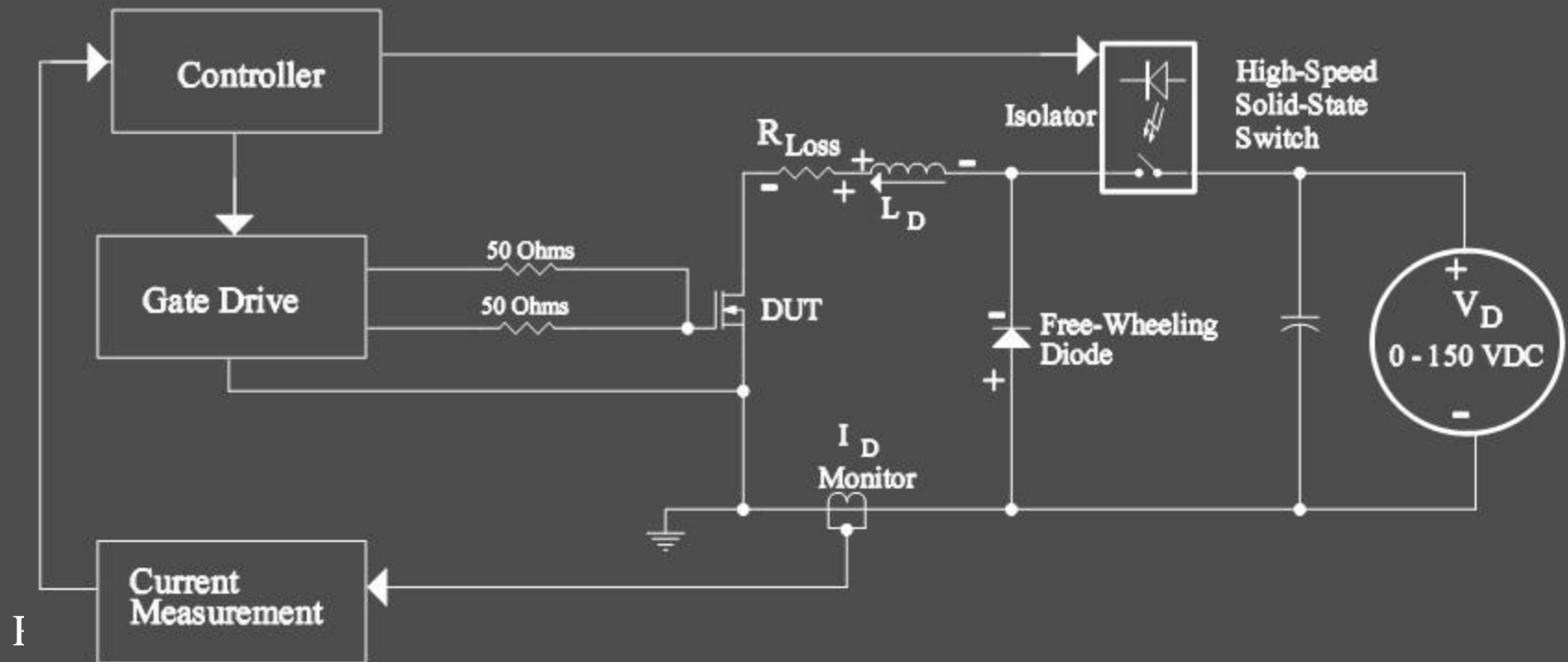
Shows DUT Passing Avalanche
Based On Measured T2 Time

Failed Avalanche Test Waveform



Shows DUT Failing Avalanche Based On Measured T2 Time

Real-World Avalanche Circuit



$$T_1 = \frac{L}{R_{Loss}} \ln \left(1 - \frac{R_{Loss} * I_P}{V_{ON}} \right)$$

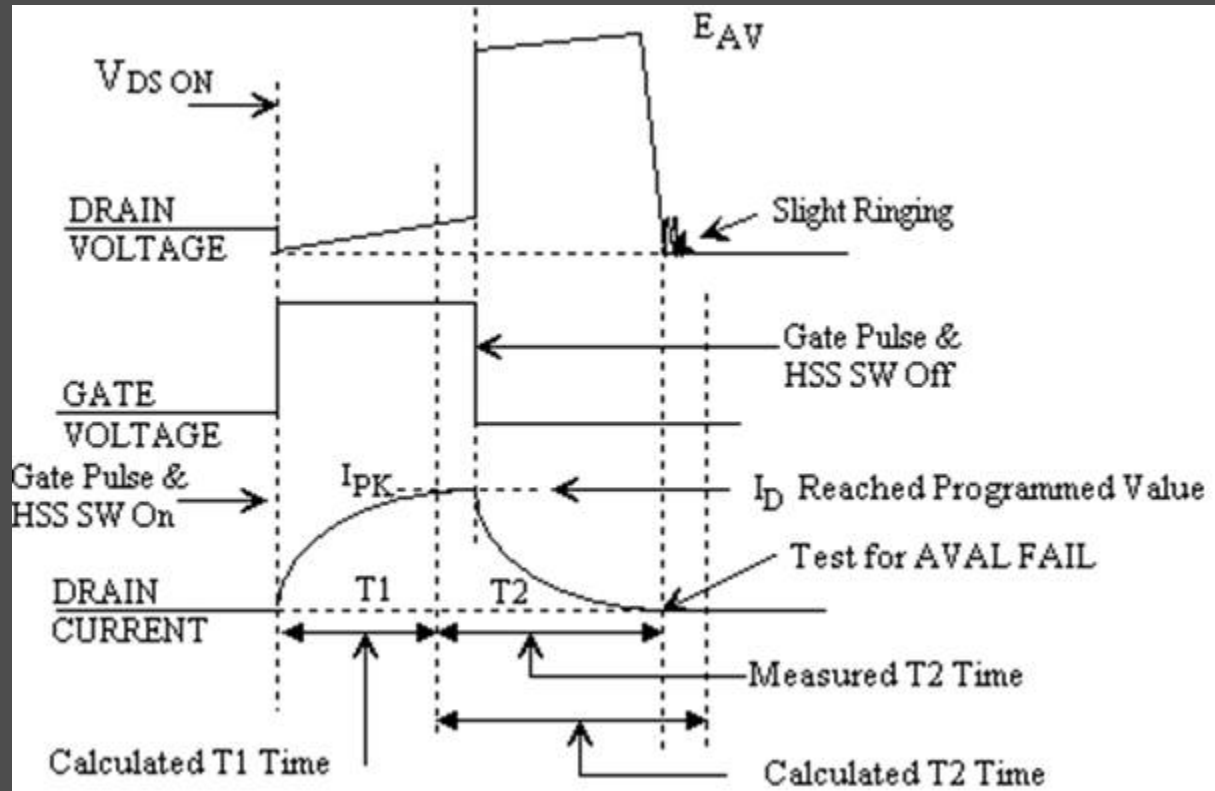
$$V_{ON} = V_{Loss} + V_{DUT ON}$$

$$V_{OFF} = V_{Loss} + V_{DUT OFF}$$

$$T_2 = \frac{L}{R_{Loss}} \ln \left(1 - \frac{V_{ON}}{R_{Loss} * I_P + V_{ON}} \right)$$

$$V_{DUT OFF} = V_{Avalanche}$$

Real-World With Losses Waveform

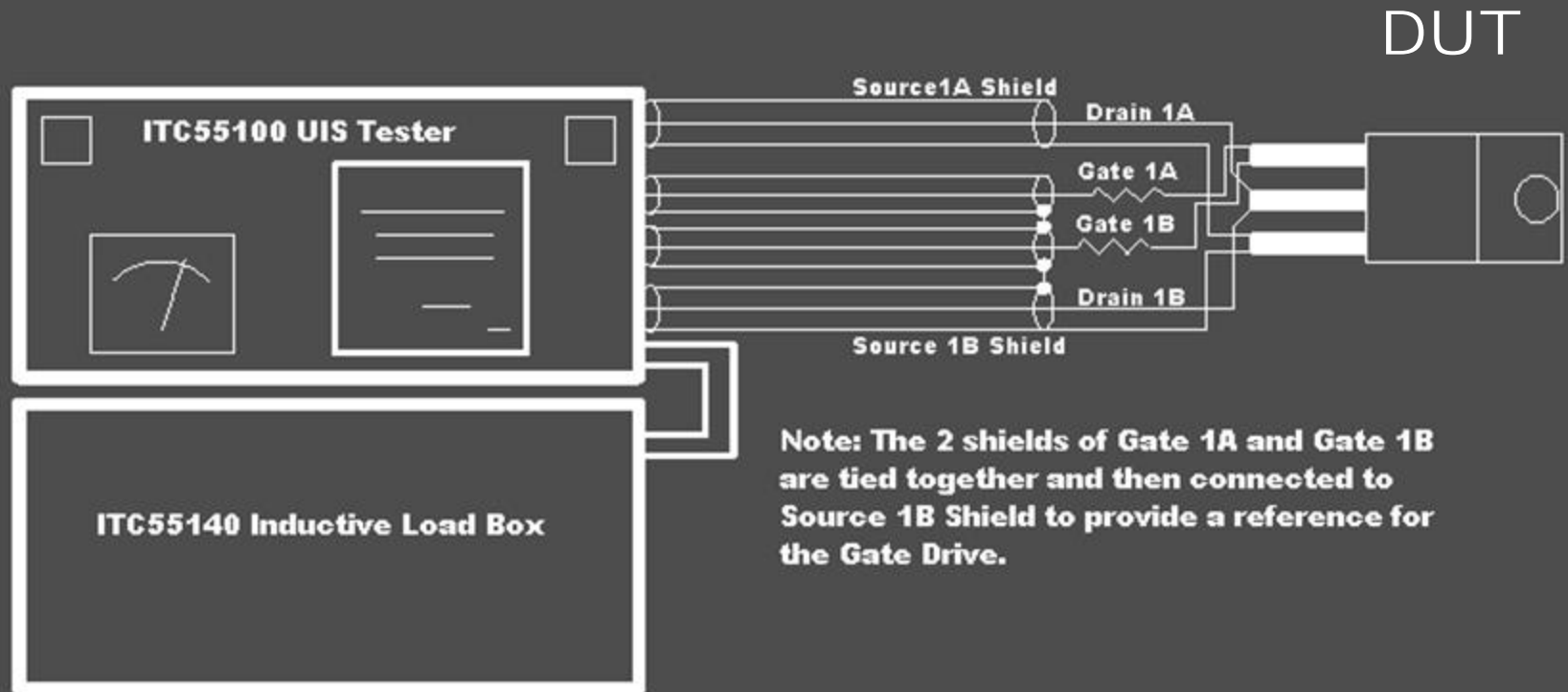


Note the “Rounded Current” Waveshape

Losses Increase T1 Time

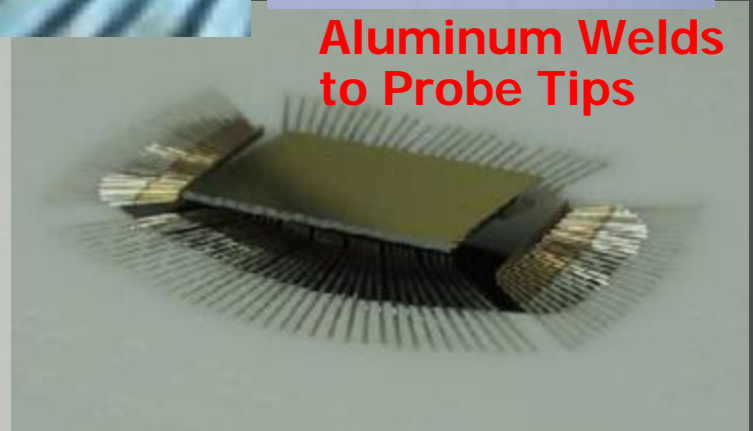
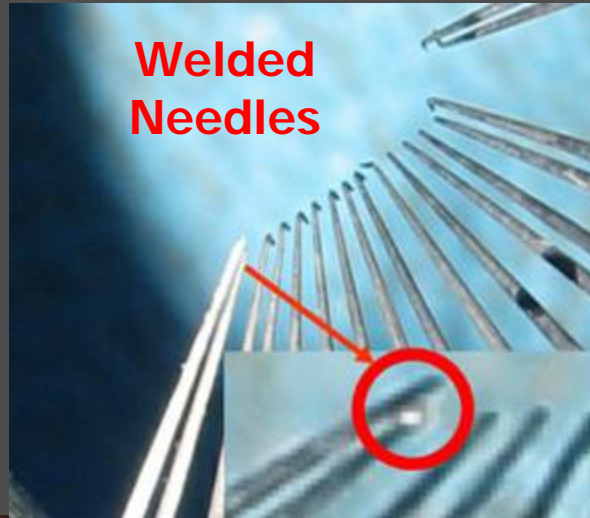
Losses Decrease T2 Time

Package Level Avalanche Testing



... now to extend this same testing to Wafer and Die

High Power Testing on Probe Cards



Wafer and Die High Power Avalanche Testing

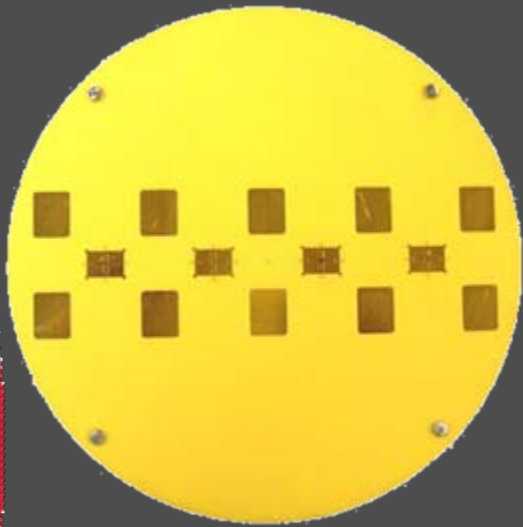
Realities:

- Probe Cards
- Probe Tips
- Testing Environment

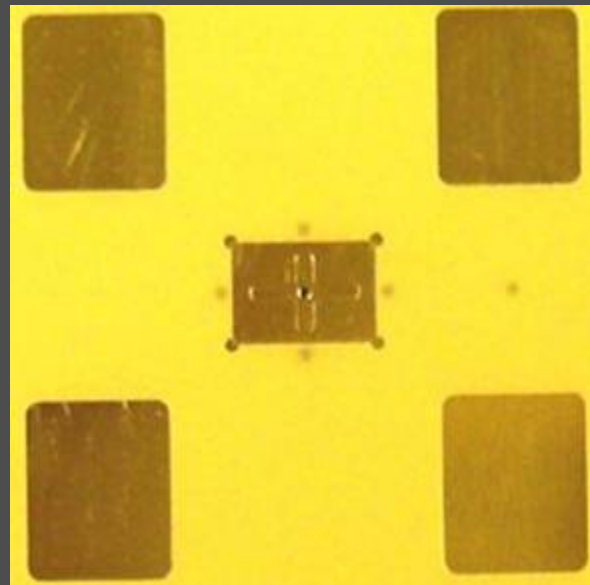
Benefits:

- Lower Cost Failures
- Faster Process Analysis
- Higher Net Yield
- Comparison with Packaged Parts

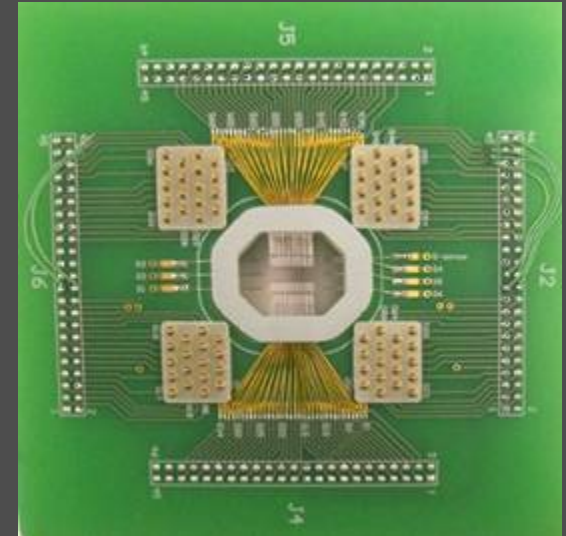
Typical Die/Chip Carrier & Probe Card



Chip Carrier

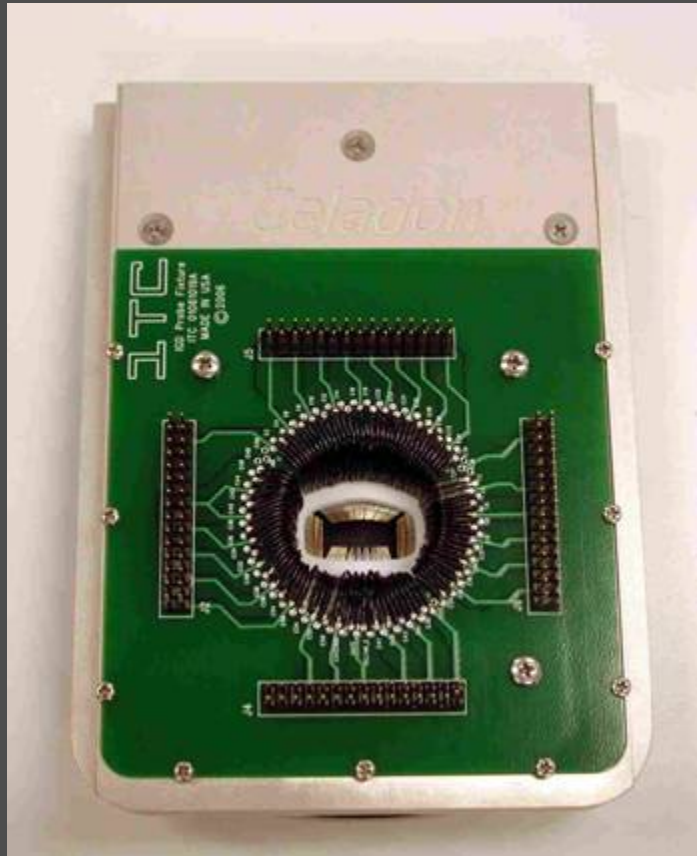


Enlarged Carrier View

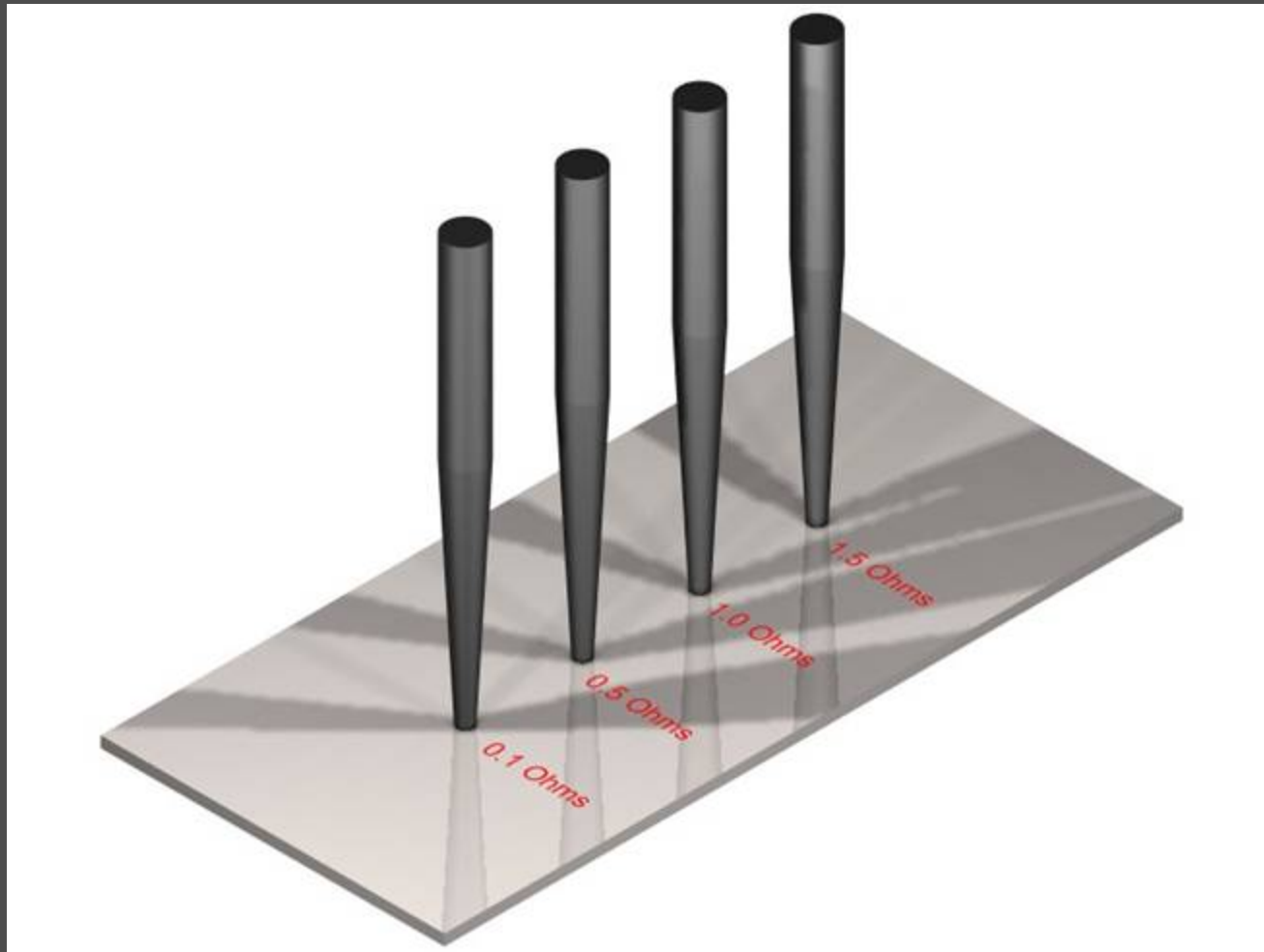


Probe Card with
5 mil tip dia probes
and Pogo Pins

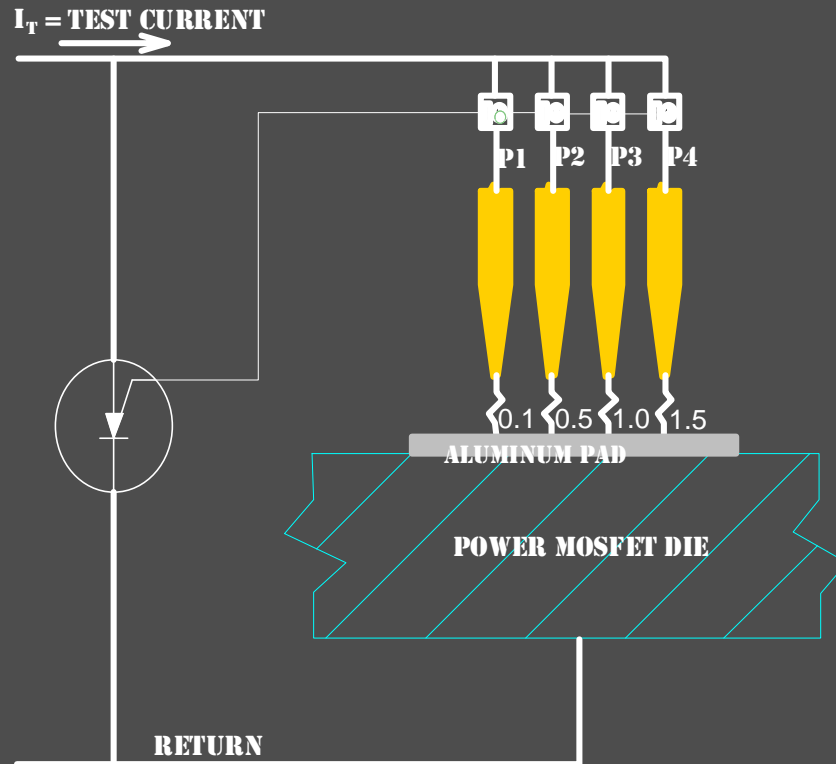
200 Amp, 1000V Probe Card



Probe Tips on Aluminum Pad



Probe Tip Protection Technique



$I_t = 20 \text{ Amps}$

$I_{\text{max}} = 5\text{A/Probe}, 5 \text{ mil dia}$

$I_{P1} = 5\text{A}, V_{P1} = 0.5\text{V}$

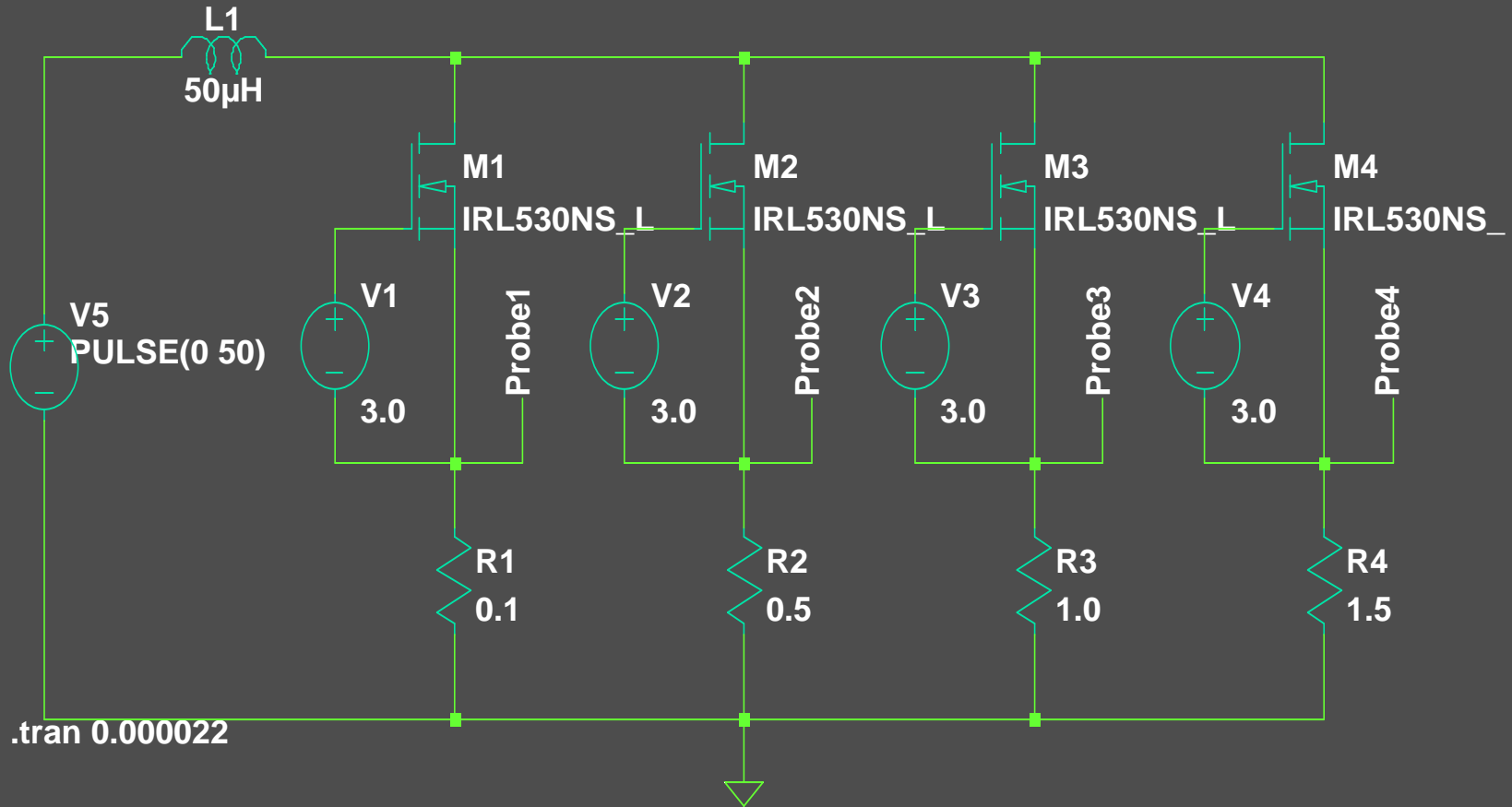
$P_{P1} = 2.5\text{W}$

Manage Probe Current & Voltage to keep POWER Dissipation from harming Probes

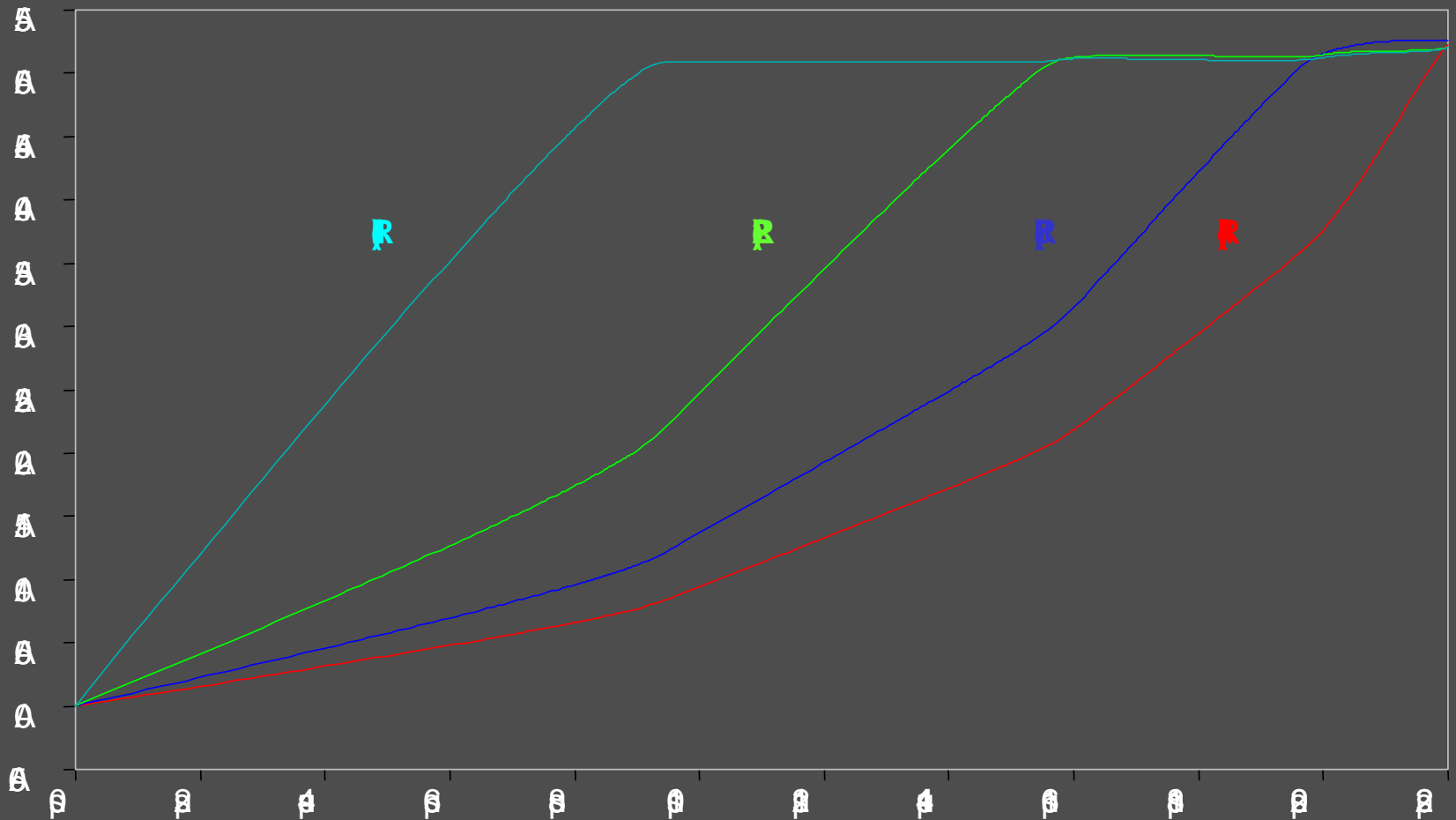
$I_{P4} = 5\text{A}, V_{P4} = 7.5\text{V}$

$P_{P4} = 37.5\text{W!!!!}$
TOO HIGH

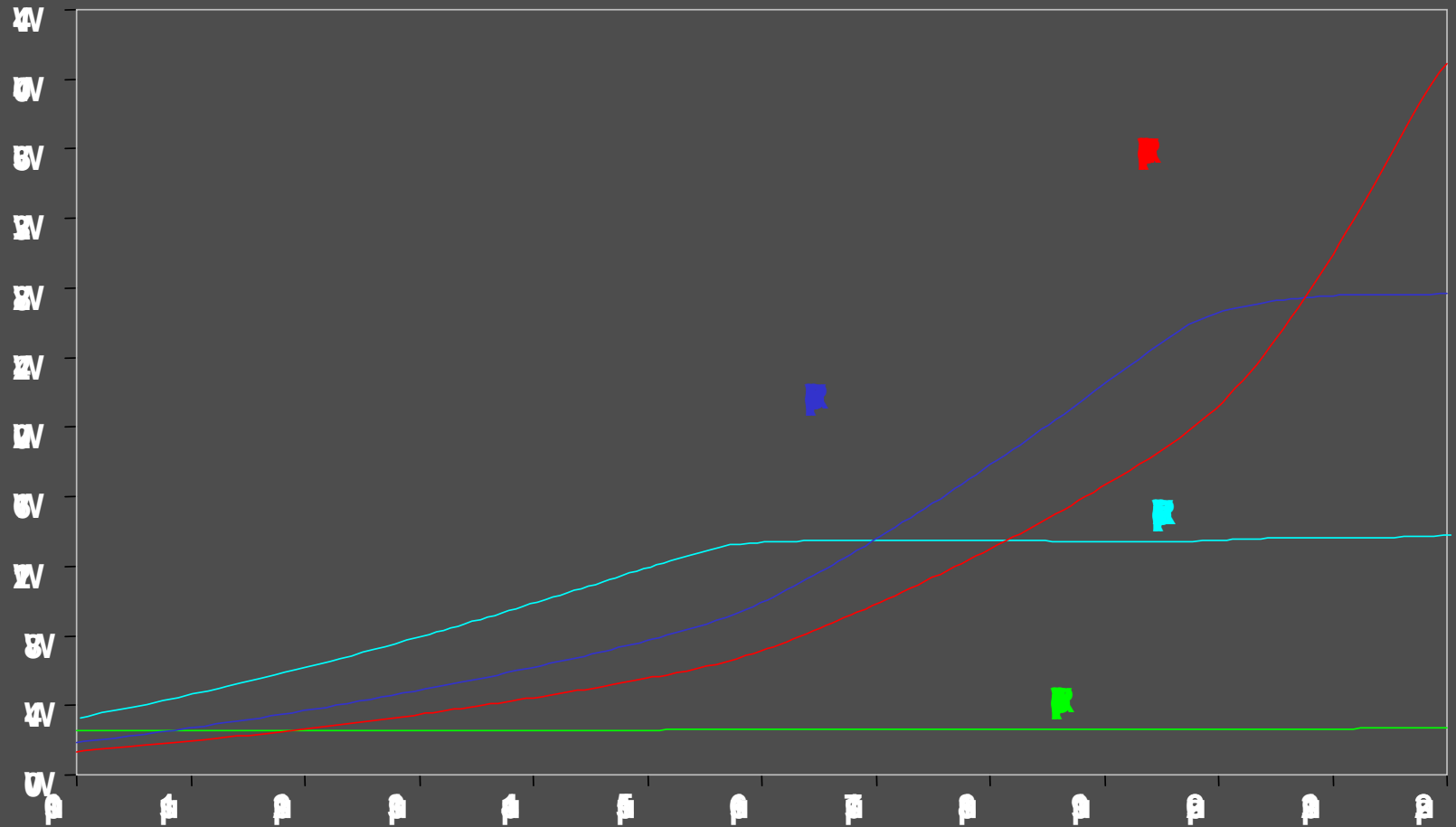
Probe Simulation Circuit



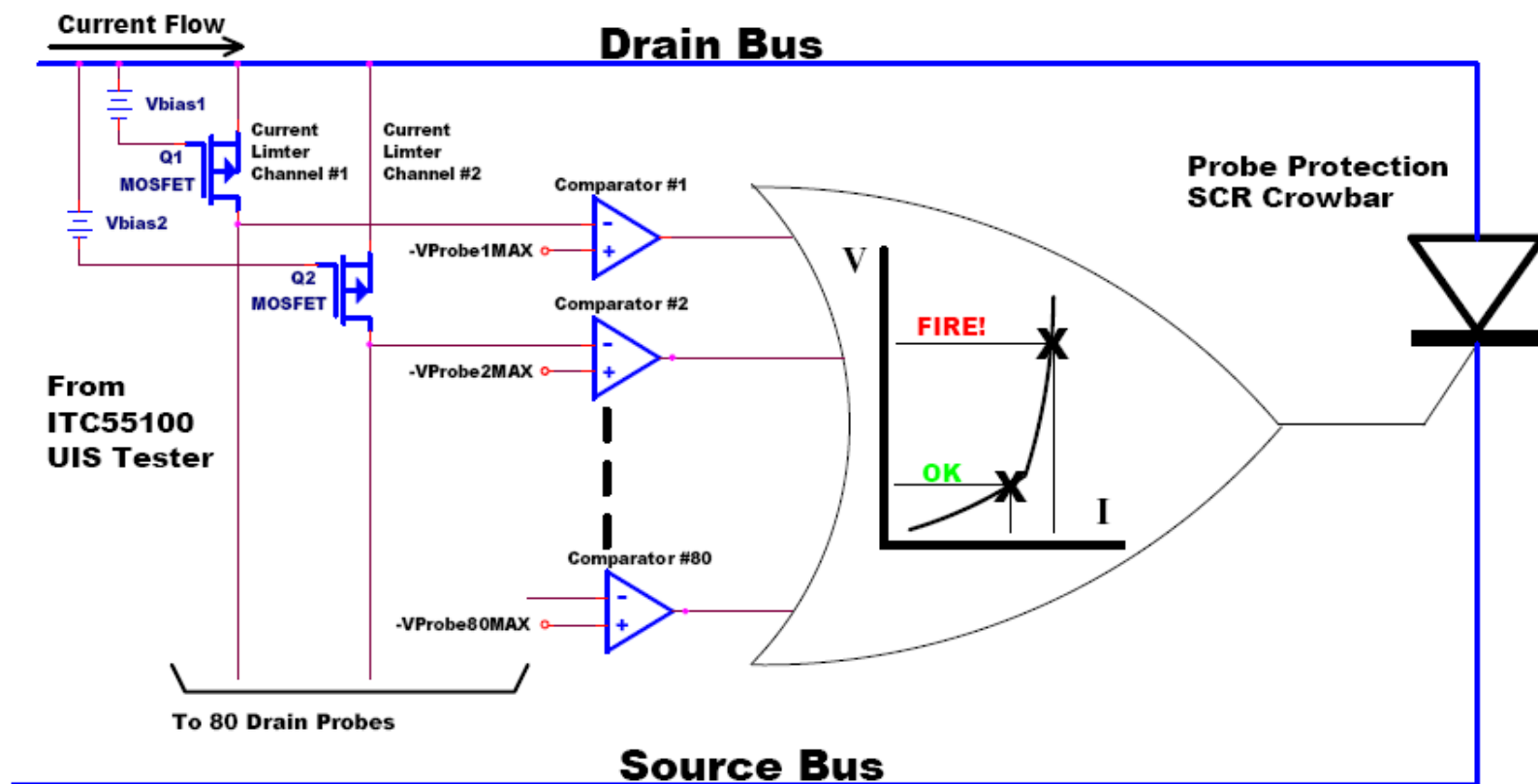
Probe Tip Currents



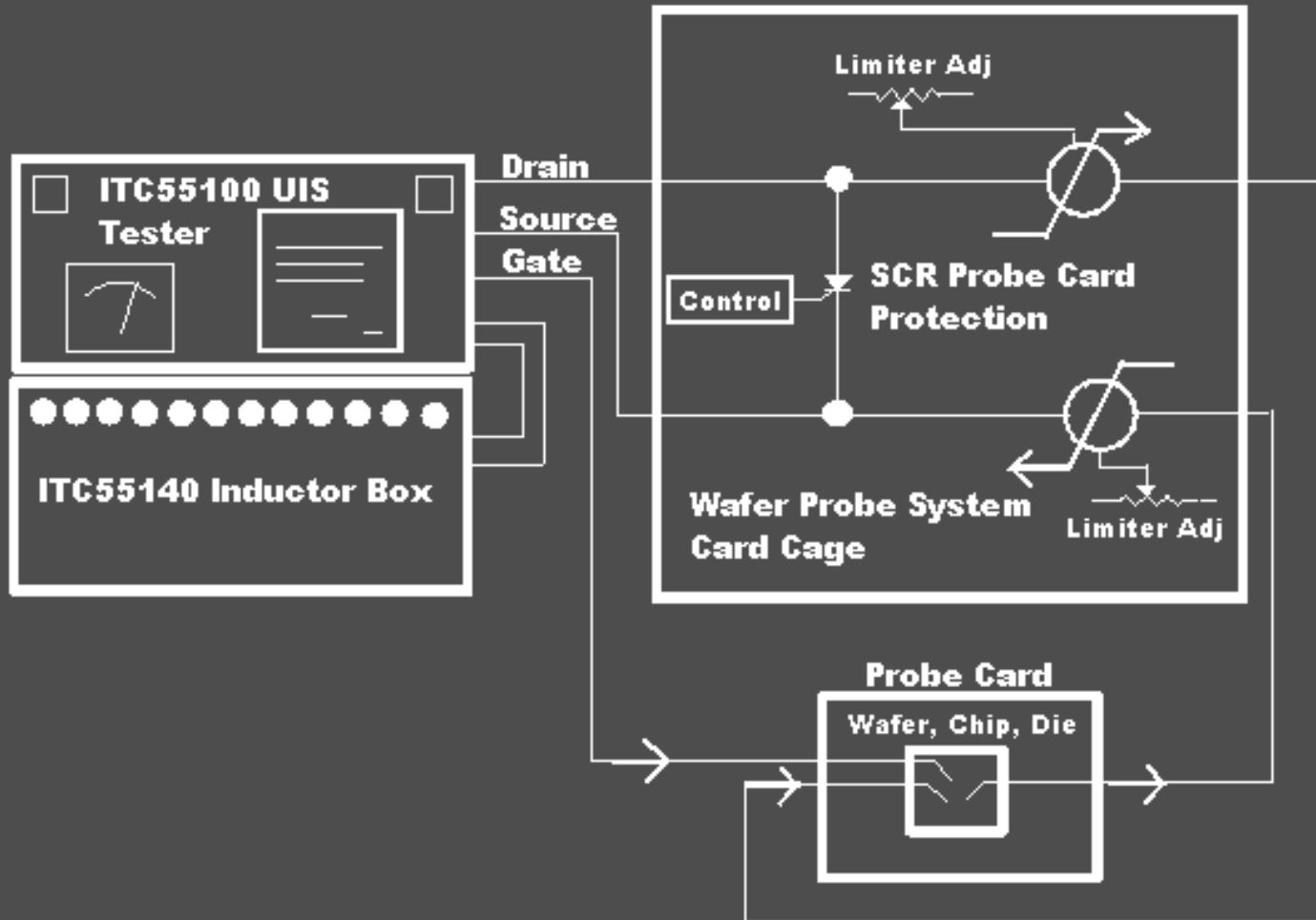
Probe Tip POWER



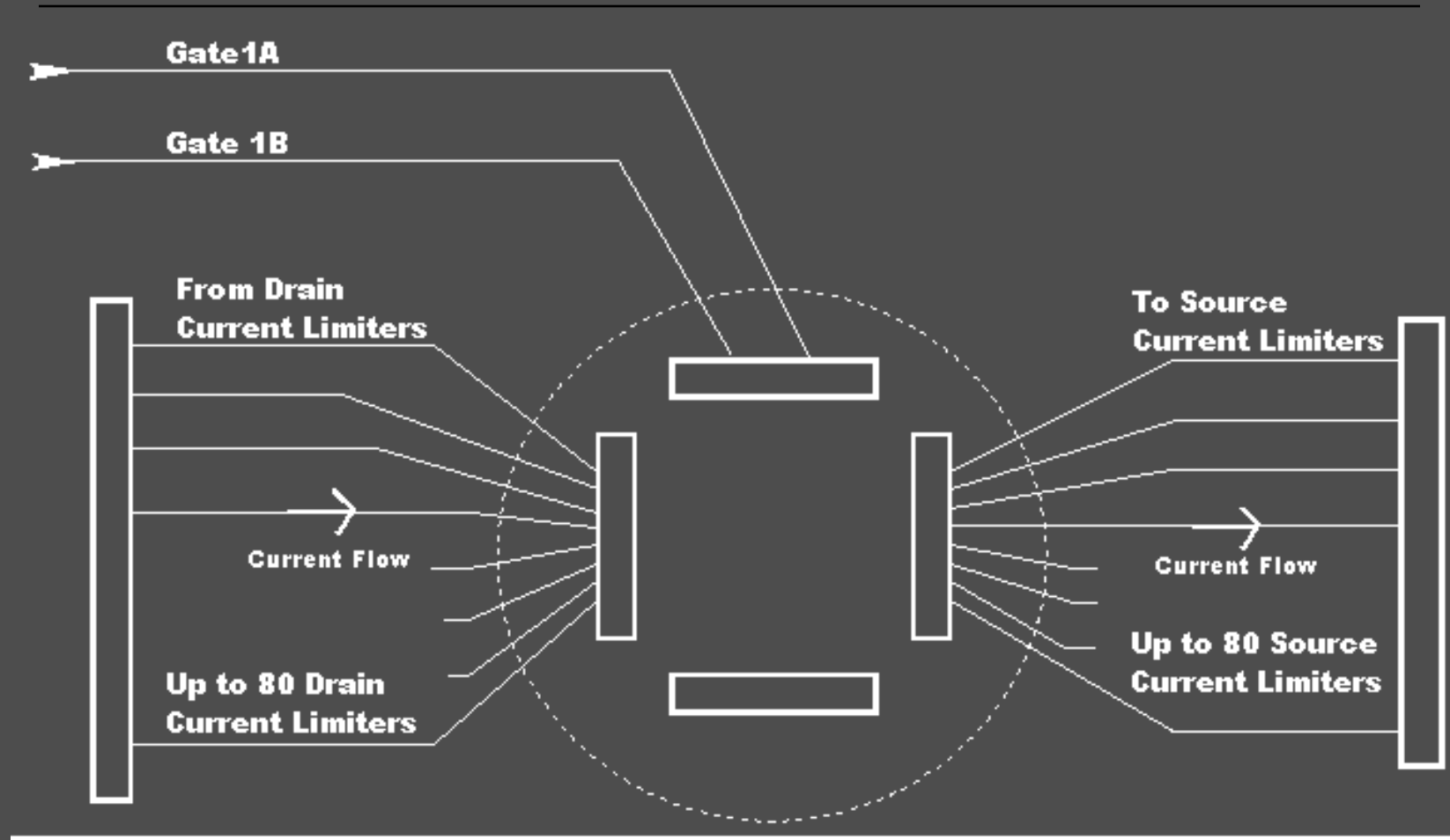
Power Limiter Showing Probe Tip Protection Concept



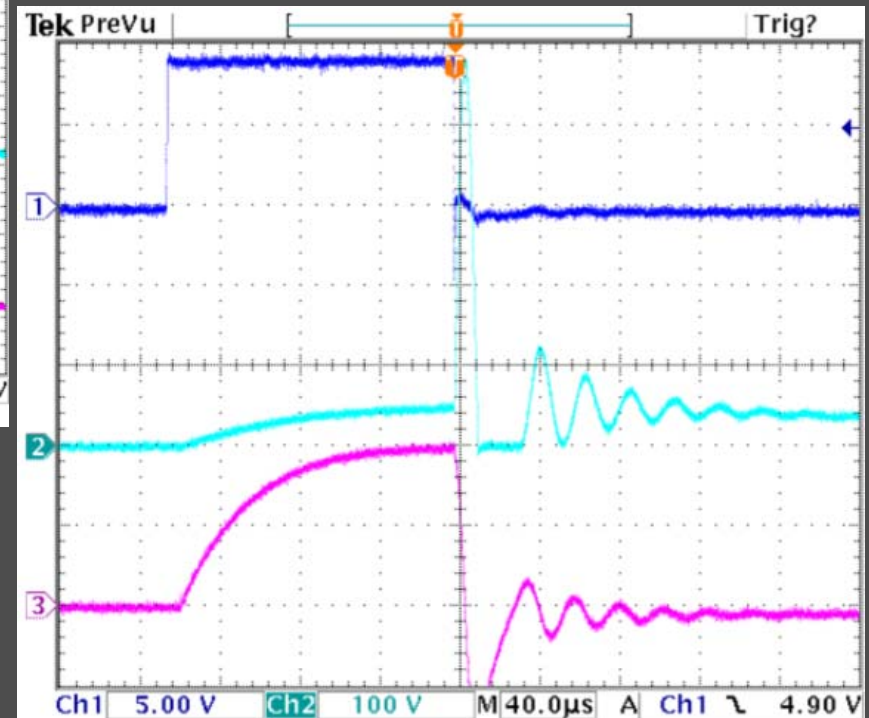
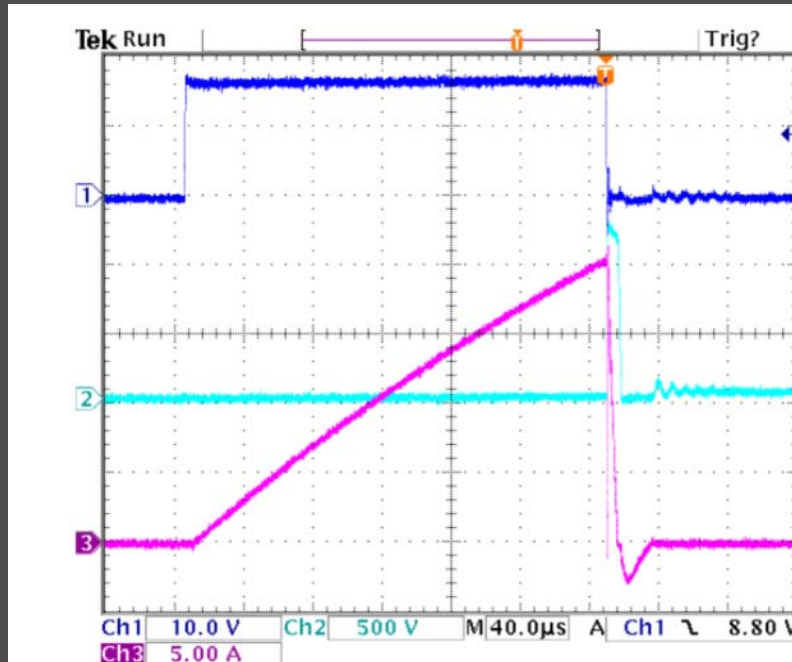
Production Avalanche WPS



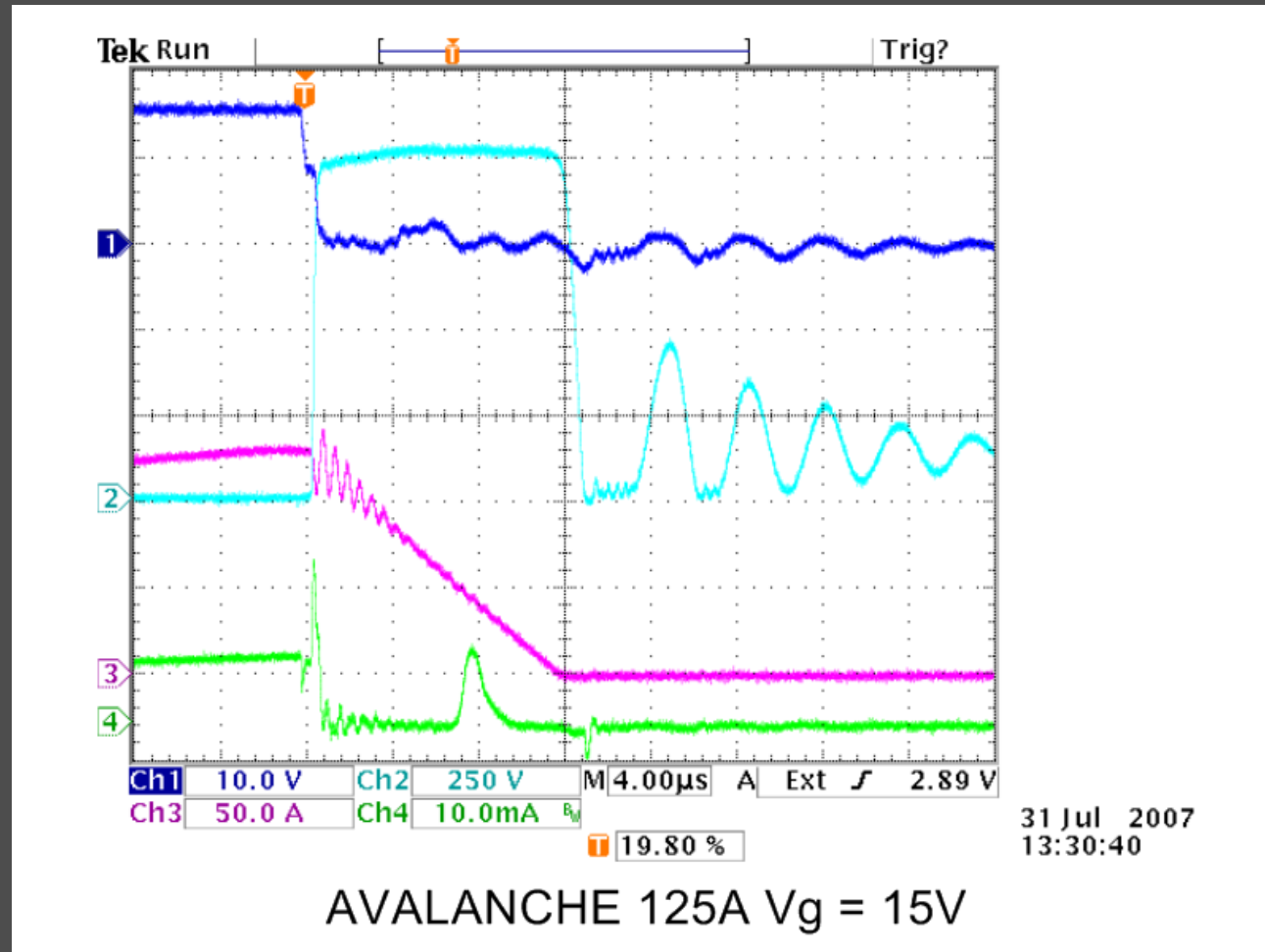
Simple Avalanche Connection Diagram



Realized Avalanche Waveforms

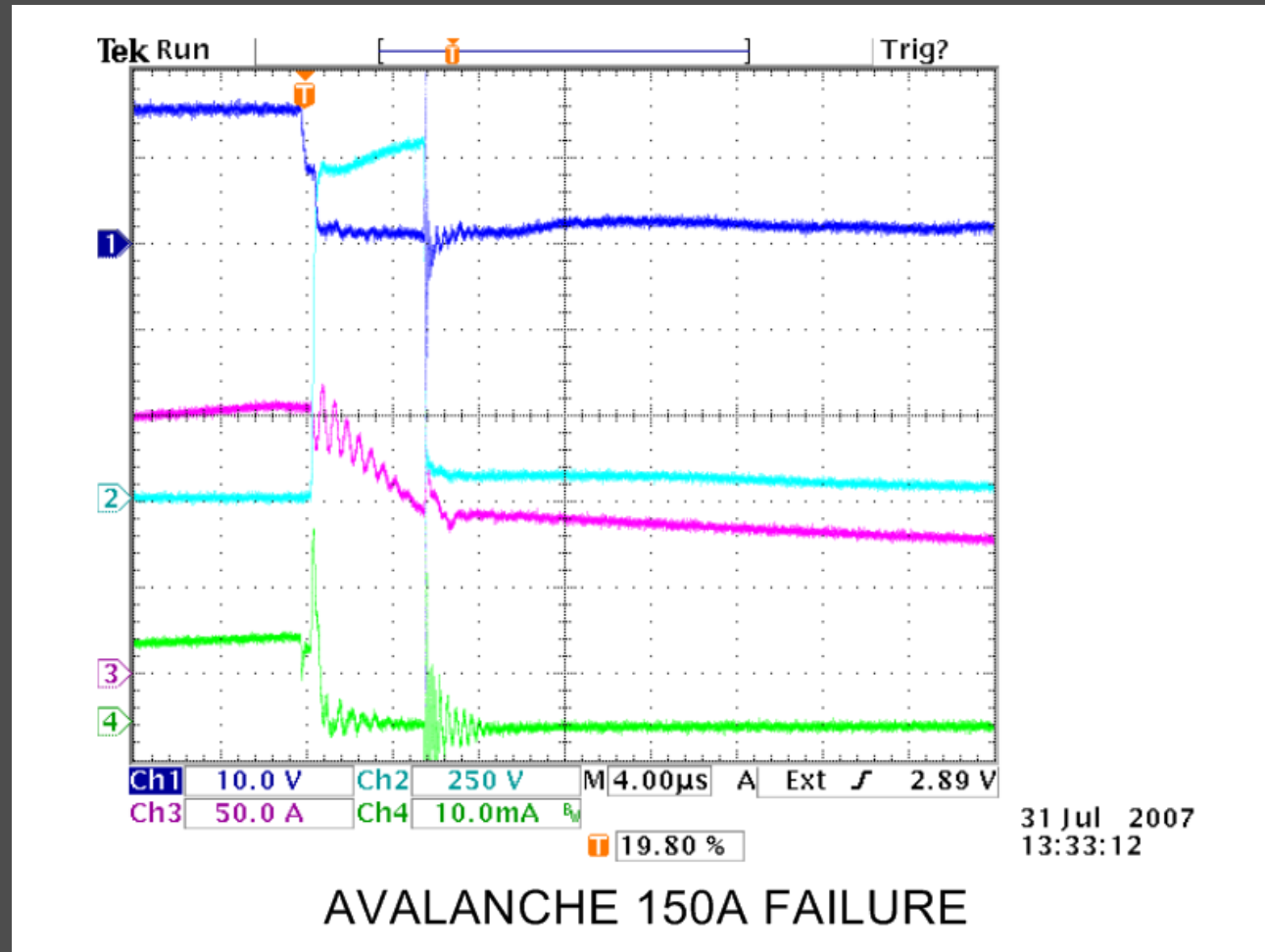


Avalanche Waveform – PASS



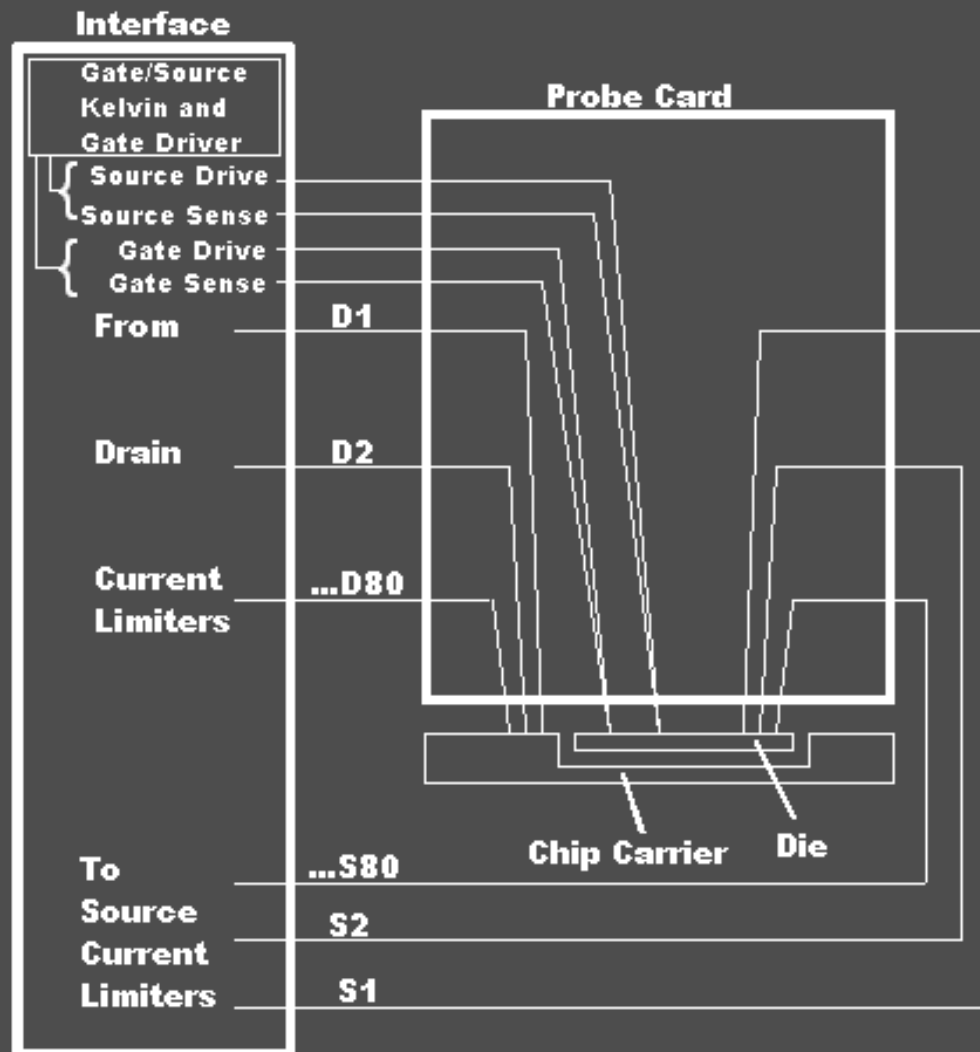
- Collector Current
- Collector Voltage
- Gate Voltage
- Sense Emitter

Avalanche Waveform – FAILURE



- Collector Current
- Collector Voltage
- Gate Voltage
- Sense Emitter

Advanced Chip or Die Level Avalanche Testing Connections



WPS Current Limiter Overview

- Patent-Pending Power Limiter Circuit
- Set for 5 Amps per Probe and uses Standard Probe Card Technology
- Limits Maximum Current In The BEST Probe
- Limits Maximum Power in the WORST Probe
- Voltage Across Contact Resistance Monitored for Complete Protection

Summary

- Allows for Standard Avalanche Test Methods to be used FULL Power
- Expandable to High Power and High Current Parts and Tests
- Power MOSFETs, IGBTs, Diodes, Transzorbts
- Avalanche, $R_{\theta_{SOA}}$, V_{DSON} , R_{DSON} , V_{CEON} , V_{F-SD} (body diode)
- All performed with the SAME equipment at the SAME Probe Station
- Allows Correlation with Packaged Parts

References

Tim McDonald, Marco Soldano, Anthony Murry, Teodor Avram *"Power MOSFET Avalanche Design Guidelines"* IR Application Note AN-1006

Kenneth Dierberger *"Understanding The Difference Between Standard MOSFETs and Avalanche Energy Rated MOSFETs"* Advanced Power Technology Application Note

"Power MOSFET Single-Shot And Repetitive Avalanche Ruggedness Rating"

Philips Semiconductor Application Note AN10273-1

Warren Schultz *"Power Transistor Safe Operating Area"* ON Semiconductor Application Note AN875/D

Michael Bairanzade *"Understanding Power Transistors Breakdown Parameters"*
ON Semiconductor Application Note AN1628/D