IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Non-contact Test at Advanced Process Nodes

SCANIMETRICS

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Overview

- Advanced CMOS nodes are a challenge for wafer testing
  - Very fine pitch, ultra-low-k dielectrics, non-Al metallization
- Advanced package and interconnect technologies make traditional wafer testing impossible
  - New package and interconnect technologies e.g. thru-Si vias
  - Proximity chip-to-chip communications
  - Optical interconnects do not have bond pads or bumps
- Non-contact testing techniques can be used to overcome these advanced node testing issues
- Data is presented confirming exceedingly low error rates and wide mechanical alignment tolerances for DC to GHz signals

Outline

- Advanced node wafer testing challenges
- Non-contact communication technology
- Applications and update
- Results from 45nm test chip
- Summary

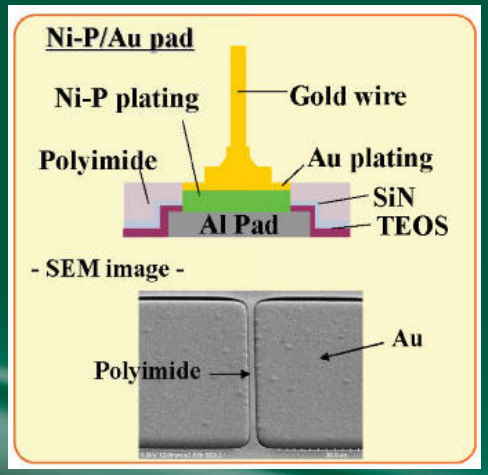
Advanced Node Testing Issues

- New materials
  - Pad and dielectric damage
- Pad pitch
- New interconnect technologies w/o bond pads
  - Thru-silicon vias
  - Redistributed Chip Packaging (RCP)
  - Proximity communication
- System-in-Package (SiP) has no BIST or DFT
- Test blindness since internal nodes are hidden
  - SiP and SoC

New Materials Issues

- At advanced nodes, ultra-low-k dielectrics and very thin layers cause major issues with conventional wafer probing
  - The metal stack is “spongy”
  - The metal layers are thin
    - Probe needles “tear” the bond pads
  - Gate dielectrics are “ultra-thin” (~10Å)
    - Stress on the die causes dielectric cracking

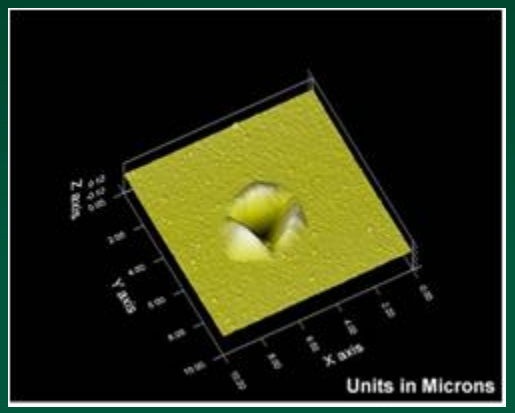
Drastic measures are being pursued

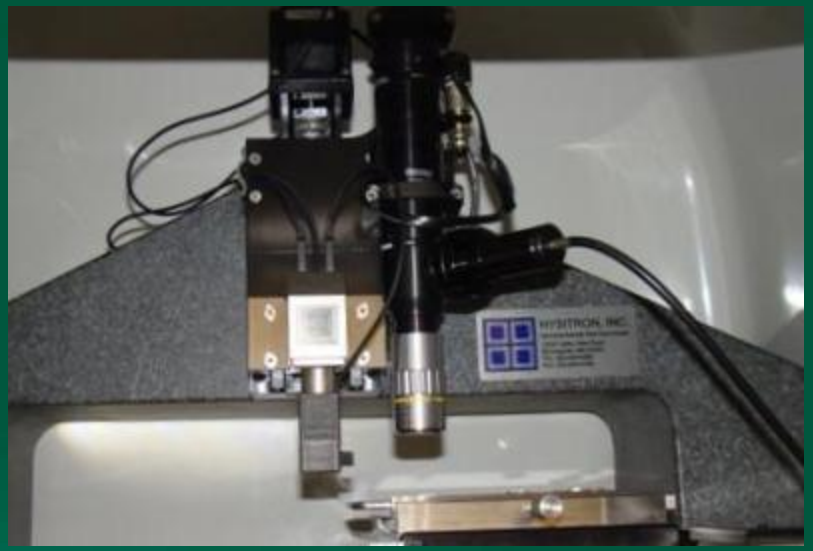


From : Togasaki, et al
Toshiba Semiconductor
2007 KDG Workshop

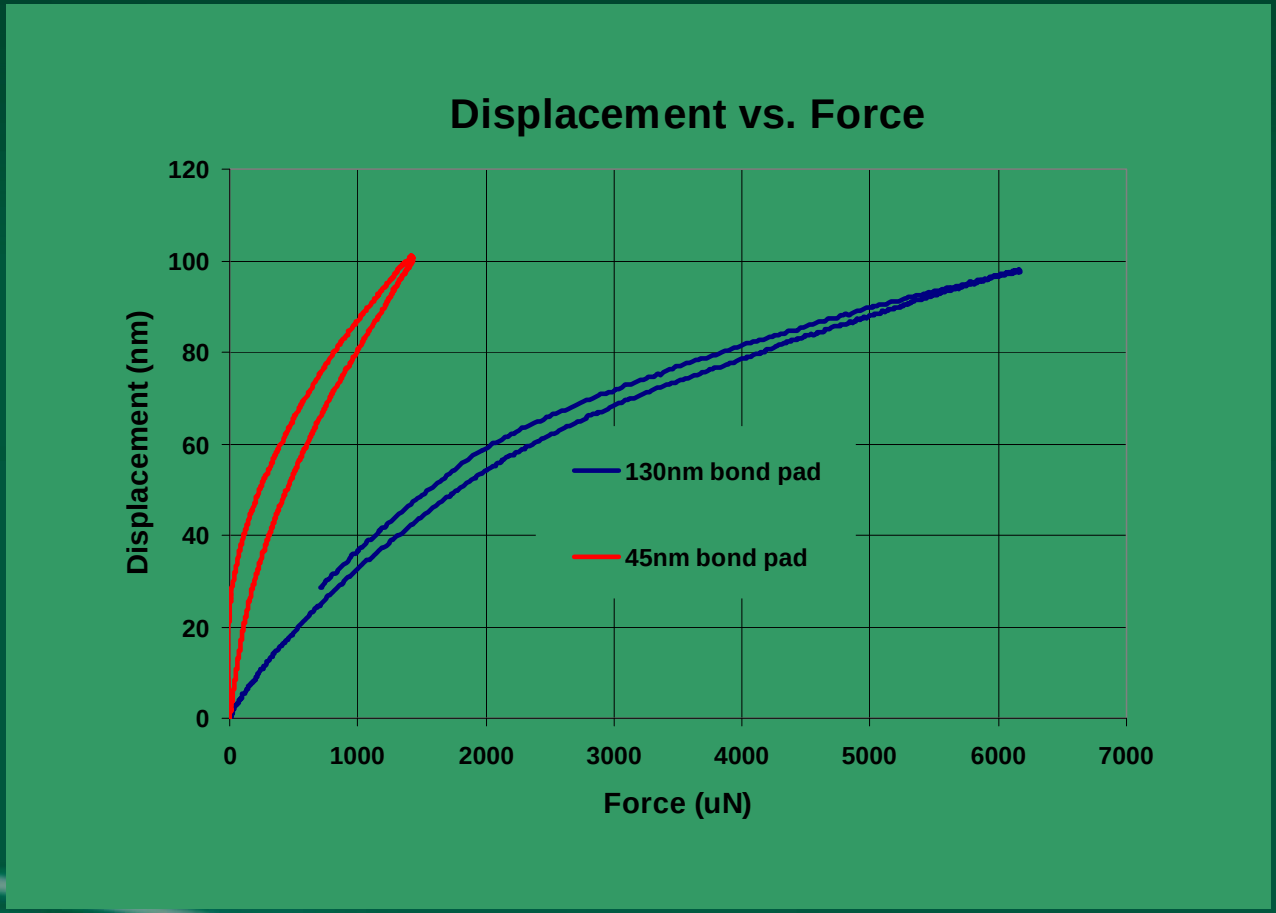
New Materials Issues

Nano-indenter bond pad measurements



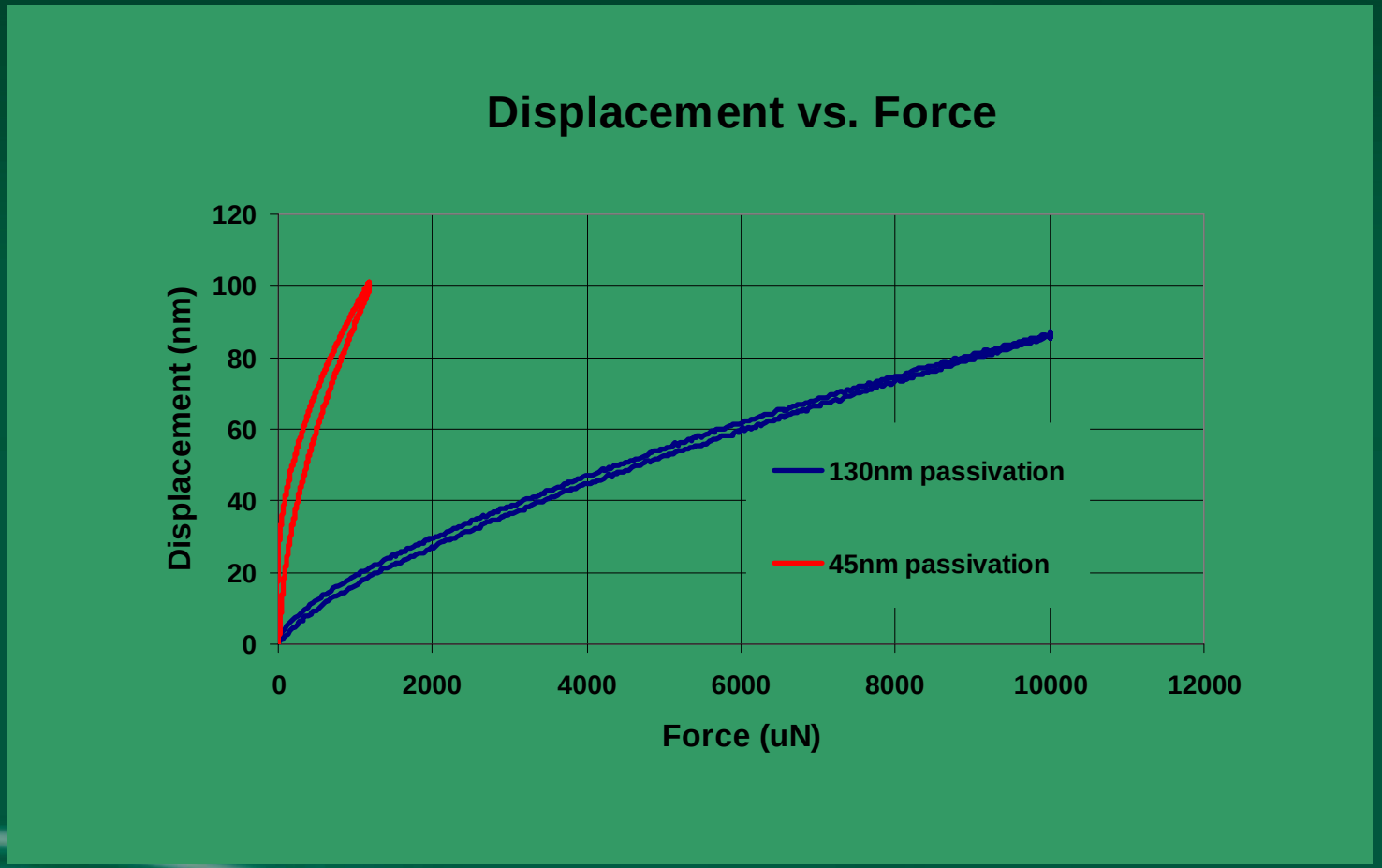


New Materials Issues



Force is 5x less for advanced process nodes

New Materials Issues



Force is 10x less for advanced process nodes

Pad Pitch Problem

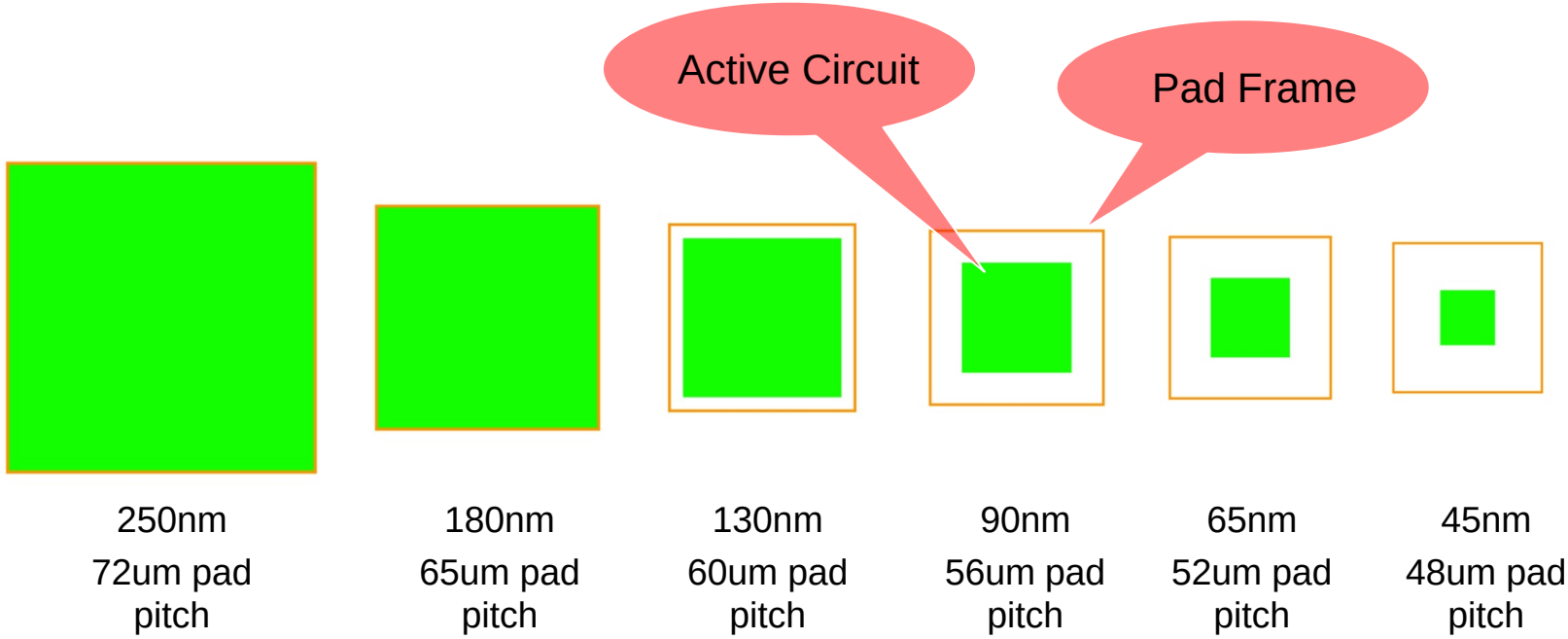
2006 ITRS for Test

Table 38a Wafer Probe Technology Requirements—Near-term Years UPDATED

Year of Production	2005		2006		2007		2008		2009		2010		2011		2012		2013	
DRAM ½ Pitch (nm) (contacted)	80		70		65		57		50		45		40		36		32	
I/O Pad Size (µm)	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y	X	Y
Wirebond	35	60	30	55	30	55	25	45	25	45	25	45	25	45	20	35	20	35
Bump	75	75	75	75	60	60	60	60	50	50	50	50	50	50	50	50	50	50
Scrub (% of I/O)	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH	AREA	DEPTH
Wirebond	25	50	25	50	25	50	20	40	20	40	20	40	20	40	20	40	20	40
Bump	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30	30

- Bond / probe pads are not shrinking with circuit dimensions
  - Probes
    - Pitch, tip size
  - Pad Damage
    - Maximum allowable damaged area
  - ESD Structures

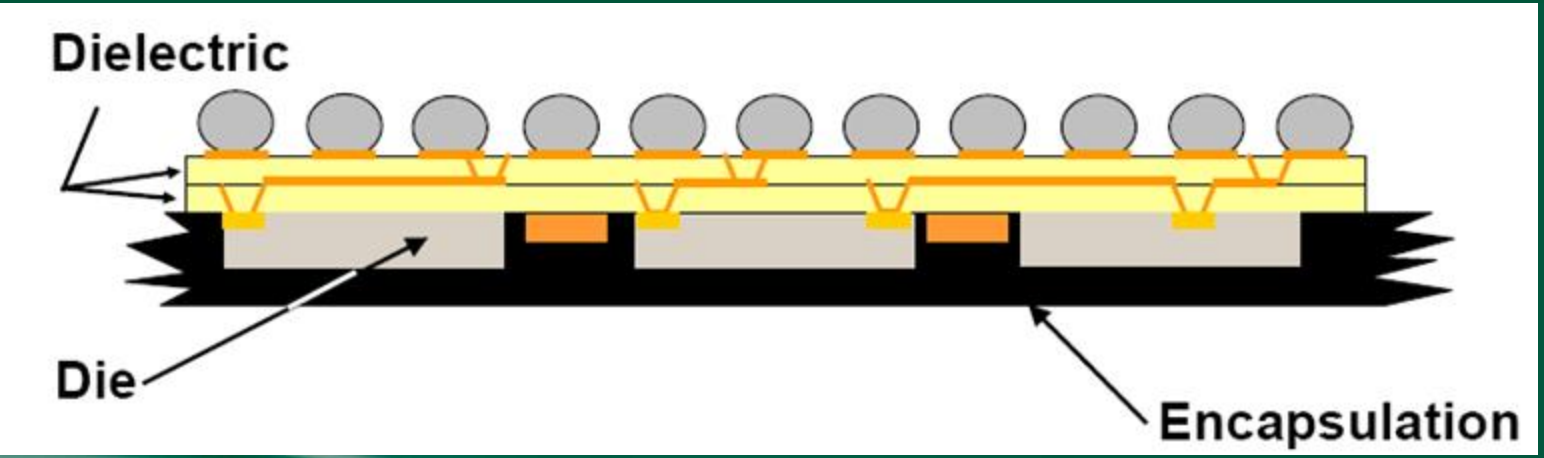
White Space Dilemma



White space is often filled with “non-value added circuitry”

New Interconnect Technologies

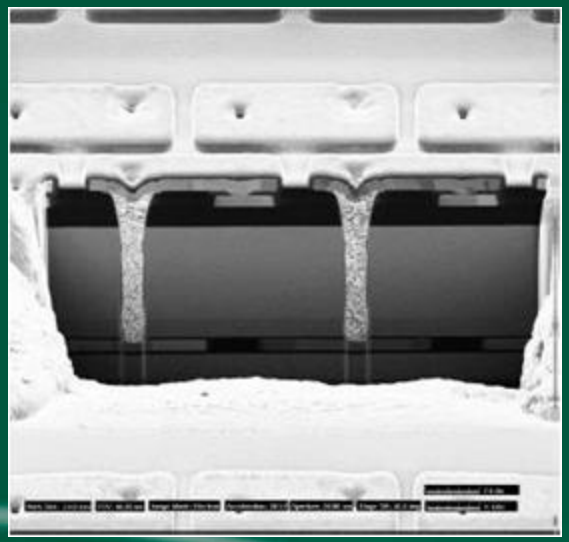
- Redistributed Chip Packaging (RCP)
  - Die connections are redistributed and brought to the outside as part of the package build
  - No pads needed on the die



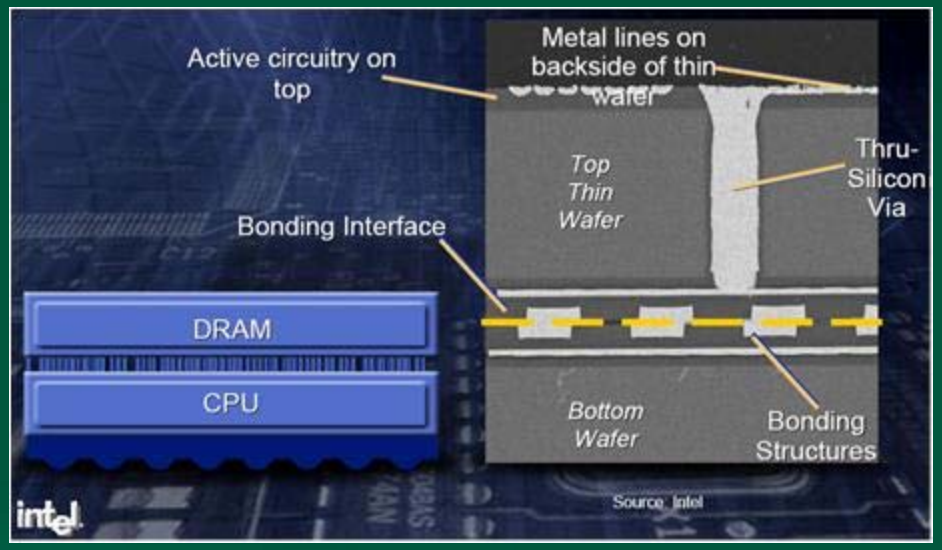
From : B. Keser
Freescale Semiconductor
2007 Freescale Technology Forum

New Interconnect Technologies

- Thru-Si vias
  - No need for pads
  - Stacked memories, Memory to processor



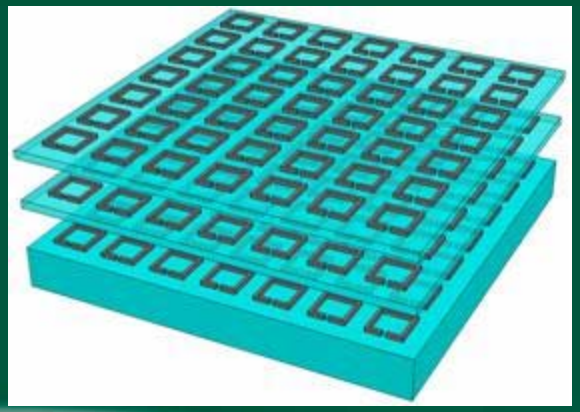
From : Fraunhofer Inst.
2005 RTI Conference



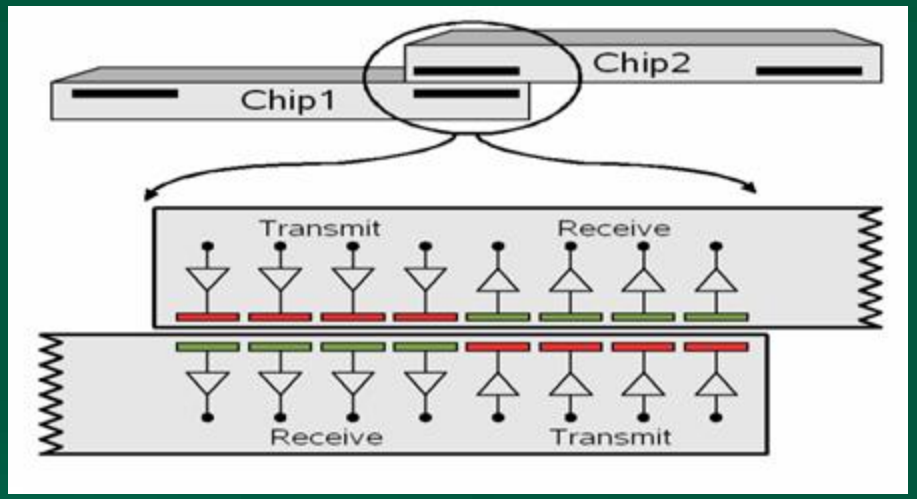
From : TM Mak
Intel
2005 Ga Tech 3S Workshop

New Interconnect Technologies

- Proximity Chip-to-Chip communications
  - No bond pads required
  - Capacitive, inductive and optical
  - Non-contact, very high speed chip-to-chip communications programs in development for I/O
    - Sun Microsystems, Intel, STMicro, HP, many others



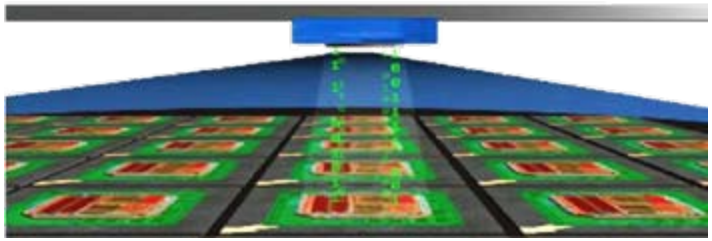
From : A. Fazzi; et.al.
ST Microsystems
2007 ISSCC

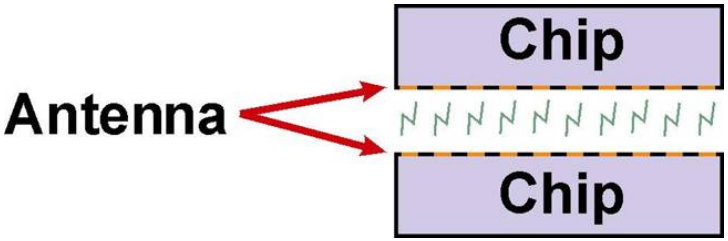


From : D. Hopkins; et al
Sun Microsystems
2007 ISSCC

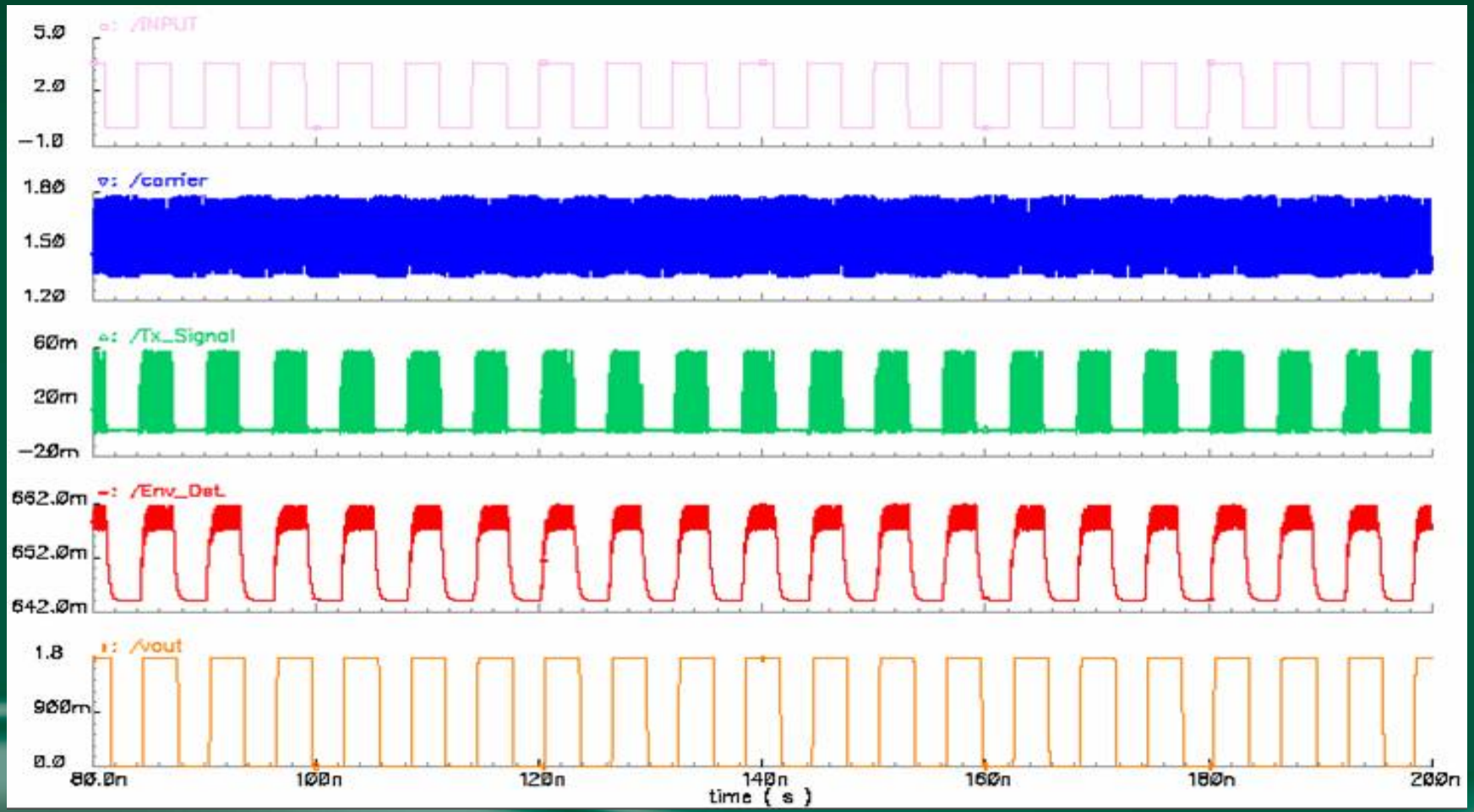
Non-contact Communication Technology

- Wireless, chip-scale communications
- Distances < 100 µm
- Pitch scales to < 20 µm
- Micro Tx/Rx on chip
- One Tx/Rx per I/O
- Fully CMOS compatible
- No impact on real-estate for most applications
- Excellent data integrity with low power
- Power transfer also possible



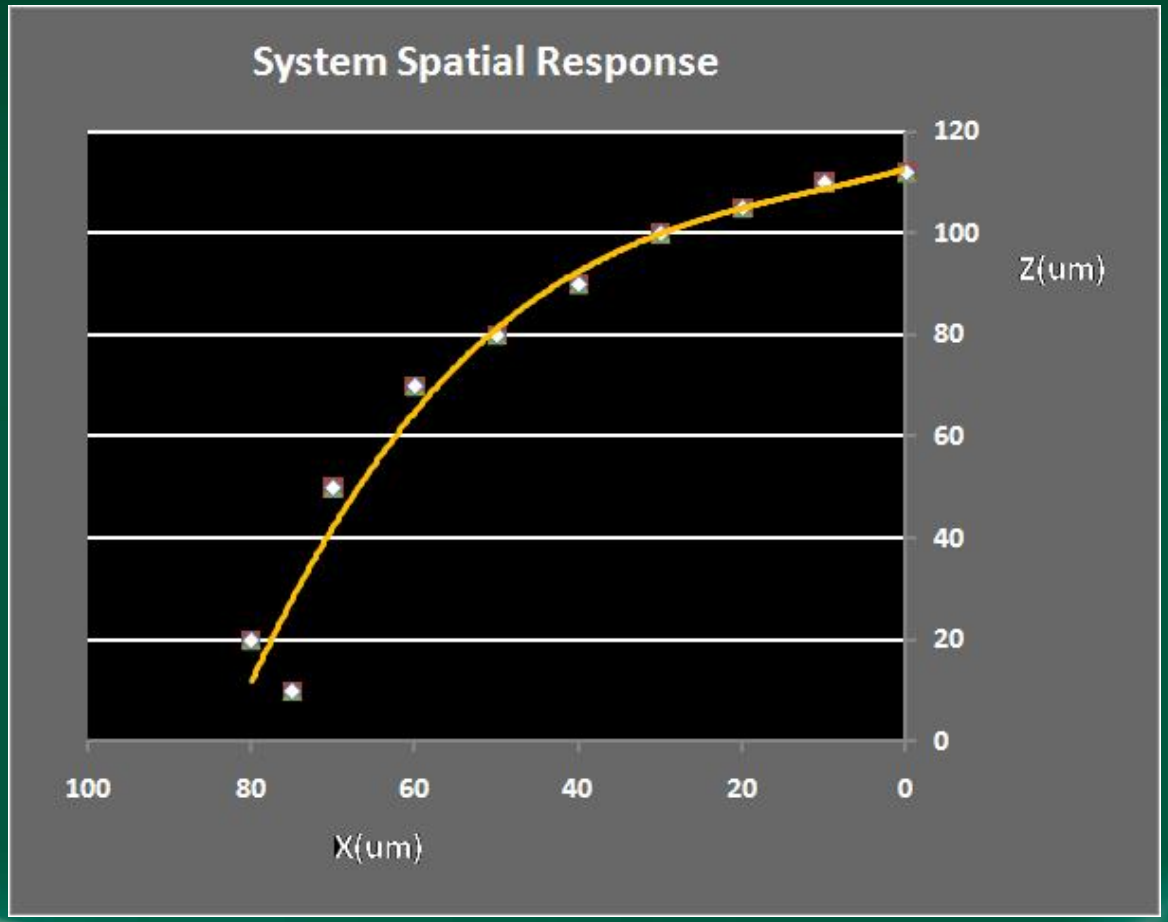


Signal Modeling



Alignment Tolerance

- Wide alignment tolerance
- 120um antennas
- Envelope of $<10^{-13}$ bit error rate

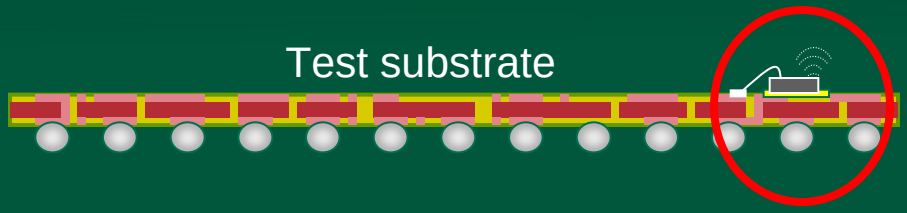


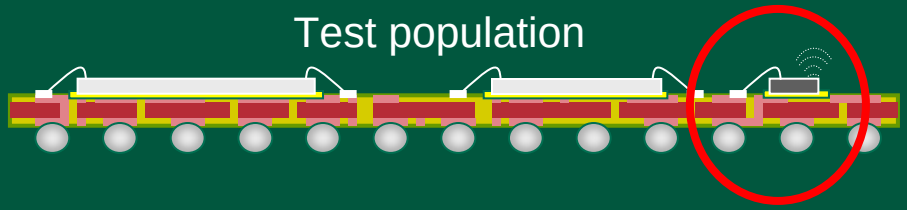
SiP Testing Application

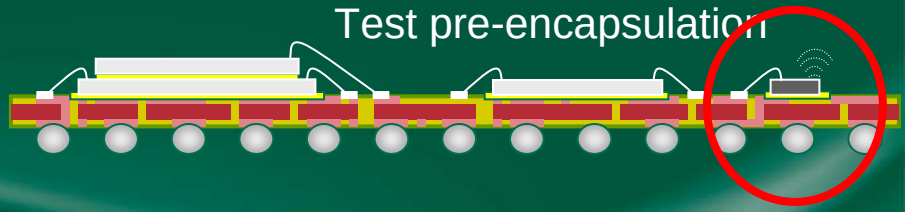
- Wireless Test Access Port (WiTAP™)
  - A chip with Scanimetrics' wireless transceivers designed to be integrated into the SiP/MCM
  - Allows testing of the SiP like a wafer during the assembly process
    - On a prober, with a probecard
- Enables more complex SiP devices
  - Lessens KGD requirements

SiP Testing Application

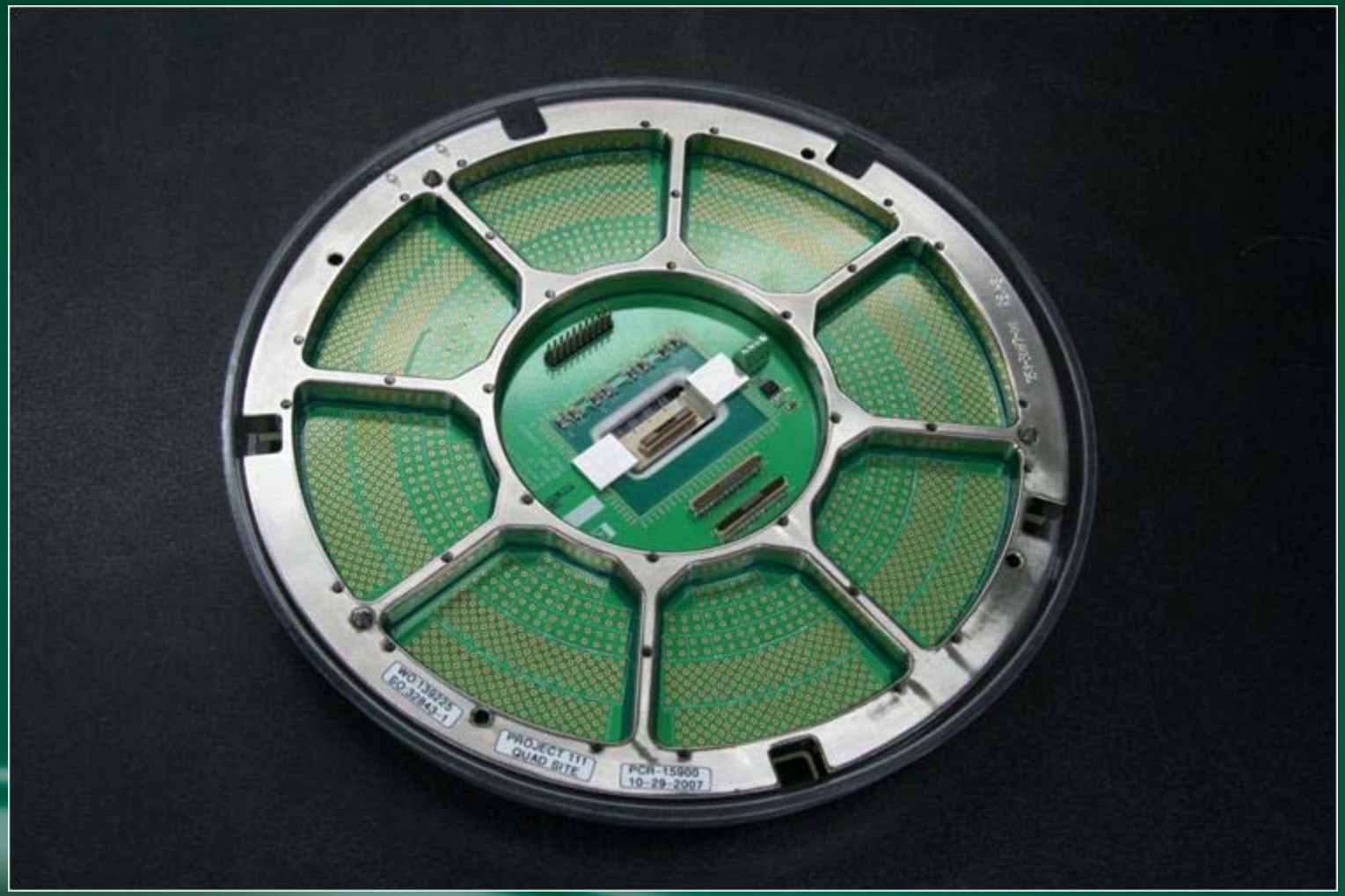
Can be Implemented as an independent chip populated on the SiP substrate or as an IP block embedded in other chips



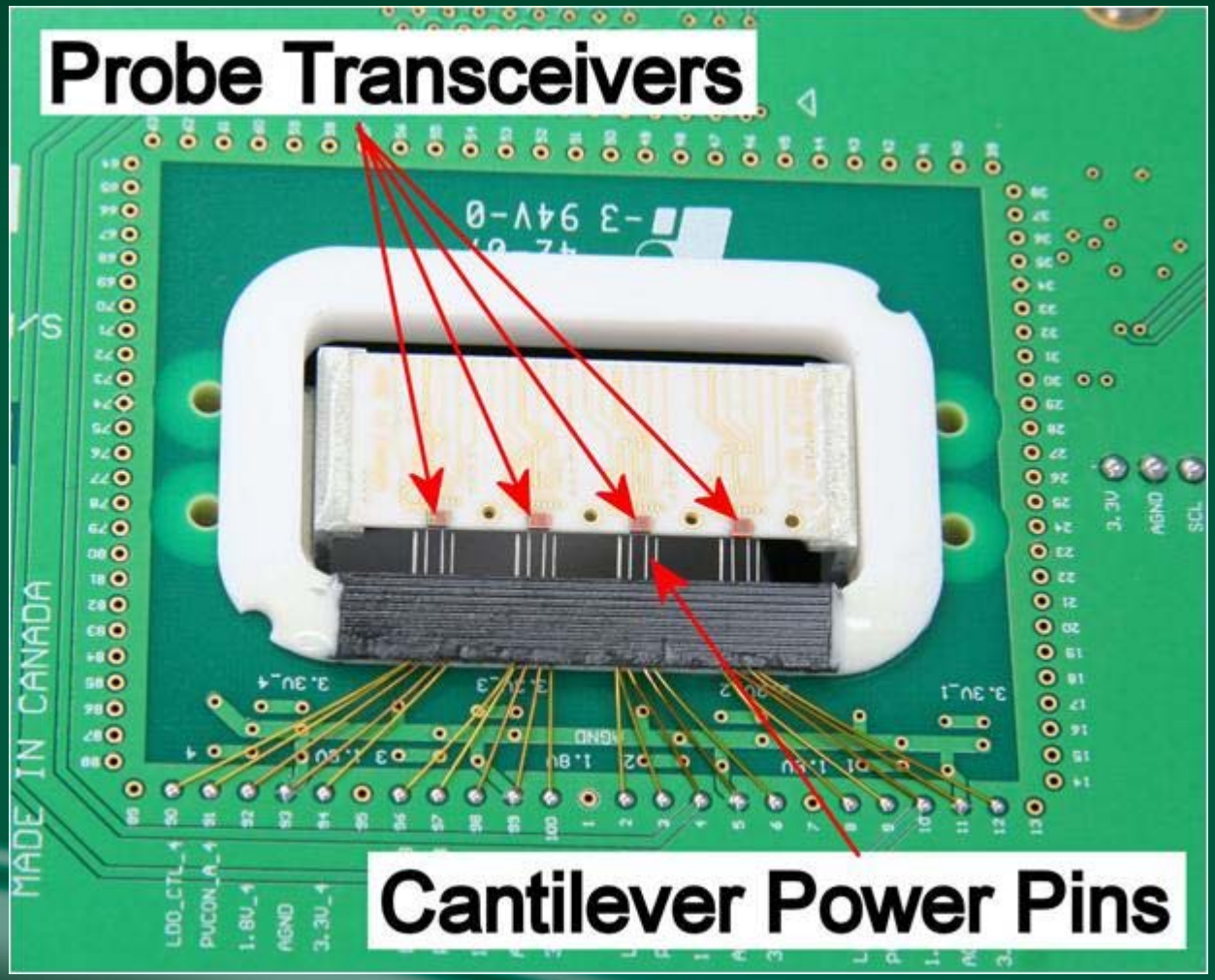




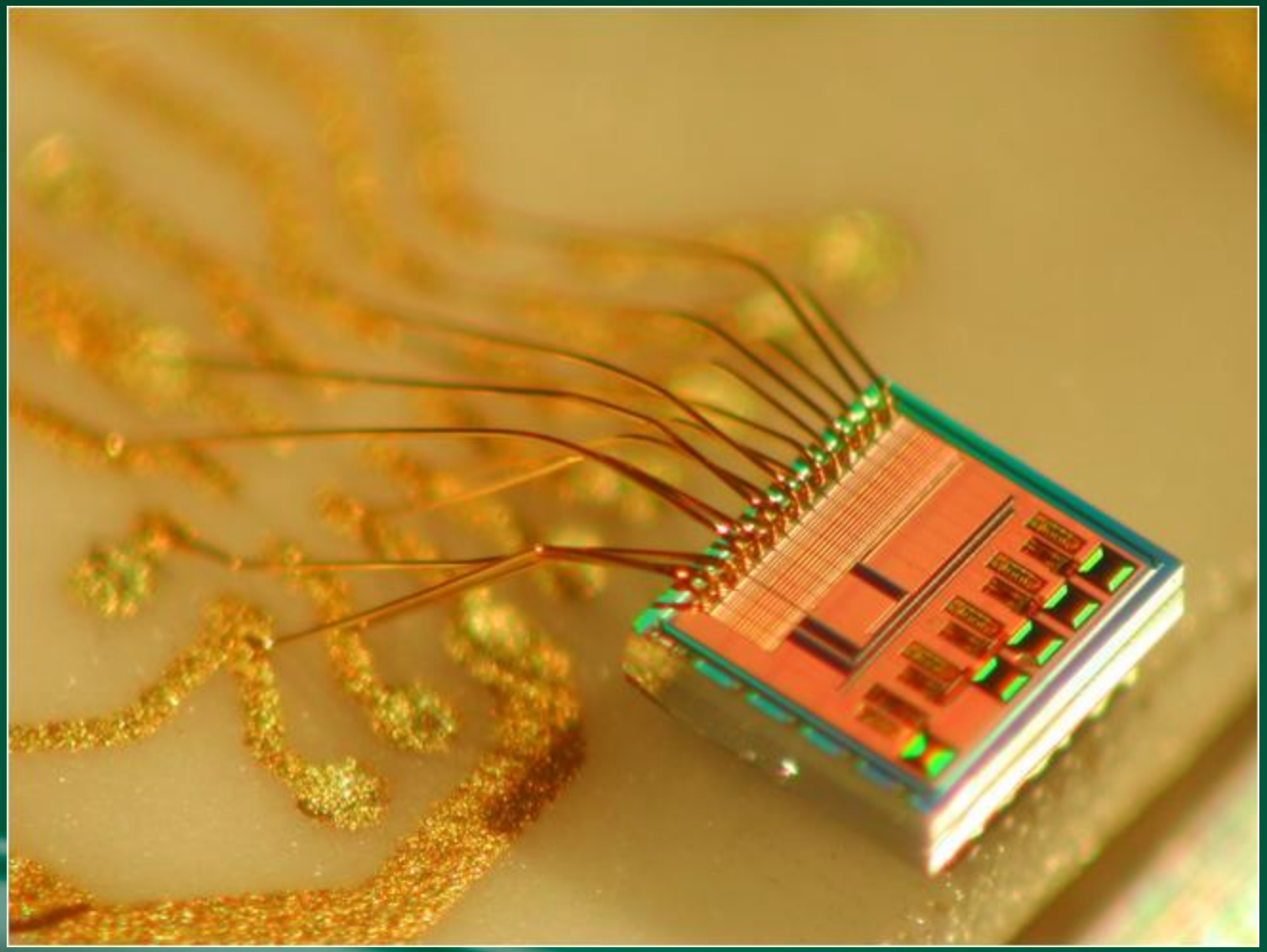
Probecard - Top View



Probecard – Bottom View

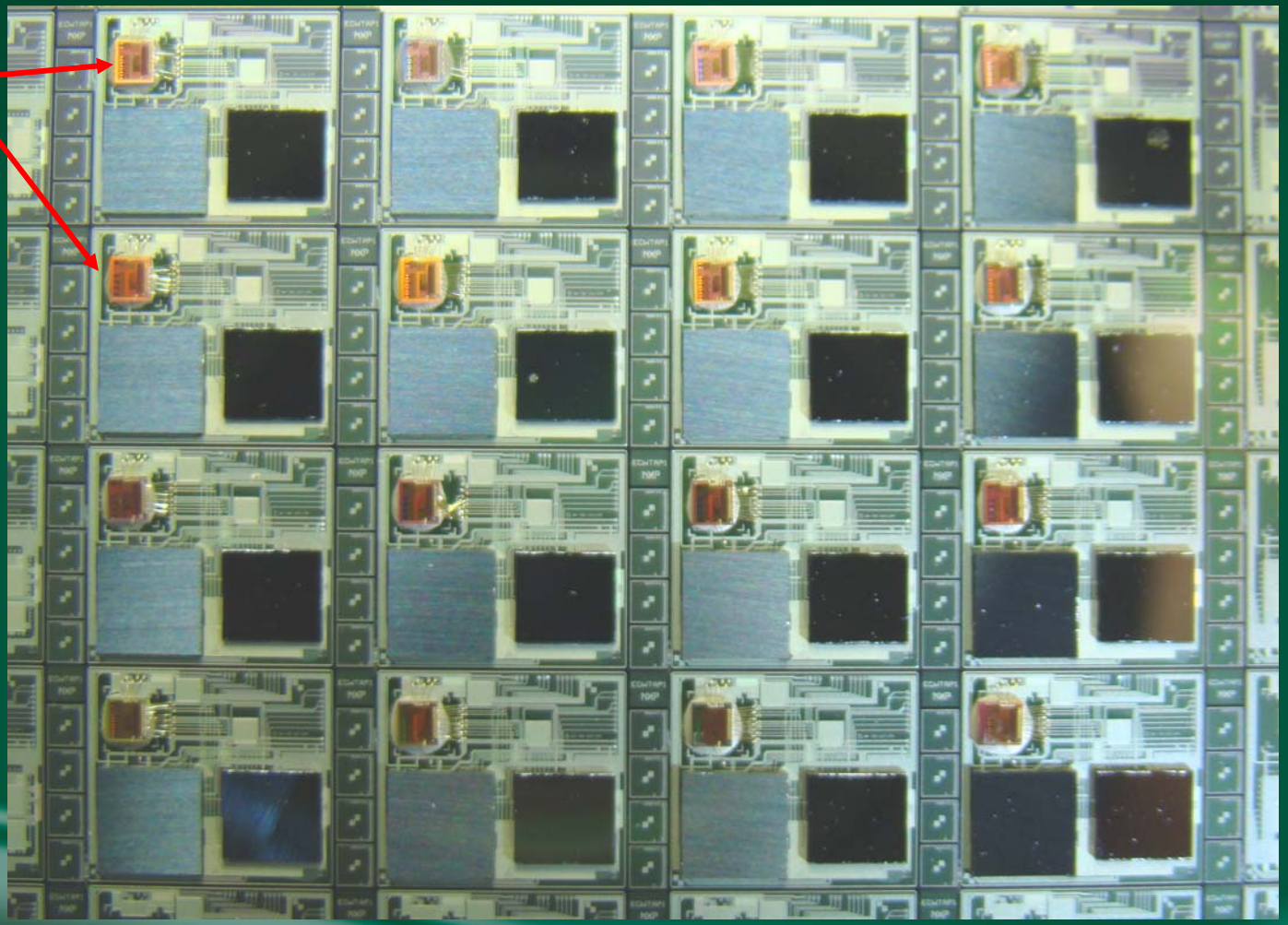


Single probe



Actual SiP Implementation

WiTAP™



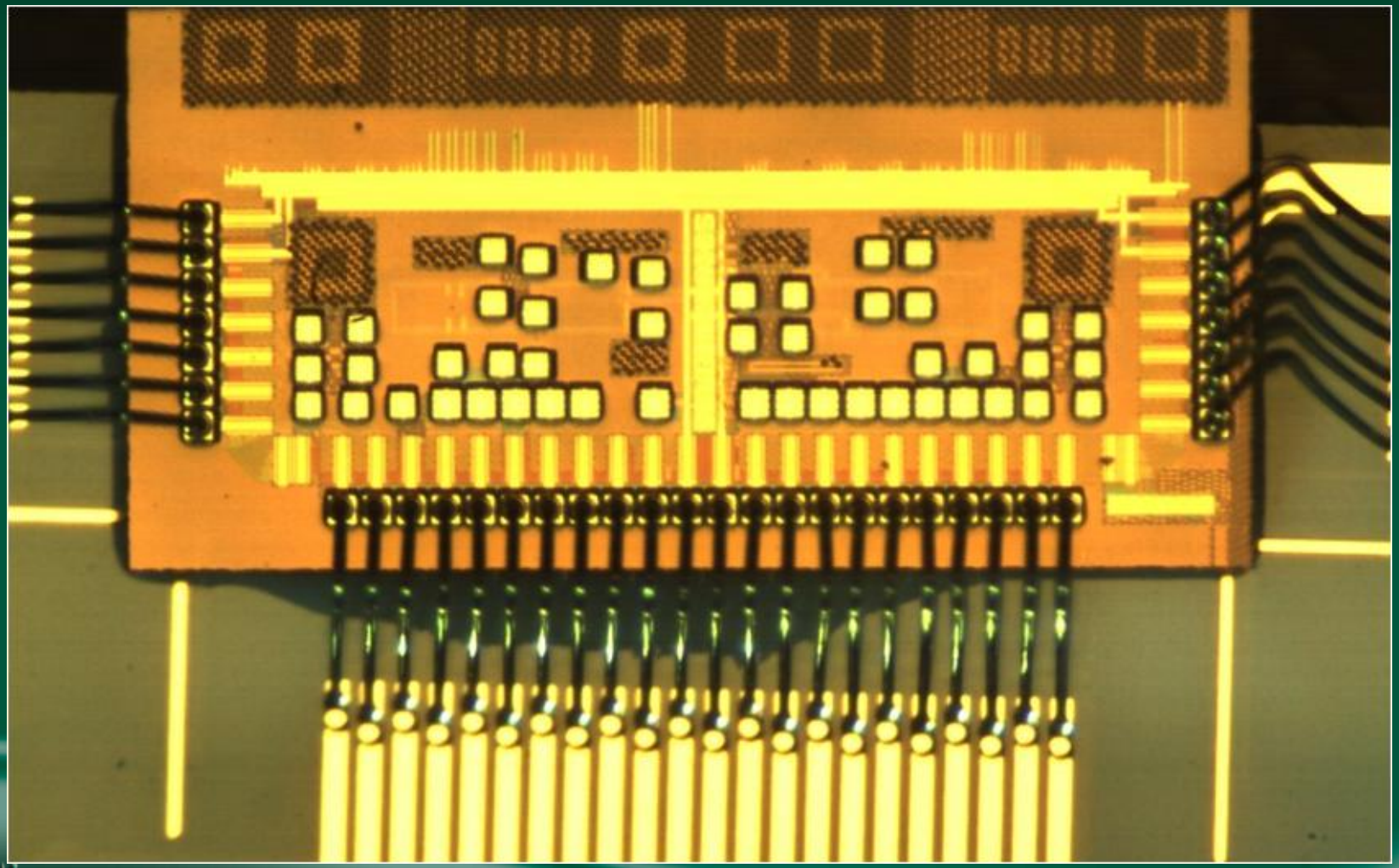
SiP Testing Summary

- Successfully run JTAG tests wirelessly on individual chips
  - Verigy (Agilent) 93k tester
  - EG4090 prober
- Built quad-site hybrid probe card
- Preparing for production qualification on customer's pilot line
- 16 chips in fabrication with enhancements and customer specific requirements

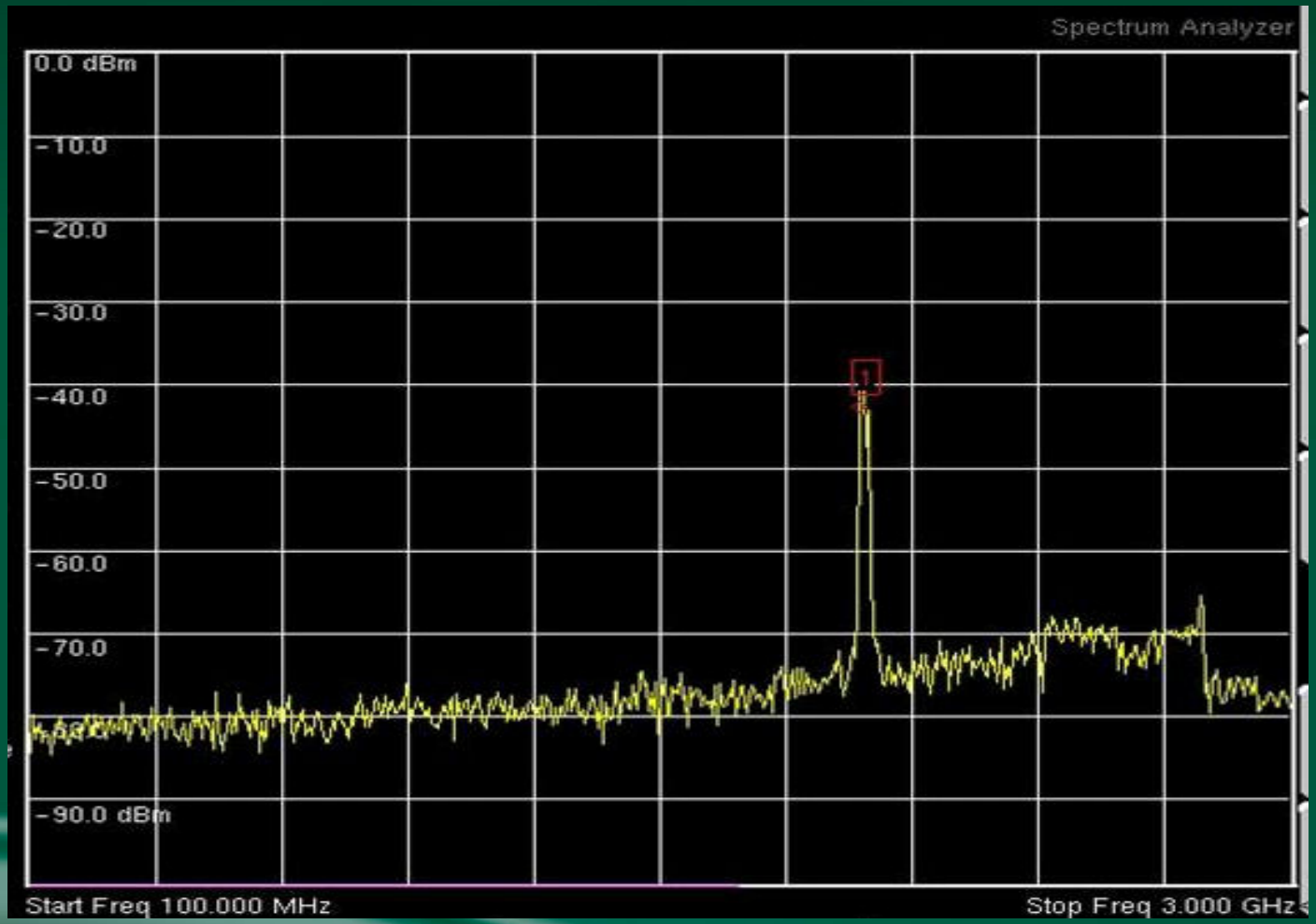
Wafer Probe Application

- Reduces contact force and scrubbing issues
- Probe pitch scales with process node
- Capability to work with new materials (low-k dielectrics)
- Interfaces can be tested at full functional speed at the wafer level (SerDes, DDR2, DDR3)
- Simpler mechanical designs
- Automatic alignment capability with lower alignment accuracy requirements
- Supports internal test points with no ESD protection requirements
- Compatible with existing equipment and processes

CMOS 45nm Test Chip



Micro-watt GHz Carriers



45nm Testing Summary

- Migrated technology to customer's 45 nm process
- Increased non-contact data rate capabilities > 1 Gbps
- Reduced pitch to 30 µm
- Reduced power consumption of transceiver circuits by 10x
- Integrating circuits into customer's I/O cells

Interconnect Application

- Test interface also used for chip-to-chip communication
- Transceiver IP block replaces bond pads, ESD structures and I/O drivers
- Capable of very high speed date rates (multi Gbps)
- Lower power consumption

Play Animation

Summary

- New testing techniques are required for advanced process nodes
- New testing techniques are required for new chip-to-chip interconnect methods
- Robust data transfer of wireless channels demonstrated at 45 nm node
- Non-contact wafer test products can be used in SiP and chip-to-chip interconnect applications as well

Thanks

- Contact the Scanimetrics team with any questions …

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