IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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Design for Probe

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TEXAS INSTRUMENTS

Agenda

- Why Design for Probe

- Die Design to First Touchdown

- What to Ask

- The Rules

- Summary

Why Design for Probe

- Avoid probe card mis-builds and lost cycle time

- Increased multisite at probe

- Optimize bump/pad layout for specific probe card technology

- Faster release to Production and ramp to volume

From Design to Probe

- Multi-phase design reviews must start as soon as possible in the die design cycle
- Early enough to influence pad layout; size, pitch, placement, …
- Rules in place to guide die design
- Close collaboration between die designers and probe card suppliers

From Design to Probe

- Design for Probe part of the Design in Excellence process
- Added 1 year ago to compliment…
  - Design for Test
  - Power Management
  - Packaging
  - Memory…
- In use by Wireless Products, Automotive, ASIC, DSP
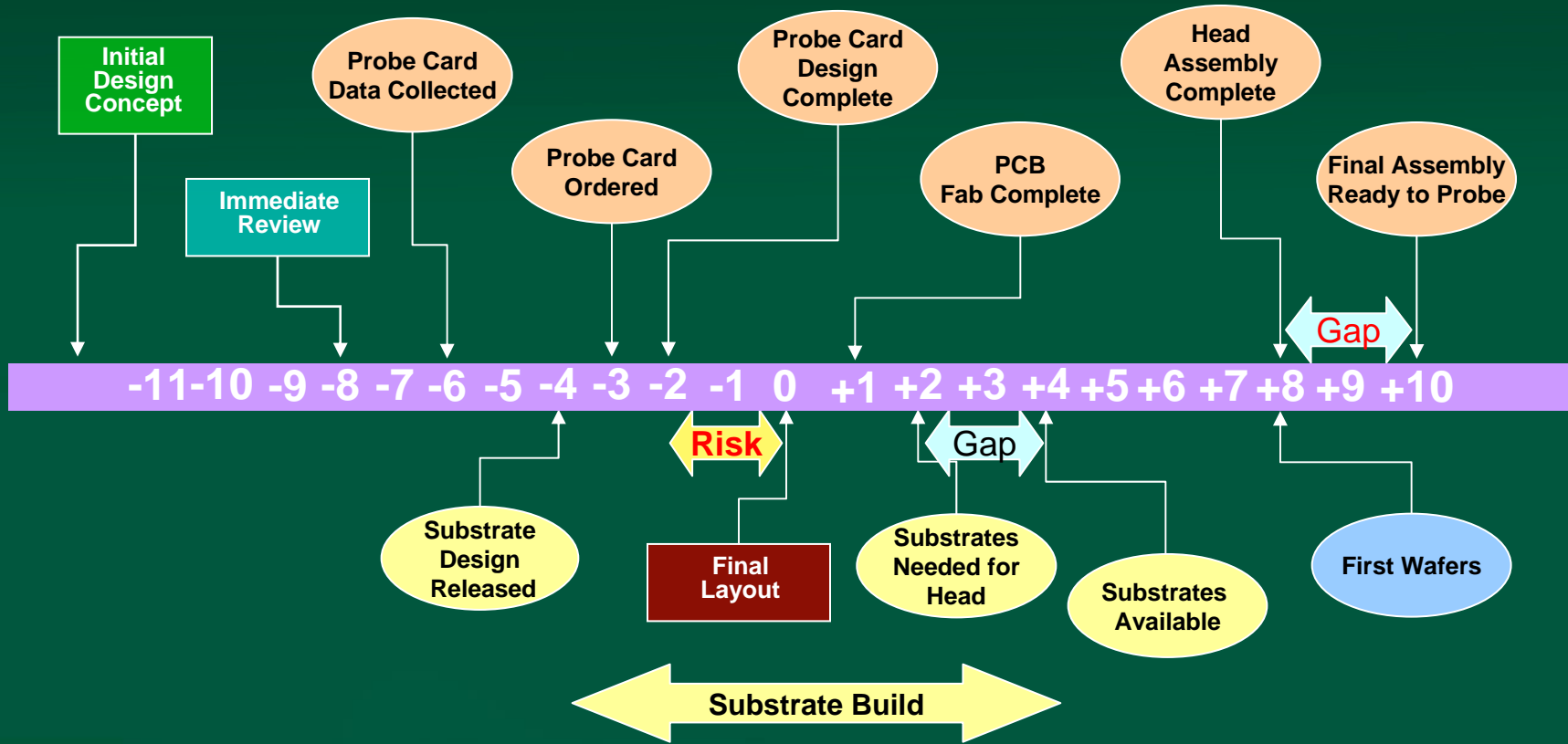
The Design Cycle

- Multi-phase reviews
  - Initial Design Concept
    - Targeted PC technology
  - Intermediate Review
    - Initial probe card design assessment
  - Final Layout Approval
    - Finalize probe card design and submit order
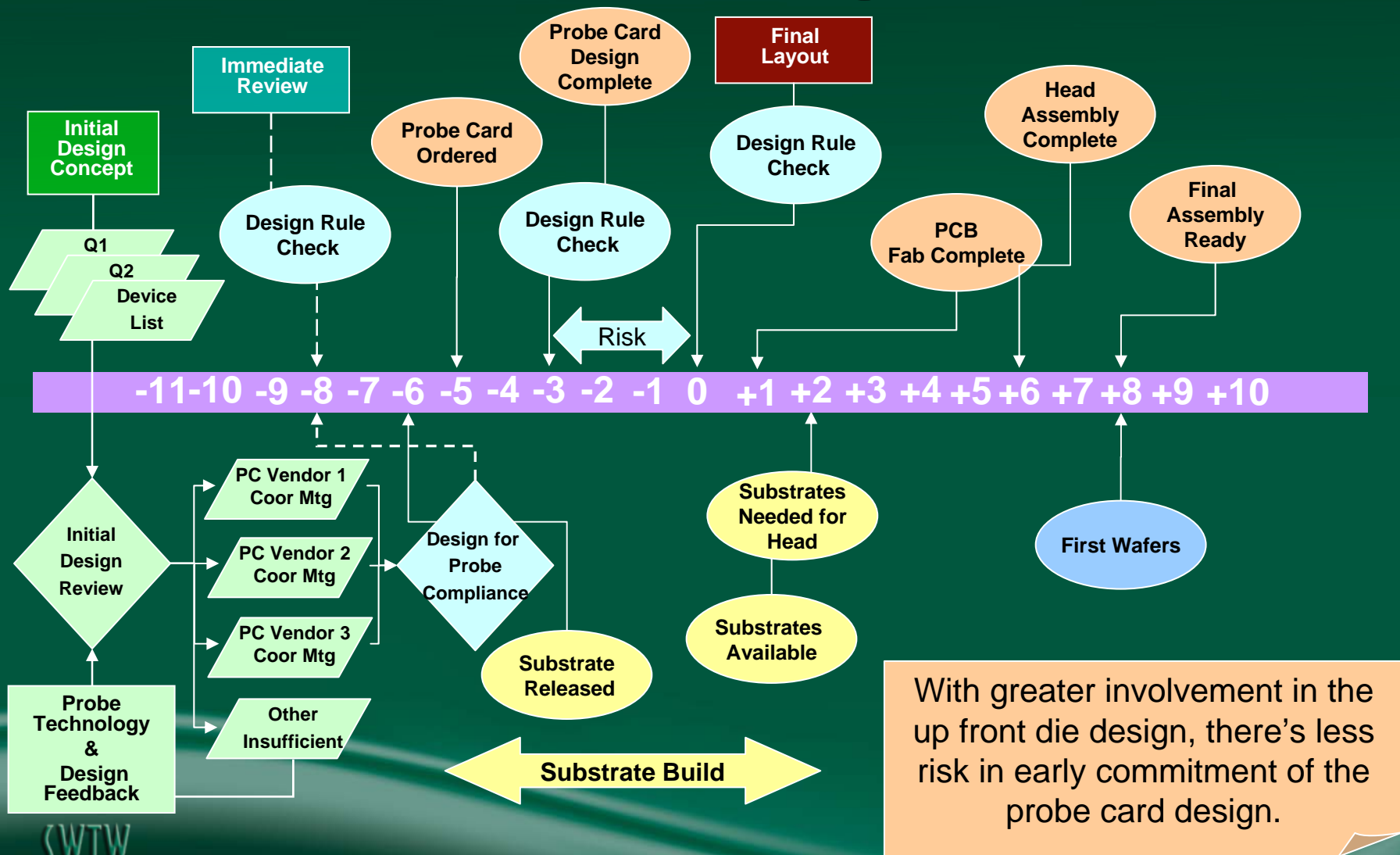 - Probe card delivery intercepts first silicon
  - Work right the first time

The Old Design Cycle

Substrates were needed for Probe Card generation 2-weeks before they're available.

The New Design Cycle

With greater involvement in the up front die design, there's less risk in early commitment of the probe card design.

What to Ask

- Minimum Pitch
- Pad Size
- No. Pads/Bump per Die
- Multisite Target
- Maximum No. Probes
- No. Probe Insertions
- Allowable PM Damage
- Core Pads/Bumps

- Temperature
- Inline vs. Staggered
- Maximum Test Freq.
- Volume of Material
- Pad/Bump Metallurgy
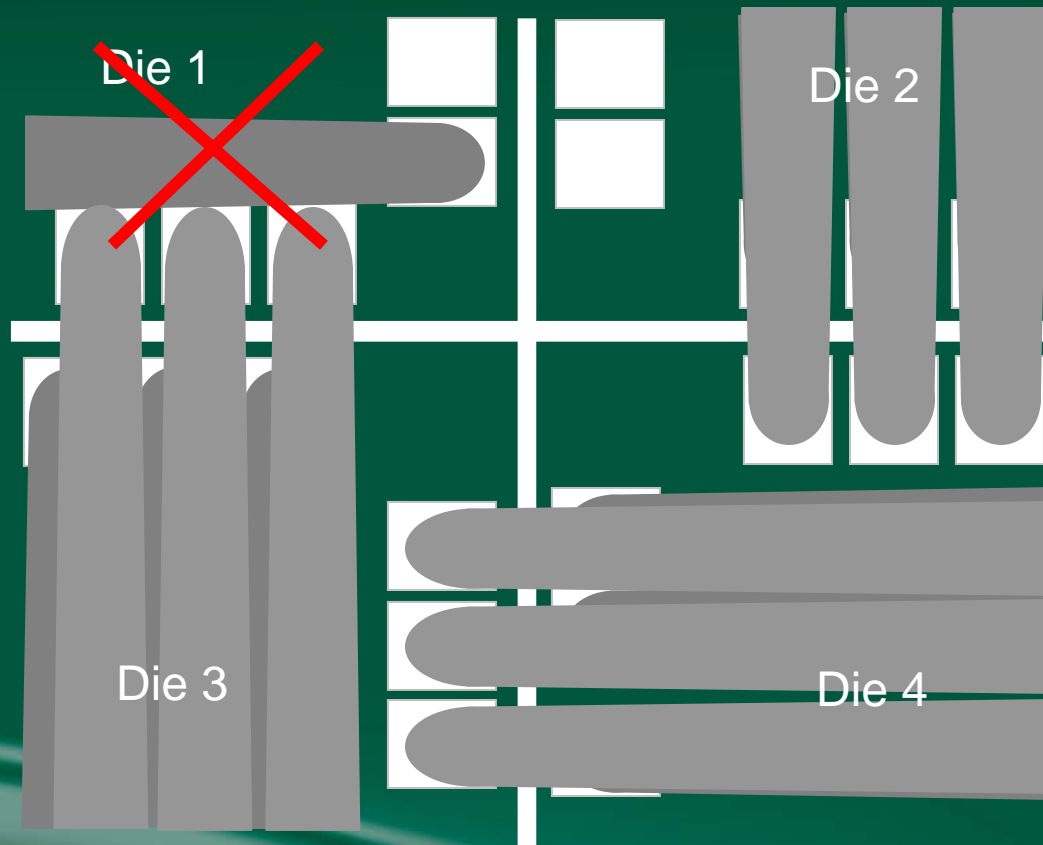- Pad/Bump Underlayment
- Date Needed

The Rules

- Design Rules written for Die Designers
  - Assume nothing
  - Detailed single use rules
  - Include illustrations
- Design Rules specific to Probe Technology
  - Close collaboration with vendors
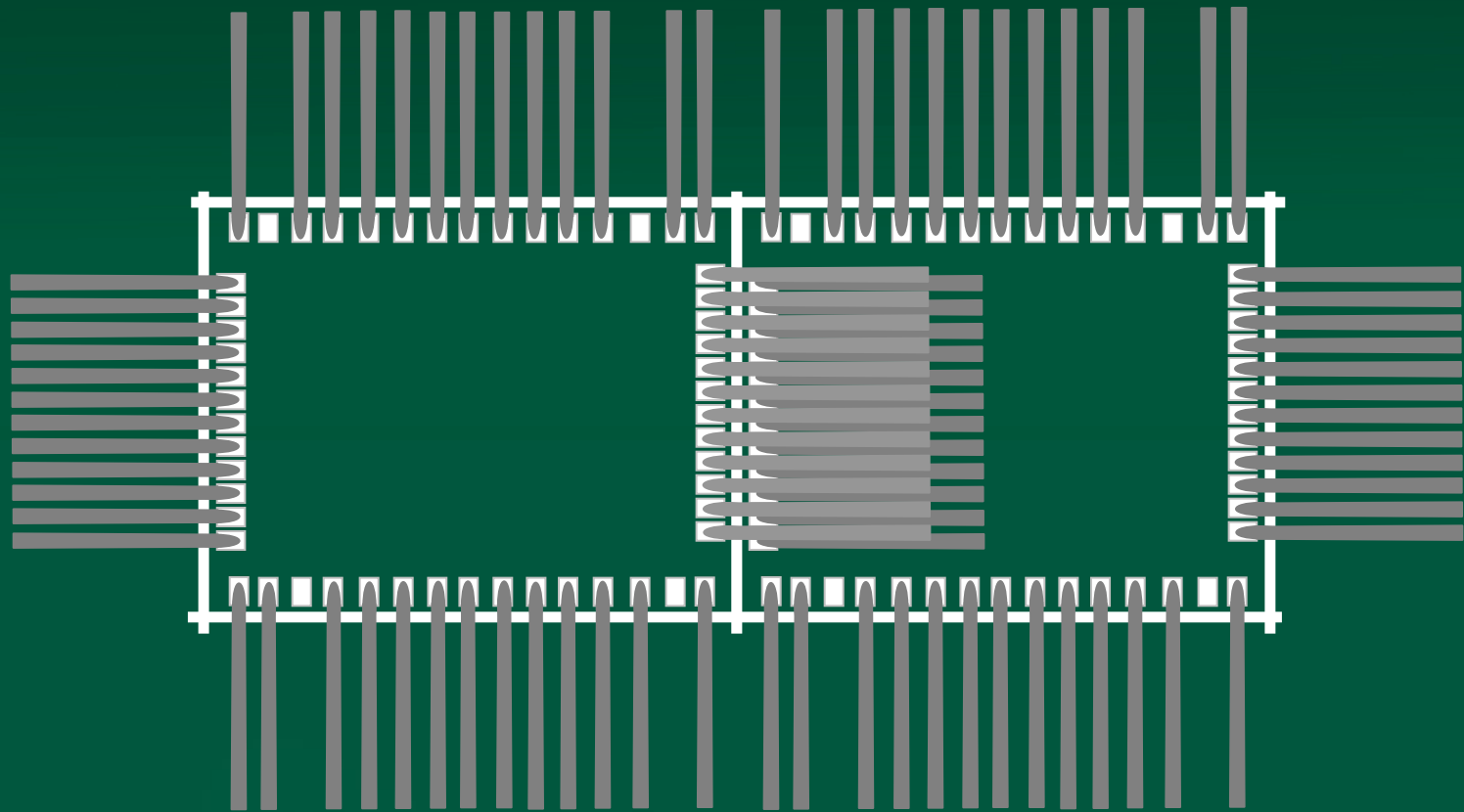- Design Rules independent of Si Node
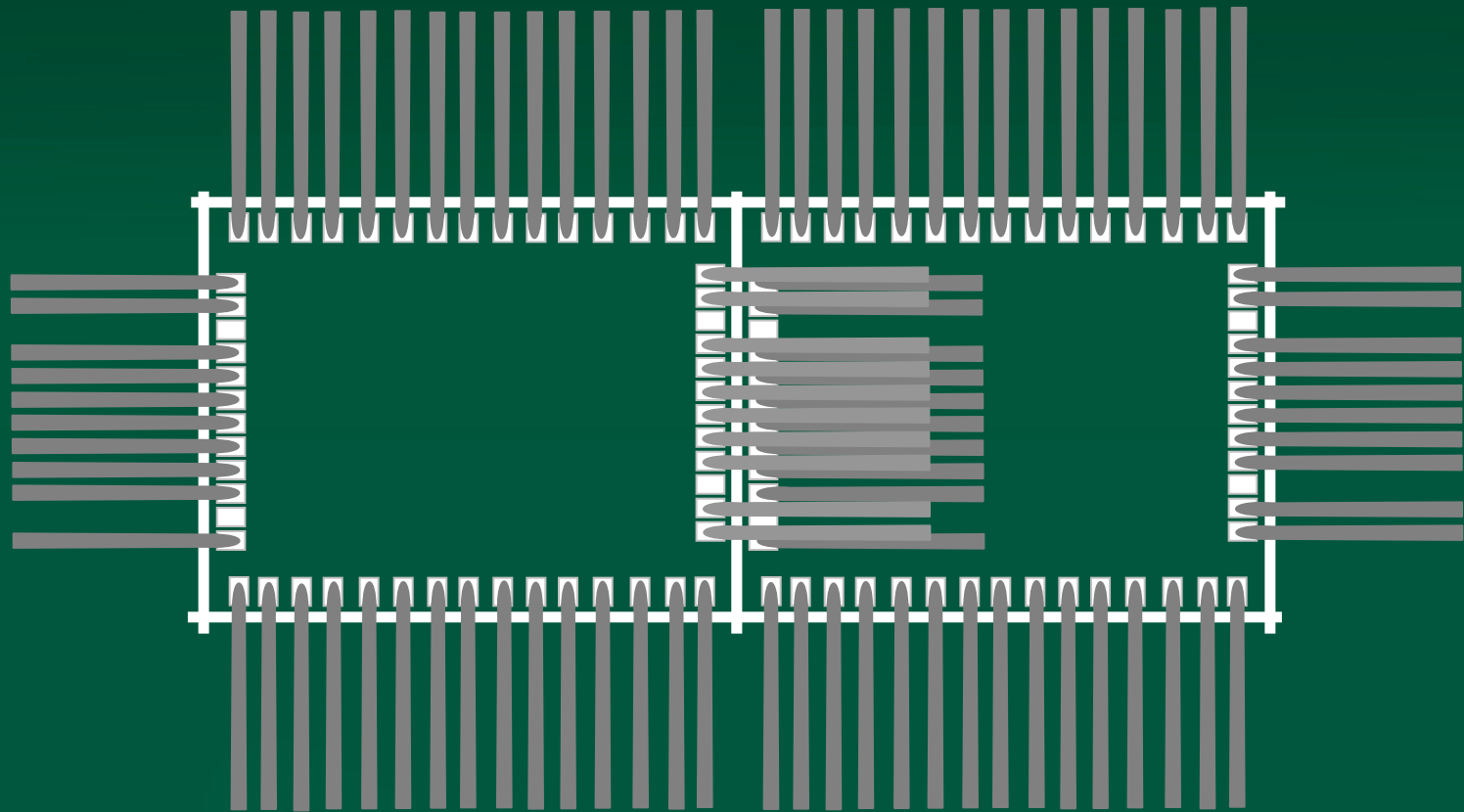
The Rules - Cantilever
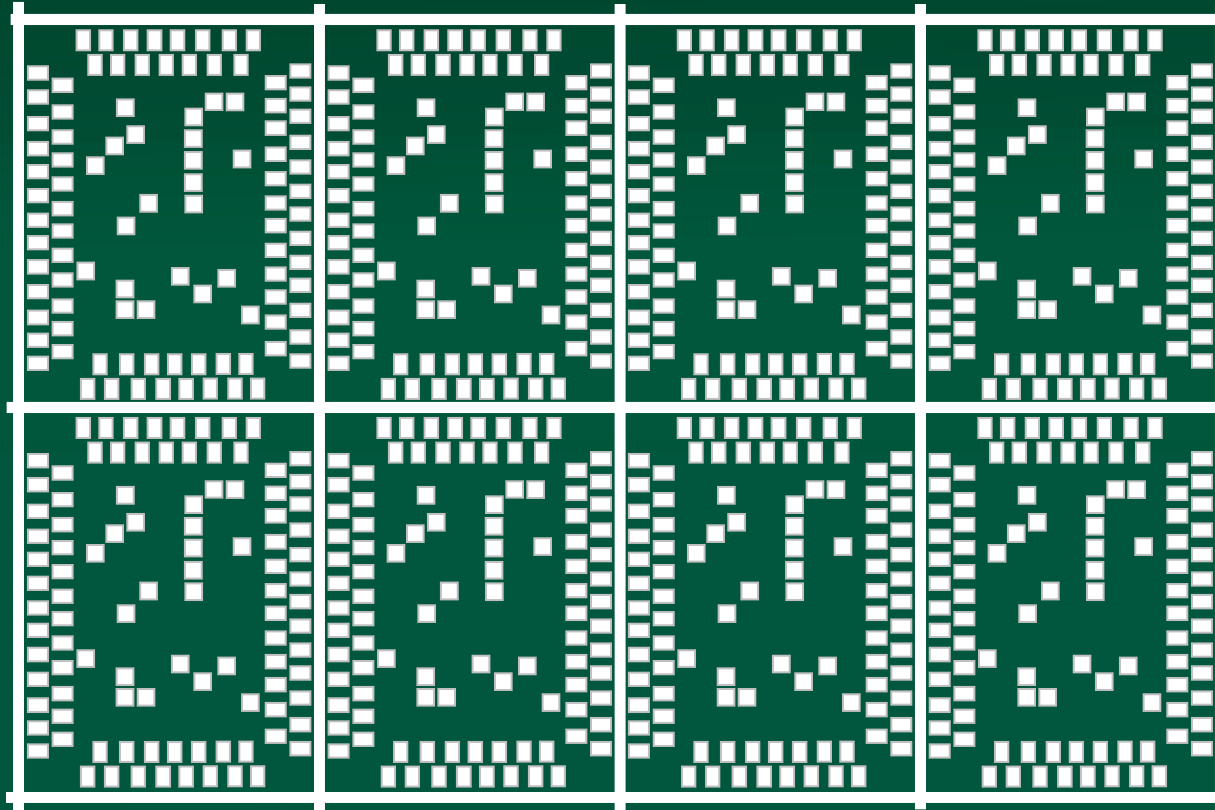
- Cantilever Corner Spacing for Multisite

Die 1

Die 2

Die 3

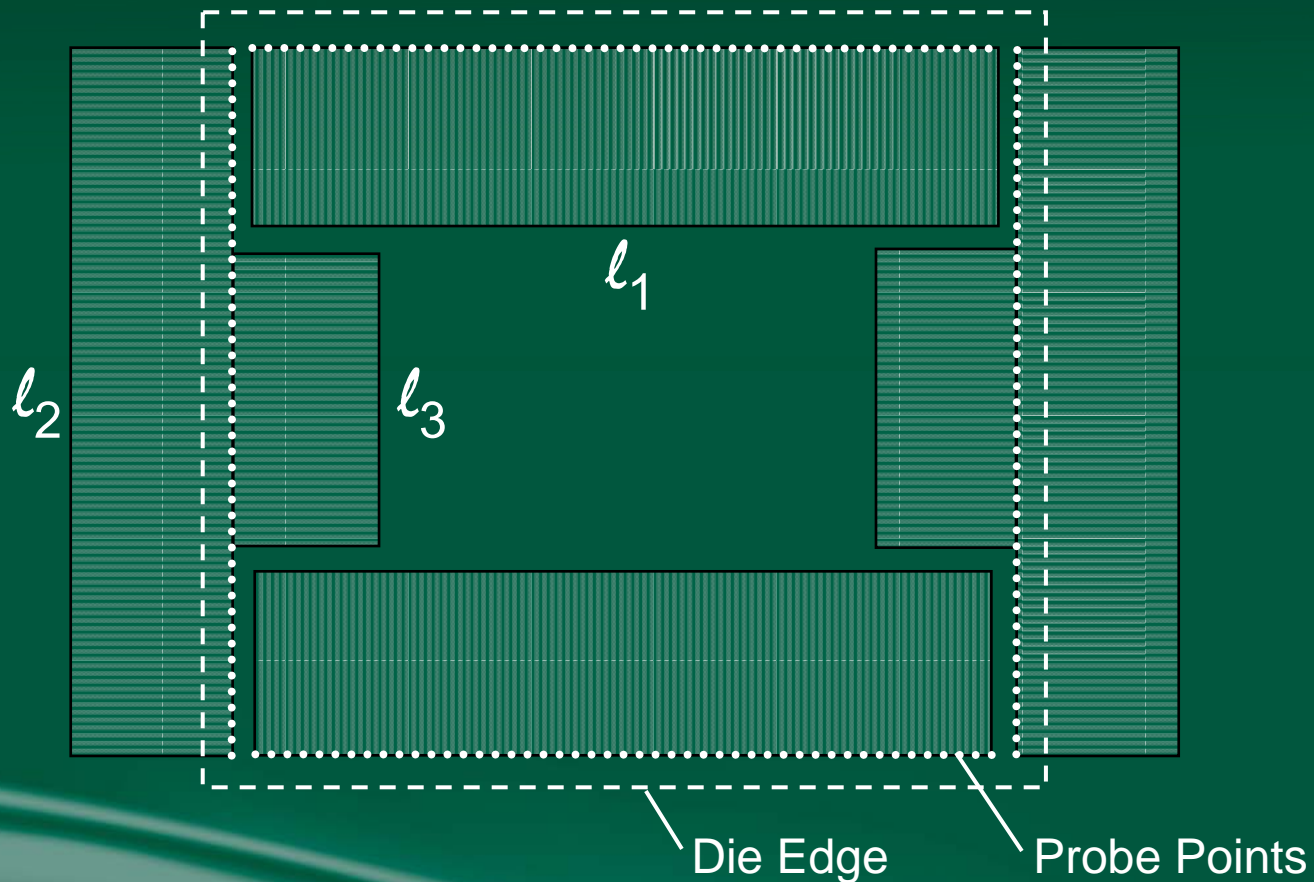Die 4

The Rules - Cantilever

The Rules - Cantilever

The Rules - VPC

The Rules – µCantilever or MEM

Number Probes - $\ell_1/\mu C_{pitch}$ or Number Probes – $(\ell_2+\ell_3)/\mu C_{pitch}$

ℓ_1

ℓ_2

ℓ_3

Die Edge

Probe Points

Summary

- A Design Review process is a must to control the release of material moving to the Probe Floor
  - Must be early and often
- Rules designed for specific probe card technology, not Si
- Careful attention to the layout of the pads/bumps can enable increased multisite test and…
- Allow the use of advanced probe card technologies that would be constrained using standard layout rules
- Close collaboration between die designers and PC vendors to insure optimal layout and on time delivery

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