IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Accelerating CAD design of Probe Cards using Allegro System Architect

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cadence

Topics

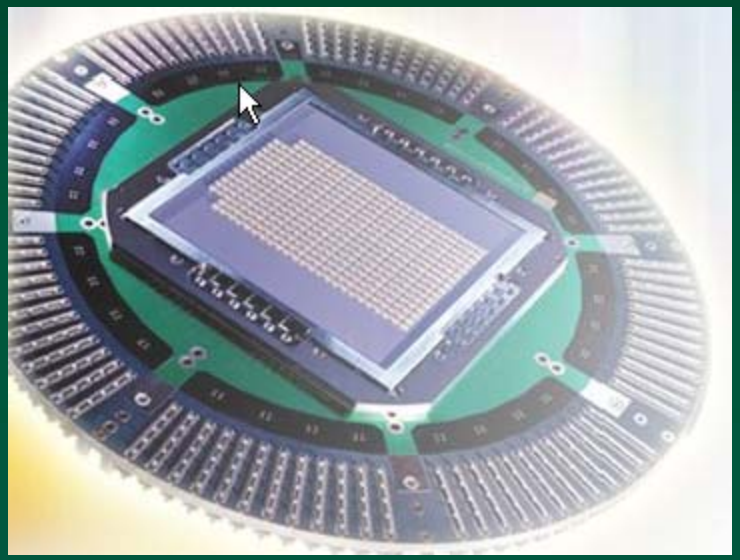
- About this paper
- Background
- Desired Goals
- How Allegro System Architect is different
- Results
  - Strengths/ Weaknesses
- Summary / Conclusion
- Follow-up

About this Paper

- Target Audience
  - Designers / Managers / Influencers associated with design of probe cards
- What is in it for you
  - knowledge about a solution which can accelerate design of probe cards significantly

Background

- Probe cards
  - Test multiple identical devices
  - More constraints
  - Larger sizes
  - Handling component changes

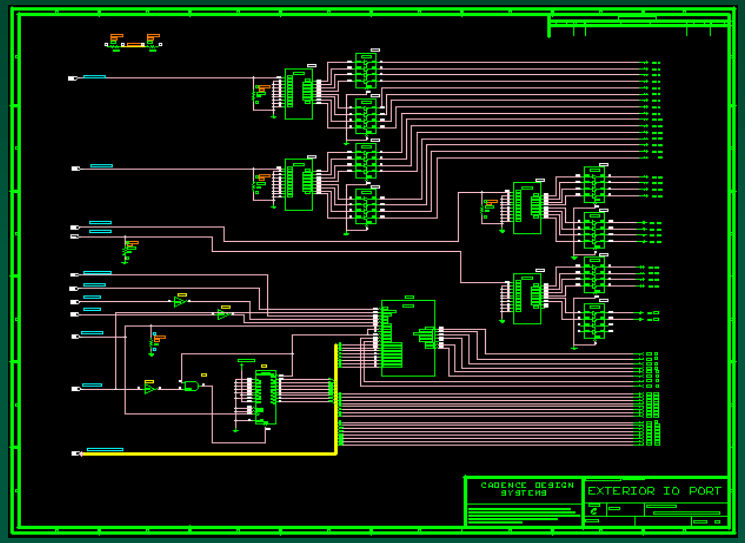


Key Design Challenges

- Symmetry
  - The devices are identical
    - But instances and nets need to be named uniquely – following a pattern
- Constraints
    - Matched delays for groups/buses
    - Total delay constraints
    - Differential pairs
    - Terminations

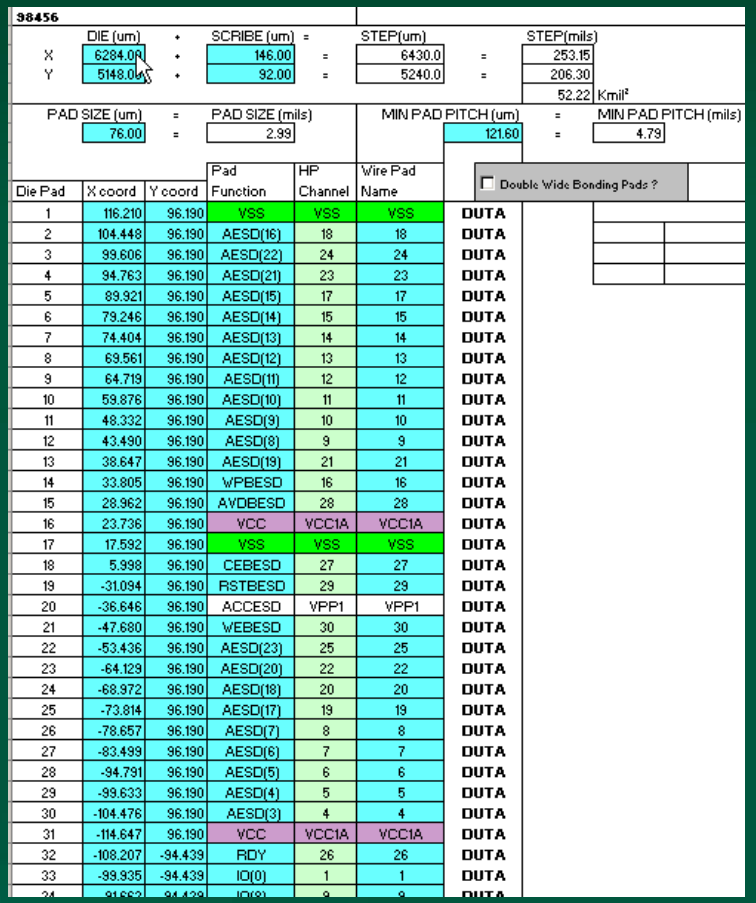
Current Solutions (1)

- Schematic based solutions
  - Easily understandable for small designs
- Problems
  - Difficult to scale for size / number
  - Time consuming top create
  - Handling change is tedious
  - Connectivity is “layout driven”; not just logic driven



Current Solutions (2)

- Custom Excel based solutions
  - Quick and Customized
- Problems
  - Need maintenance
  - Typically handle only netlists – no constraints
  - can't handle change



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	DIE (um)		SCRIBE (um)		STEP(um)		STEP(mils)
X	6284.00	+	146.00	=	6430.0	=	253.15
Y	5148.00	+	92.00	=	5240.0	=	206.30
							52.22 Kmil²

PAD SIZE (um)	=	PAD SIZE (mils)	MIN PAD PITCH (um)	=	MIN PAD PITCH (mils)
76.00	=	2.99	121.60	=	4.79

Double Wide Bonding Pads ?

Die Pad	X coord	Y coord	Pad Function	HP Channel	Wire Pad Name	
1	116.210	96.190	VSS	VSS	VSS	DUTA
2	104.448	96.190	AESD(16)	18	18	DUTA
3	99.606	96.190	AESD(22)	24	24	DUTA
4	94.763	96.190	AESD(21)	23	23	DUTA
5	89.921	96.190	AESD(15)	17	17	DUTA
6	79.246	96.190	AESD(14)	15	15	DUTA
7	74.404	96.190	AESD(13)	14	14	DUTA
8	69.561	96.190	AESD(12)	13	13	DUTA
9	64.719	96.190	AESD(11)	12	12	DUTA
10	59.876	96.190	AESD(10)	11	11	DUTA
11	48.332	96.190	AESD(9)	10	10	DUTA
12	43.490	96.190	AESD(8)	9	9	DUTA
13	38.647	96.190	AESD(19)	21	21	DUTA
14	33.805	96.190	WPBESD	16	16	DUTA
15	28.962	96.190	AVDBESD	28	28	DUTA
16	23.736	96.190	VCC	VCC1A	VCC1A	DUTA
17	17.592	96.190	VSS	VSS	VSS	DUTA
18	5.998	96.190	CEBESD	27	27	DUTA
19	-31.094	96.190	RSTBESD	29	29	DUTA
20	-36.646	96.190	ACCESD	VPP1	VPP1	DUTA
21	-47.680	96.190	WEBESD	30	30	DUTA
22	-53.436	96.190	AESD(23)	25	25	DUTA
23	-64.129	96.190	AESD(20)	22	22	DUTA
24	-68.972	96.190	AESD(18)	20	20	DUTA
25	-73.814	96.190	AESD(17)	19	19	DUTA
26	-78.657	96.190	AESD(7)	8	8	DUTA
27	-83.499	96.190	AESD(6)	7	7	DUTA
28	-94.791	96.190	AESD(5)	6	6	DUTA
29	-99.633	96.190	AESD(4)	5	5	DUTA
30	-104.476	96.190	AESD(3)	4	4	DUTA
31	-114.647	96.190	VCC	VCC1A	VCC1A	DUTA
32	-108.207	-94.439	RDY	26	26	DUTA
33	-99.935	-94.439	IO(0)	1	1	DUTA

The underlying problem

Why do current solutions break

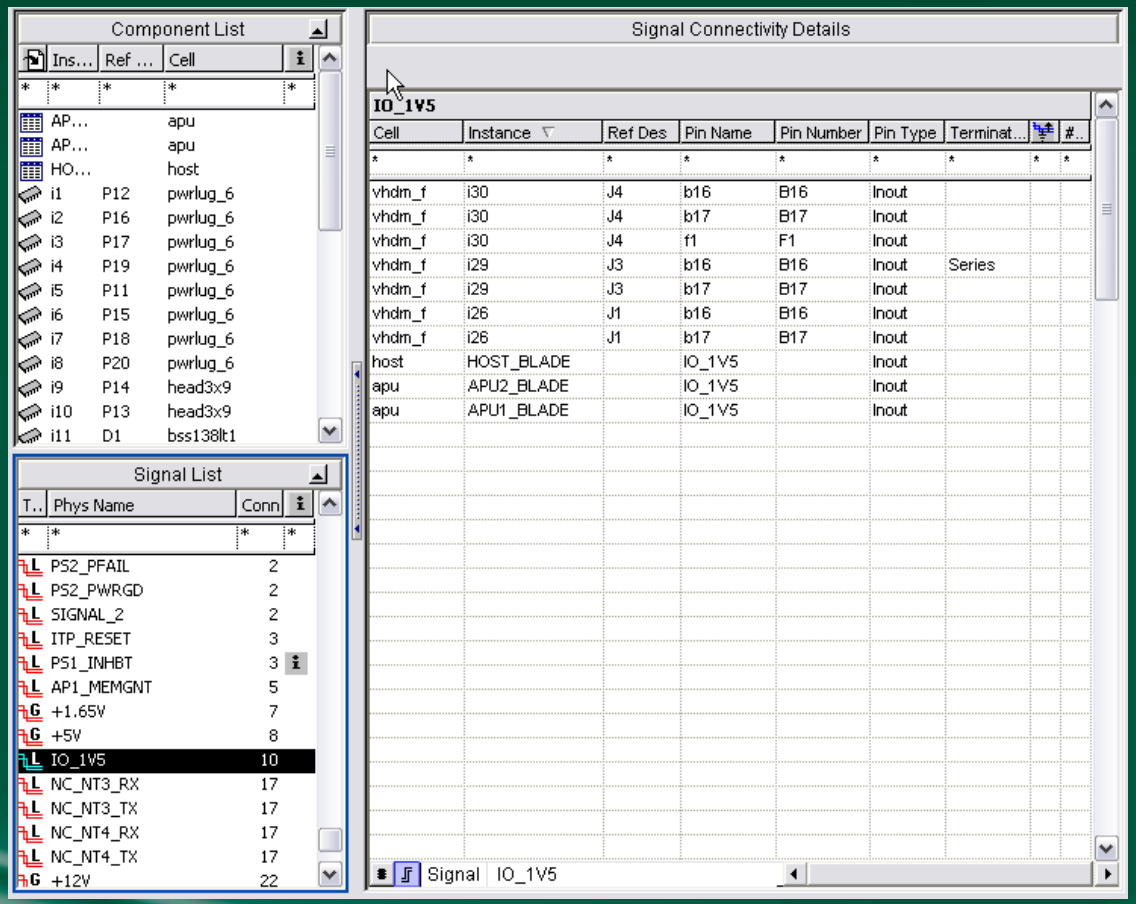
- A large amount of data is being manipulated
- Can’t handle patterns or replication natively
- Graphics based netlisters – but graphics dont add value
- connectivity is driven – back to front!

Spreadsheet Editor for design creation

Spreadsheet Editor for connectivity

Key Components

1. Component and Signals in tabular / spreadsheet like views



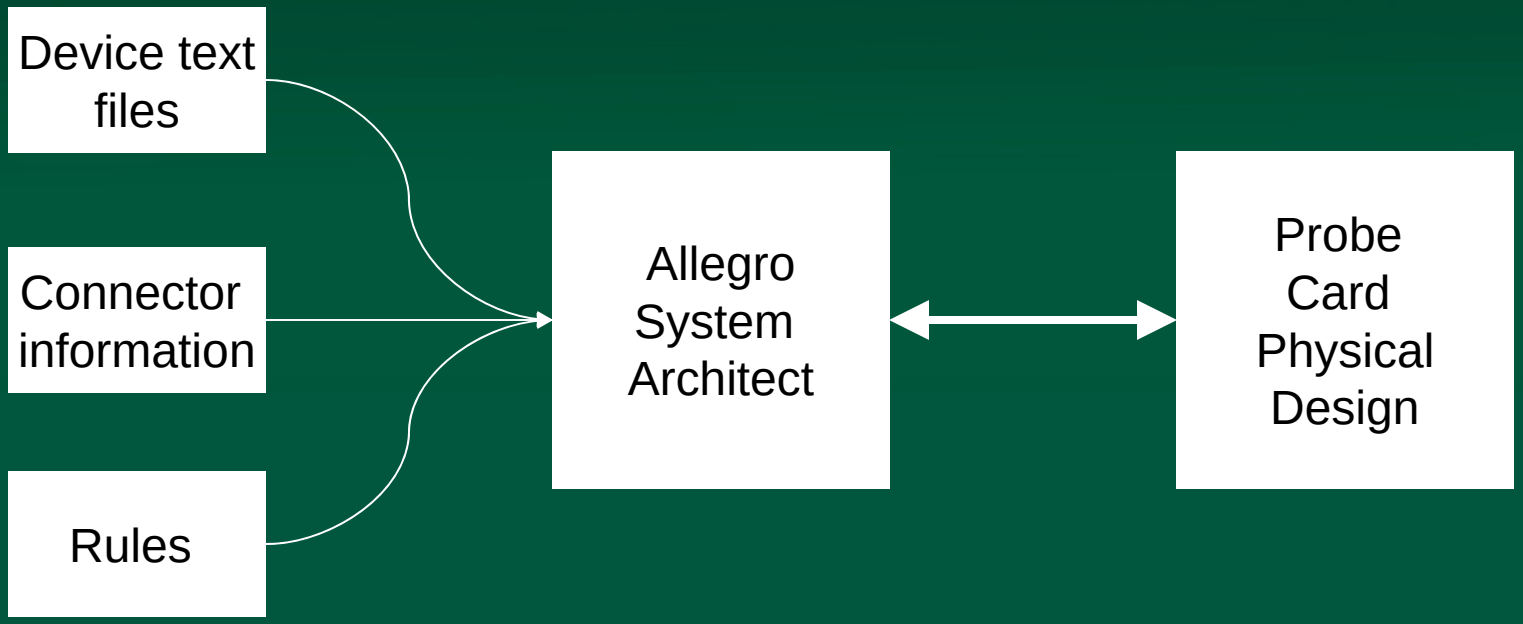
Technical aspects of Allegro System Architect

- A spreadsheet based editor for design connectivity
  - Patterns, copy-paste, sort, filter, find-replace over large amounts of data
  - Understands CAD data natively
  - Spreadsheet formats allows connectivity to be driven from layout
  - Clean access to text imports, exports, differences

How does a spreadsheet solution help

Problem	Solution
Large data sets	Spreadsheet Editor – No need for symbols – Handle thousands of nets/pins
Patterns and replication	Use copy paste, sort, filter find replace
Layout Driven Connectivity	Can drive connectivity in either direction with equal ease
Constraint Management	Understands CAD data natively

Design Flow


Device text files
Connector information
Rules
Allegro System Architect
Probe Card Physical Design

Strengths / Weaknesses

- Strengths
  - Spread Editing of Connectivity
  - Eco management / speed
  - Constraint handling
  - Layout driven connectivity

- Weakness's
  - Documentation schematics are not aesthetic

Typical Results

- Significant Reduction in time – especially if using schematic based methods
- Better productivity if constraints need to be managed (for large digital devices)
- Work required to substitute home-grown solutions with this solution
- Gains increase with Volume & design size
  - Not worth effort for very small / very infrequent designs spins

Follow-on

- Talk to the authors
  - Mike Goode , mgoode@cadence.com
- Avoid graphics – the next time you build a probe card
- Send us questions and comments