IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Overcoming the Challenges of Parallel RF Test

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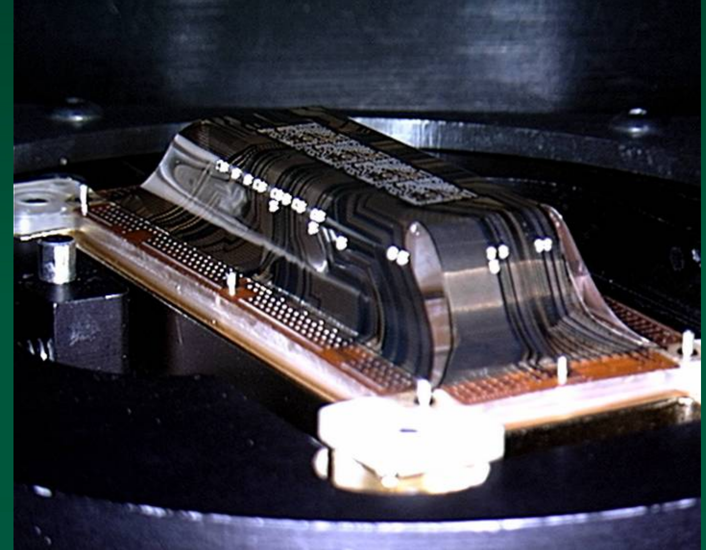
Outline

- The Challenges
- Roadblocks
- Clearing the Obstacles
- Summary



The Challenges

Decrease the cost to wafer-test RF devices

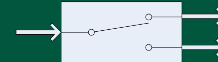
- Cost to Test one die:

$$\mathrm{Cost}/\mathrm{die} = f\left(\frac{\$_{\mathrm{ProbeCard}}}{\mathrm{Touchdowns}} + \$_{\mathrm{Station}} * t_{\mathrm{Test}}\right)$$

- From this:
  - Increase Life of Probe card (more touchdowns).
  - Minimize Test Time.
  - Test more die per touchdown.
- Setup:
  - You have “zero time” to debug the test program, after wafers arrive.
- It’s all easy, right?

The Challenges
Example: SPDT RF Switch

- Known Good Die RF Test:
  - Confirm Operation.
  - Verify:
    - Low Insertion Loss (connected path)
    - Isolation (disconnected path)
    - Linearity (3rd Harmonic)



- Consider testing in parallel:
  - 1 die

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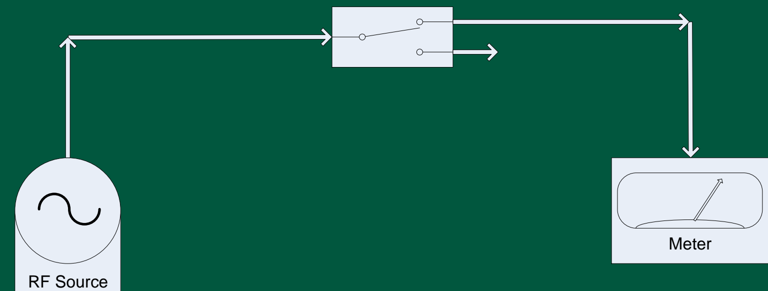

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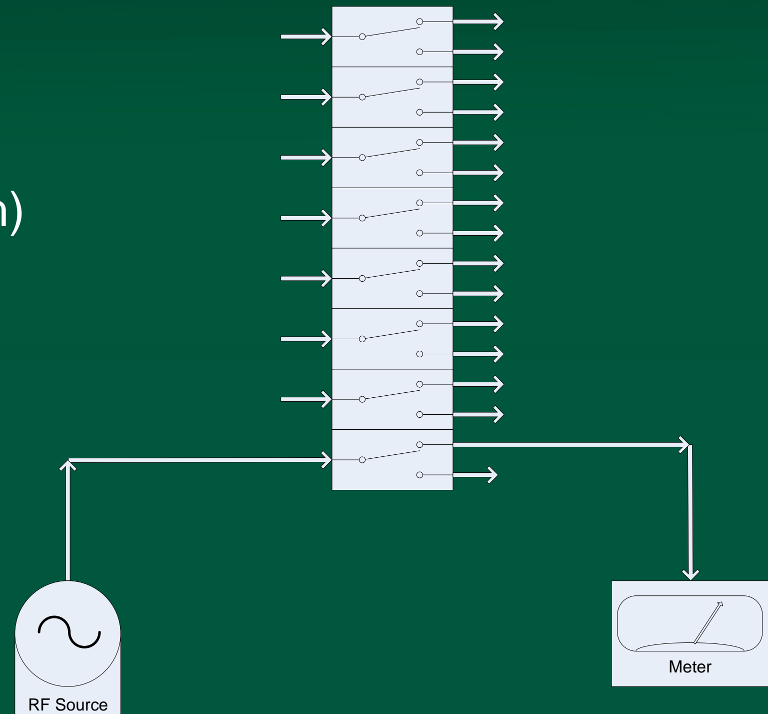


- Consider testing in parallel:
  - 1 die
  - 2 die
  - 8 die?

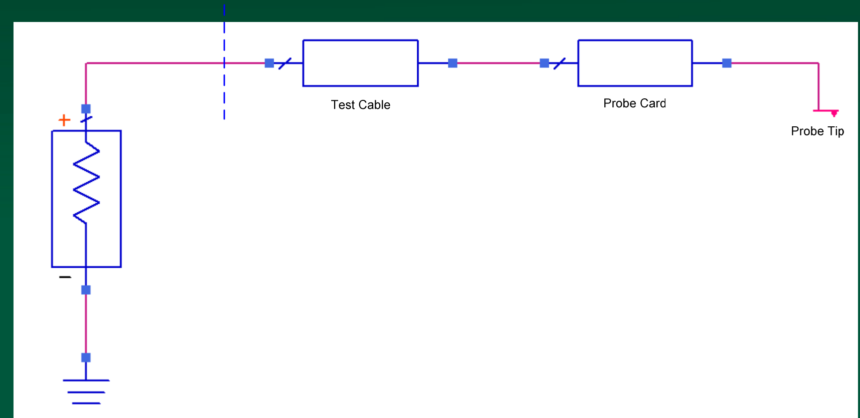
Roadblocks

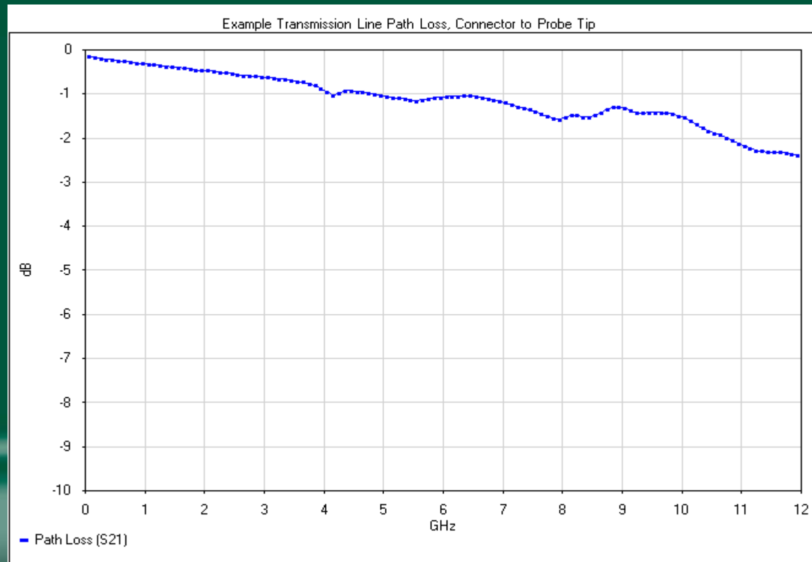
- RF Calibration
- RF Isolation
- Parallelism
- Multi-DUT Test Program Debug
- Wafer and Prober Availability

Roadblock #1

Do you know the losses of your transmission path?

- RF Calibration



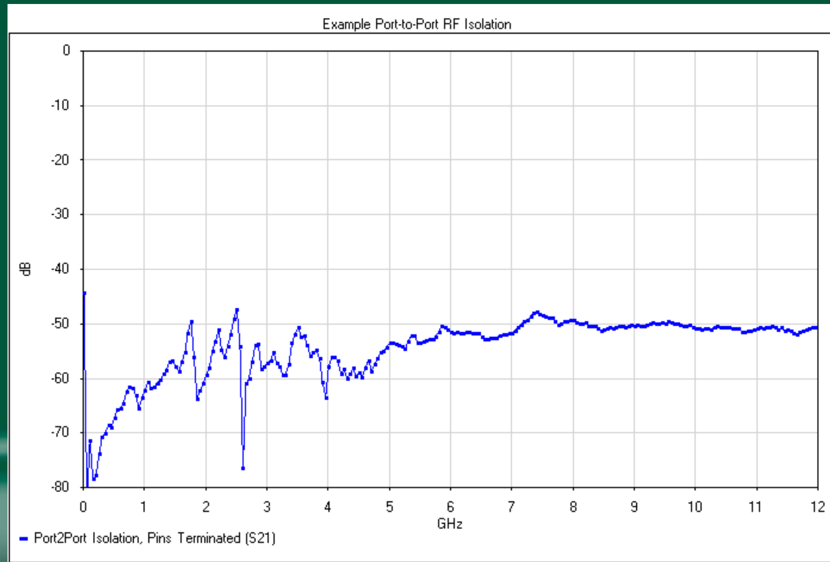


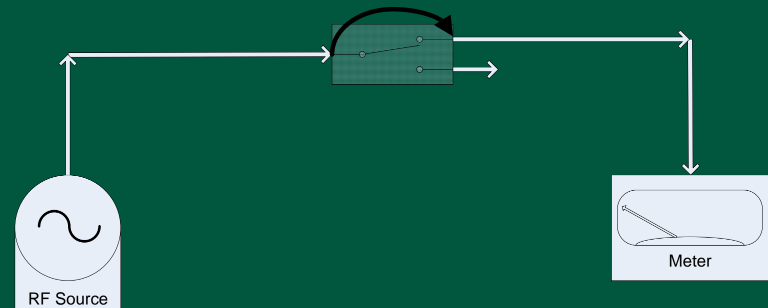
- All probes have path loss
  - (Some have less than others).
- Characterize the loss
- Subtract from measurement

Roadblock #2

Are you measuring your die or your probe card?

- RF Isolation
  - Port-to-Port
  - Die-to-Die





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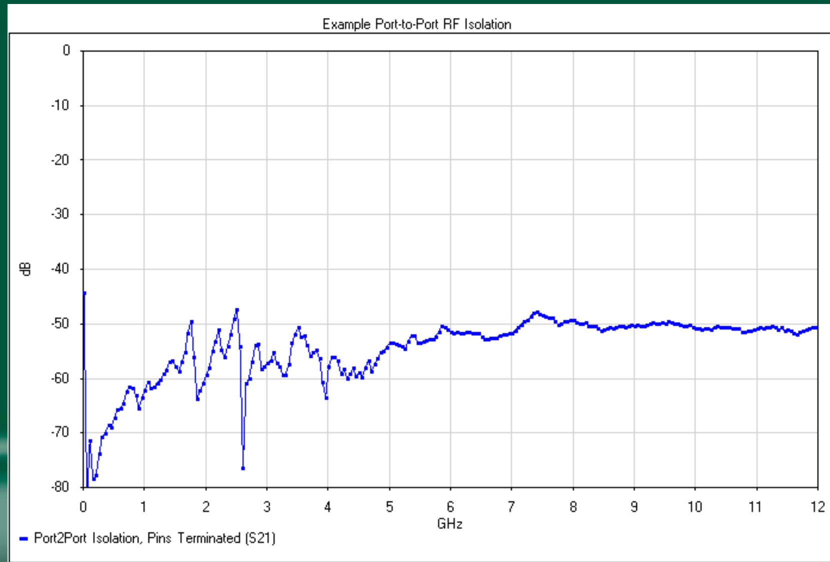
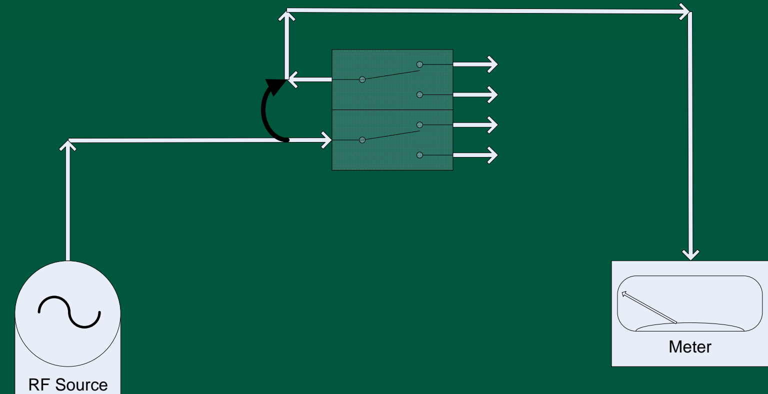
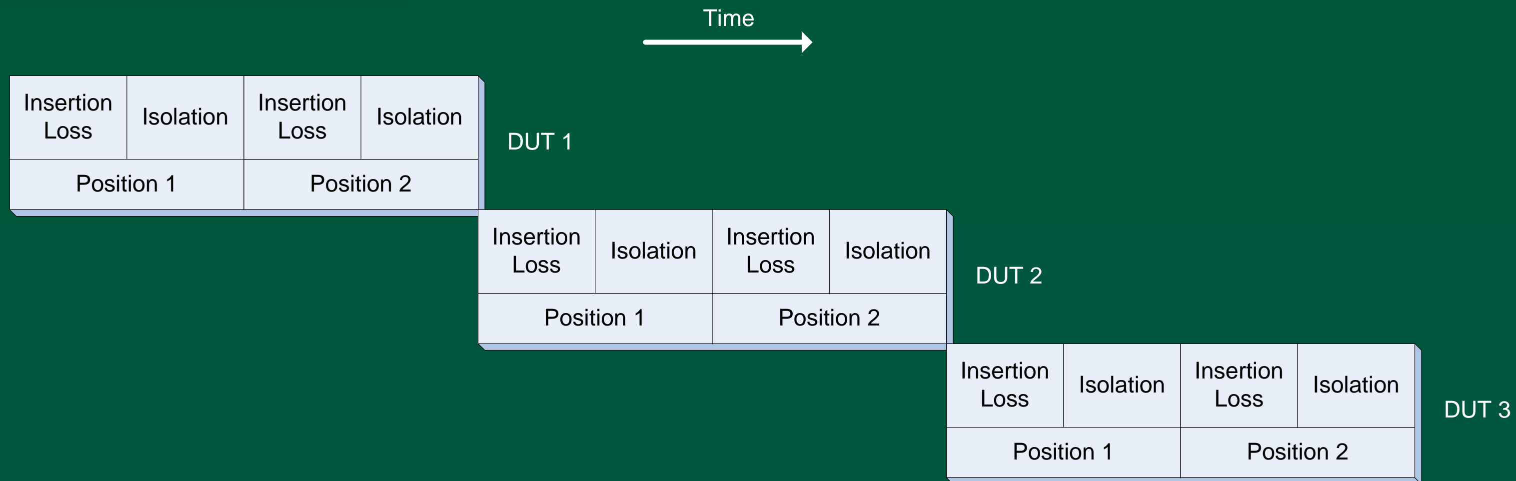




Roadblock #3

Have you fully-optimized your test program?



Roadblock #4

Have you fully debugged your probe card?

- *How much time do you have to optimize this program?*
- *How many wafers will you get to use?*
- *What is broken:*
  - *The silicon?*
  - *The test program?*
  - *The probe card?*

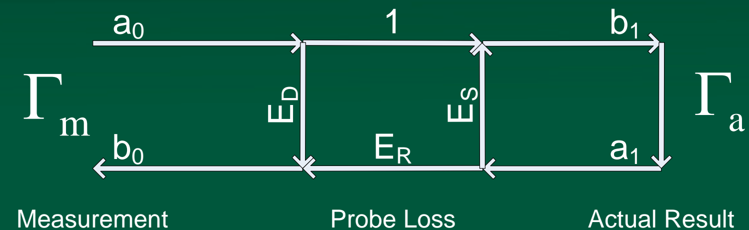
Clearing the Obstacles
Building your system

- RF Calibration:
  - Vector
  - Scalar
    - Direct measurement
    - Short-Open
- Catering your system for Parallel Test
- Test Optimization

RF Calibration

What is it?

- Probes have electrical loss.
- Measurements include the loss.



- *Calibration:*
  - *Characterize the transmission path.*
  - *Remove (de-embed) the loss from the measurements.*

E_D: Directivity
E_S: Source Match
E_R: Frequency Tracking

- Scalar Calibration:
  - Magnitude loss only.
- Vector Calibration:
  - Magnitude and phase.

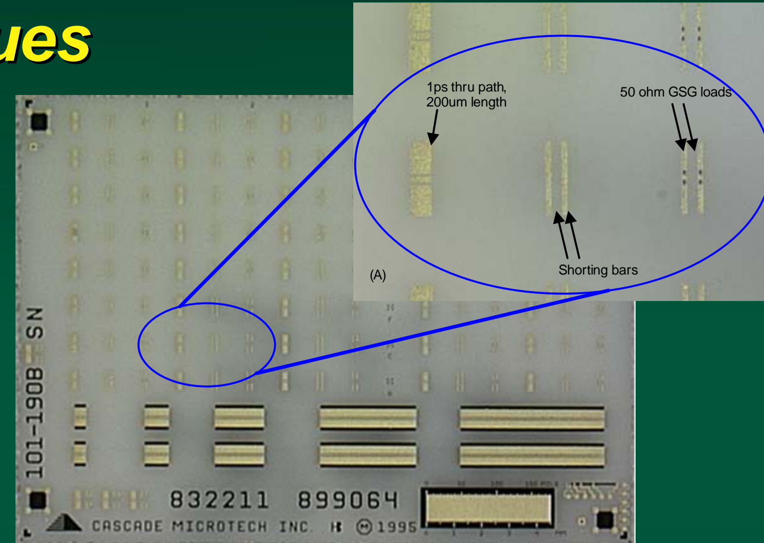
$$\Gamma_m = E_D + \frac{E_R \Gamma_a}{1 - E_S \Gamma_a}$$

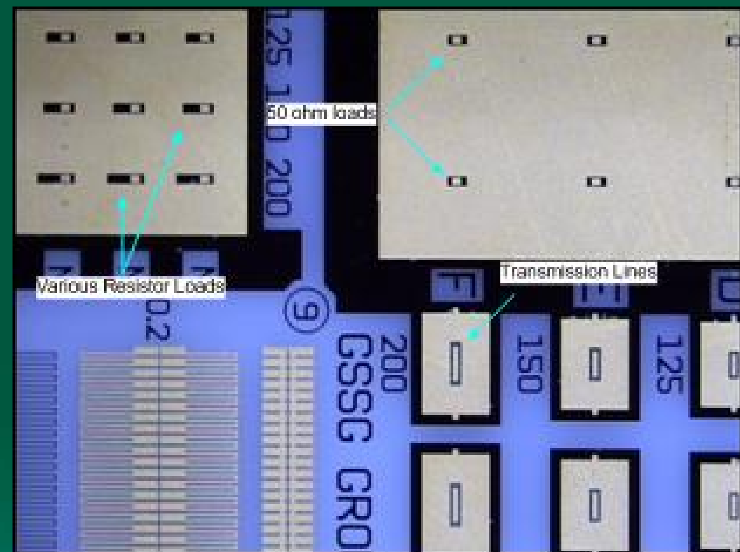
Vector RF Calibration

2-port techniques

- Measure 4 standards:
  - Short
  - Open
  - Load (50 ohms)
  - Thru path between ports.

- Disadvantages:
  - Probe standards.
  - Standards must match probe topology.
  - VNA software required.
  - Difficult to integrate within an ATE environment.
  - Vector calibration usually not required for KGD test.

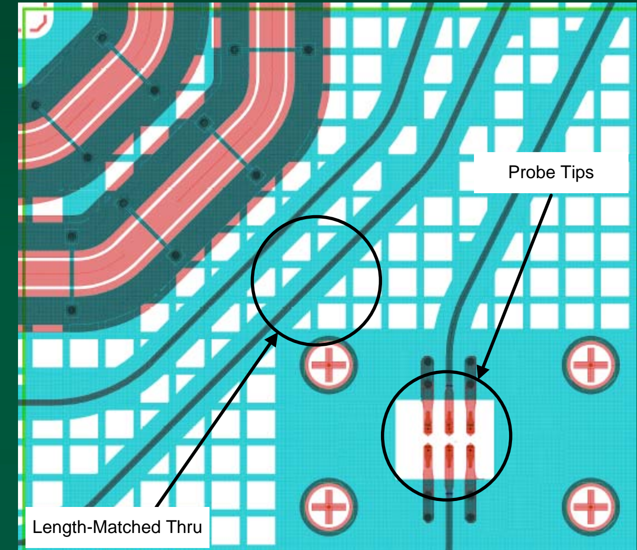




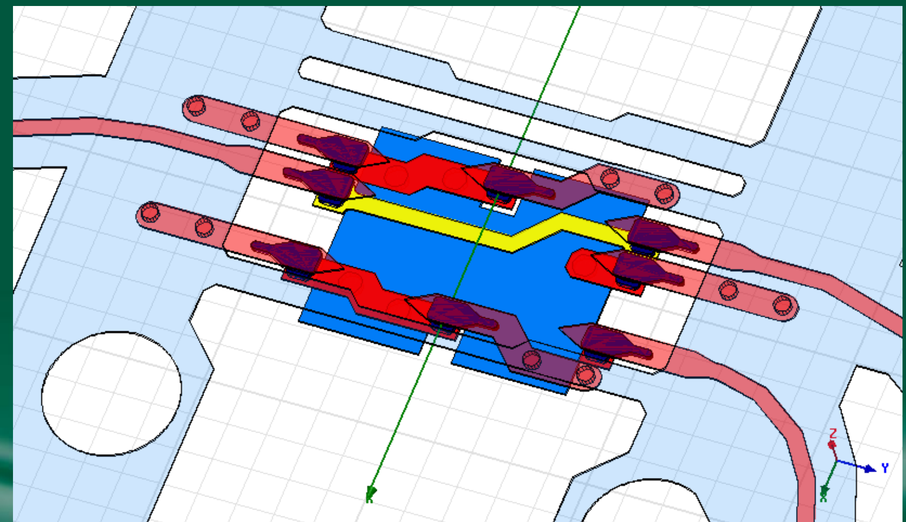
Scalar RF Calibration

Simple characterization techniques

- Direct Measurement:
  - Use two ports.
  - Measure the loss, end-to-end.
  - Divide loss by 2.



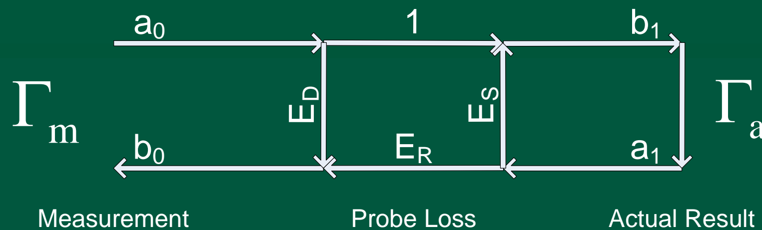
- Implementation:
  - Length-matched thru.
  - Cal-thru.
  - On-die thru.



Scalar RF Calibration

Measure Short-Open to characterize RF path loss

- Directivity (E_D) and Source Match (E_S) are generally small.
- Probe Short, Open. Take average.
- *Predicted loss is usually within 0.2dB @ 2 GHz*



$$\Gamma_m = E_D + \frac{E_R \Gamma_a}{1 - E_S \Gamma_a}$$

$$E_D \downarrow 0; E_S \downarrow 0; \qquad \Gamma_m = E_R \Gamma_a$$

$$\Gamma_{m-Open}\Big|_{\Gamma_a = 1} = E_D + \frac{E_R}{1 - E_S};$$

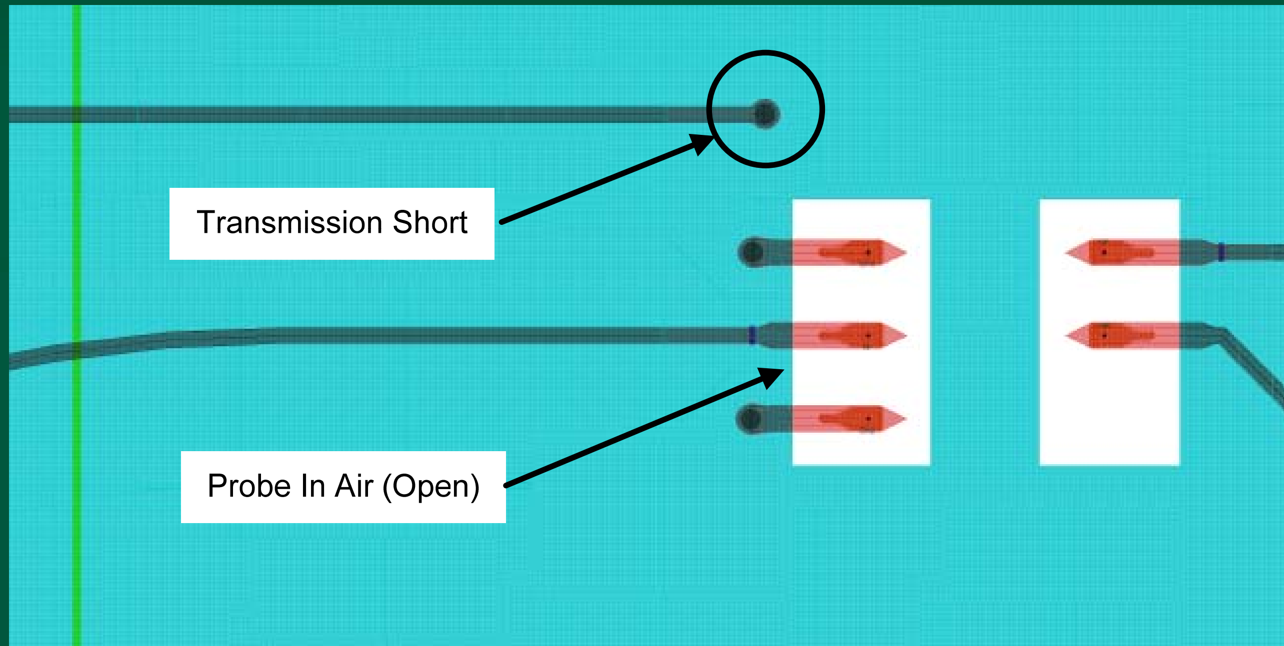
$$\Gamma_{m-Short}\Big|_{\Gamma_a = -1} = E_D - \frac{E_R}{1 + E_S}$$

$$E_R = \frac{\Gamma_{m-Open} - \Gamma_{m-Short}}{2}$$

Scalar RF Calibration

Measure Short-Open to characterize RF path loss

- Incorporate Shorting path into probe:

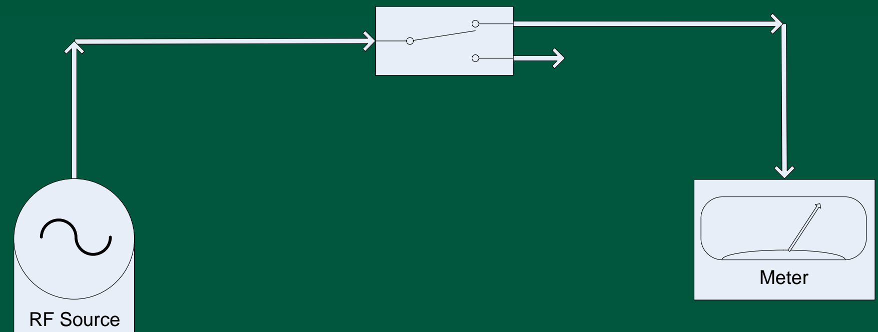


Clearing the Obstacles

Cater your system for Parallel test

Time →

Insertion Loss	Isolation	Insertion Loss	Isolation
Position 1		Position 2	



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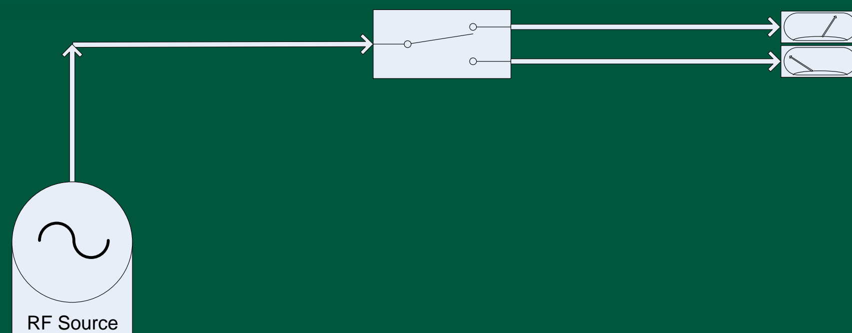

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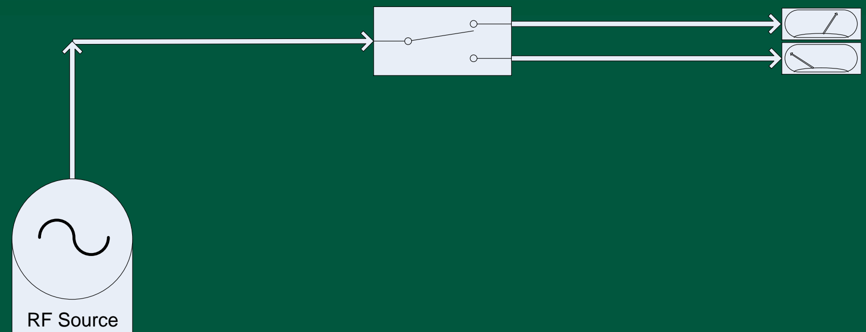

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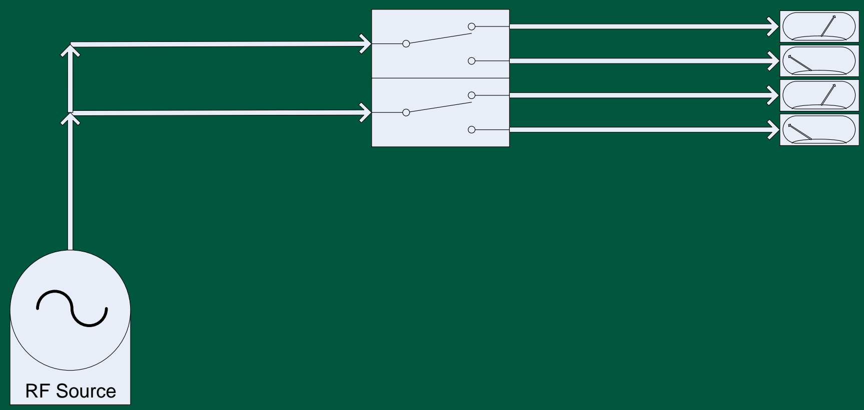

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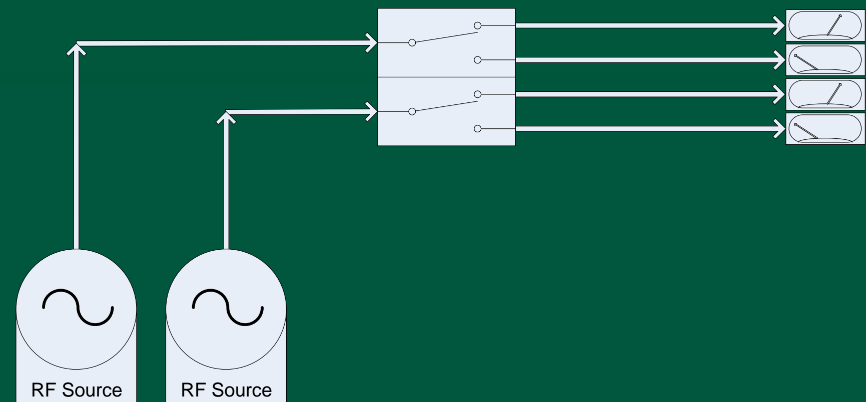
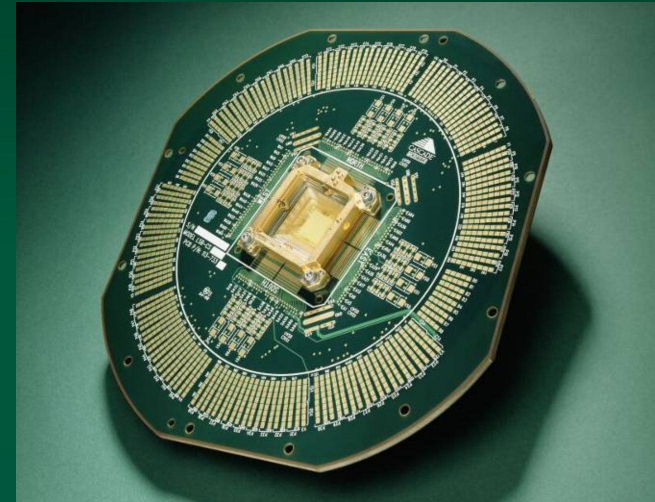


Reduce Isolation requirements by testing at different frequencies.

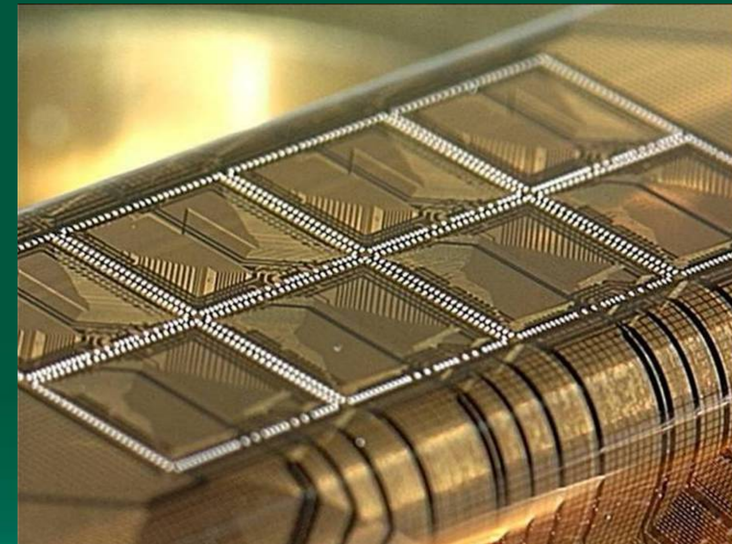
Debugging the Test Program

A significant challenge of Parallel RF Test



- *Reality Check:*
  - *Most devices are not as simple as this example…*

- *Parallel Test Setup:*
  - *Develop test without burning up wafers.*
  - *Develop test with few wafers at a manual station.*
  - *Optimize test time.*
  - *Assure complete test coverage of part.*



Pyramid Accel™ Concept

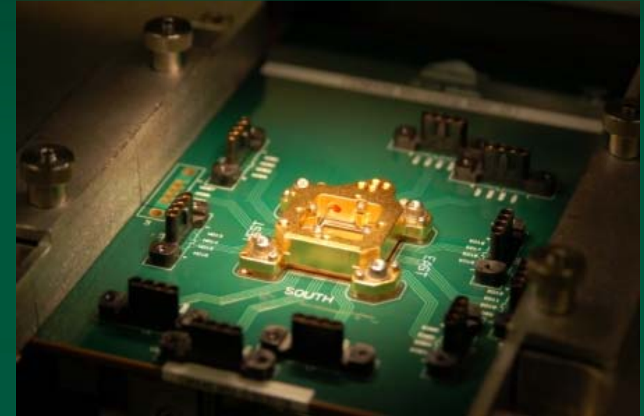
Enabling Parallel RF Test

- Design Test program.
- Design Probe card.
- Obtain blind-build packaged parts.

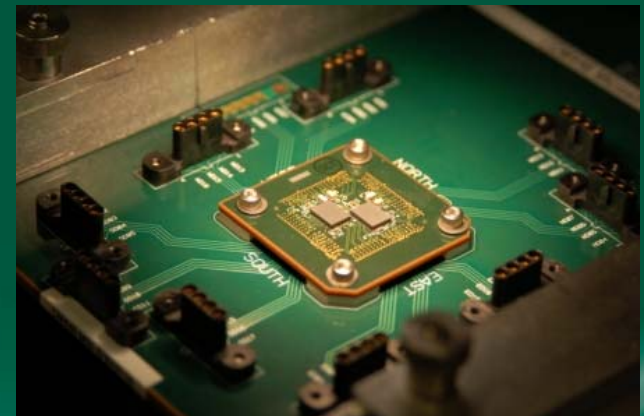
- Temporarily eliminate:
  - Wafer prober (cost & availability)
  - Wafers (develop prior to their arrival)

- Test with packaged parts.
- Optimize test program.

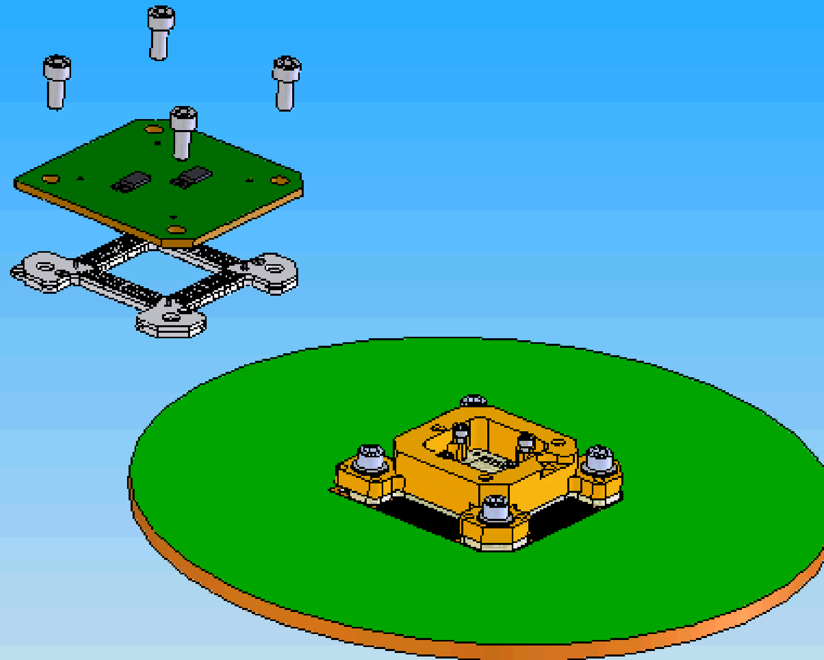
Pyramid Probe "Core"



Pyramid Accel Debug Fixture



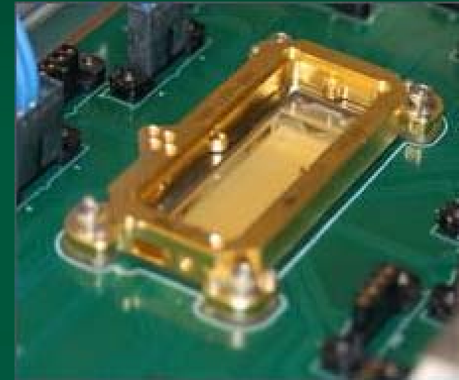
Pyramid Accel™ Fixture



Pyramid Accel™ Fixture
Enabling Parallel RF Test

- Test features:
  - Enables test of complex probe cards.
  - Socket option allows you to replace blind-build parts.
  - Electrical performance similar to Pyramid Probe performance.

Pyramid Probe Core



Pyramid Accel Debug Fixture

- Golden Probe:
  - Keep an Accel fixture at the production test site.
  - Validate probe card & test program are still functioning properly.

Summary

Parallel RF Test presents a unique Challenge

- Calibrate RF path loss using scalar techniques.
- Characterize port-to-port isolation.
- Design probe card to optimize for parallel test.
- Write a true parallel-processing test program.
- Optimize your test program as early as possible.
  - Assure adequate test coverage.
  - Lower your test cost per die.

Summary

Thank You!