IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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The Advanced Cantilever Probe Card with High Bandwidth (>3GHz) and Experimental Result

June 8-11, 2008

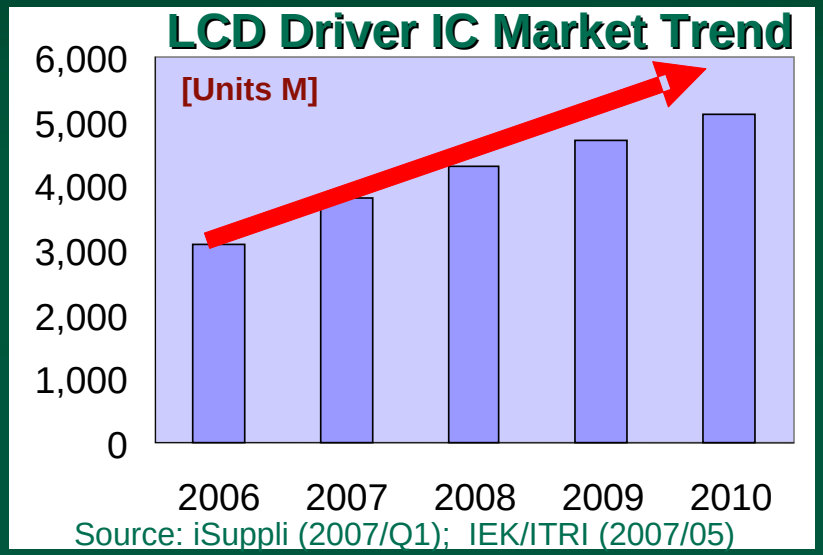
San Diego, CA USA

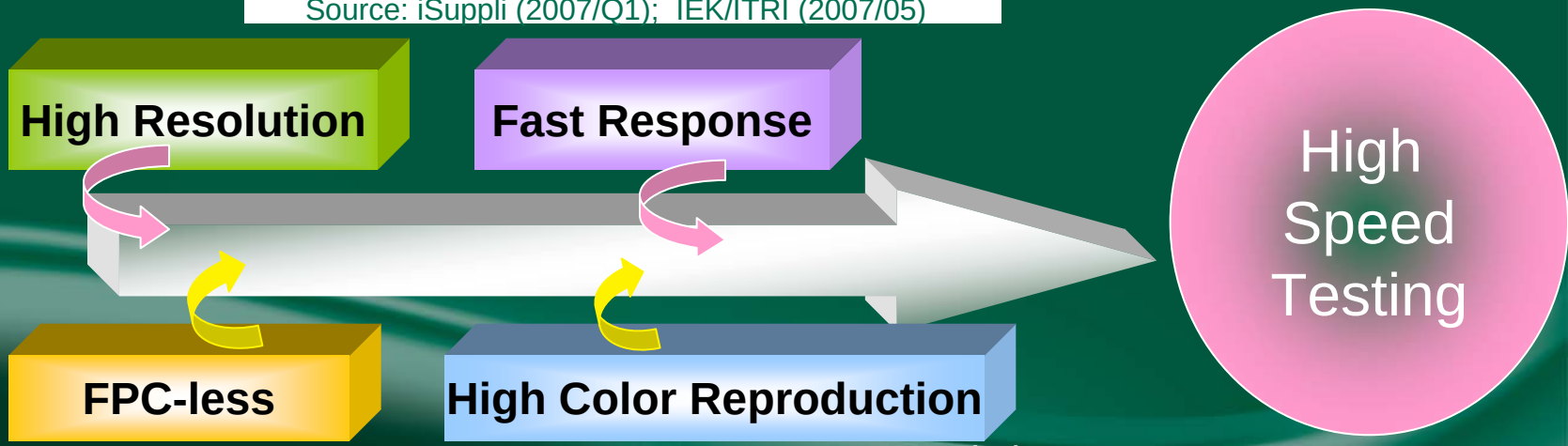
Outline

- Introduction & Background
- Objectives & Goal
- Modeling & Analysis
- Experiment, Validation & Customer Verification
- Summary & Conclusion
- Follow-On Work

Introduction & Background

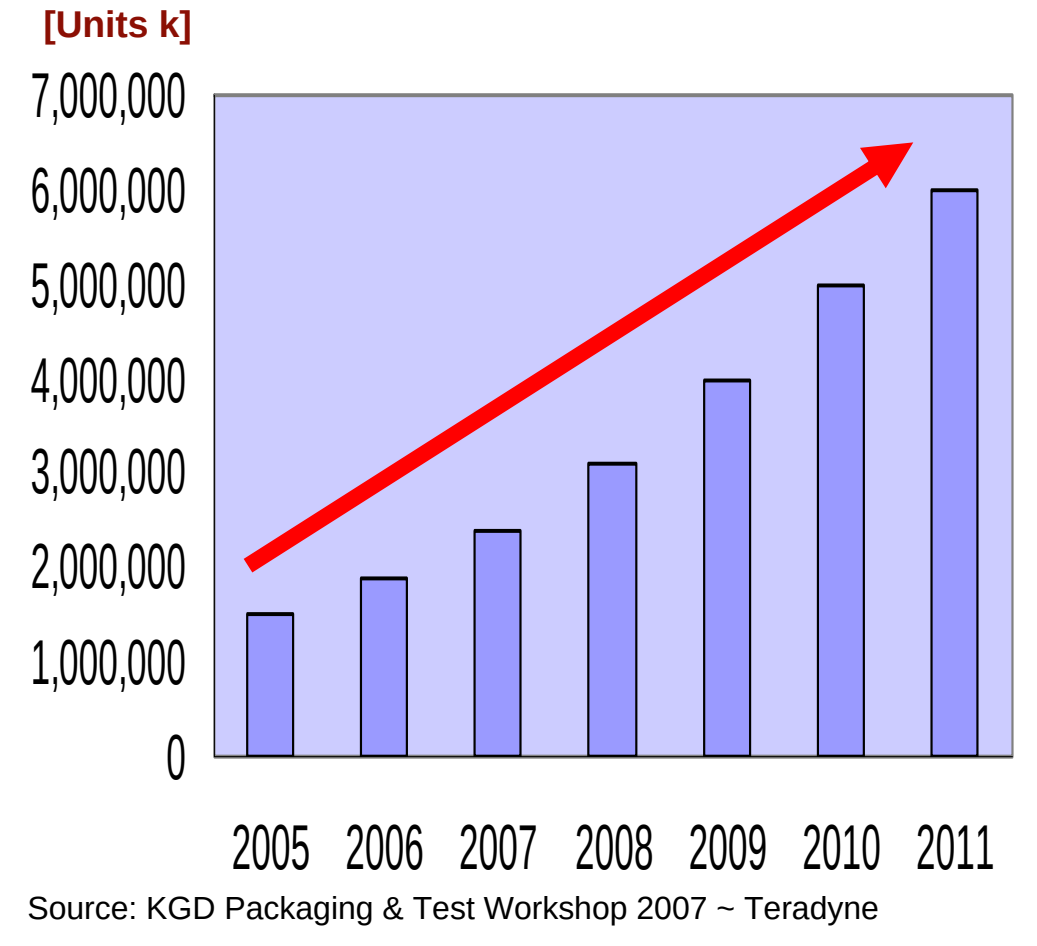
- High Speed Market (LCD, Memory, Logic…)





Introduction & Background

- High Frequency Market



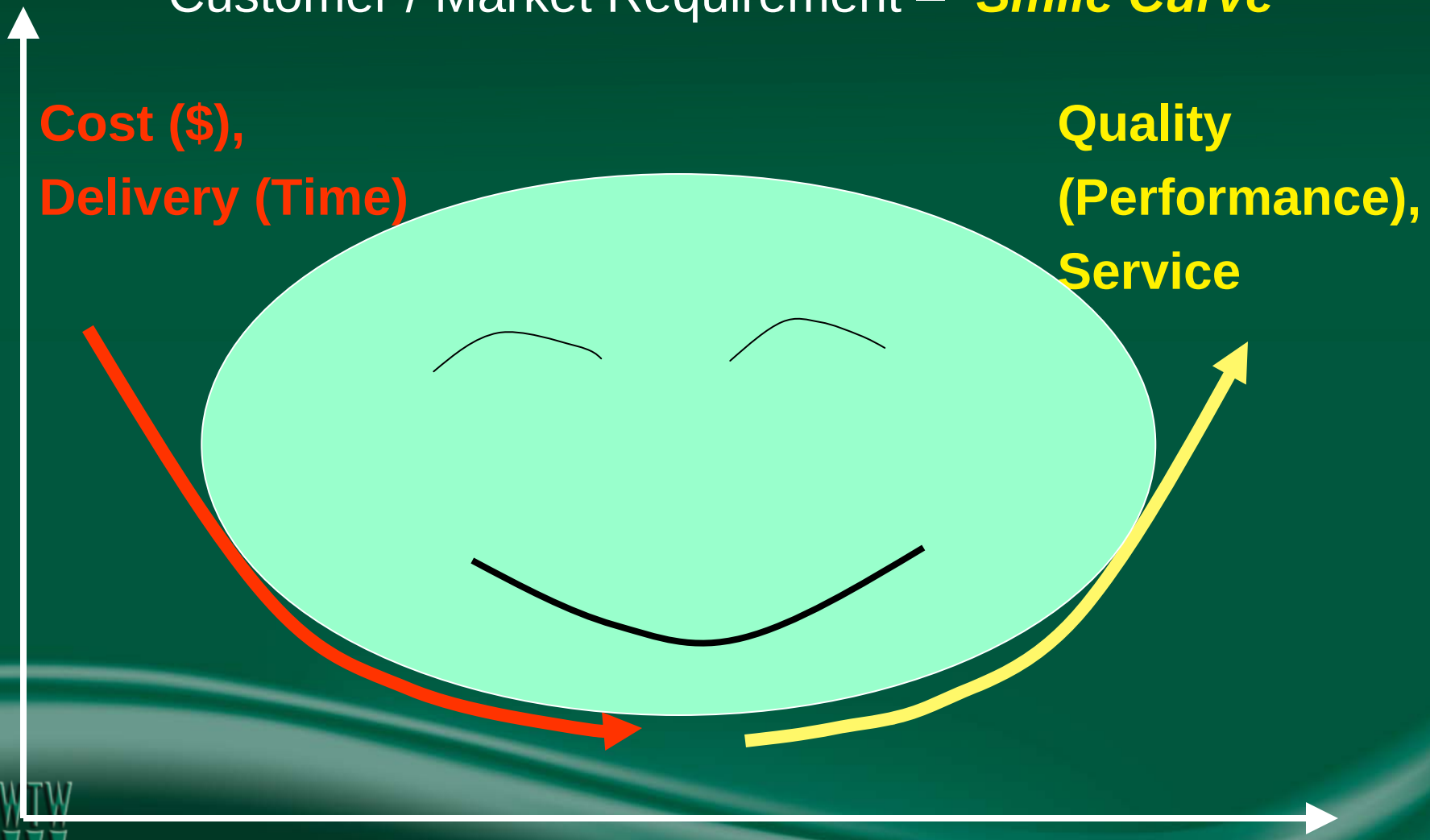
Source: KGD Packaging & Test Workshop 2007 ~ Teradyne

Wireless Devices

- Cellular Handsets
- Cordless Phone
- WLAN
- Bluetooth
- GPS
- UWB
- WiMax
- DVB-H & T-DMB
- Zigbee

Introduction & Background

Customer / Market Requirement – "***Smile Curve***"



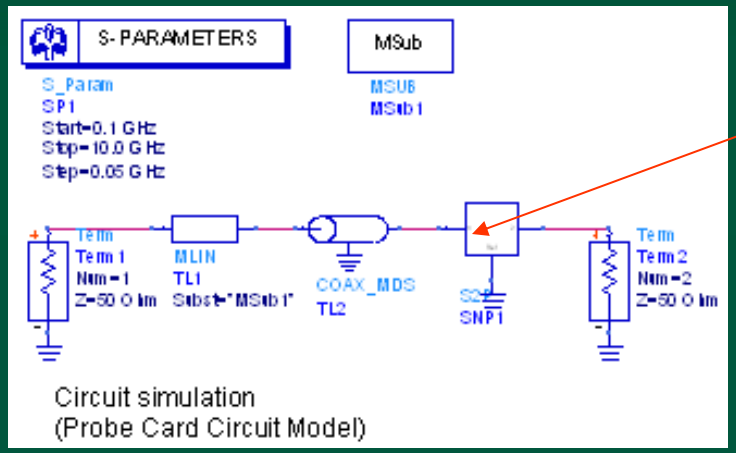
Objectives & Goal

- Objectives – Reduce the total cost for high speed device testing
  - High performance (>3GHz, >1Gbps)
  - Low total cost (CP/FT test cost…)
  - Short delivery time (< 2 weeks)
  - Fine pitch (< 35 um)
- Strategy – How ??
  - Improve the "**Signal Integrity"** issue of the normal cantilever probe card.

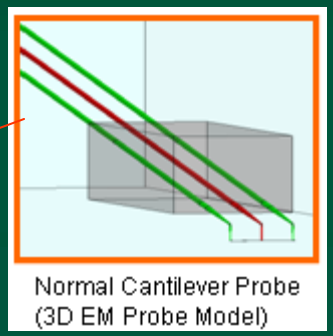
Modeling & Analysis

- Modeling – The EM model of the probe card

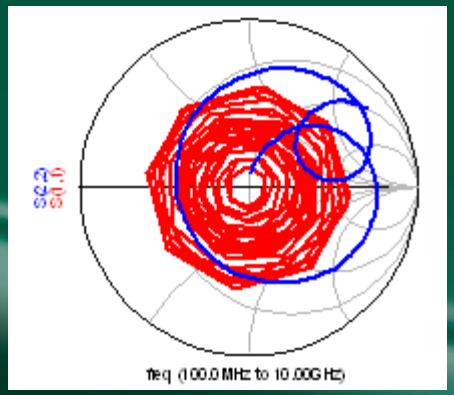
  EM model(Probe), Circuit model(Probe Card)

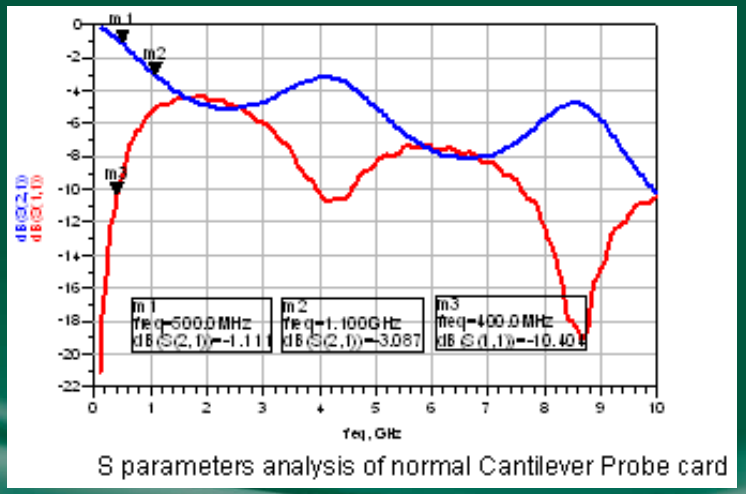


Circuit simulation
(Probe Card Circuit Model)



Normal Cantilever Probe
(3D EM Probe Model)





S parameters analysis of normal Cantilever Probe card

Modeling & Analysis

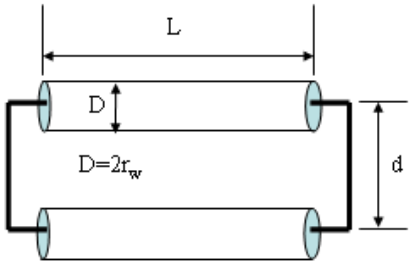
- Modeling–Inductance of the cantilever probe

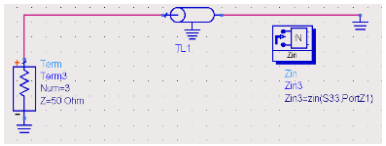
Inductance Formula for Round Wire

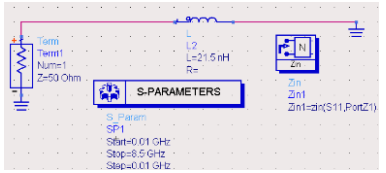
$$L_S = \frac{\mu_0}{2\pi}\ell\left\{\ln\left[\frac{\ell}{d}+\sqrt{\left(\frac{\ell}{d}\right)^2+1}\right]+\frac{d}{\ell}-\sqrt{(\frac{d}{\ell})^2+1}\right\}$$ Self Inductance

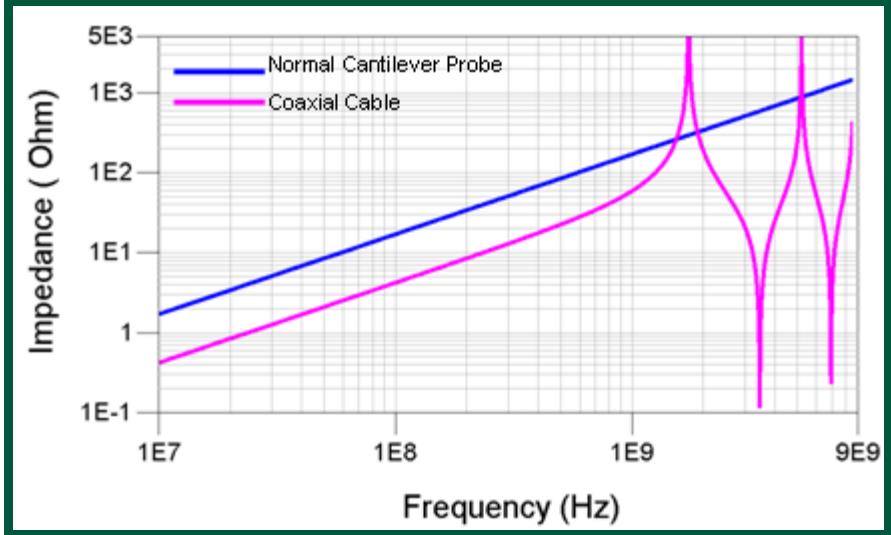
$$L_M = \frac{\mu_0}{2\pi}\ell\left\{\ln\left[\frac{\ell}{r_w}+\sqrt{\left(\frac{\ell}{r_w}\right)^2+1}\right]+\frac{r_w}{\ell}-\sqrt{(\frac{r_w}{\ell})^2+1}\right\}$$ Mutual Inductance

$$L_{loop} \cong 2(L_S - L_M) \quad \text{if } \ell \gg r_w,\ \ell \gg d$$





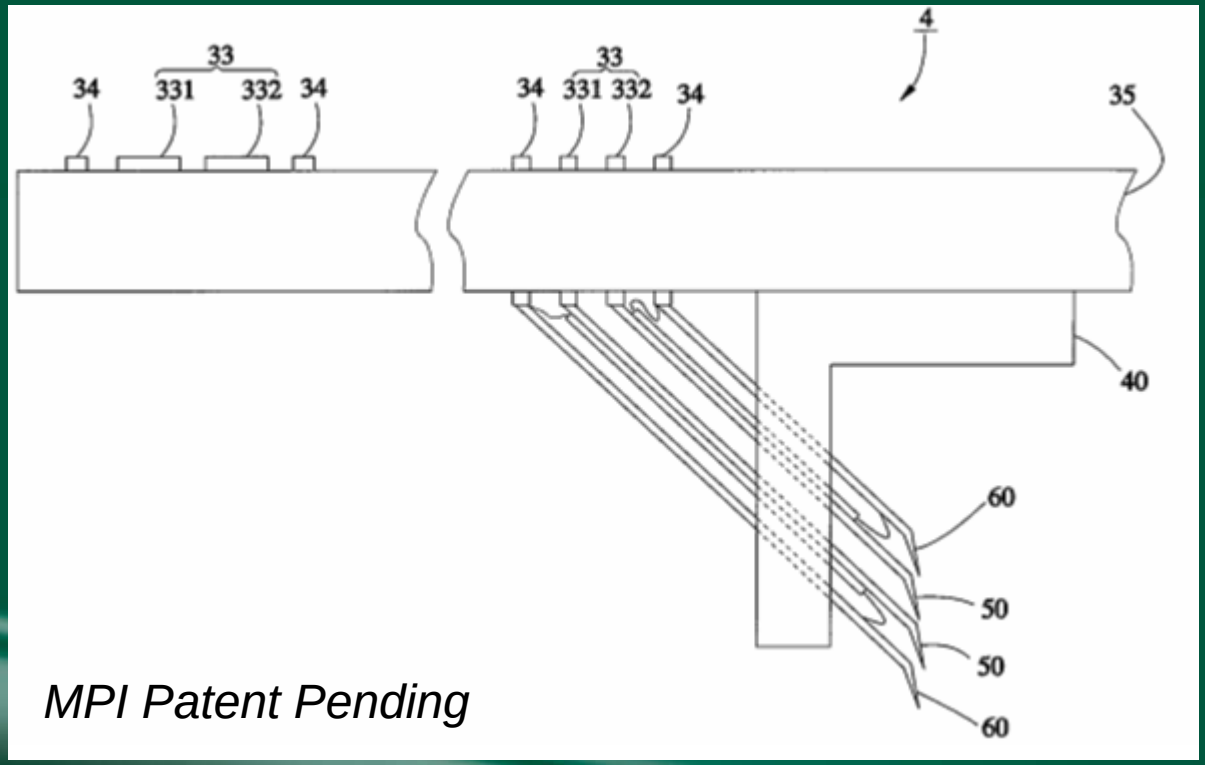




	Formula
Normal Cantilever Probe	21.4nH

Modeling & Analysis

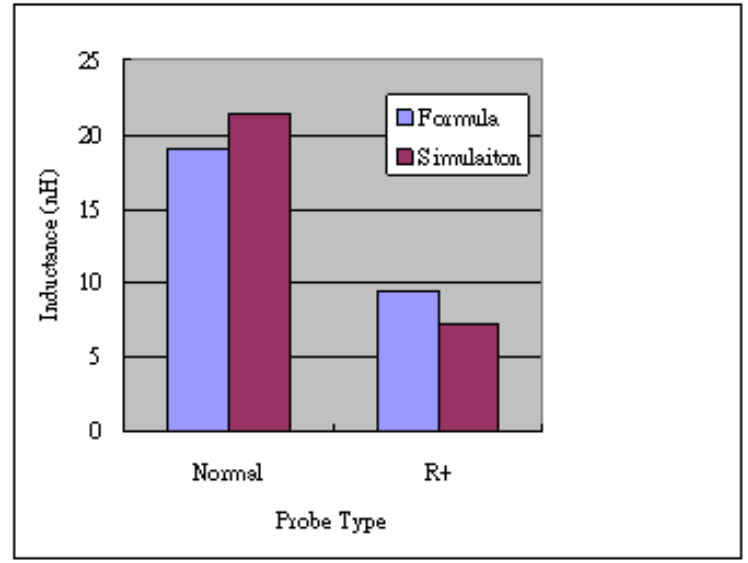
- Modeling – The impedance compensated cantilever probe (R+)



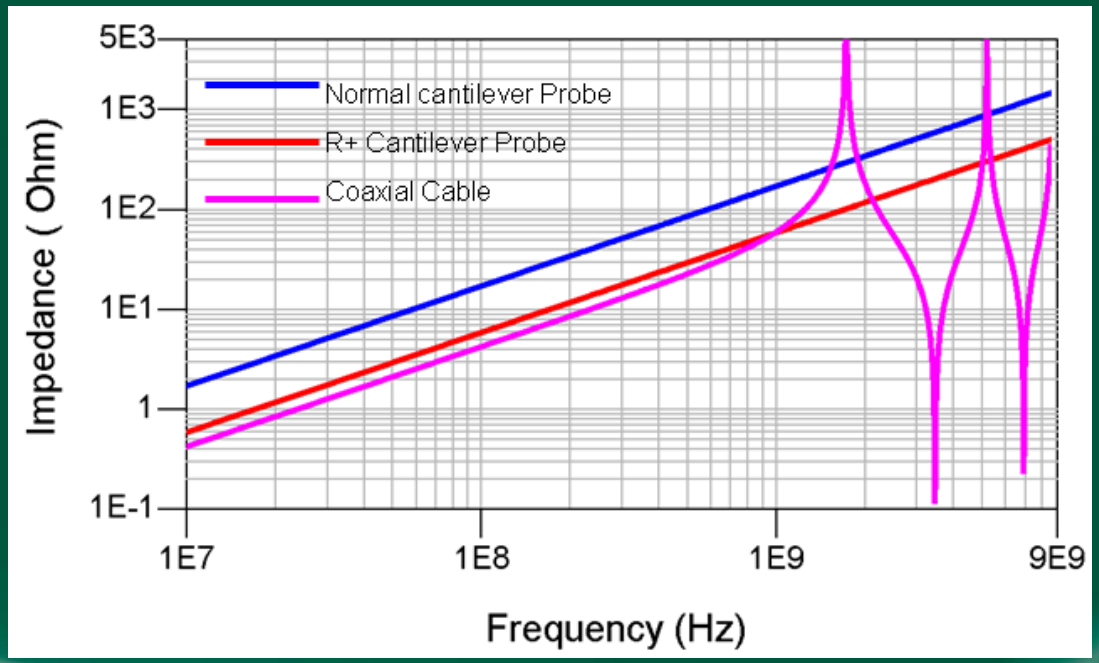
MPI Patent Pending

Modeling & Analysis

- Modeling – Inductance comparison



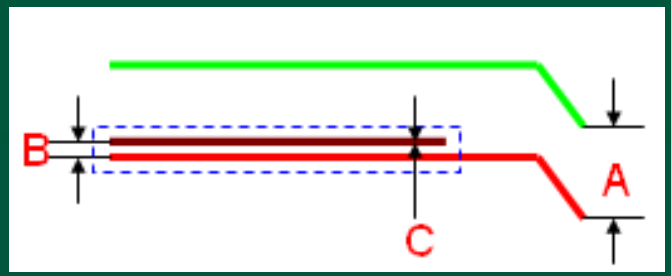
	Formula	HFSS Simulation
Normal Probe	21.4nH	19.1nH
R+ Probe	7.25nH	9.44nH

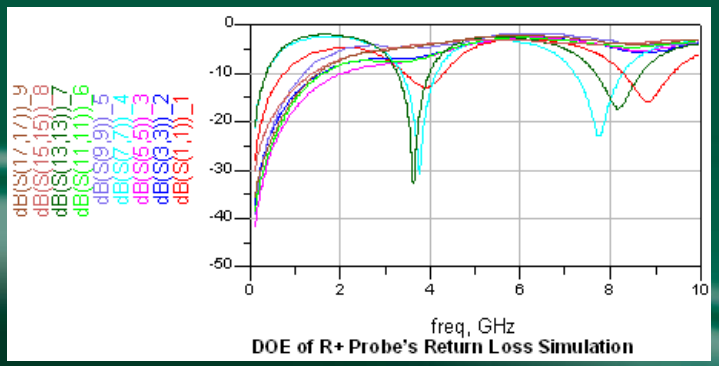


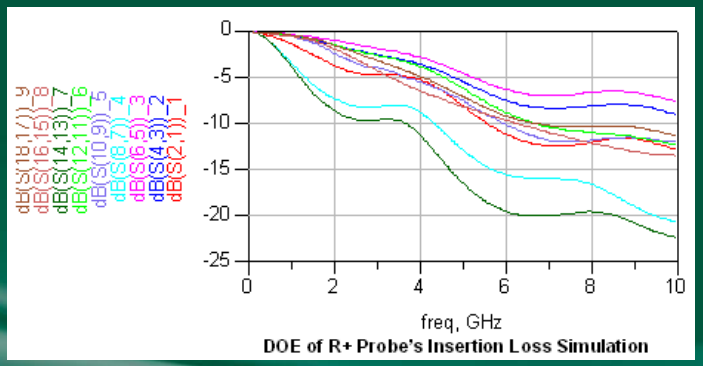
Modeling & Analysis

- Improve the R+ probe's impedance matching with DOE method (EM Simulation result)

Exp.	A (um)	B (mil)	C (mil)	ABC	S21(-1dB)	S21(-3dB)	S11(-10dB)
1					810 MHz	1.68 GHz	750 MHz
2					1.56 GHz	3.50 GHz	1.57 GHz
3					2 GHz	4.12 GHz	2.05 GHz
4					450 MHz	895 MHz	360 MHz
5					210 MHz	2.27 GHz	1.195 GHz
6					1.64 GHz	3.39 GHz	1.63 GHz
7					460 MHz	850 MHz	355 MHz
8					1.48 GHz	2.48 GHz	1.40 GHz
9					1.65 GHz	2.89 GHz	1.5 GHz







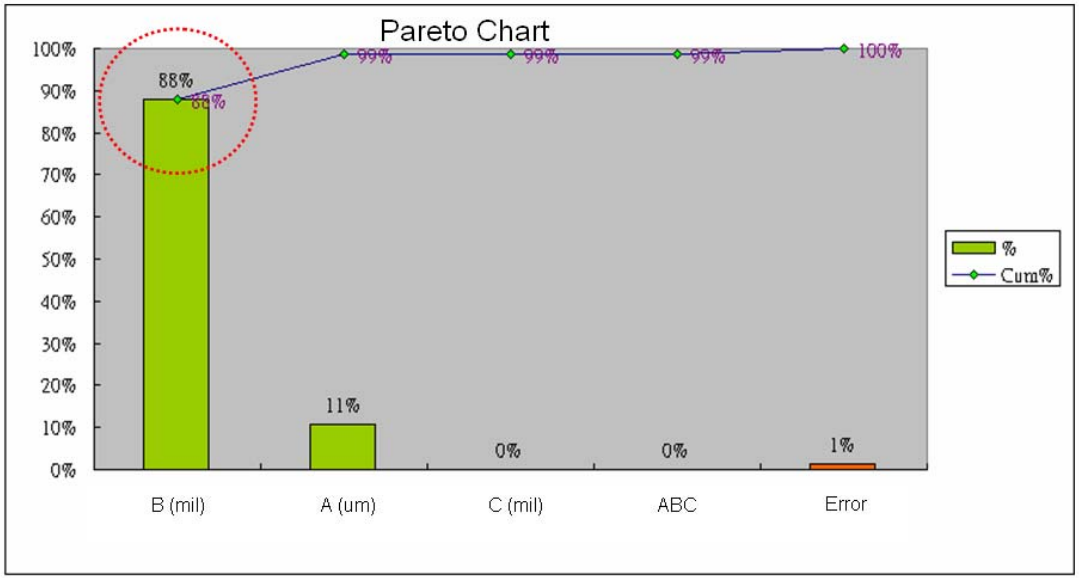
Modeling & Analysis

- ANOVA

Target : high frequency @ S11(-10dB)

Quality judgment : Larger the better

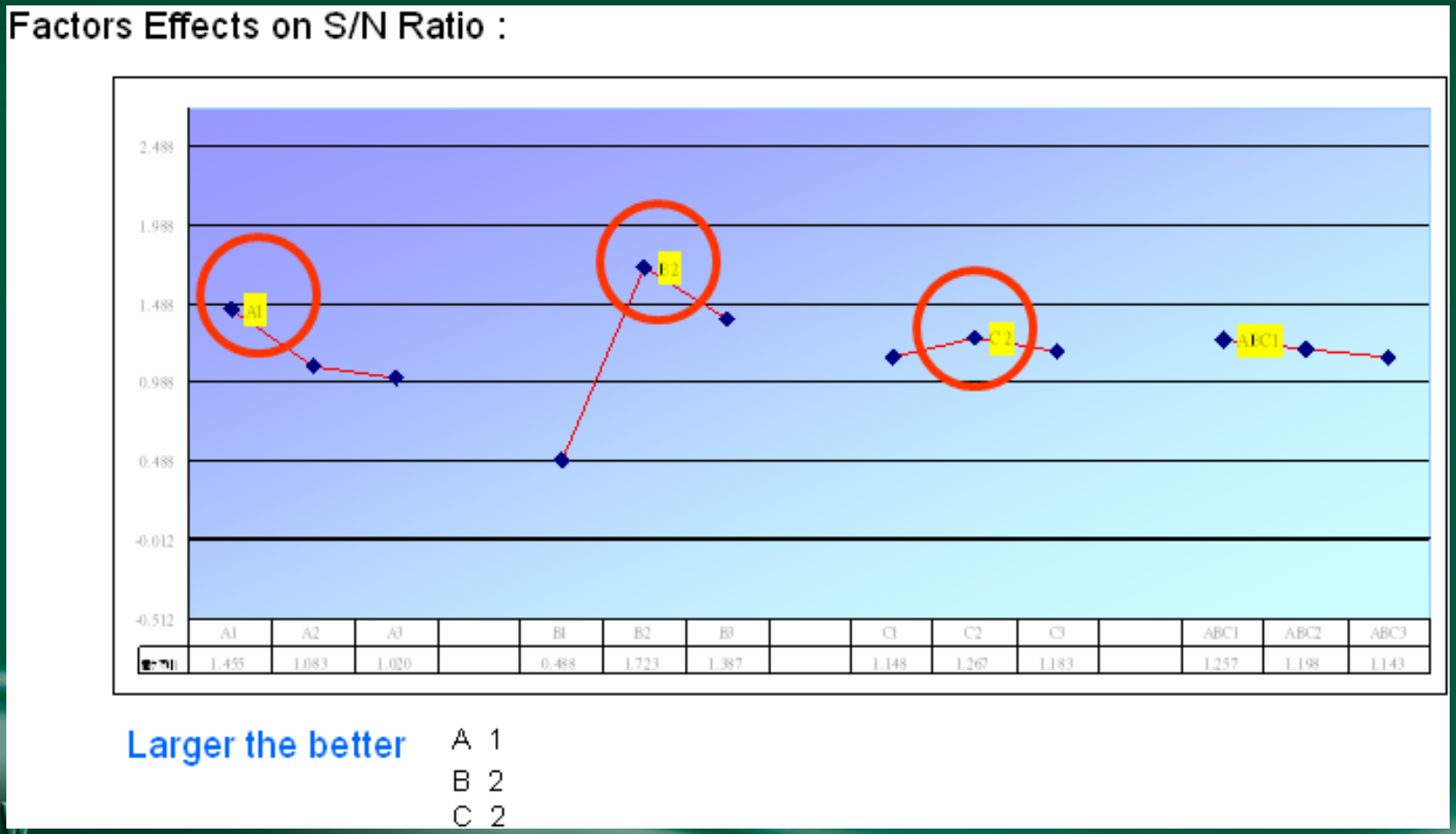
ANOVA Result :



A (um)
B (mil)
⇒ High effect from ANOVA result

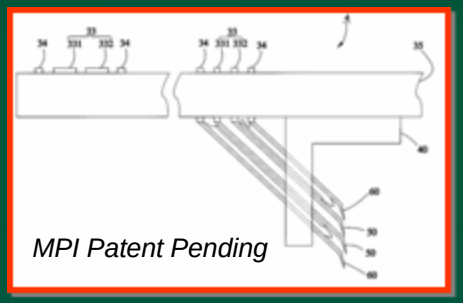
Modeling & Analysis

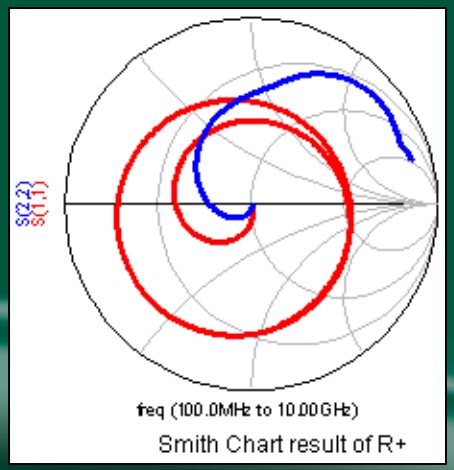
- S/N Chart



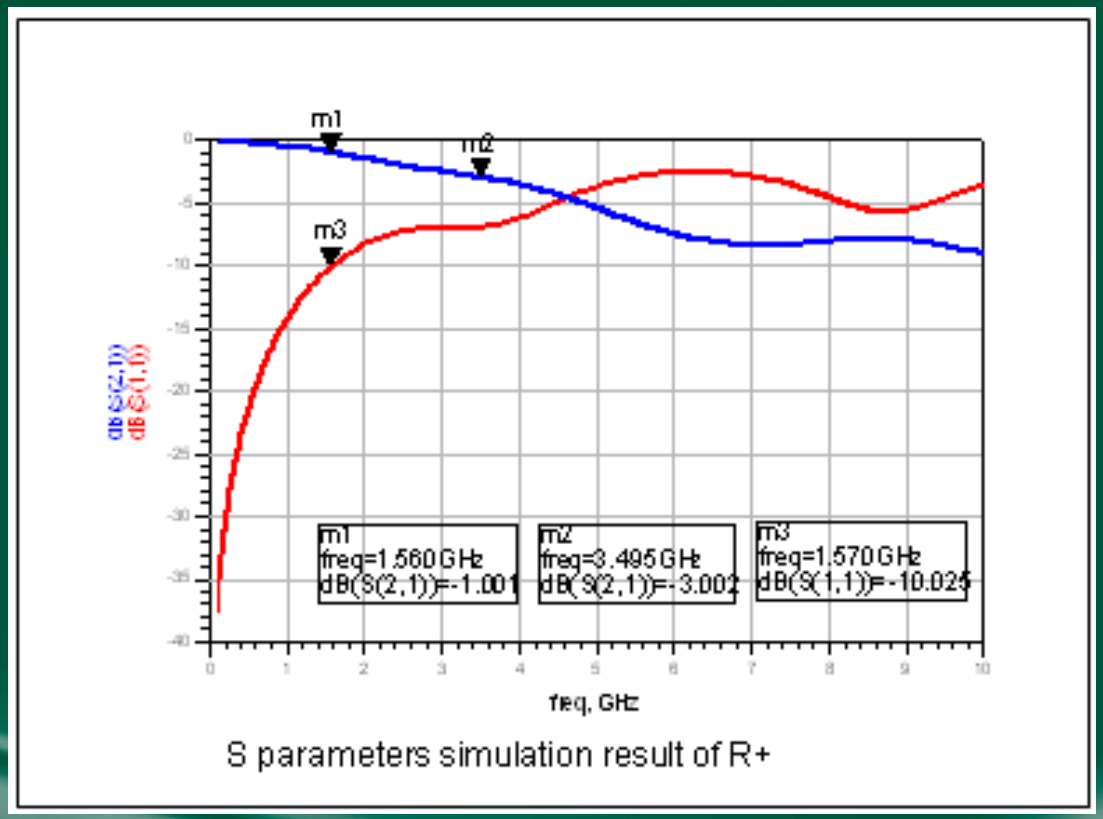
Modeling & Analysis

- Modeling – The impedance compensated cantilever probe (R+ probe)





Smith Chart result of R+

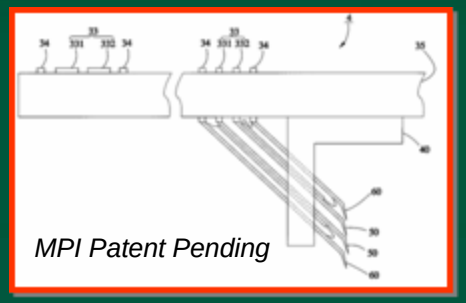


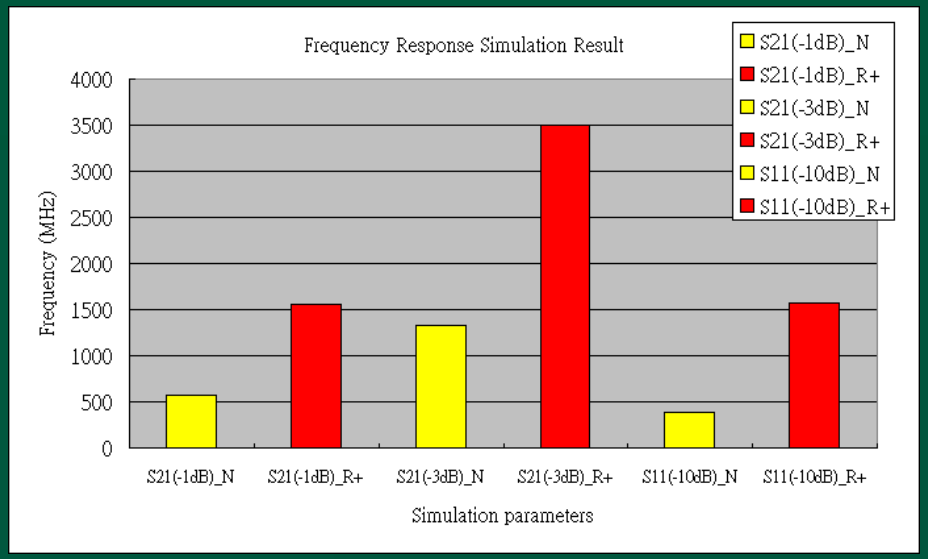
S parameters simulation result of R+

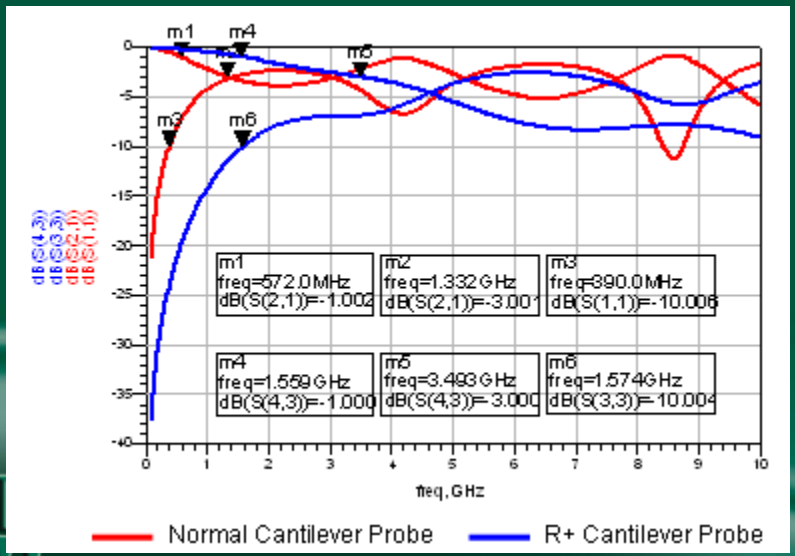
Modeling & Analysis

- Analysis – Frequency Domain response

  S21,S11 (R+ probe vs. normal probe)



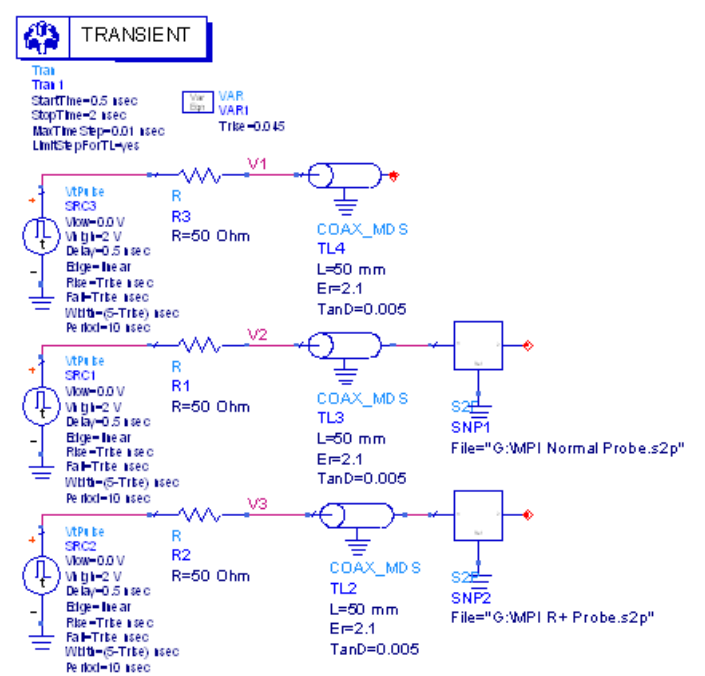




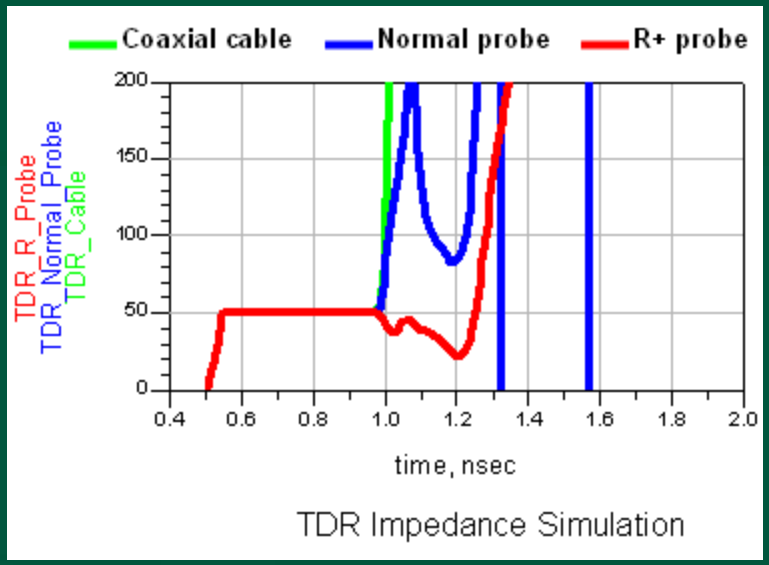
Modeling & Analysis

- Analysis – Time Domain response

  Impedance (R+ probe vs. normal probe)



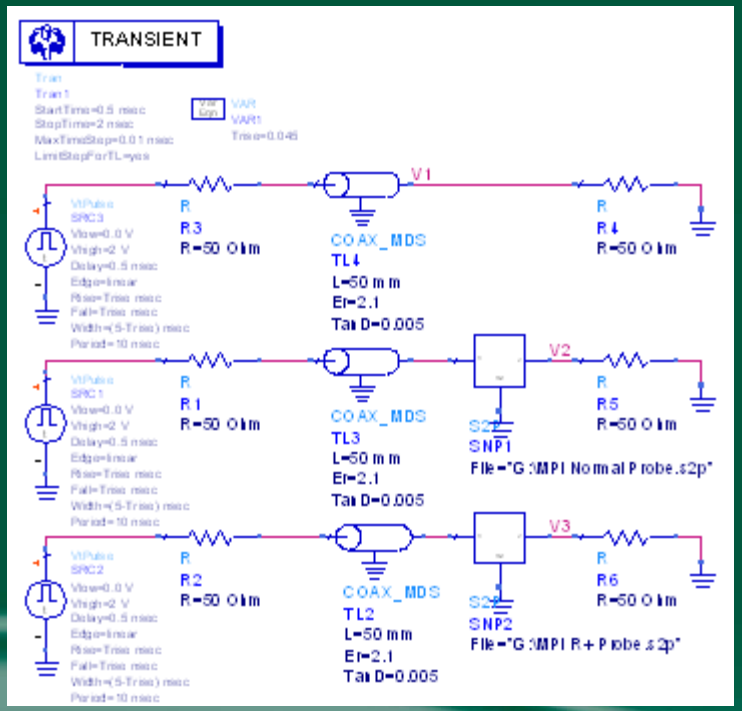
TDR schematic simulation used ADS schematic tools

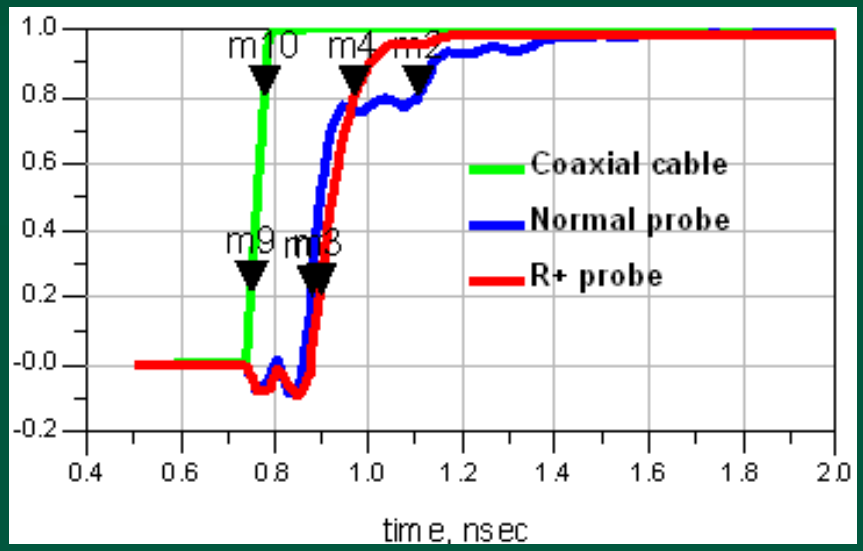


Modeling & Analysis

- Analysis – Time Domain response

  Rising time 20~80% (R+ probe vs. normal probe)





Rising time for Coaxial cable (20%~80%)

778.3 ps – 751.3 ps = 27 ps

Rising time for Normal probe (20%~80%)

1106 ps – 879.3 ps = 226.7 ps

Rising time for R+ probe (20%~80%)

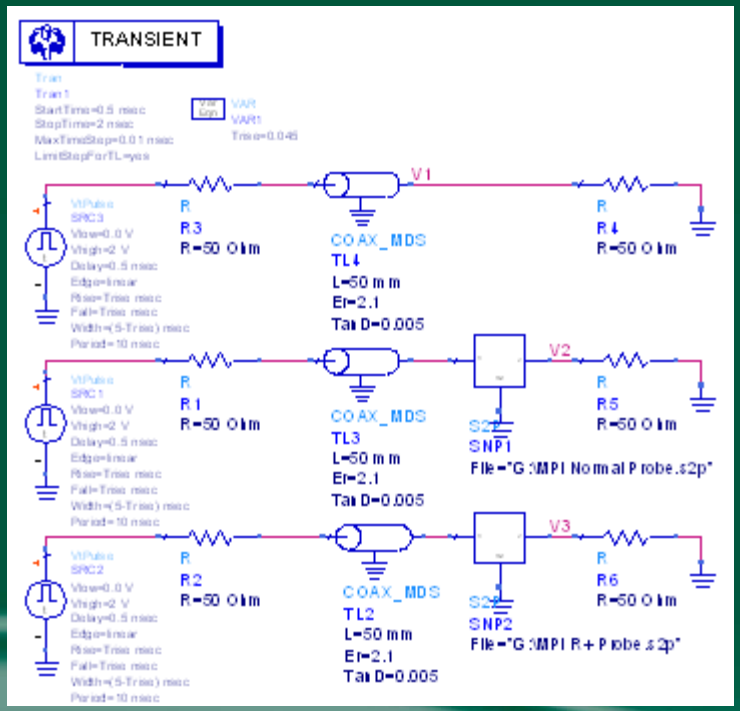
971.3 ps – 899.3 ps = 72 ps

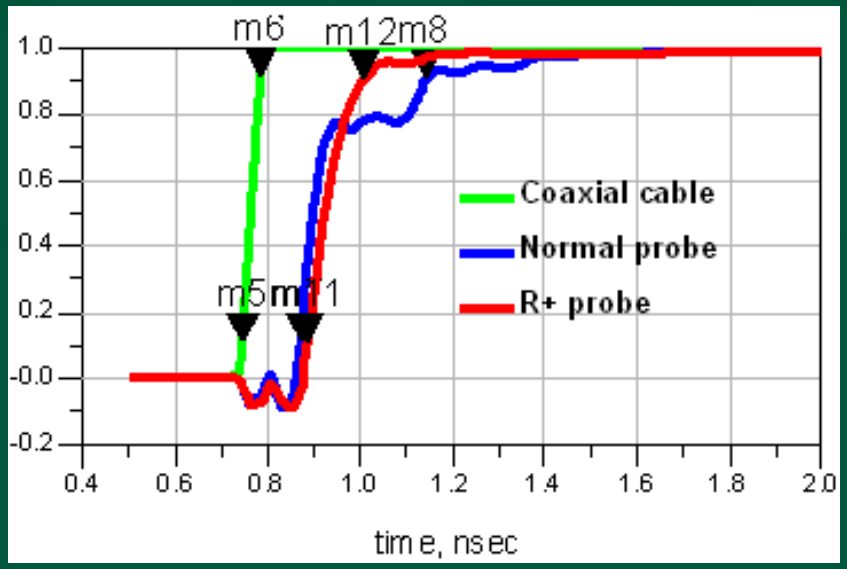
m1 time=879.3psec V2=203.3mV	m4 time=971.3psec V3=800.7mV
m2 time=1.106nsec V2=800.5mV	m9 time=751.3psec V1=218.6mV
m3 time=899.3psec V3=208.6mV	m10 time=778.3psec V1=803.0mV

Modeling & Analysis

- Analysis – Time Domain response

  Rising time 10~90% (R+ probe vs. normal probe)





Rising time for Coaxial cable (10%~90%)

783.3 ps – 746.3 ps = 37 ps

Rising time for Normal probe (10%~90%)

1143 ps – 746.3 ps = 396.7 ps

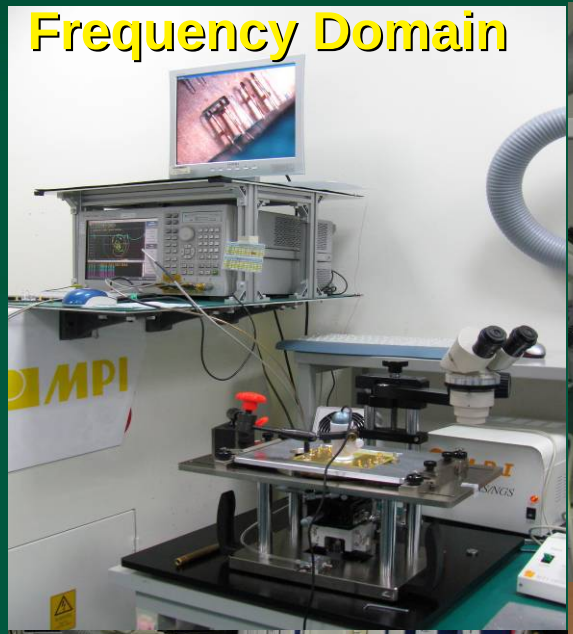
Rising time for R+ probe (10%~90%)

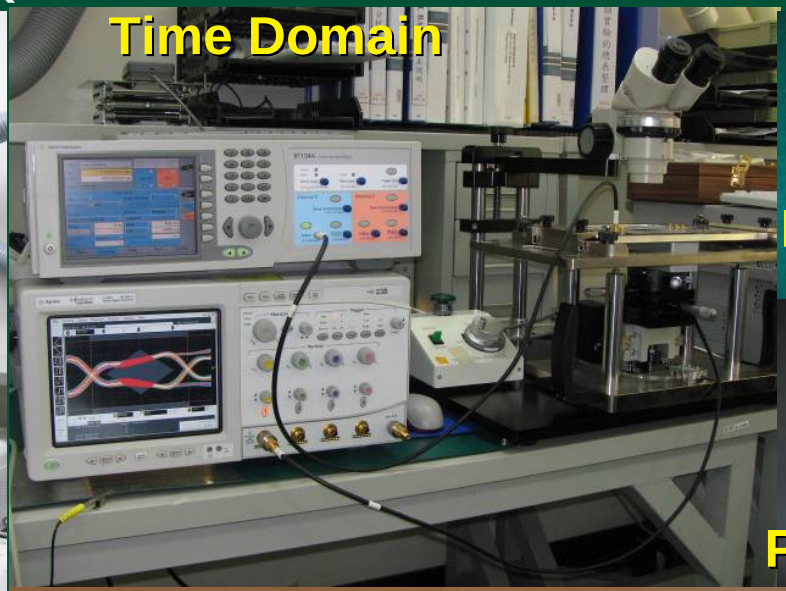
1007 ps – 889.3 ps = 117.7 ps

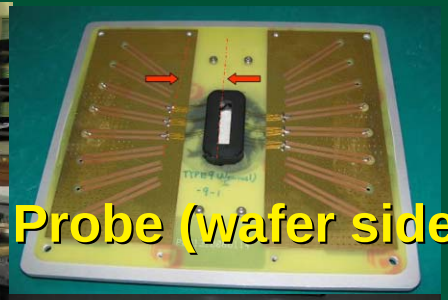
m7 time=871.3psec V2=109.6mV	m12 time=1.007nsec V3=900.2mV
m8 time=1.143nsec V2=902.6mV	m5 time=746.3psec V1=110.4mV
m11 time=889.3psec V3=107.9mV	m6 time=783.3psec V1=911.2mV

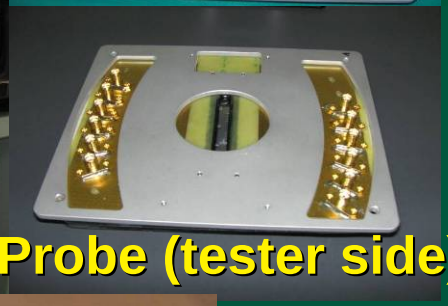
Experiment & Validation

- Experiment structure
- Calibration (SOLT+Port extension, TRL)





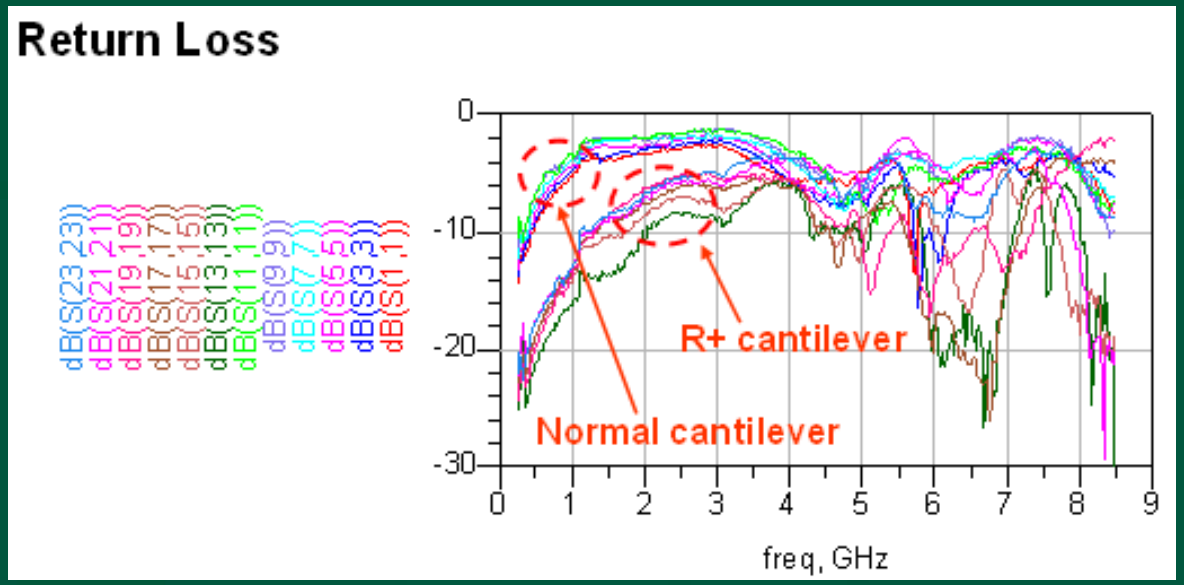


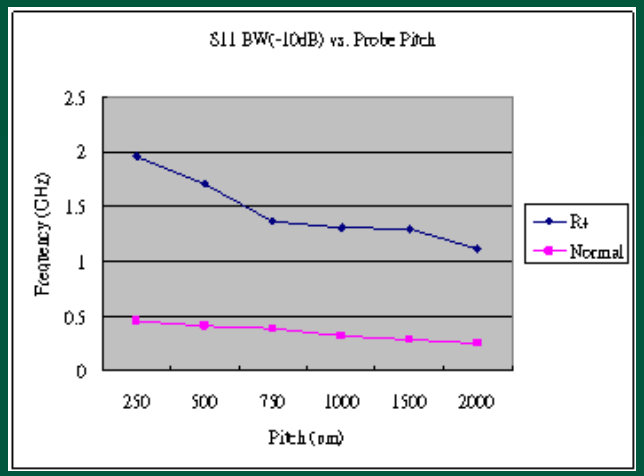


Experiment & Validation

- Frequency Domain response result

  S11 - R+ probe vs. normal probe

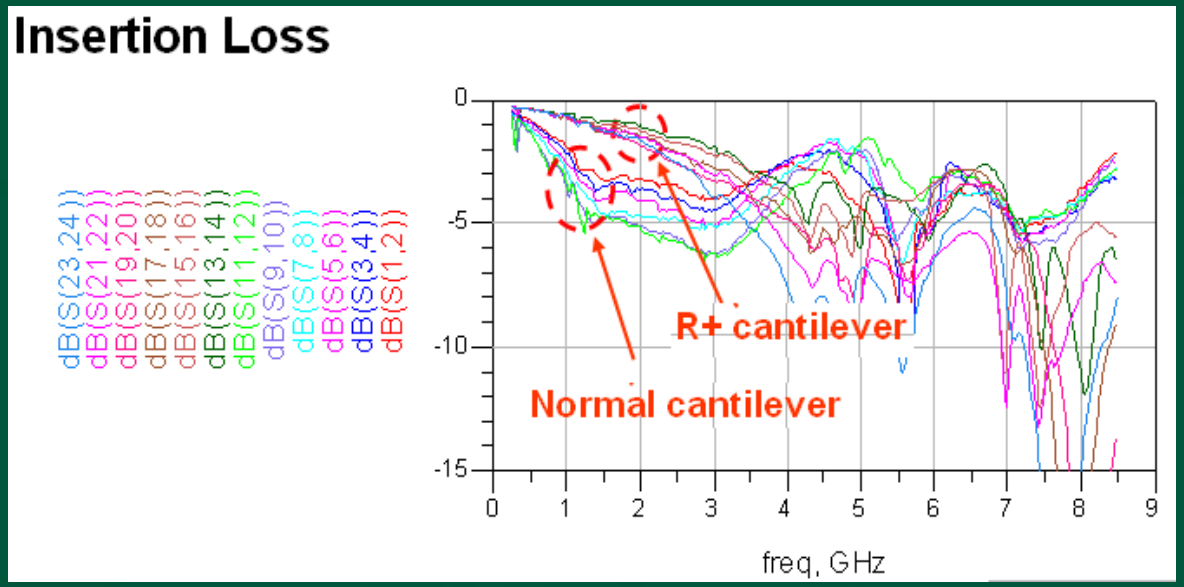


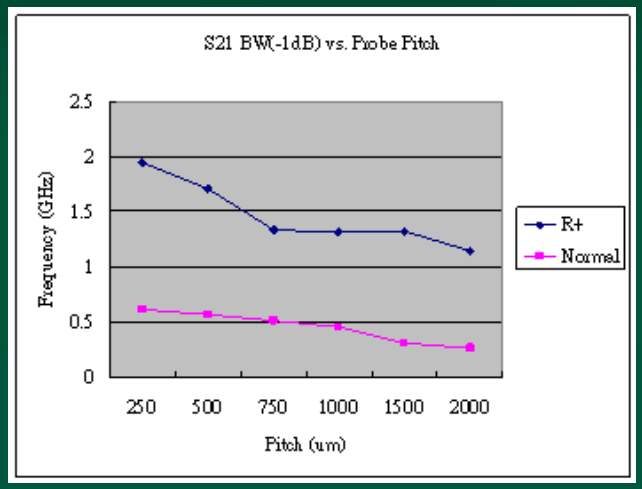


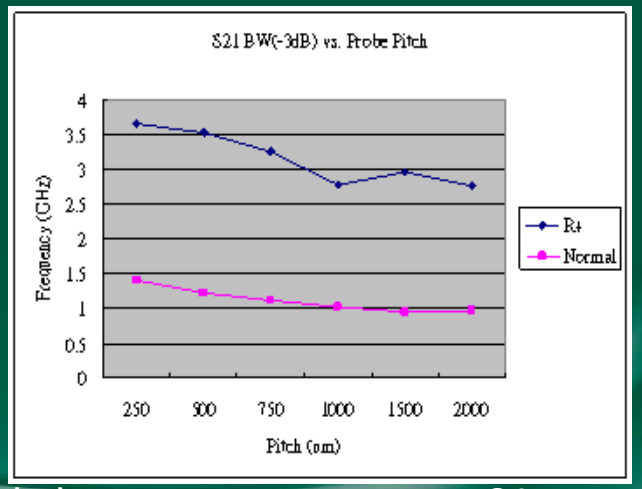
Experiment & Validation

- Frequency Domain response result

  S21 - R+ probe vs. normal probe

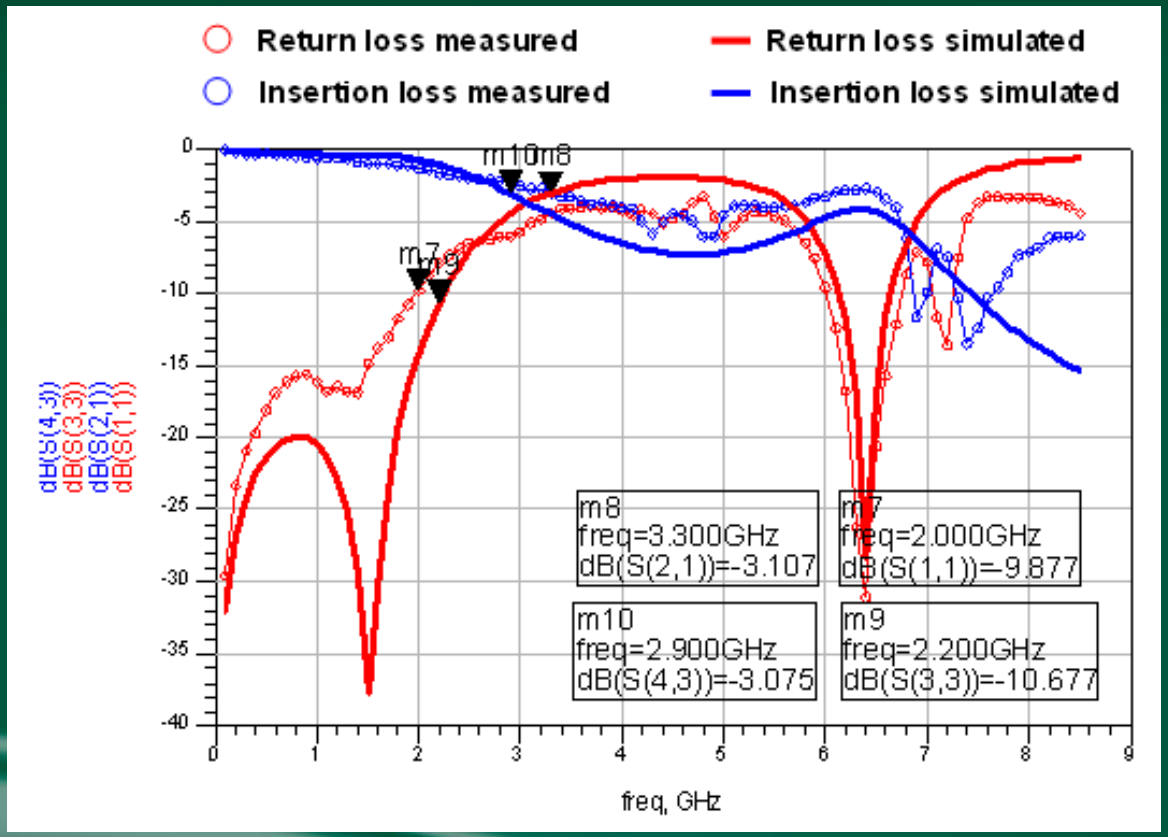






Experiment & Validation

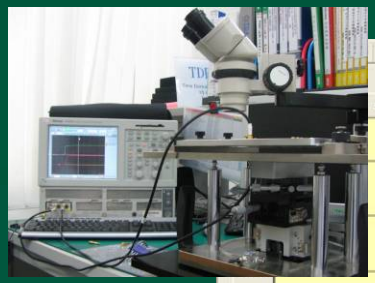
- Circuit model vs. experiment result

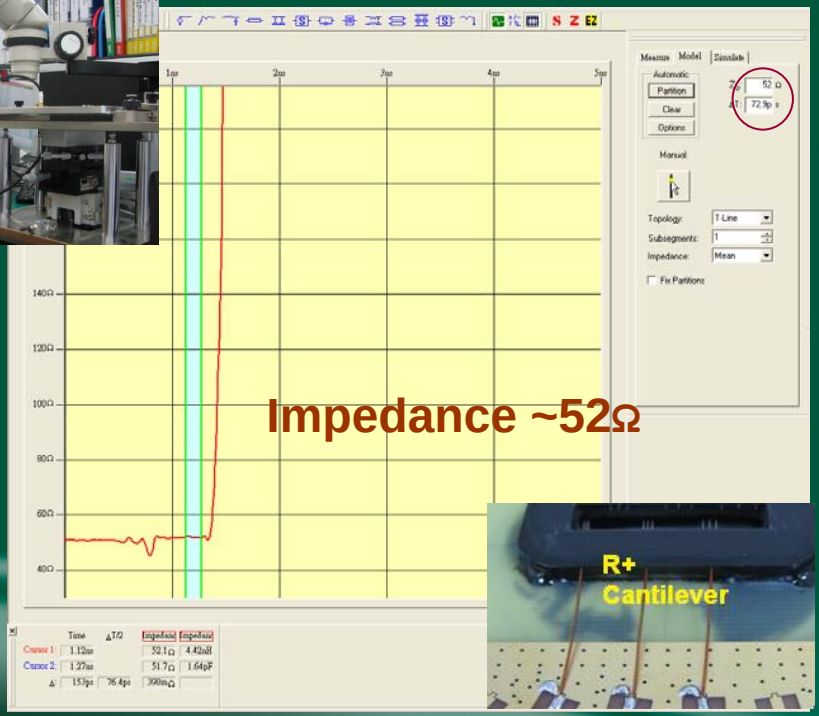


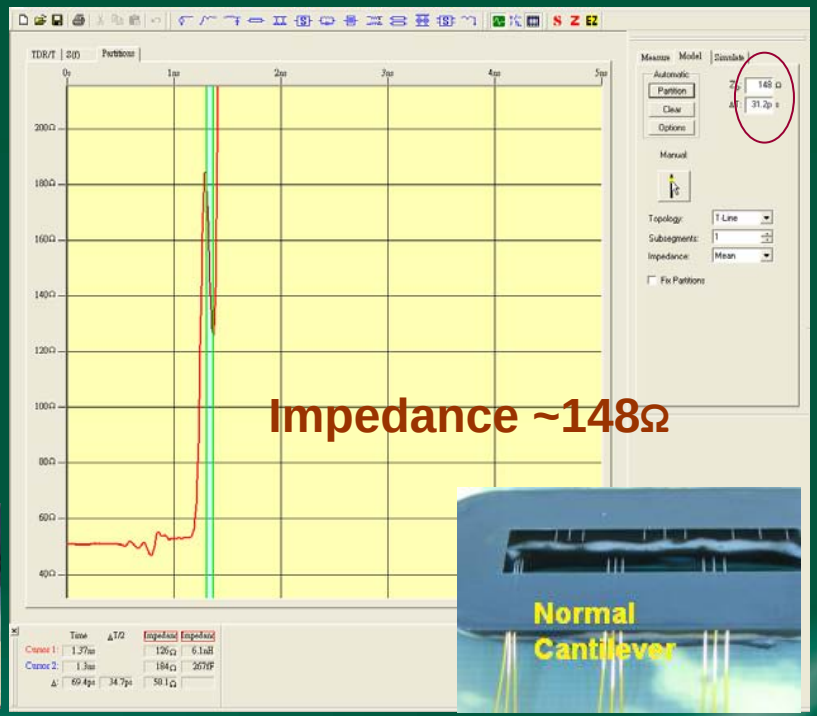
Experiment & Validation

- Time Domain response result

  Impedance (R+ probe vs. normal probe)







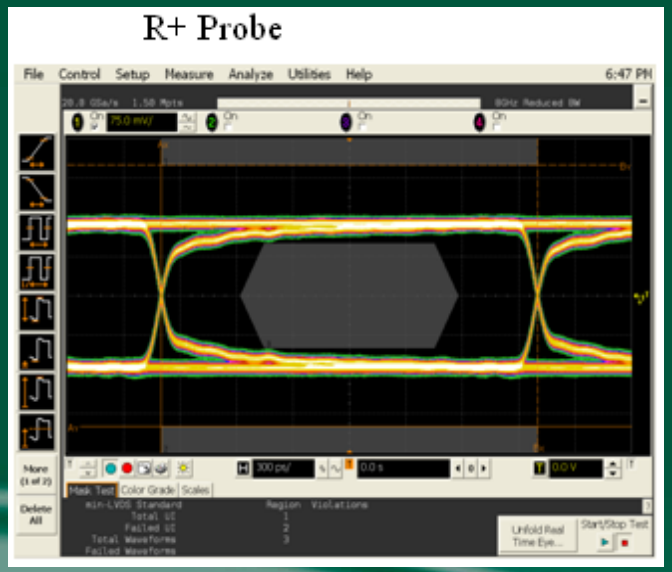
Experiment & Validation

- Time Domain response result

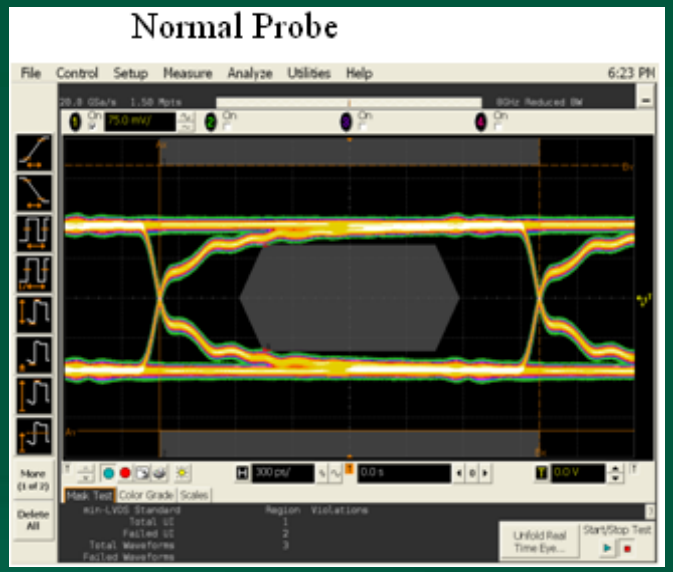
  LCD - mini-LVDS (R+ probe vs. normal probe)

Input Data Rate : 500 Mbps
Input Voltage: +/- 150 mV

R+ Probe



Normal Probe



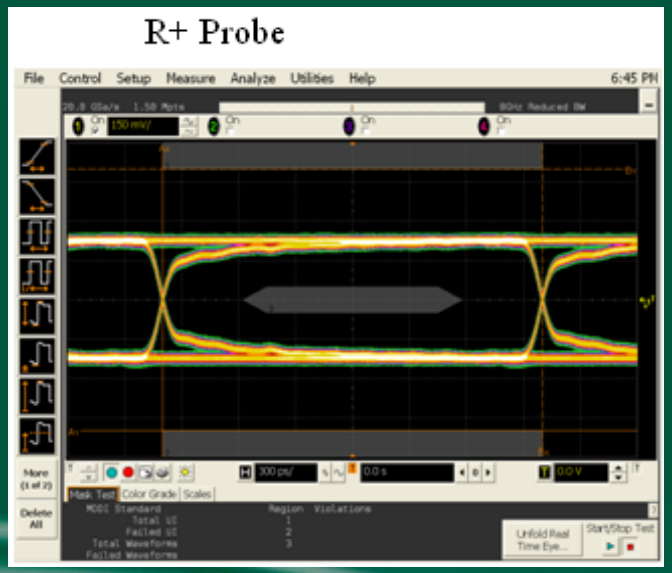
Experiment & Validation

- Time Domain response result

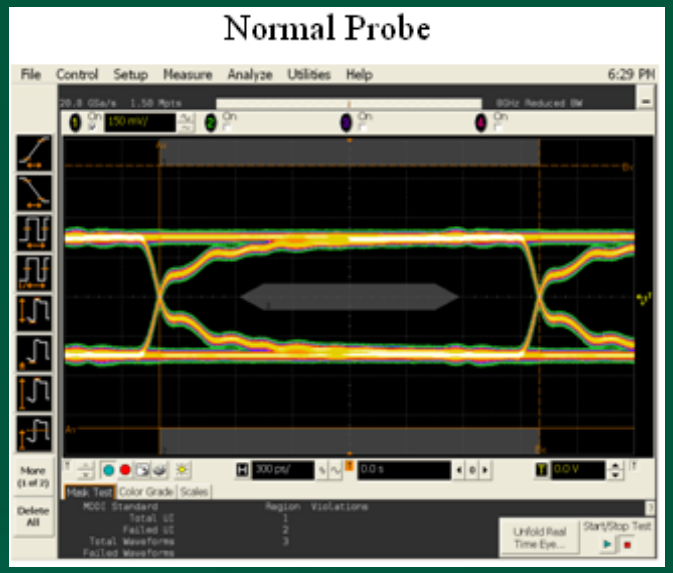
LCD – MDDI (R+ probe vs. normal probe)

Input Data Rate : 500 Mbps
Input Voltage: +/- 250 mV

R+ Probe



Normal Probe



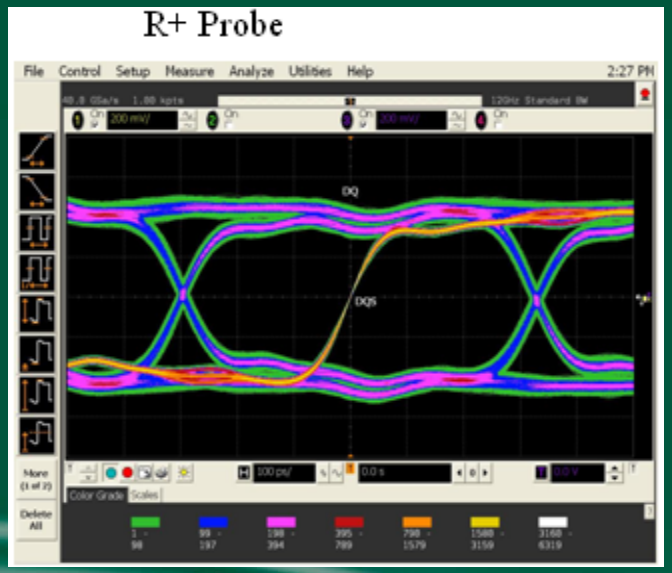
Experiment & Validation

- Time Domain response result

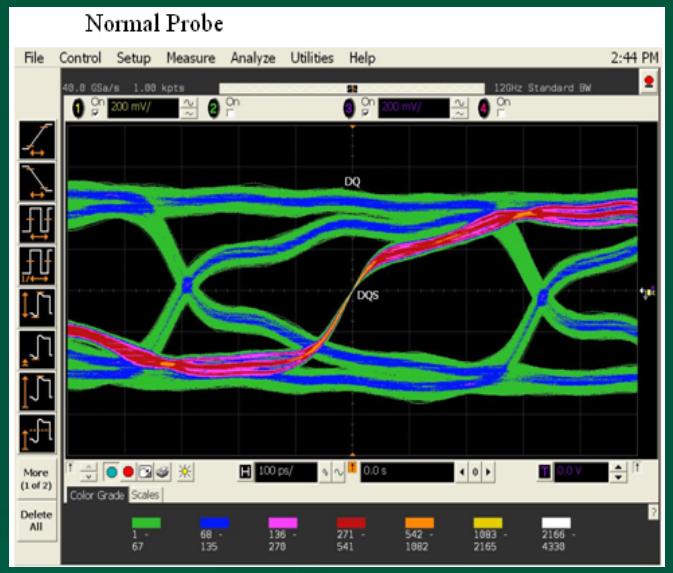
Memory - DDR-III (R+ probe vs. normal probe)

Input Data Rate : 1.6 Gbps
Input Voltage: +/- 1 V

R+ Probe



Normal Probe



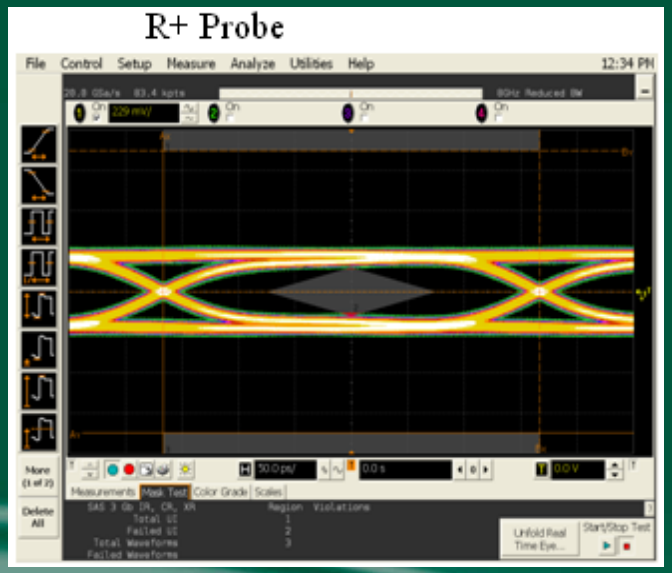
Experiment & Validation

- Time Domain response result

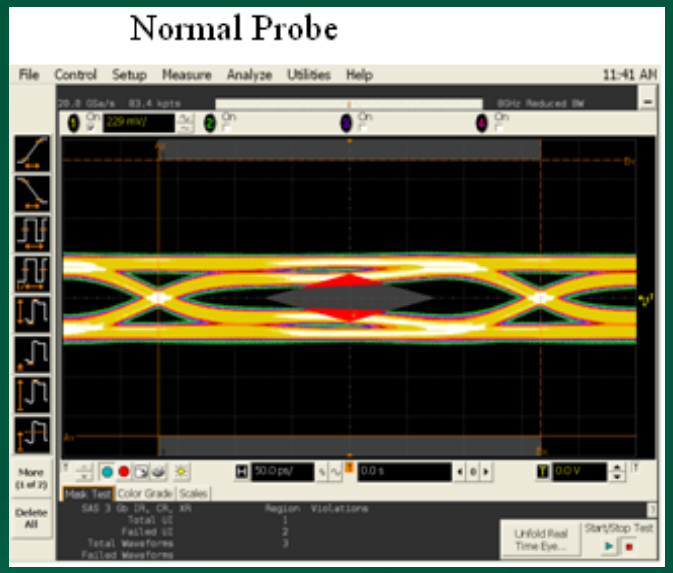
Logic - SATA-II (R+ probe vs. normal probe)

Input Data Rate : 3.0 Gbps
Input Voltage: +/- 250 mV

R+ Probe



Normal Probe



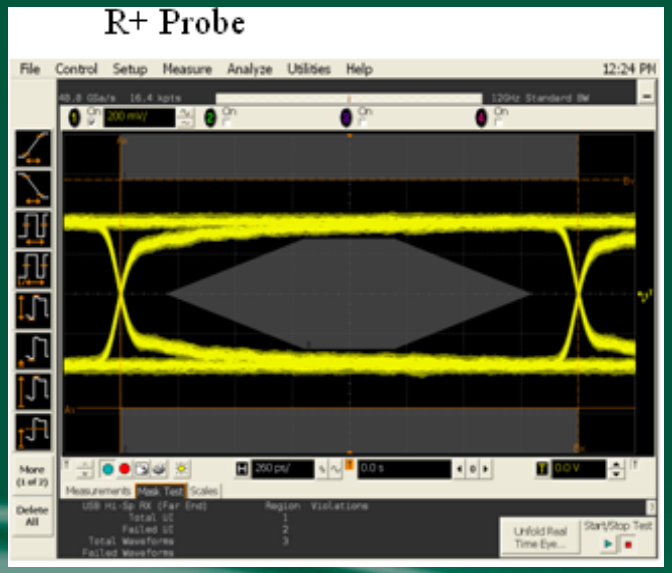
Experiment & Validation

- Time Domain response result

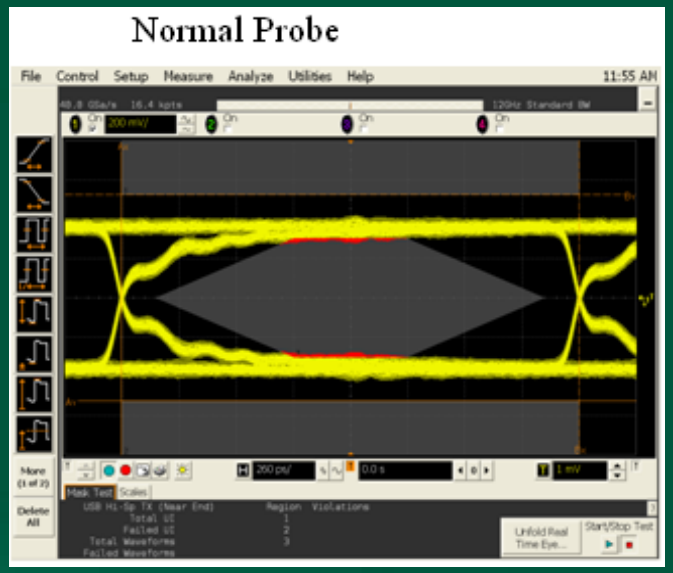
Logic - USB 2.0 (R+ probe vs. normal probe)

Input Data Rate : 480 Mbps
Input Voltage: +/- 500 mV

R+ Probe



Normal Probe



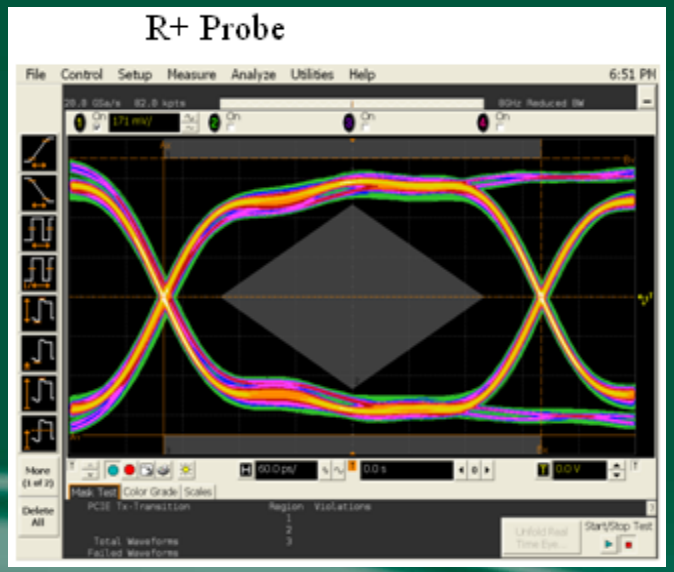
Experiment & Validation

- Time Domain response result

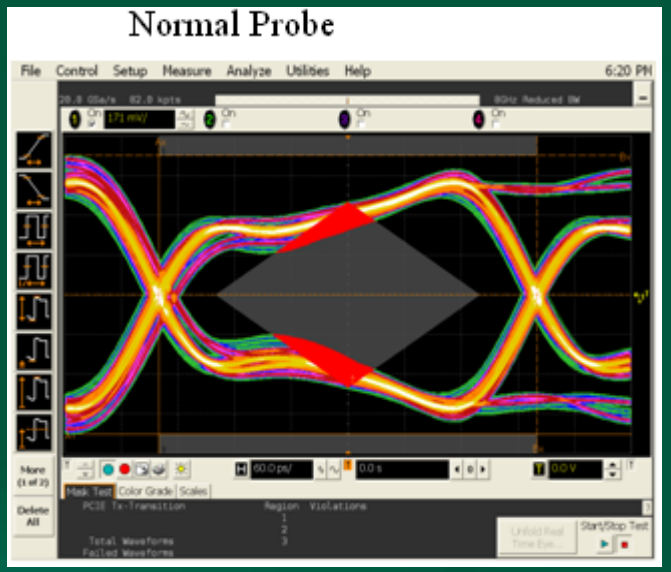
Logic - PCI Express-I (R+ probe vs. normal probe)

PCI E-I (Tx)
Input Data Rate : 2.5GMbps
Input Voltage: +/- 650 mV

R+ Probe



Normal Probe



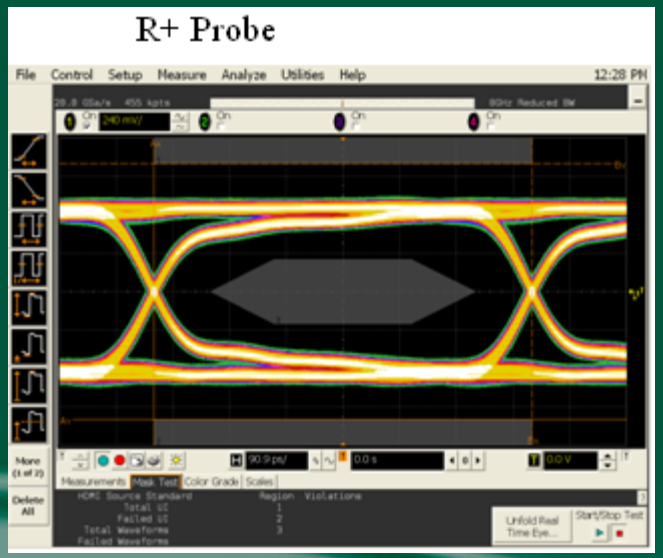
Experiment & Validation

- Time Domain response result

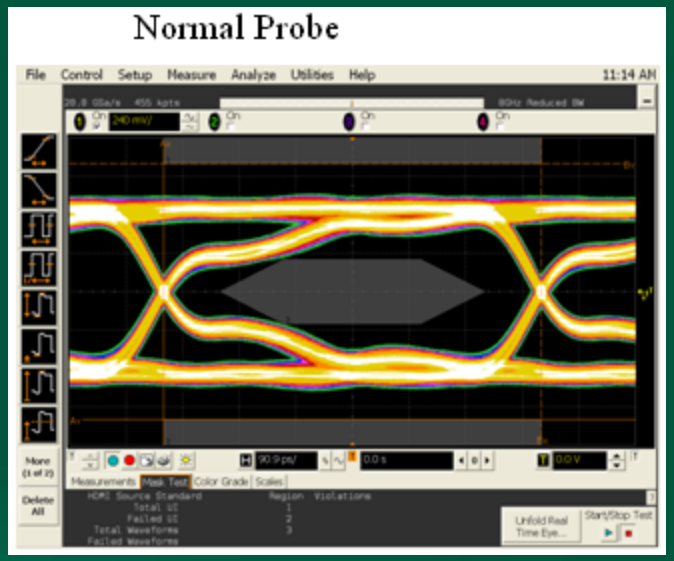
Logic - HDMI (R+ probe vs. normal probe)

HDMI (Source)
Input Data Rate : 2.5 Gbps
Input Voltage: +/- 400 mV

R+ Probe



Normal Probe



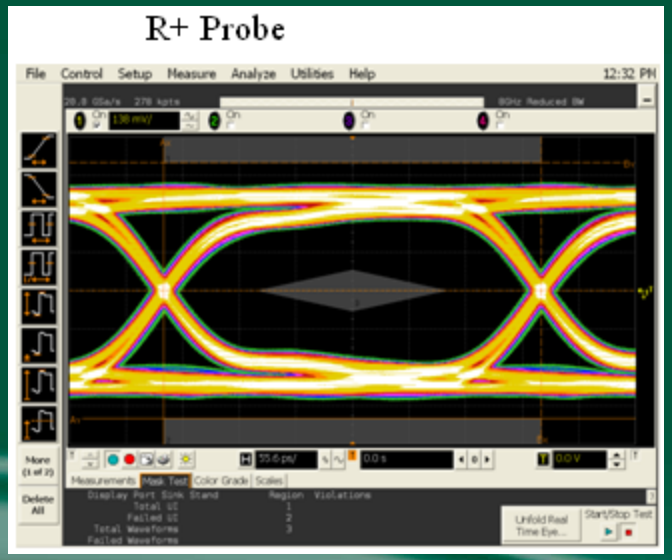
Experiment & Validation

- Time Domain response result

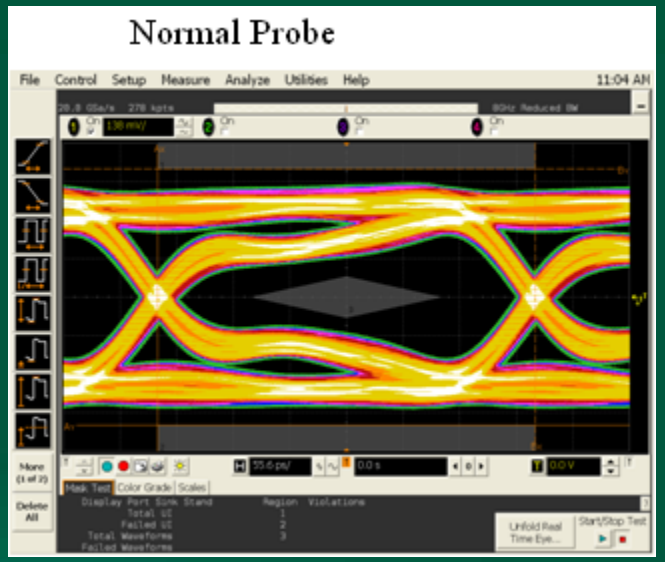
Logic - Display Port (R+ probe vs. normal probe)

Display Port (Sink)
Input Data Rate : 2.7 Gbps
Input Voltage: +/- 400 mV

R+ Probe



Normal Probe



Experiment & Validation

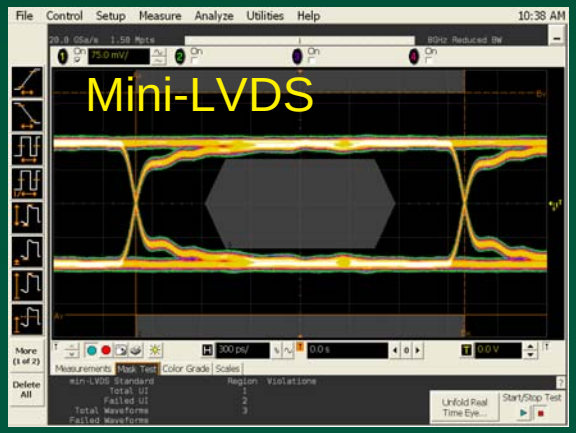
- Frequency Domain response result

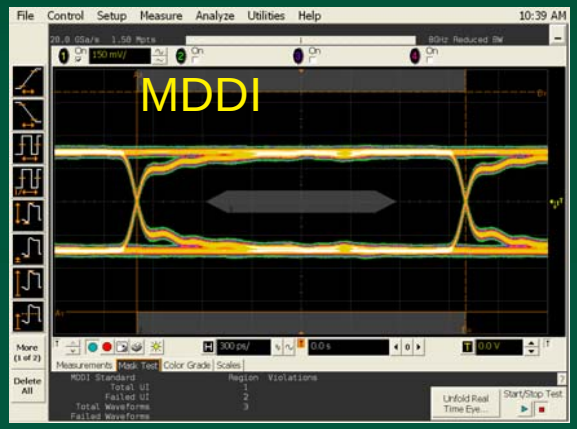
  R+ probe card (PCB + needle)

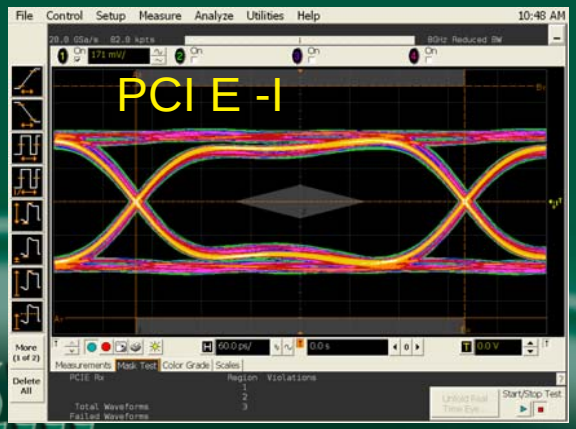
Experiment & Validation

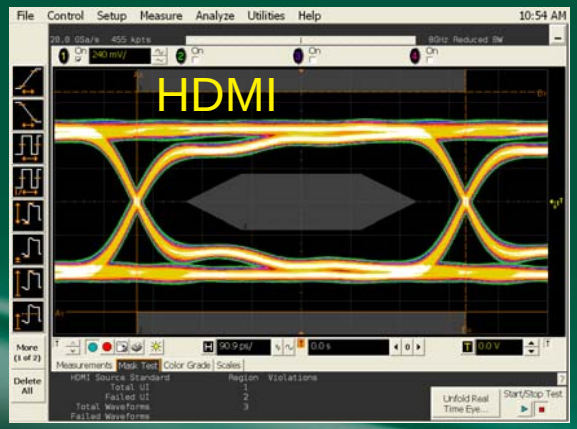
- Time Domain response result

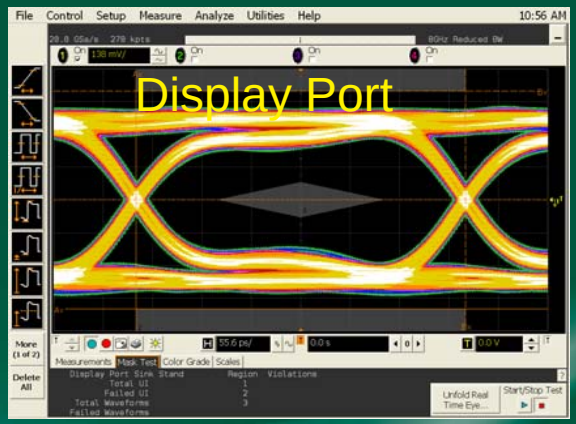
  R+ probe card (PCB + needle)











Customer Verification

- Shmoo comparison

  Interface: mini-LVDS

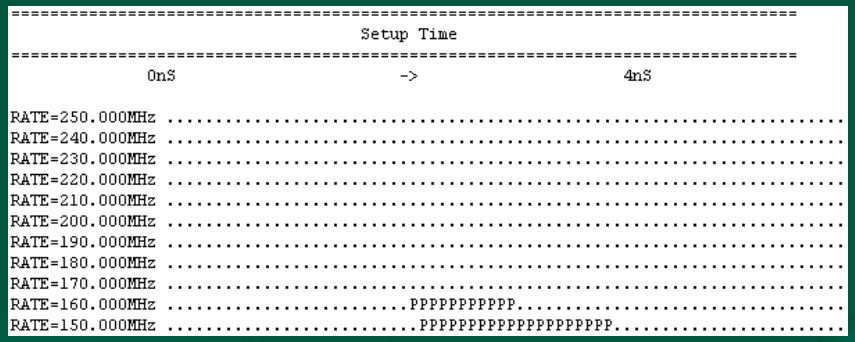
  Data Rate: 500 Mbps

  Application: Large Panel

R+ Cantilever Probe

VS.

Normal Cantilever Probe



Summary & Conclusion

- The probe is the main factor to decrease the frequency bandwidth performance of the cantilever probe card.
- The impedance compensated cantilever probe (R+) has successful been developed and validated the superior SI performance of the probe card. (Patent pending)
- Hundreds of R+ probe cards have been released to mass production of customer's high speed device testing.

Application & Specification

- $S21_{-3dB}$ Bandwidth: > 3GHz
- Inductance: 7~10 nH
- Fine pitch: < 35 um
- Real application of R+ probe cards ➔
  LCD (mini-LVDS, MDDI, …), Memory (DDR-III),
  Logic (USB2.0, PCI E-I, …)
- Lead-time < 2 weeks

Follow-On Work

- Improving the impedance compensated structure toward to the needle tip.
- Ongoing work ~ higher speed device testing probe card for RF application devices.

Acknowledgements

Great thanks to MPI (MJC Probe Inc.) teamwork :

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- Robert Kao
- Rex Liao

Q & A

Thank you very much .