IEEE SW Test Workshop

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A Challenge of 150k Probes on 300mm

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This work is under NEDO entrustment project.

NEDO [The New Energy and Industrial Technology Development Organization] is Japan's largest public R&D management organization.

Outline

1. What is ASET
2. Background
3. Target & issue
4. Probe detail
5. Countermeasure
6. Results & field data
7. Summary

about ASET?

- Association of Super-Advanced Electronics Technologies (ASET) is a consortium making up with Japanese electronics companies.
- Established :1996
- Purpose:

  Contribute to the enhancement of the competitiveness of Japanese industry and the establishment of an advanced information society.
- Activities:

  Research and develop on industry-wide fundamental technologies in the semiconductor and other advanced electronics technology fields as well as practical applications of research results.

http://www.aset.or.jp/english/e-index.html

Member Companies

ADVANTEST Corporation
DAI NIPPON PRINTING Co., Ltd
Elpida Memory, Inc.
FUJITSU Ltd.
Hitachi, Ltd.
Hitachi High-Technologies Corporation
Hitachi Kokusai Electric Inc.
HOYA Corporation
IBIDEN Co., Ltd.
IBM Japan
Intel Corporation
JEOL Ltd.
nac Image Technology Inc.
NEC Corporation
NEC Electronics Corporation
NIKON Corporation
NIPPON CONTROL SYSTEM Corporation
NuFlare Technology, Inc.
Panasonic Corporation
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SAMSUNG ELECTRONICS Co., Ltd
SHARP Corporation
SHINKO ELECTRIC INDUSTRIES Co., Ltd
SII Nano Technology Inc.
TOKYO ELECTRON Ltd.
TOPPAN PRINTING Co., Ltd
TOSHIBA Corporation
TOYOTA MOTOR Corporation
ULVAC, Inc.
YAMAICHI ELECTRONICS Co., Ltd
ZyCube Co., Ltd.

Total 32 Companies

Organization

3D-Integration Technology Research Dept.

Design Environment Technology Lab. (Tokyo)	Chip Test Technology Lab. (Kawasaki, JAPAN)	3D-Integration Basic Technology Lab. (Hachioji)
6 Companies	ADVANTEST Panasonic SHARP TOKYO ELECTRON YAMAICHI ELECTRONICS The Univ. of Tokyo Toyama Prefectural Univ. 5 Companies/ 2 University	11 Companies

Background

Why is Known Good Die (KGD) necessary?

3D-SiC Using many Chips (Dies)

If Yield of Die is low

⇒ Yield of 3D-SiC falls in proportion to the Yield of Dies, Suddenly

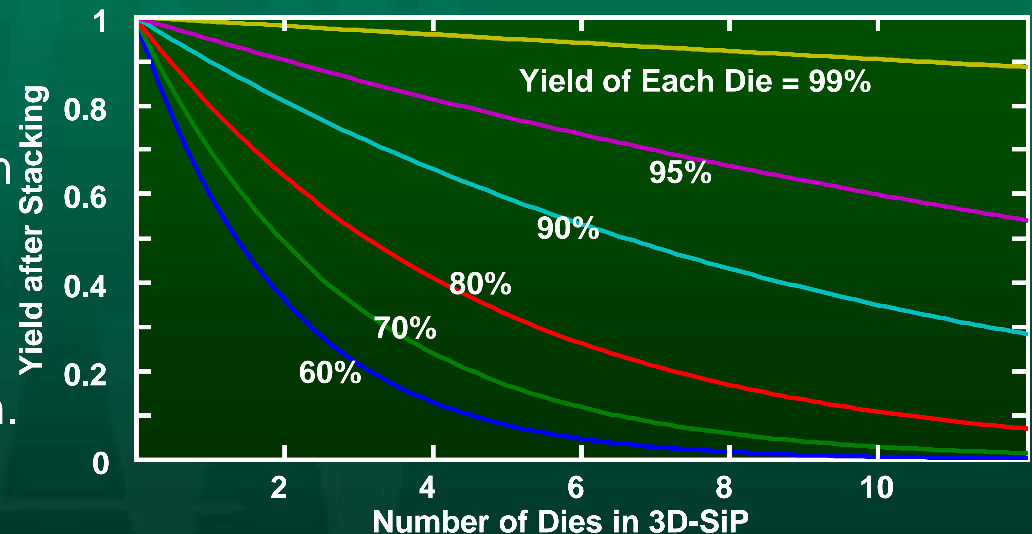
For getting KGD,

It is necessary to satisfy two condition.

1) At speed test on wafer

2) Wafer or Die Level Burn-in

〔yield of each die vs. after Stacking 〕



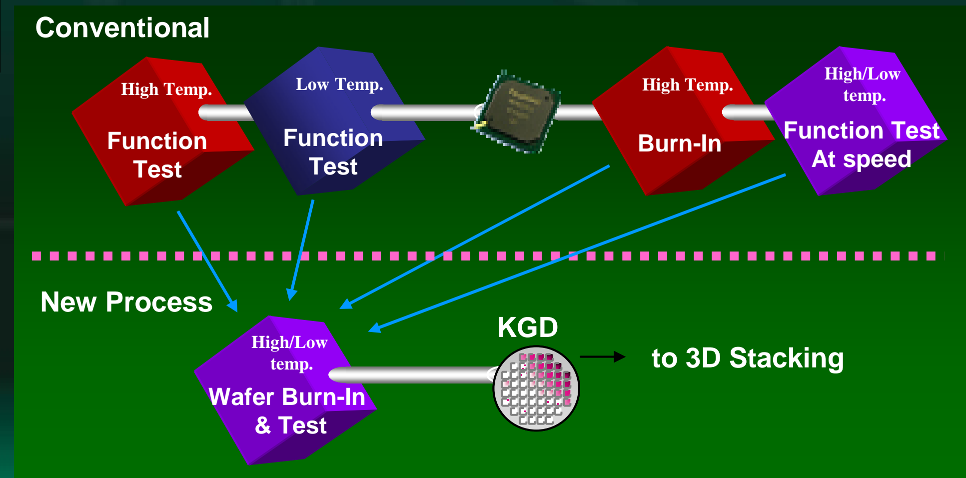
Why is 1-TD Full-Wafer Contactor Studied?

High-speed prove card and die-level sockets are very expensive.

It is effective for cost reduction to perform burn-in and test, simultaneously.

The 1-TD Probe enables Integration of Wafer-Wafer and Wafer-Die.

〔new process for KGD 〕



Study about Target Device

The number of pads and Power per one wafer

Device Type	Number of chips/wafer	P/S and grand number/wafer	Signal numbers/wafer	Power
SoC high end	500	VDD 256 ~ / chip GND 256 ~ / chip	I/O 512 ~ / chip	~ 10kA ~ 30kW
		Total 250,000 / wafer	Total 250,000 / wafer	
SoC middle class	1000 ~ 2000	VDD 100 ~ / chip GND 100 ~ / chip	I/O 256 ~ 512 / chip	~ 5kA ~ 15kW
		Total 400,000 / wafer	Total 500,000 / wafer	
SoC low end	3000 ~ 5000	VDD 50 ~ / chip GND 50 ~ / chip	I/O 256 ~ / chip	~ 5kA ~ 10kW
		Total 500,000 / wafer	Total 750,000 / wafer	
DRAM	500 ~ 1500	VDD 25 ~ / chip GND 25 ~ / chip	Dr. 30 ~ / chip I/O 15 ~ / chip	~ 300A ~ 400W
		Total 75,000 / wafer	Total 68,000 /wafer	
Flash memory	500 ~ 1500	VDD 10 ~ / chip GND 10 ~ / chip	Dr. 10 ~ / chip I/O 10~ / chip	~ 100A ~ 200W
		Total 30,000 / wafer	Total 60,000 /wafer	

Source : Prepared by Chip Test Research Laboratory using ITRS's roadmap, etc

It was decided the object device as a memory and SoC less than middle class.
And it is clear that number of contact pads have to be reduced.

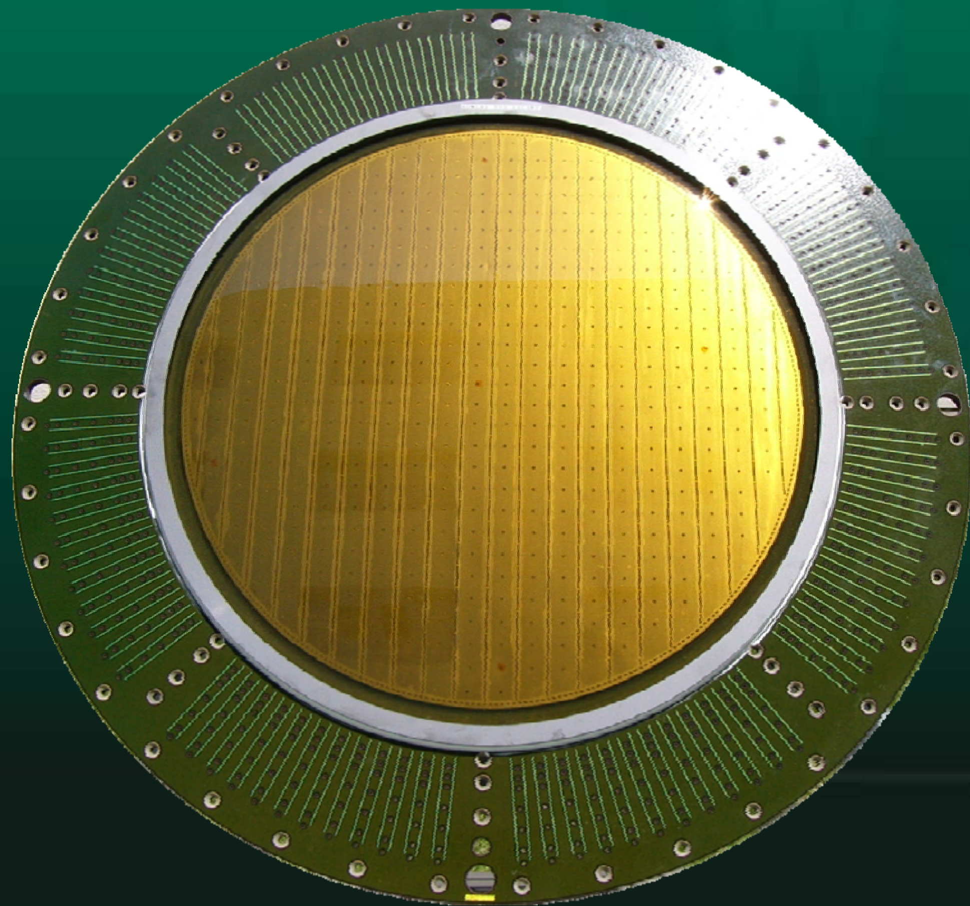
Target of the probe Card

- Wafer Size : 300mm
- Probe Quantity : 150k
- Pad Size : 60μm
- Pad Pitch : min 90μm
- Current : 5kA / wafer
- Power : 15kw / wafer
- Temperature : -40 – 125 deg. C

The Issue for 150k contact on 300mm

- The total load on 300mm wafer is
  7,000N (700 kg) or more
- Uniform pressure in the 300mm area
- Stable contacts without scrub

150k Probe Card Over View



For Memory & Logic

150k Bumps

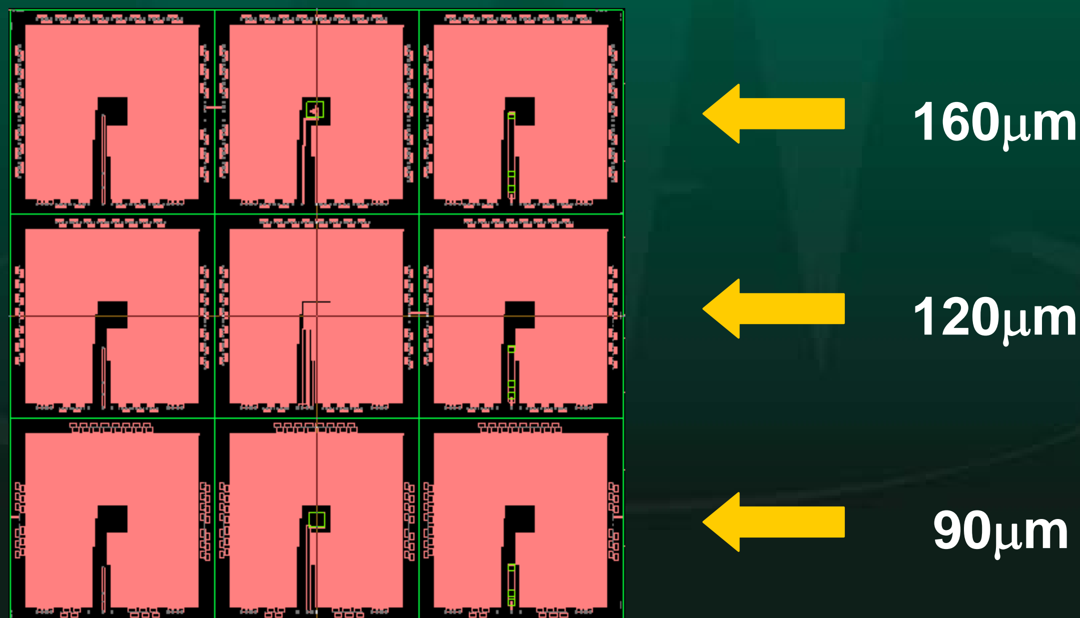
Min. Pitch 90μm

Membrane with Bumps

Pressurization using atmosphere

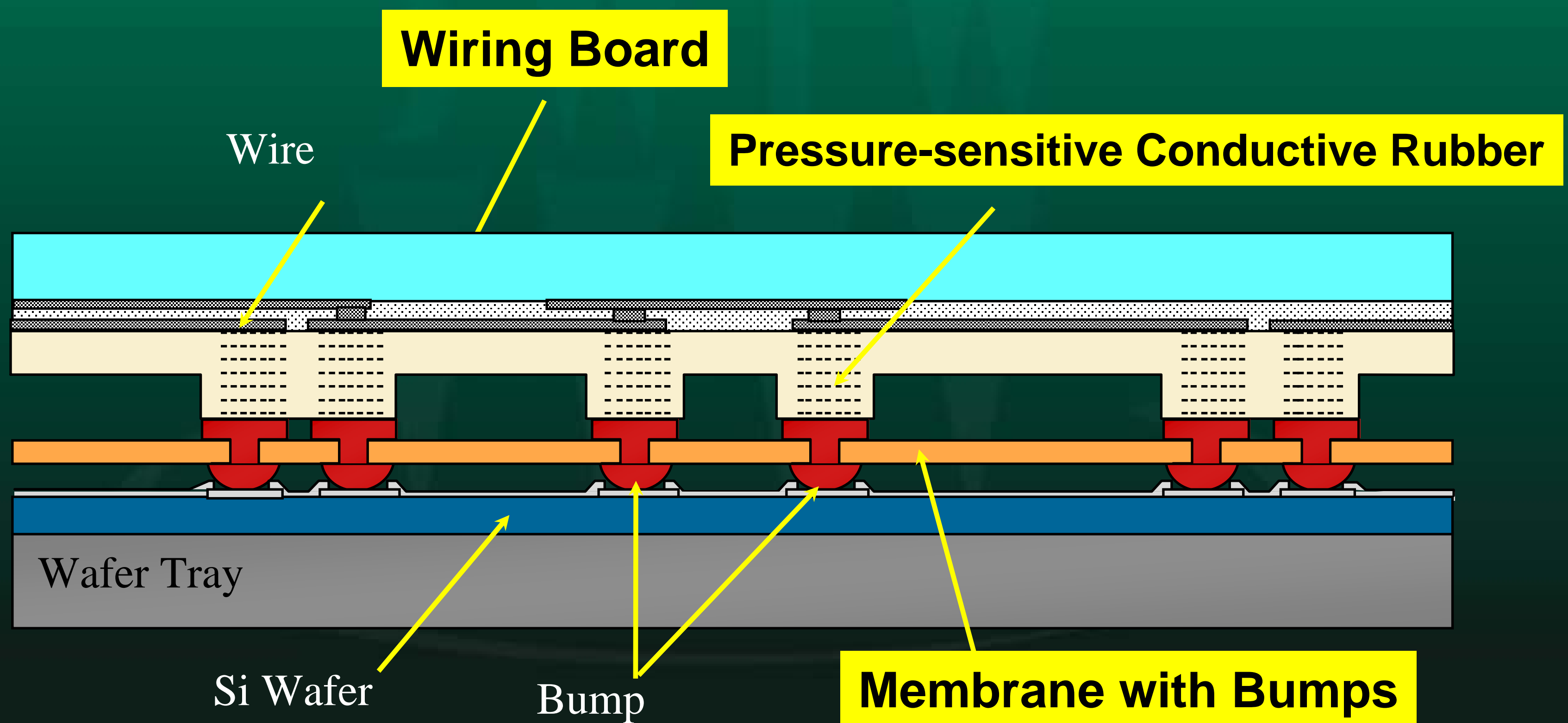
150k Probe Card Detail

Pad Pitch	160μm	120μm	90μm	Total
Bumps	49,147	51,322	50,114	150,583

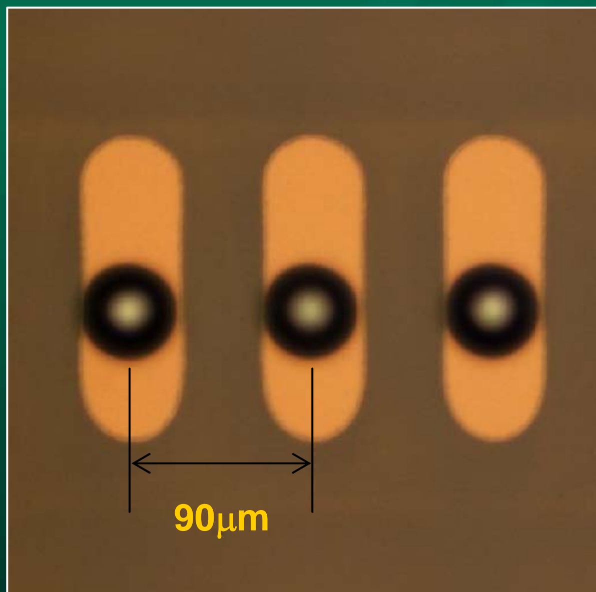


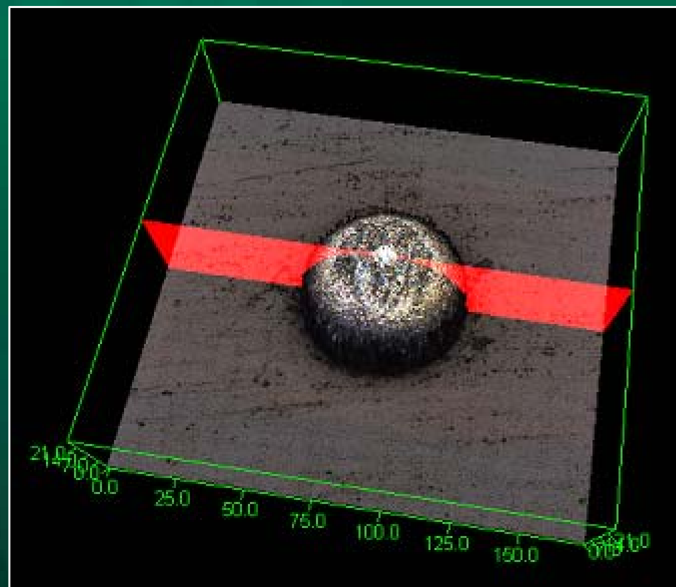
TEG Pattern for evaluation

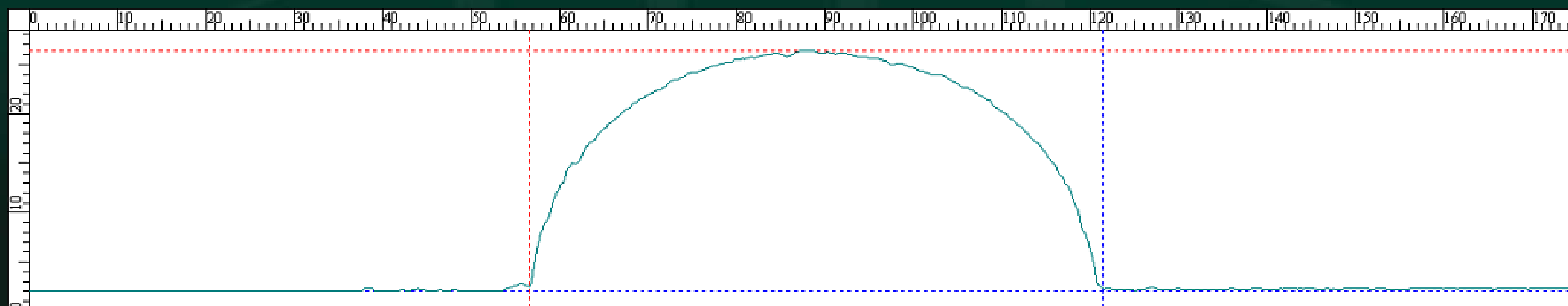
Detailed Structure of Probe



Contact Bump



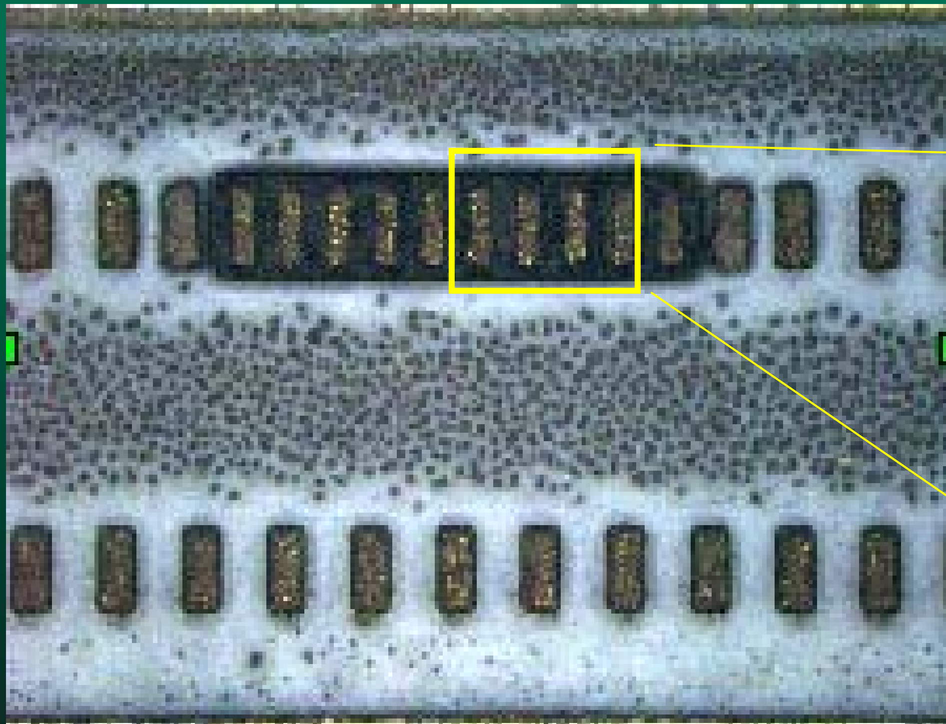


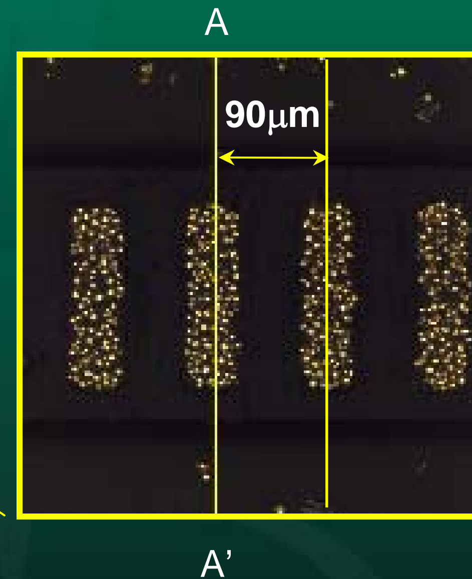


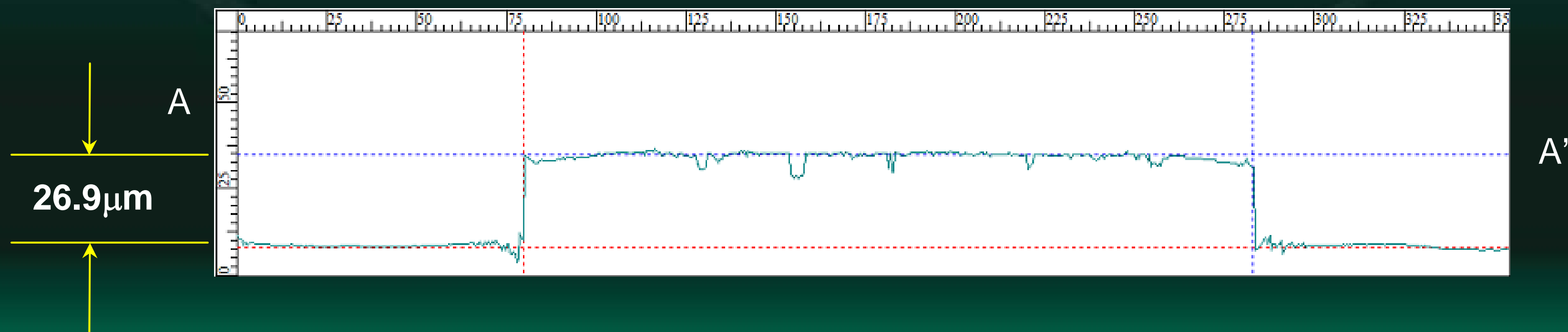
始点	終点	計測結果	近似値R
X = 56.530 um	X = 121.424 um	高度差 : 24.330 um	中心 X : ------
Y = 87.882 um	Y = 87.882 um	平面距離 : 64.894 um	中心 Y : ------
Z = 26.390 um	Z = 2.060 um	空間距離 : 69.305 um	中心 Z : ------
		角度 : -20.552 deg	半径 : ------

Pressure-sensitive Conductive Rubber

JMT



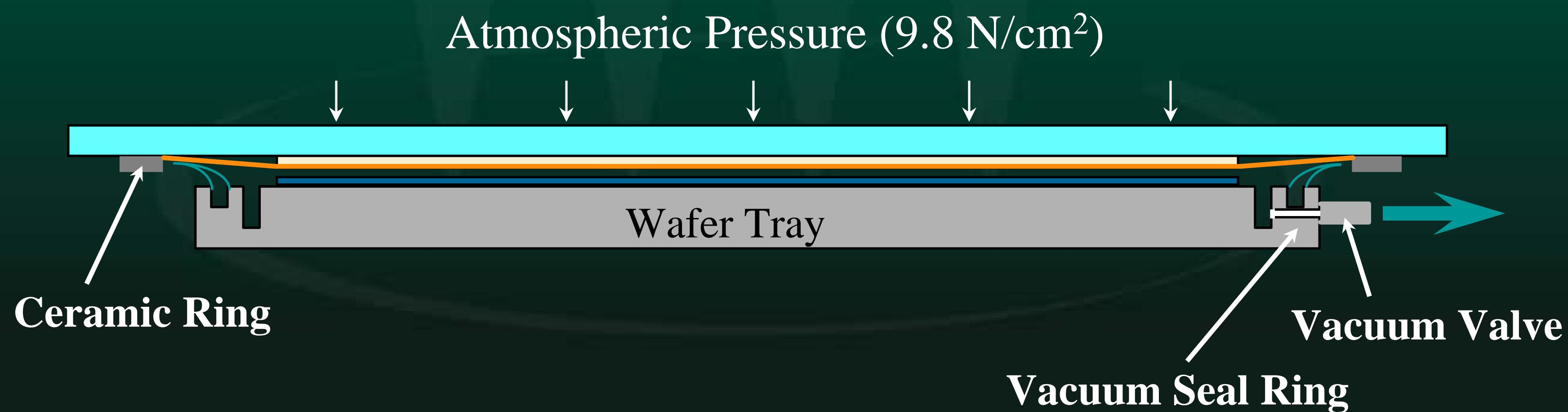




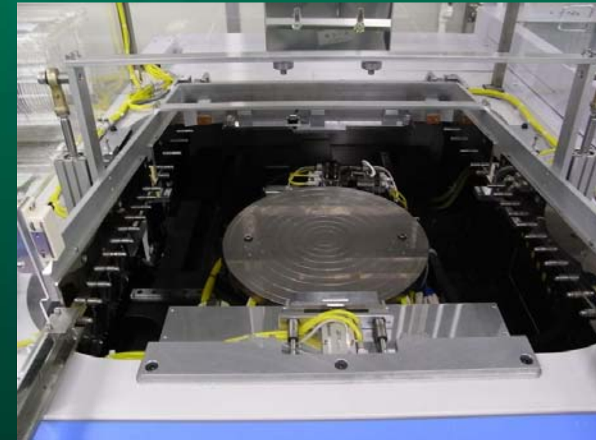
Atmospheric Pressure

Total load :

$15.3[cm]^2 \times \pi \times 97[kPa] = 7{,}129\ [N]$



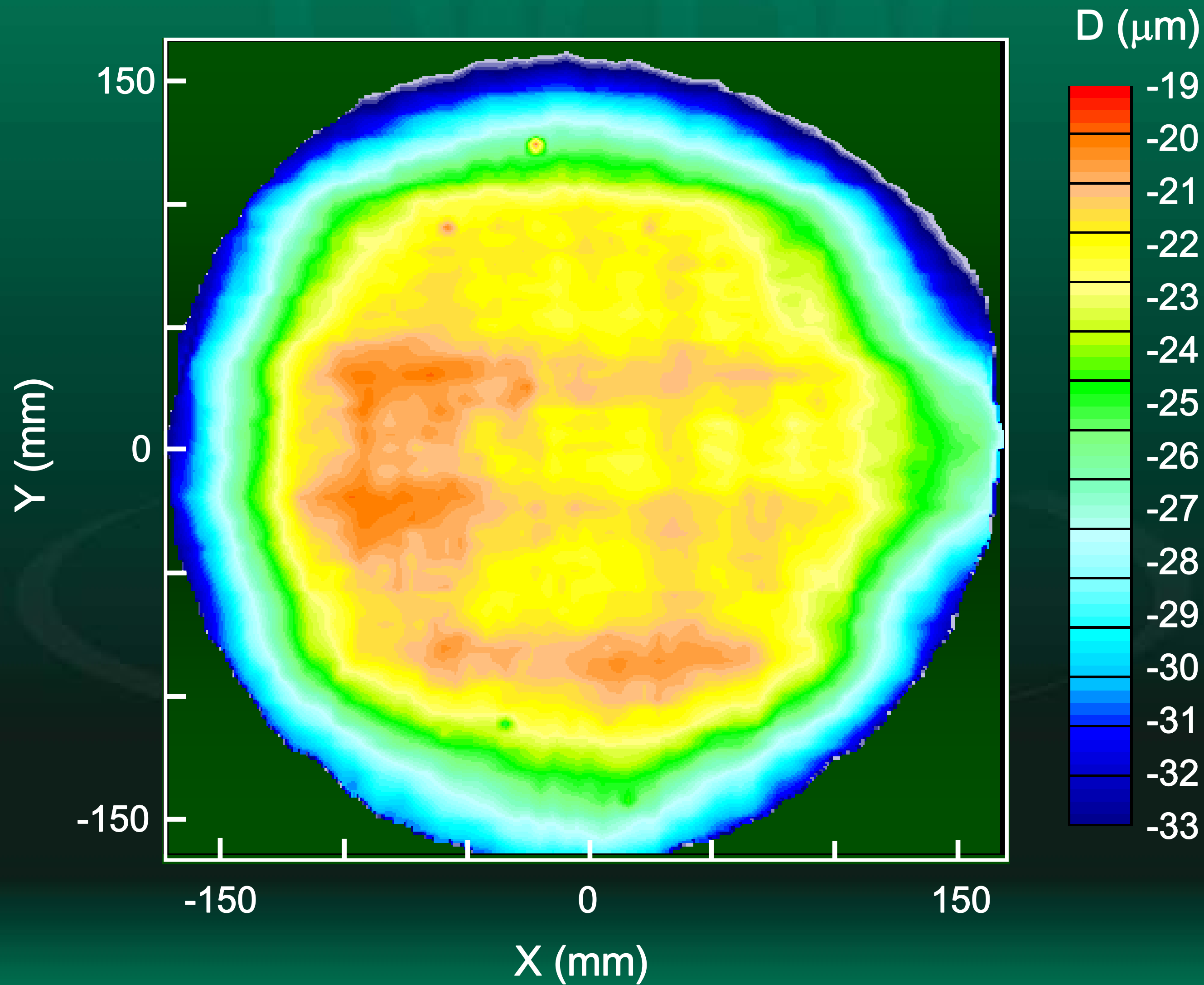
Alignment Station



Base Machine : TSK UF300
Max. z-load : 100kg

Alignment Station by TSK

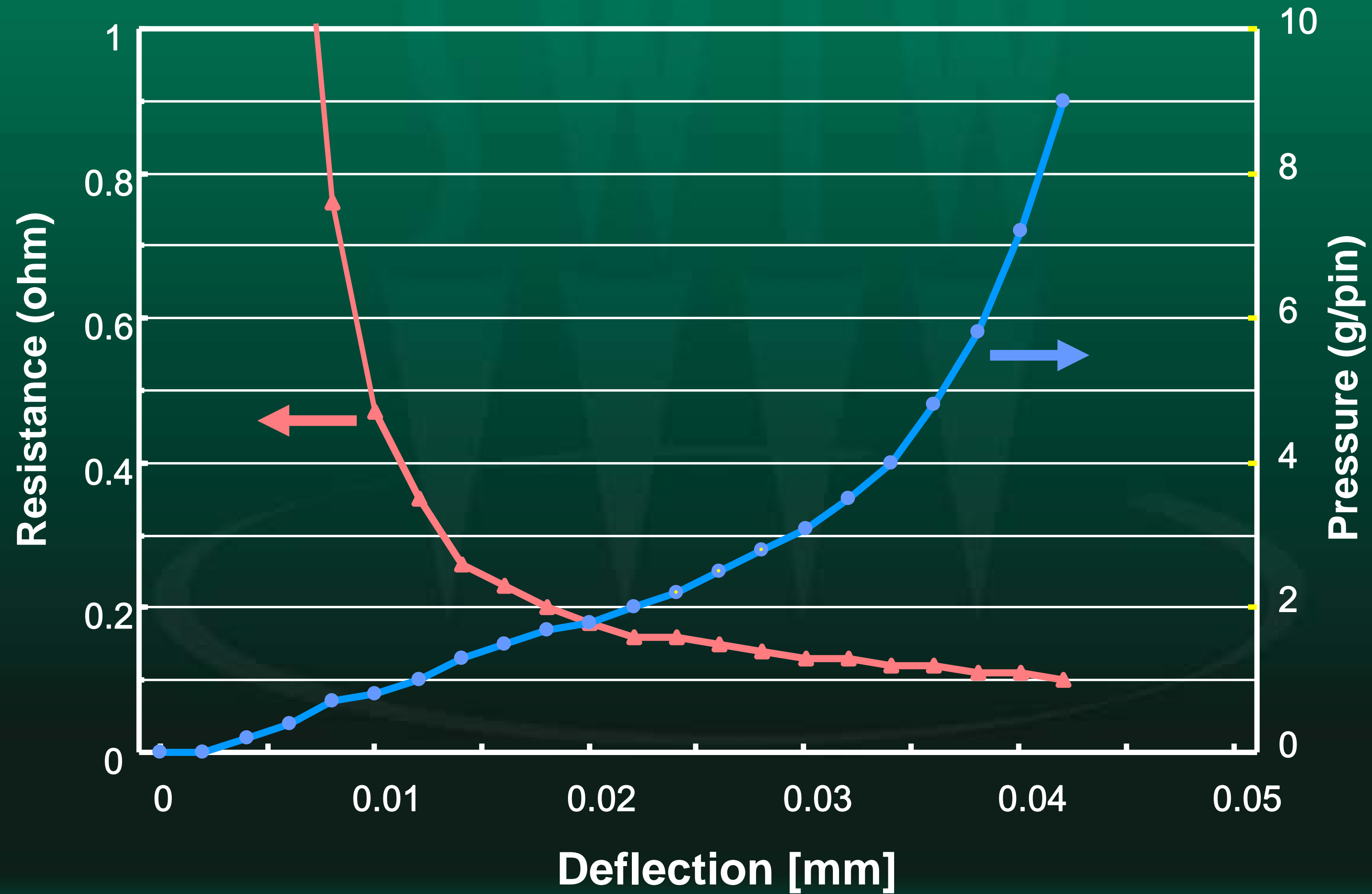
PCB Bend Characteristic



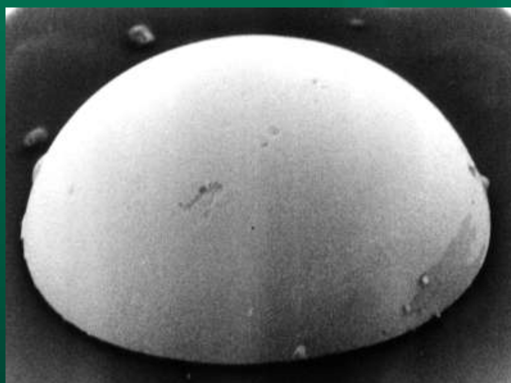
PCB Deflection

Chart: Deflection [um] vs. Distance from Center [mm]

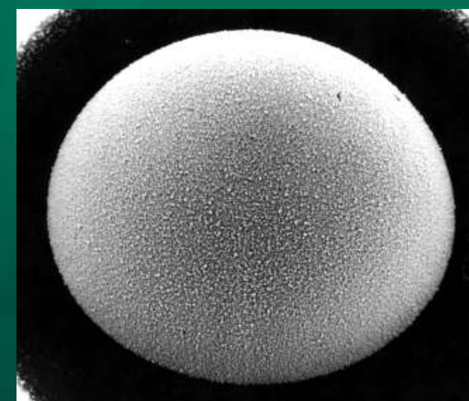
PCR Characteristic

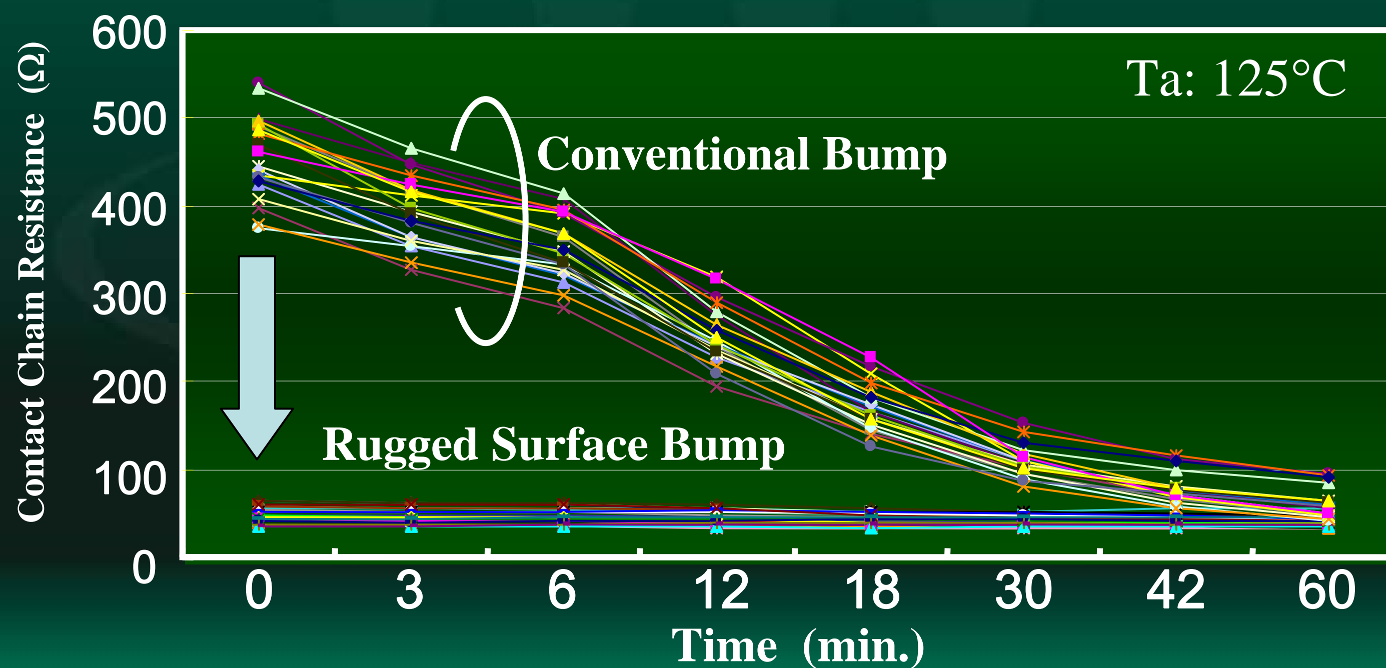


Bump surface



Rugged Surface





150k Contact Results

Pad Pitch	160μm	120μm	90μm	Total w/o dummy
Bumps*	49,147	51,322	50,114	150,583
Load [mN] / Bumps	39	39	39	
Load [N] / Wafer				5,850
Result	Bump contact + PCR +Circuit = 100 ~ 200 [mΩ]/ pin			○

* Count out Dummy Bumps of out side

History

Bump Q'ty

150k
80k
60k
40k
20k

1999
2003
2007
2009

13g / Bump
10g / bump
8g / Bump
4g / Bump

300mm Wafer
200mm Wafer

WB300HP
Panasonic

Summary

- Stable contacts have been achieved by 150k bumps.
- The total load on 300mm wafer is 7,000N or more, which is achieved by using a uniform atmospheric pressure method .
- Probe card does not need special structure (e.g. stiffener) nor special alignment system.

This leads to a realization of a cost effective and new concept test system.

Acknowledgements

Special Thanks to :

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Panasonic : Mr. Miyake
ASET : Mr. Inagaki , Mr. Kada,
and All of Chip Test Technology Lab. members

This work was developed
based on the WLBI technology of Panasonic.