IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 7-10, 2009

San Diego, CA

Optimization of Wafer Level Test Hardware using Signal Integrity Simulation

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A DOVER COMPANY

Agenda

- **Industry Drivers**
- **Wafer Scale Test Interface Simulation**
- **Simulation Techniques**
- **Capturing Interfaces**
- **Full Test Interface Simulation Example**
  - Components that most impact performance
  - Optimization of interfaces
  - Full system results

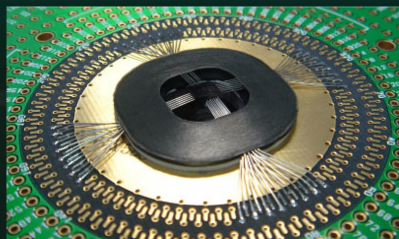
Wafer Scale Test - Industry Drivers

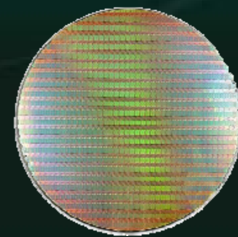
- Industry Expectations
  - Short lead-times
  - Low cost - varies with complexity
  - High quality - First Pass Success!
- Challenges
  - DUT complexity - faster, smaller, integrated
  - Test hardware complexity - fine pitch, low inductance, matched impedance

Don't let this happen to you

Lowering the Cost of Test

- **Eliminate Guesswork Through Signal Integrity Simulation**
  - Ensure performance prior to fabrication
  - Eliminate re-spins and time consuming lab analysis
- **Simulate All Structures in the Path from the Tester to the DUT**

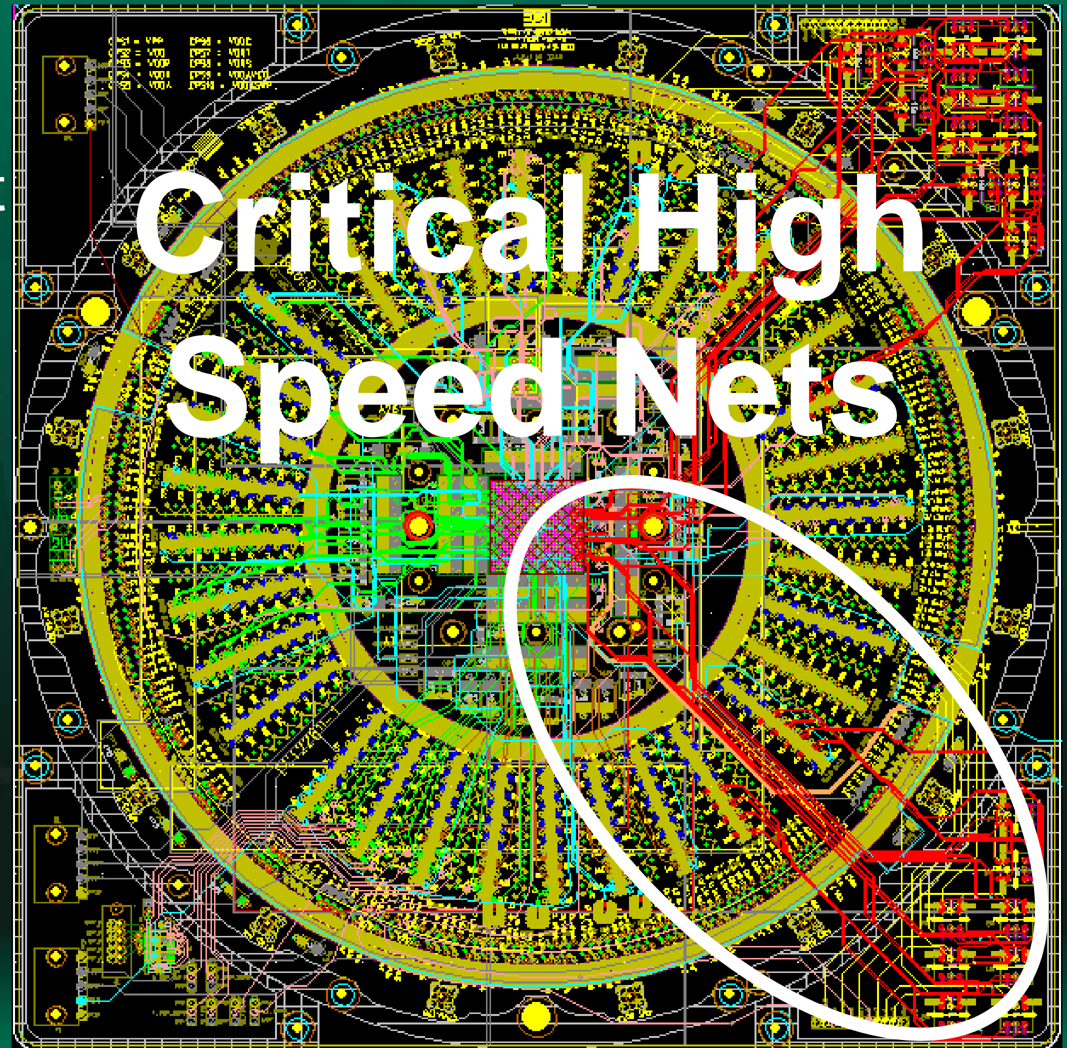




Tester *Probe Card* *IC Device (DUT)*

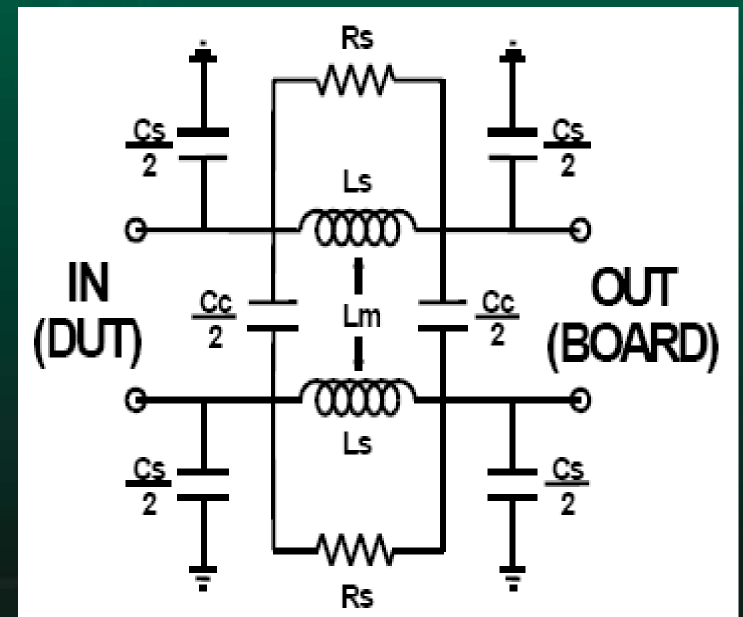
Test Interface Simulation

- **Focus on Critical Nets**
  - Full PCB signal integrity simulation not necessary
  - Not all traces are high speed
  - Similar layouts require single simulation
  - Good isolation in multilayer PCB minimizes crosstalk



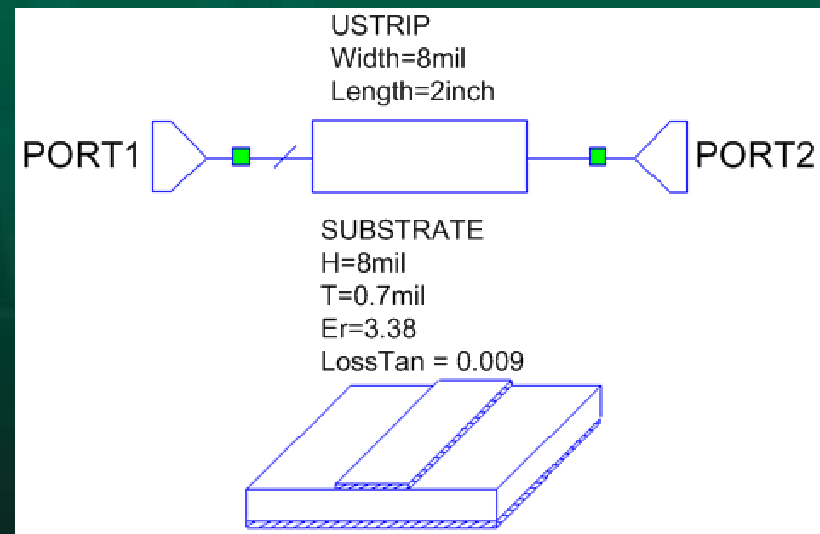
Simulation Techniques

- **Lumped Element Models (SPICE)**
  - Generic (not pinout specific)
  - No physical length
  - Ideal elements
  - Must be highly distributed to be accurate into GHz range
  - Appropriate for component (capacitor, inductor, balun) models



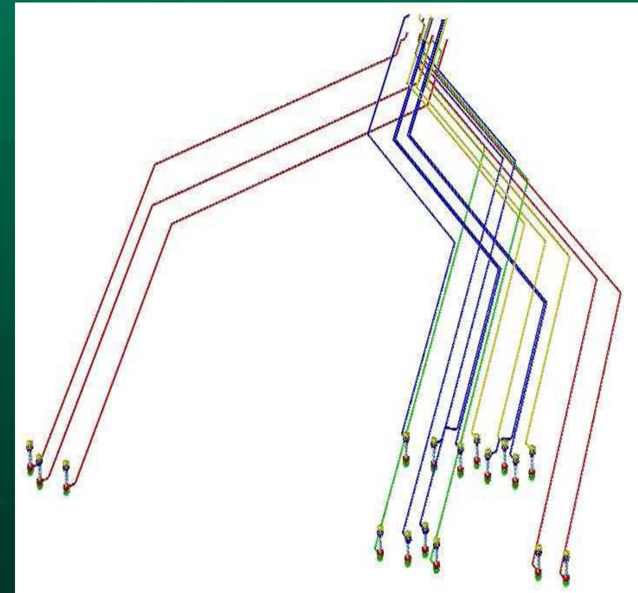
Simulation Techniques

- **Transmission Line Models**
  - Cross-sectional per unit length model
  - Captures physical properties of materials
  - Appropriate for straight traces



Simulation Techniques

- **2.5D Electromagnetics**
  - Captures effects of bends and cross-talk
  - Makes approximations for vias, conductor thickness, etc.
  - Appropriate for planar geometries



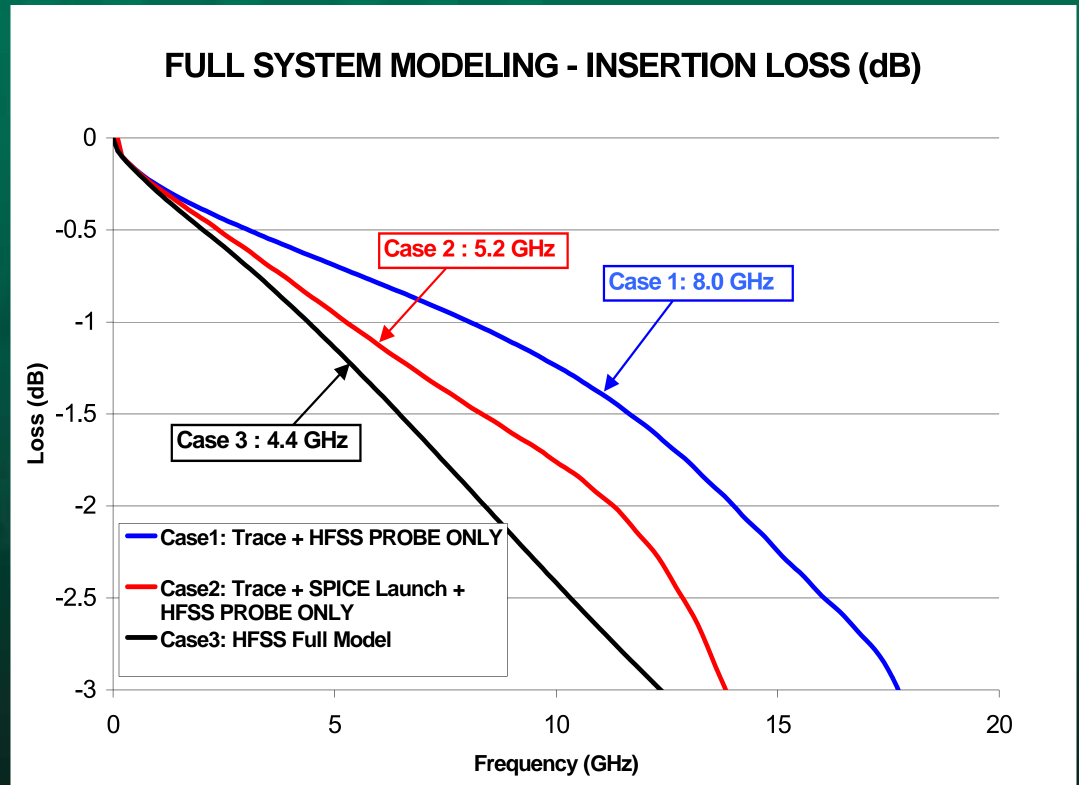
Simulation Techniques

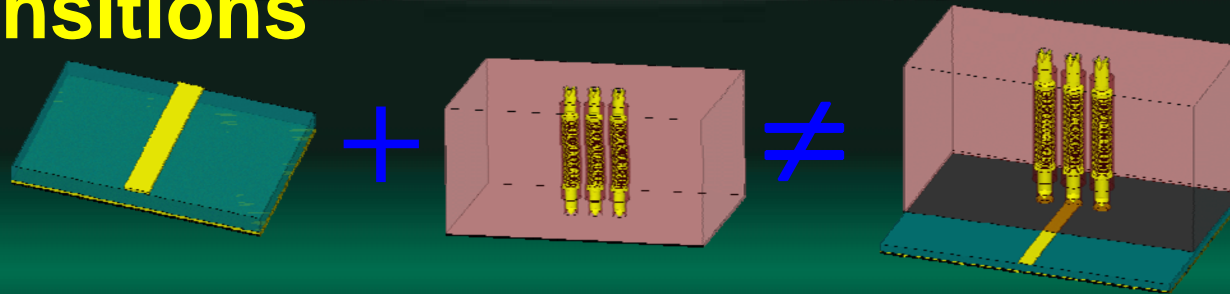
- **Full 3D Electromagnetic Simulation**
  - Probe Cards
  - Connectors
  - Vias
  - Packages
- **Most Rigorous Simulation Technique**
- **Captures All Losses of Physical Environment**

Interface Simulation

- **Sum of Pieces:**
  - 1dB Contactor
  - 1dB Board
  - 1dB Connectors, Launches

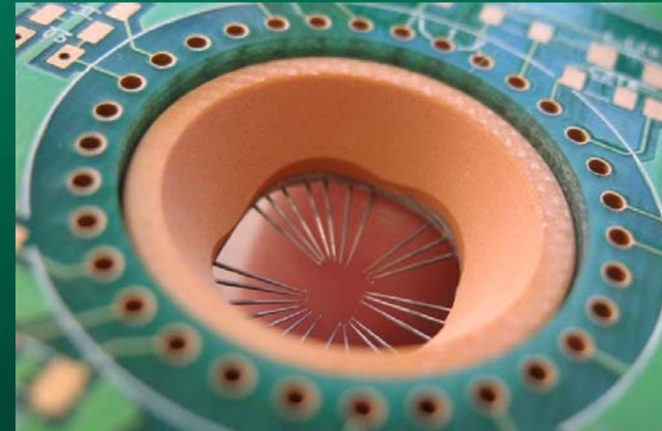
  ≠ 3dB @ *n* GHz
- **Collection of Pieces Approach Does Not Account for Transitions**

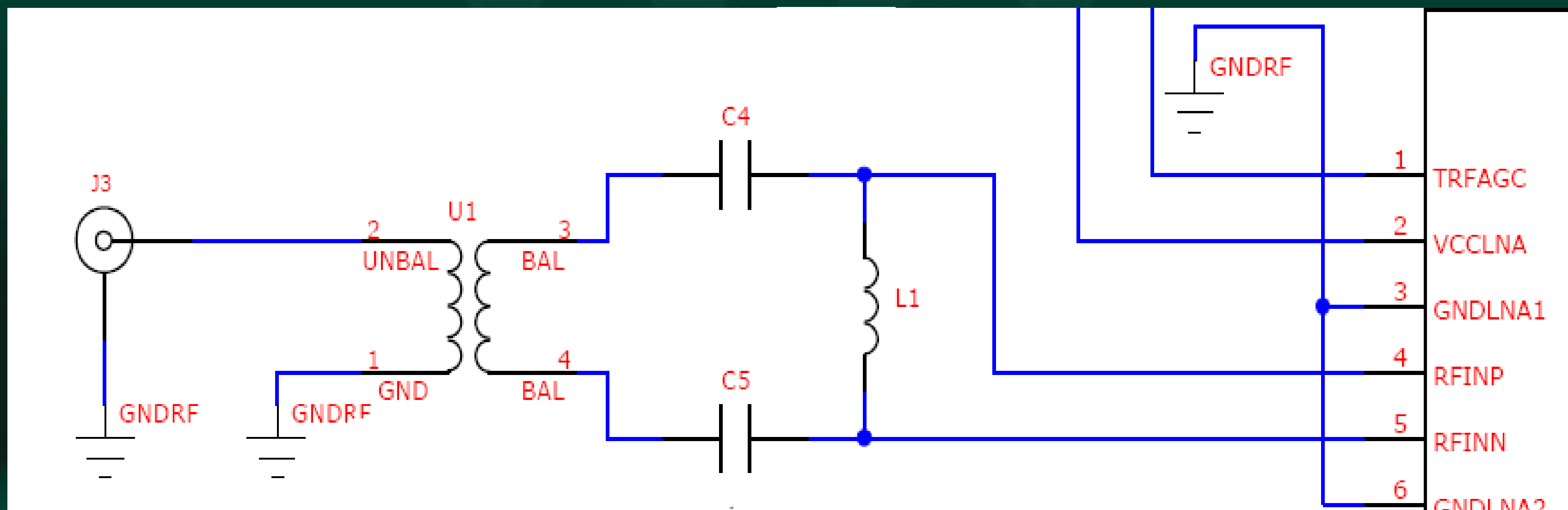




Case Study: High Speed Probe Card Test

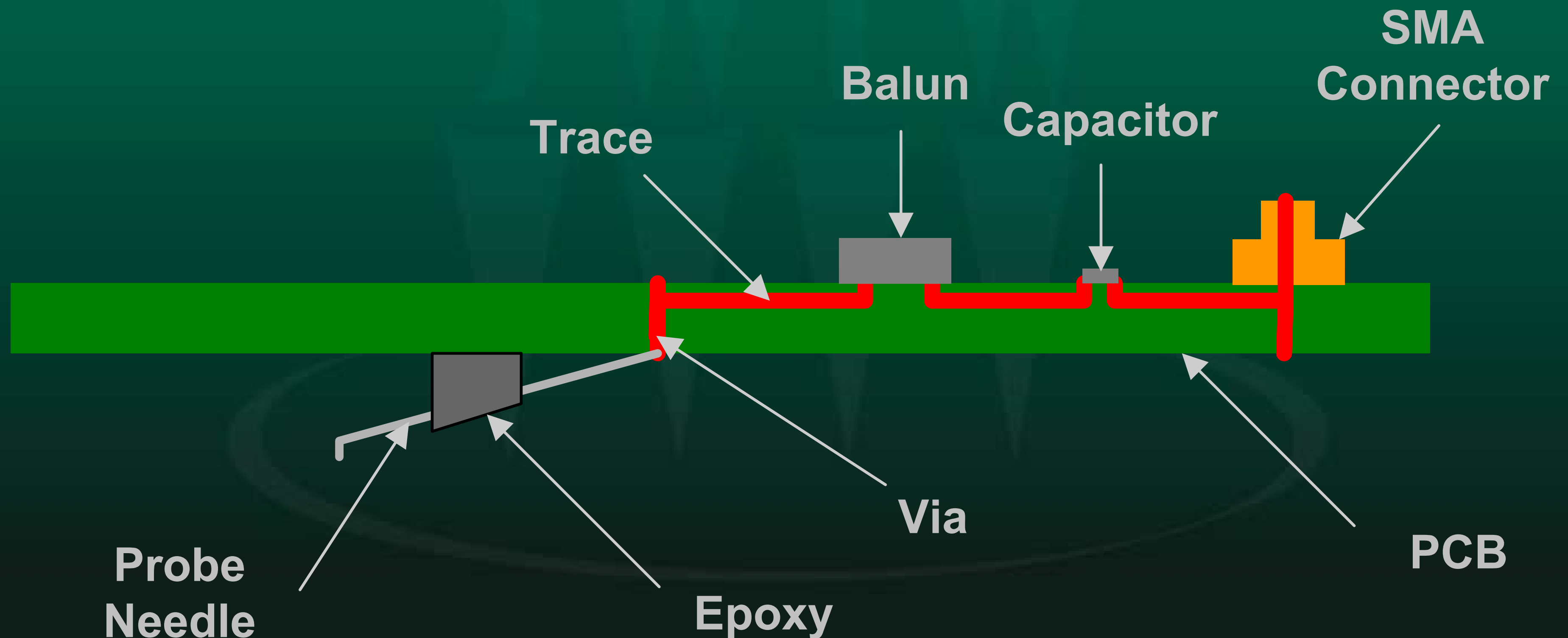
- Testing of RF Input to DUT
- 2.4 GHz Test Requirement
- Will a Probe Card Support This?





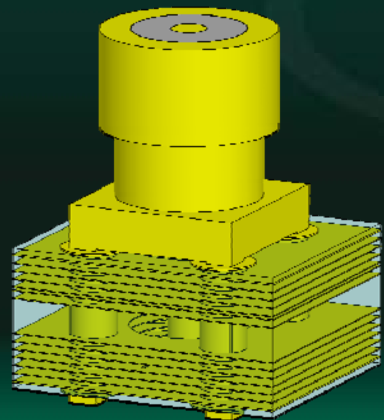
Probe Card Test Interface

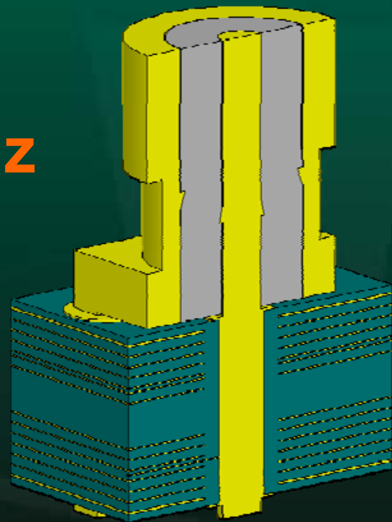
- Physical Description of Components



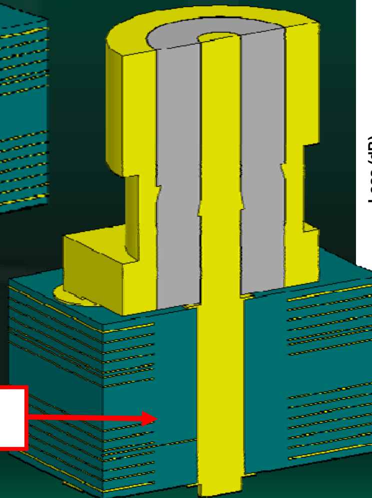
Connector Optimization

- Signal Pin Creates Impedance Mismatch with Standard Footprint
- Optimizing PCB Ground Clearance Diameter Improves Results
- Worst Case
  1dB @ 1.5Ghz
- Best Case
  1dB @ 6GHz



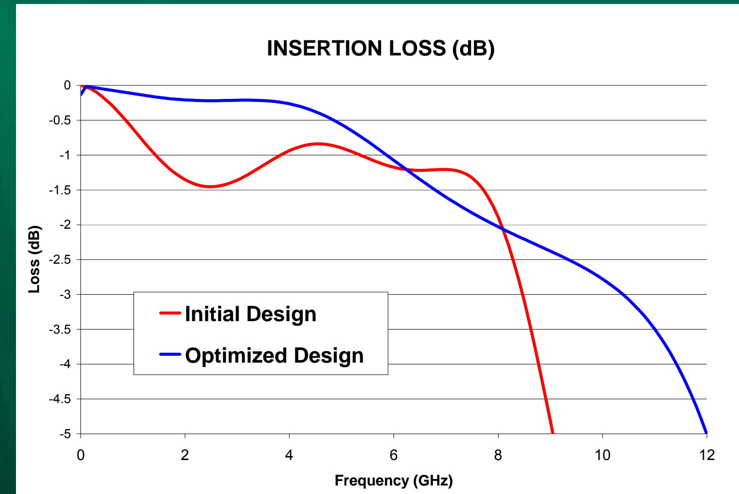


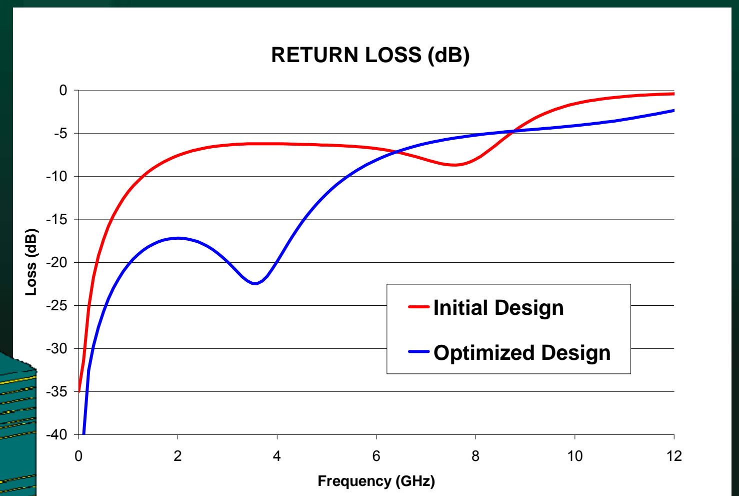
Initial Design



Increased Clearance

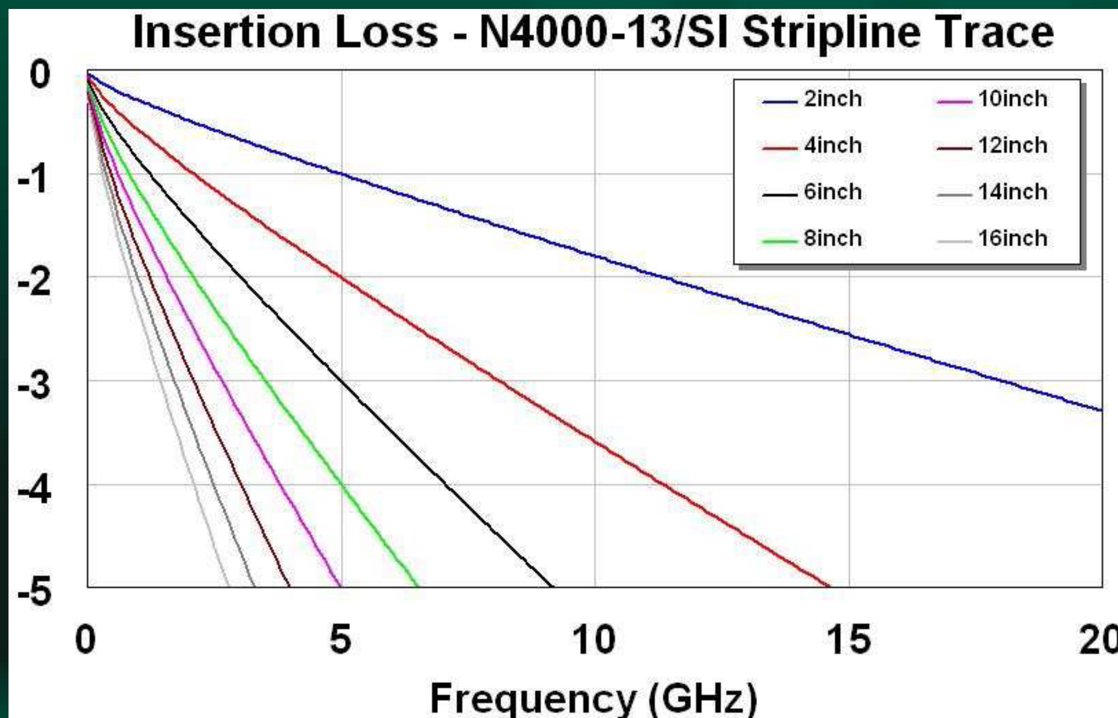
Optimized Design

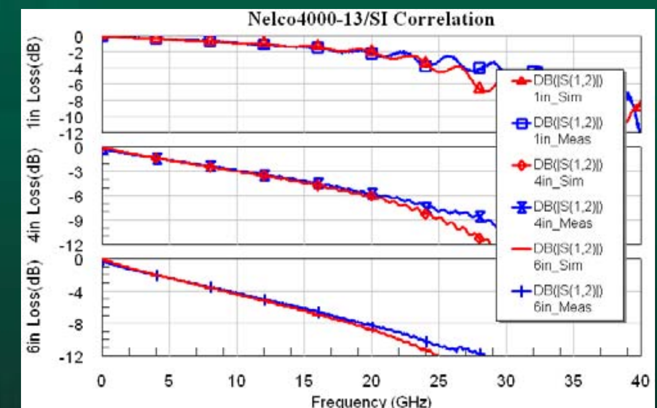


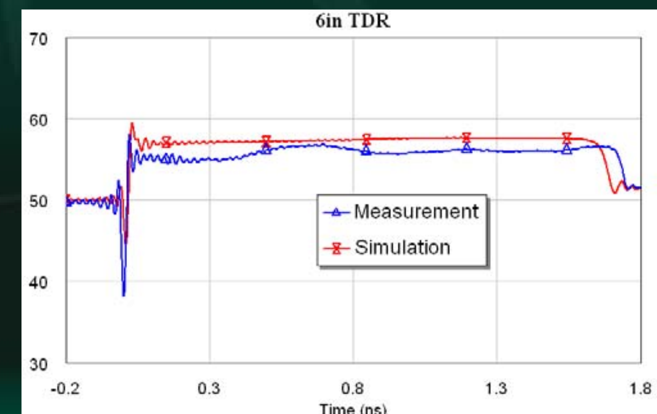


Trace Length Loss

- Often Major Contributor to Overall Loss
- Must Correlate with Manufacturing Process
- Worst Case (16”) 1dB @ 300 MHz
- Best Case (2”) 1dB @ 5 GHz

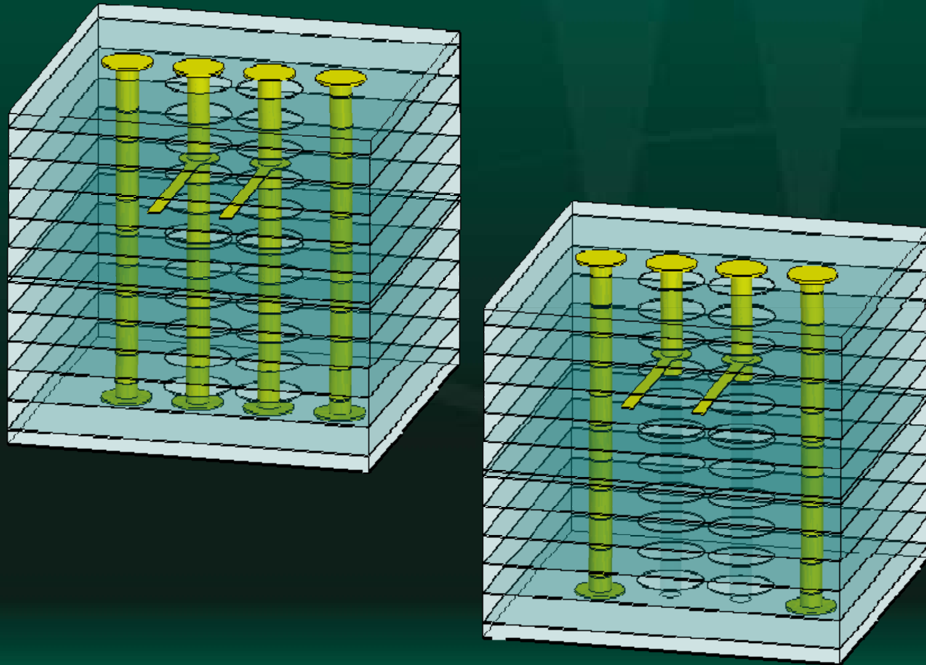


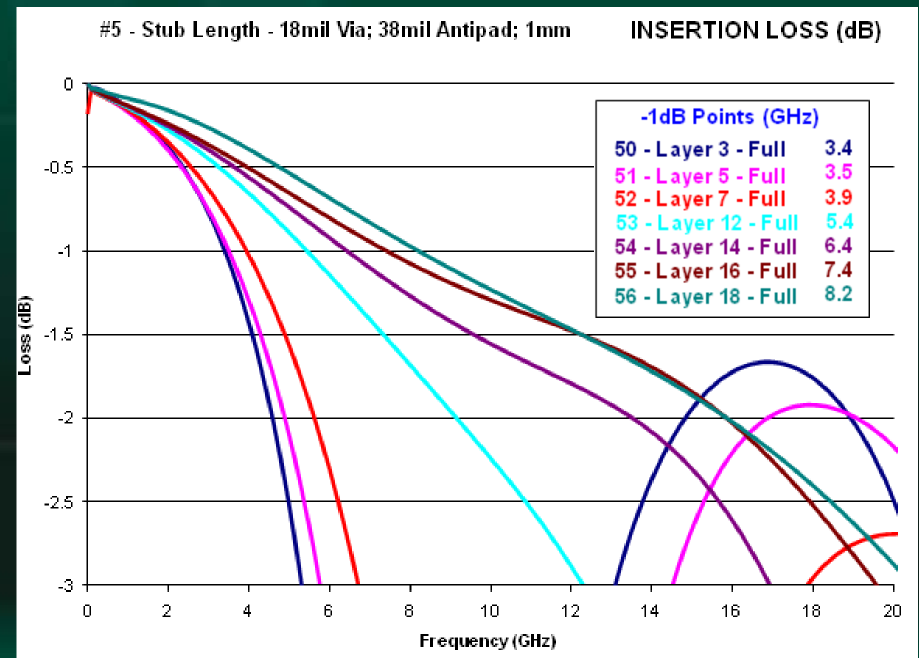




Optimization: Stub Removal

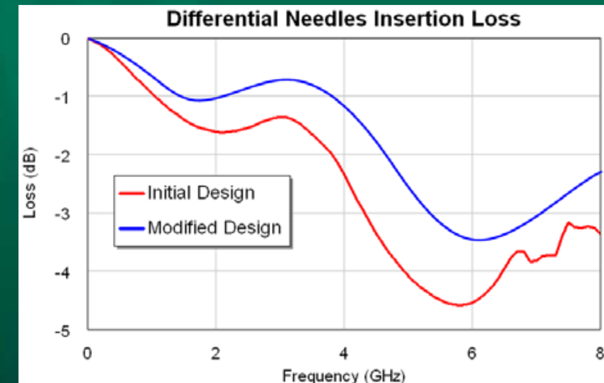
- Stub – Full Length Via and Inner Layer Trace
- Backdrill – Remove Via to Trace Layer
- Worst Case 1dB @ 2 GHz
- Best Case 1dB @ 8 GHz

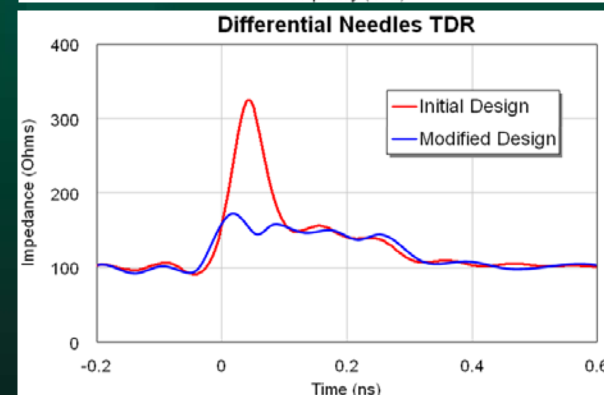


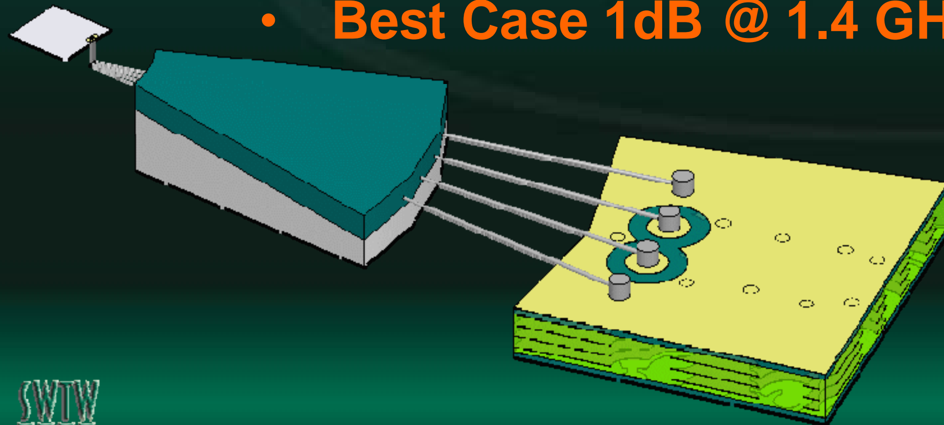


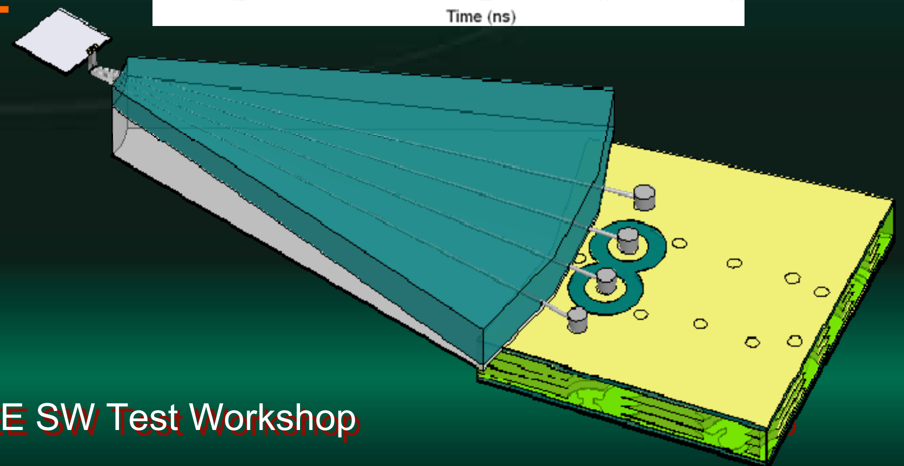
Probe Needle Optimization

- **The needles have very high impedance, above 300 Ohms.**
- **Impedance can be lowered with epoxy to improve performance**
  - **Worst Case 1dB @ 1 GHz**
  - **Best Case 1dB @ 1.4 GHz**



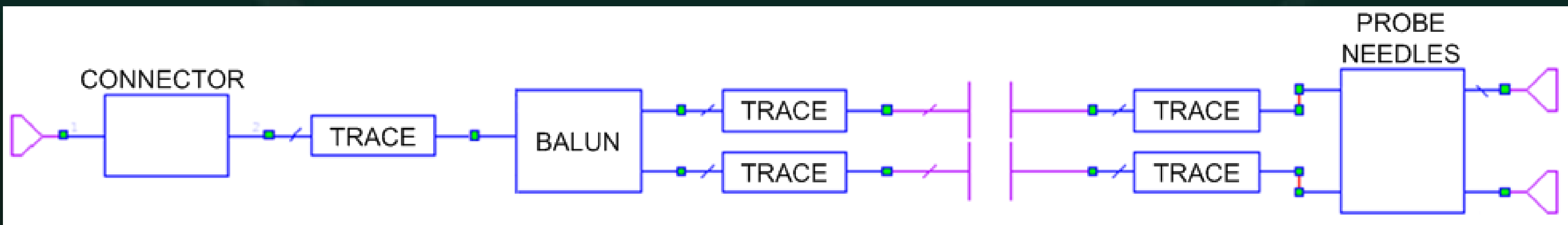






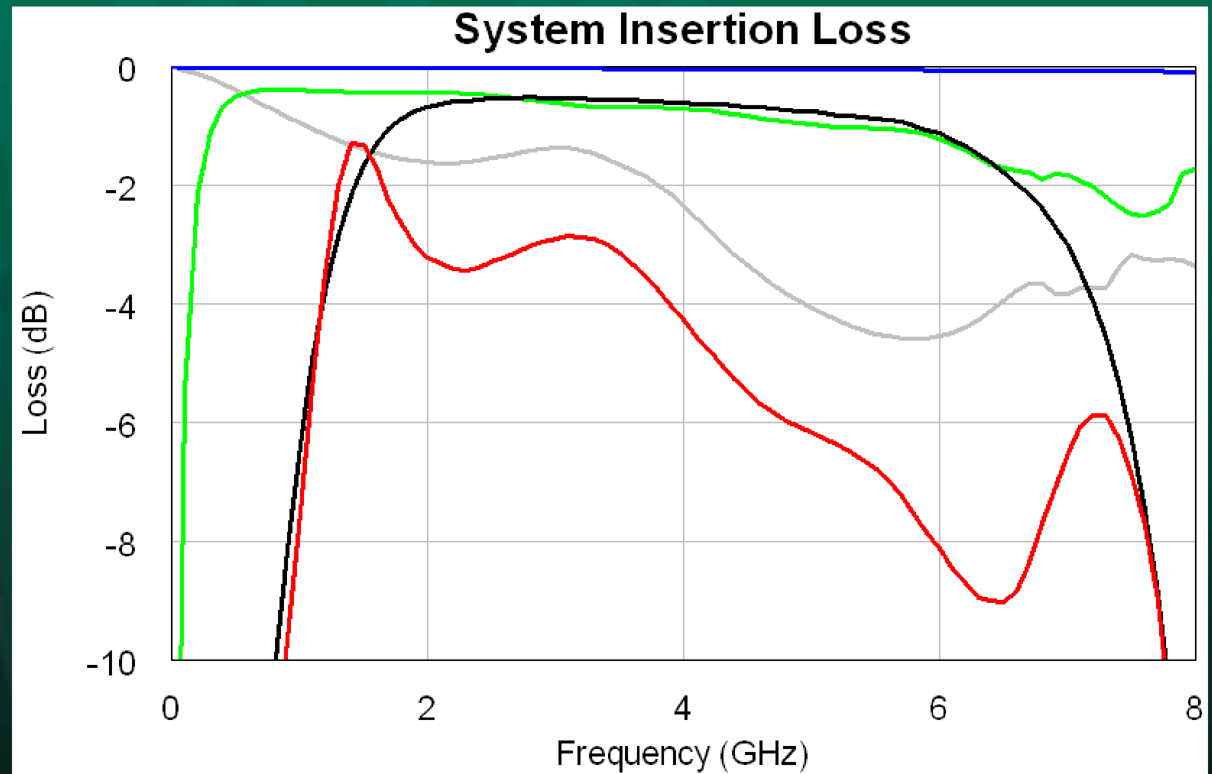
System Simulation

- **Model Includes:**
  - Connector
    - 3D EM simulation
  - PCB traces
    - Transmission line models
  - Balun
    - Manufacturer SPICE model
  - Capacitors
    - Manufacturer SPICE model
  - Vias
    - 3D EM simulation
  - Probe card
    - 3D EM simulation



System Performance

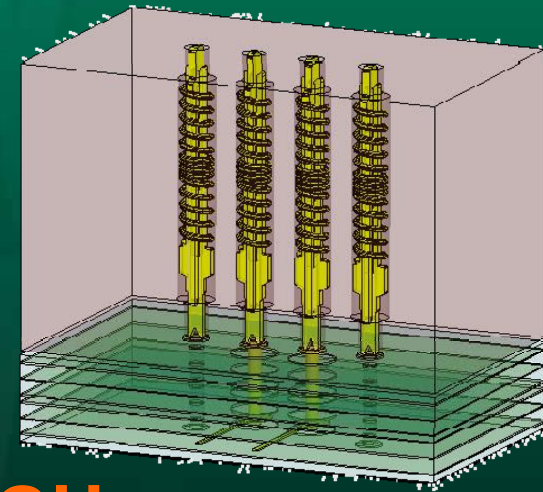
Full System
Connector
Balun
PCB
Probe Needles

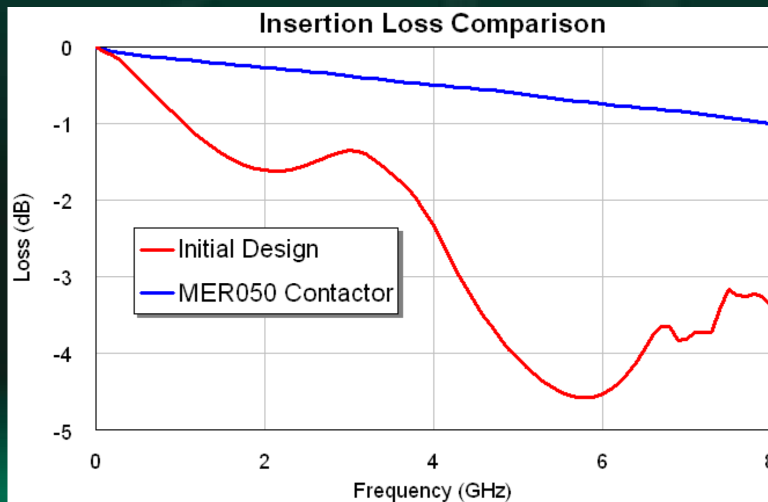


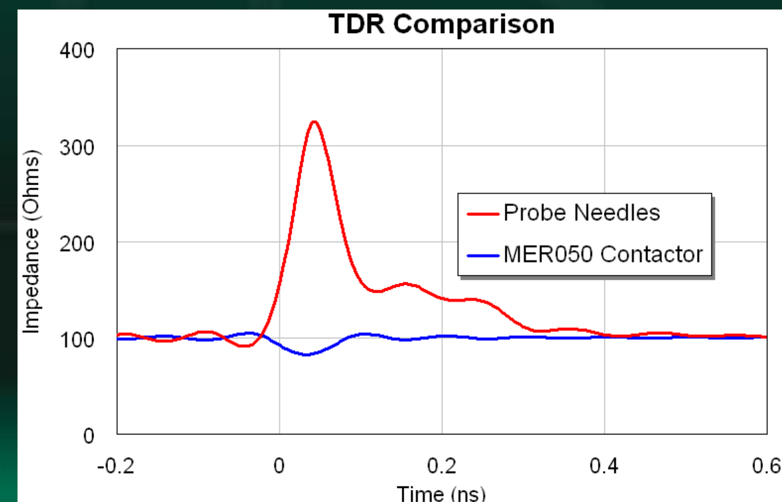
- Total System 3dB Loss point @ 1.9 GHz
- **Probe needles account for majority of loss**

Probe Needle Alternative

- **Spring Probe**
  - Probes 3mm vs needles 50mm
  - Probe impedance 80-120Ω
  - Needle impedance 125-300Ω
- **Probes 1dB @ 21.4 GHz**
- **Probes w/ 50mm trace 1dB @ 8.0GHz**

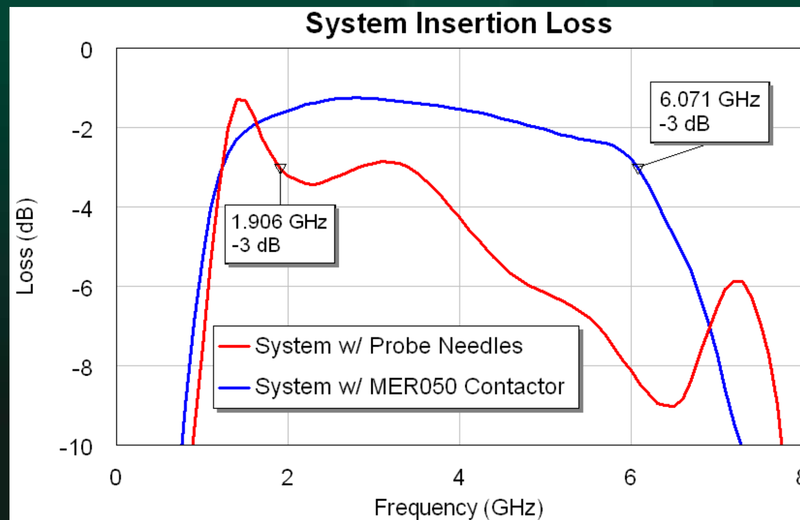


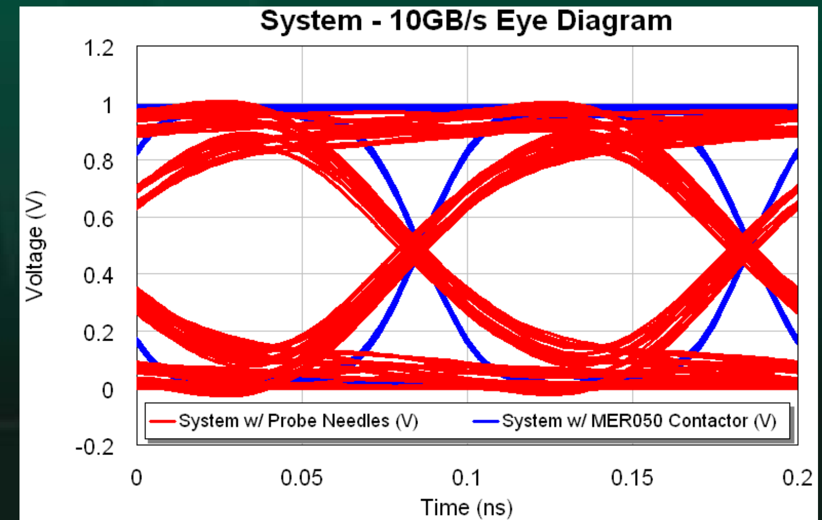




Probe Card vs. Contactor System Simulation Results

- **Bandwidth**
  - Probe Card 3dB @ 1.9 GHz
  - Spring Probe 3dB @ 6.1 GHz
- **10GB/s Eye Diagram**
  - Probe Card 44ps rise-time
  - Spring Probe 24ps rise-time





Going Forward

- **Other Variables Not Optimized:**
  - Via diameter, trace width, board material, clearance diameters, ground vias, package, etc.
- **Future Work**
  - Performance matrix for Engineers to quickly determine loss given tester, probe type, board material

							Insertion Loss		20-80 Output Rise Time		
							S12		10ps	50ps	100ps
VIEW	Pitch	Probe	PCB	GND	Trace	Length	-1dB	-3dB	INPUT	INPUT	INPUT
X	0.4mm	Gem040	N4000-13	GSSG	Stripline	02in	3.8	12.1	15.9	53.9	103.7
X	0.4mm	Gem040	N4000-13	GSSG	Stripline	12in	0.4	1.8	81.8	116.2	153.3

Summary

- System Performance Impacted by Choice of Hardware Components and Design of Performance Board
- Simulation Can Optimize Performance Before Fabrication
- Simulation Reduces Lab Characterization and Re-spins and Provides Fastest Path to Production