IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Test-data validation

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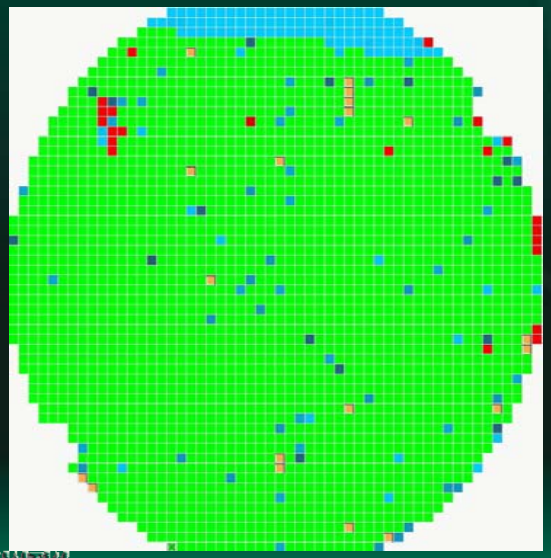
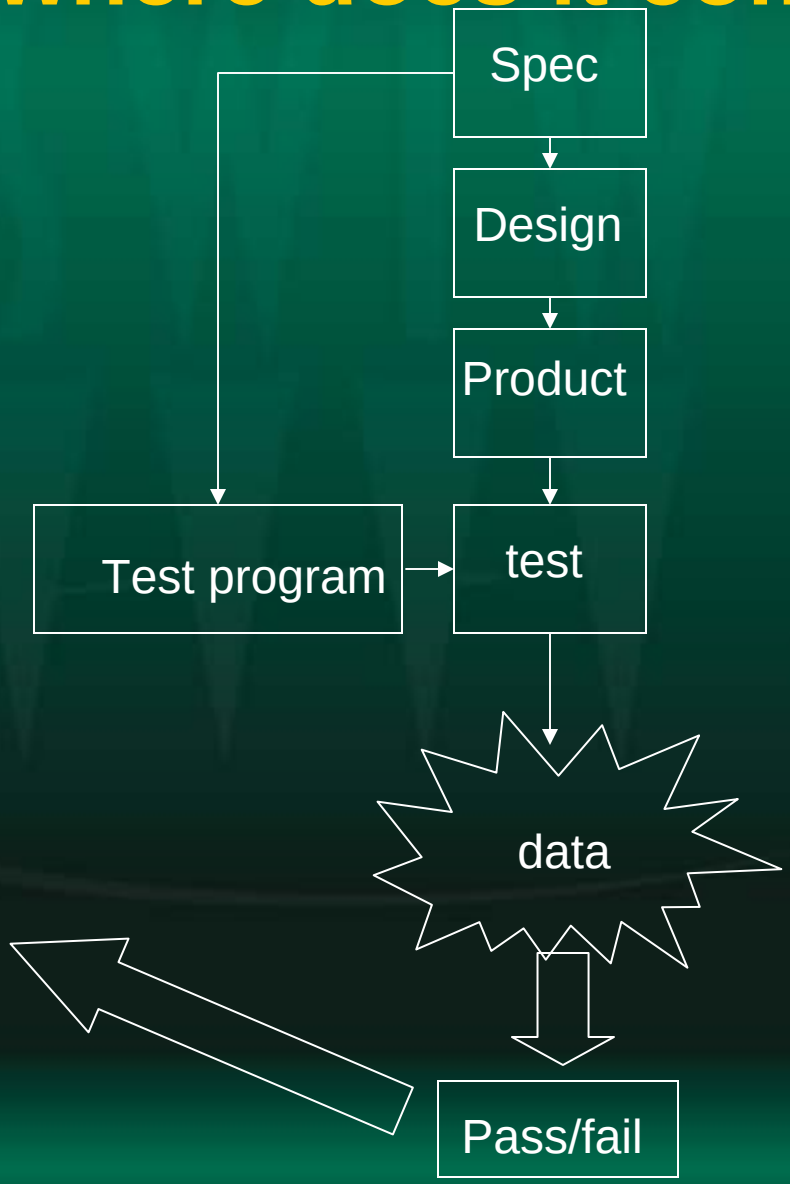
Understanding Test-Data

- Where does the test-data come from?
- Part-variance / Test-variance
- Artifacts
- Zero defect
- Known good die (bare-die delivery)

Test-Data; where does it come from?



Wafer-map

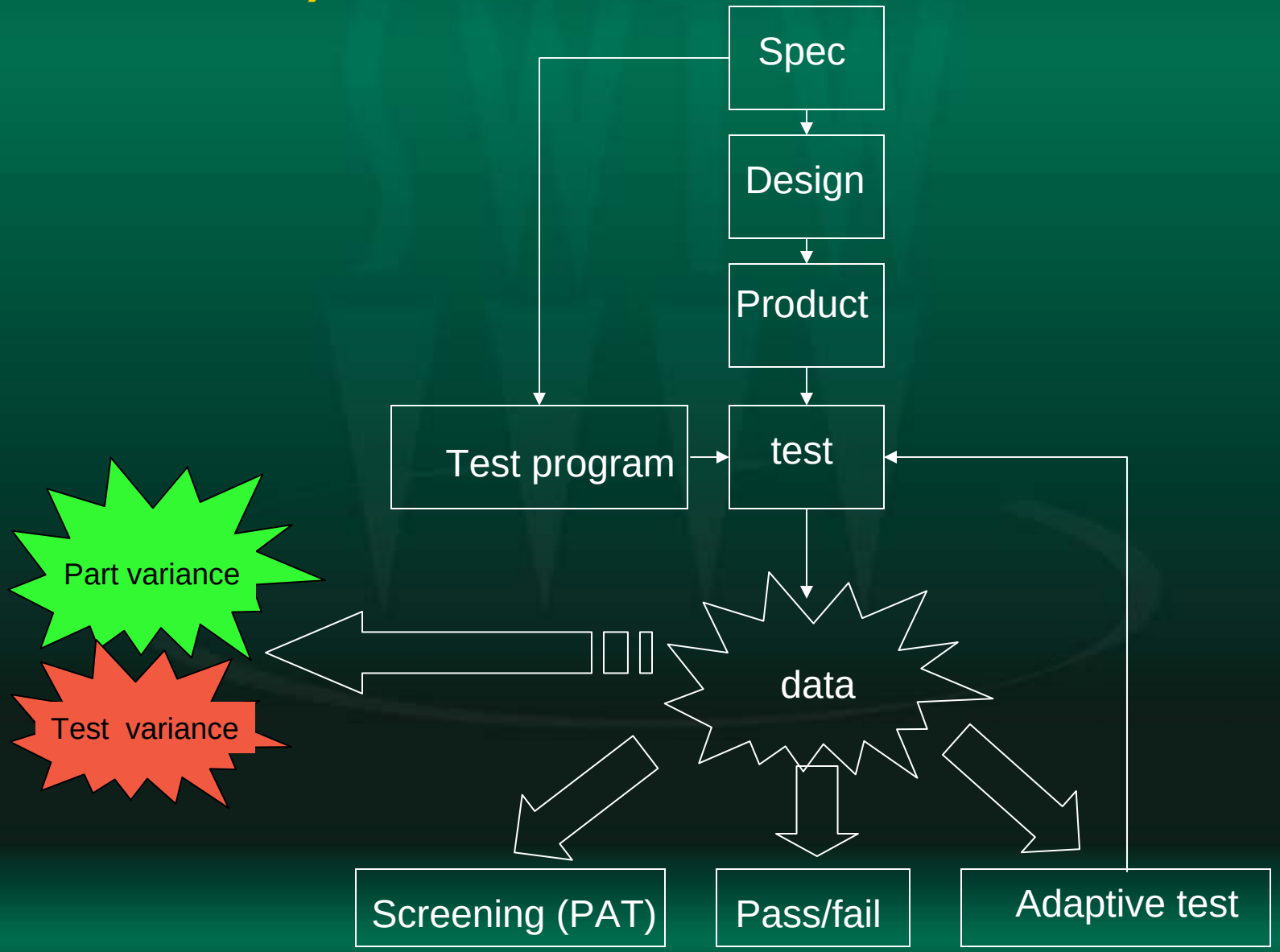


Test program preparations

- **Repeatability**
  - Run 1 device at least 50 times
  - Check variance
- **Capabilities**
  - Cp, Cpk, shape, etc
  - Check limits
- **Gage R&R**
  - Use multiple variable; testers, load boards, probe-cards, etc
- **When all above is good, production can be tested**
- **Test engineer take all the time for “perfect set-up”**

- ***Is this guaranty for reproducibility ?***

Test-Data; where does it come from?



Part variance;
This is where we are interested in!

- **In semiconductor industry, the goal is to make all die according specification & 100% identical!**
  - Do we succeed in this? No, that is why we test!
  - At test, it is the first time you really can check full electric functioning.
- **Test-program is written to verify proper functioning and confirm the specifications.**

- **based upon the test data all kind of actions/decisions are made!!**
  - Pass/fail
  - Classification
  - SPC
  - Etc..
- **First production release is done on ideal / perfect set-up**
  - New probe card, engineering set-up, etc
- **But life is not perfect..**

Test-engineers are living on the edge!

Test variance

- **This is what we don't want, but have to deal with!**
- **Understanding where it comes from;**
  - Equipment (tester/prober/handler)
  - Materials (probe-card/contactor/load-boards/DIB)
  - Conditions (temp/humidity/pressure/over-travel Cres/film resistance)
  - Test-program (resolution/concessions)
- **Can we limit the influence of test variance?**
  - Prediction
  - Correction

Artifacts

- **“An** artifact **is the error or misrepresentation introduced by a technique and/or technology” (wikipedia)**
- **In Semi-Conductor data-sets we have artifacts caused by:**
  - Reticle dependency
  - Test-site dependency
  - Test set-up failures
  - Others (not further specified)
- **Way to get rid of artifacts;**
  - Fine tune your test set-up, process
- **Some times we have to live with the fact that artifacts are present.**
  - Data correction in that case is a good alternative

Good test set-up

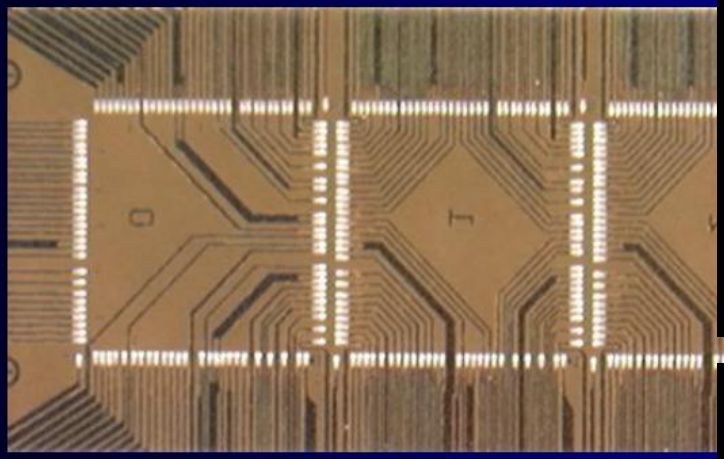
- **Calibrate tester before test run**
- **Calibrate entire test set-up**
  - Load-board (DIB)
  - Connections (Pogo-tower, cable connections)
  - examples from previous SWTW presentations
    - signal compensation for multi site probing,
      - Gert Hohenwarter; RF testing
      - Paul O'Neil **Cascade MicroTech Europe**
    - Floor vibration TI, Al Wegleitner

Add-up; synchronization @ multi-site

Old compared to ne

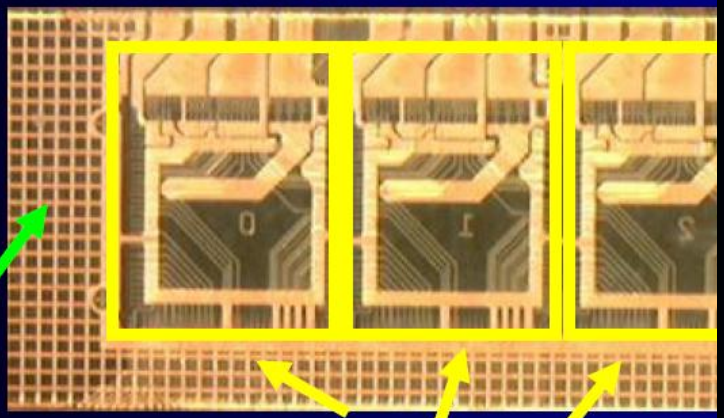
OLD rev A

1 metal layer



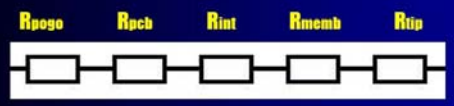
NEW Rev B

GND



Symmetry over a

Put it all together and what do you get?



= 0.1 +4.0 +0.1 +5.0 +0.2 ohms

= 9.4 ohms

WAY TOO HIGH! We should be targeting 2-3 ohms or less.

Now what do we have for Rprobe?

= 0.1 +0.5 +0.05 +0.8 +0.2 ohms

= 1.7 ohms

Much better. But does it work?

Correlation

- **Can correlation-wafer probing increase the quality of the production?**
- **Test correlation wafer (golden wafer)**
  - Before testing load the corresponding test-datalog
  - During probing compare each die location between “golden” parametric values and actual values
- **Correlate on bin-level (Pass/Fail)**
- **Correlate to full parametric distribution level**
  - Shape of distribution
  - Location of distribution (drift)

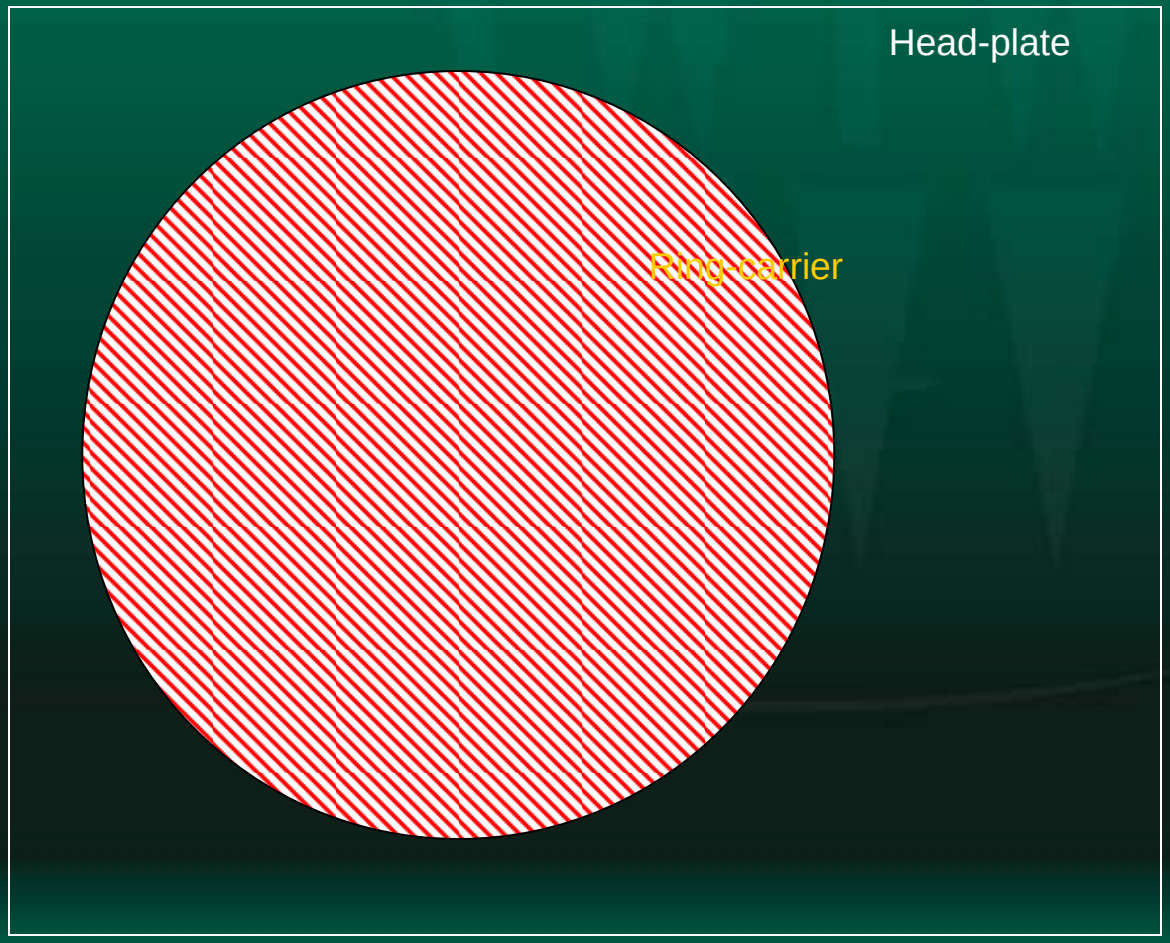
First time right vs. Retest

- **Ultimate goal: No/Limited retest**
- **Reduce retest**
  - Eliminate test variance
  - Retest for measurement fails only (no valid reading)
    - Retest recovery analysis

Probe-card deflection

- **Probe-card has influence on test-data**
  - Probing at high temperature
    - No equal heat distribution while probing
  - Increased complexity in probe-cards
    - Larger die
    - More and more multi side
    - More contact pressure required
- **Robustness of probe process**
  - No equal forces on all contacts while probing
    - 2006 SWTW Gunther Boehm **Feinmetall GmbH**
- **Sometimes correction of z-height solves these problems**

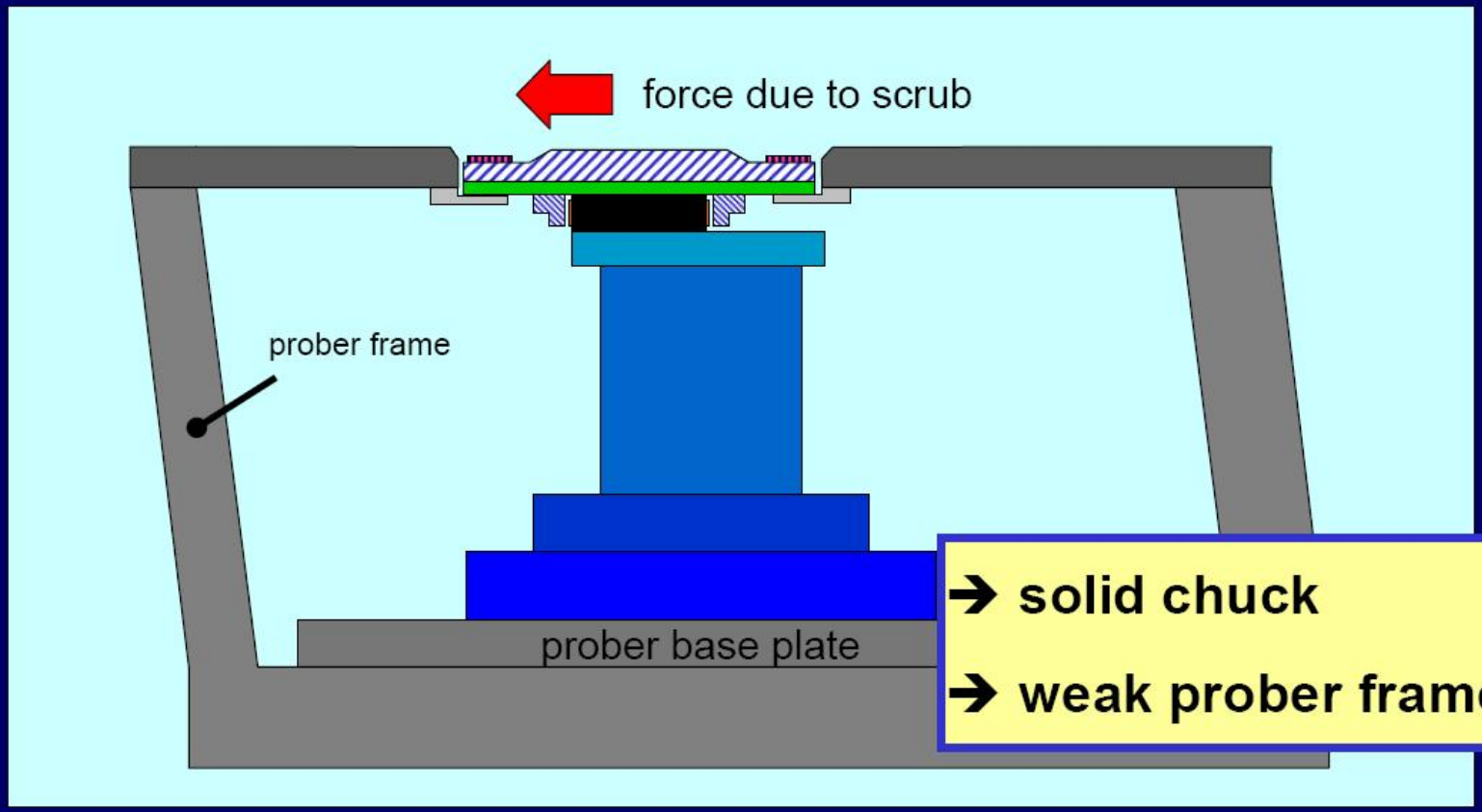
Thermal distribution



Area where temperature varies during probing. This includes the entire probe-card area

Know what happens in the prober

Influence of Lateral Force



SWTW June 2006 FEINMETALL GmbH, MIC Division, G. Boehm 18

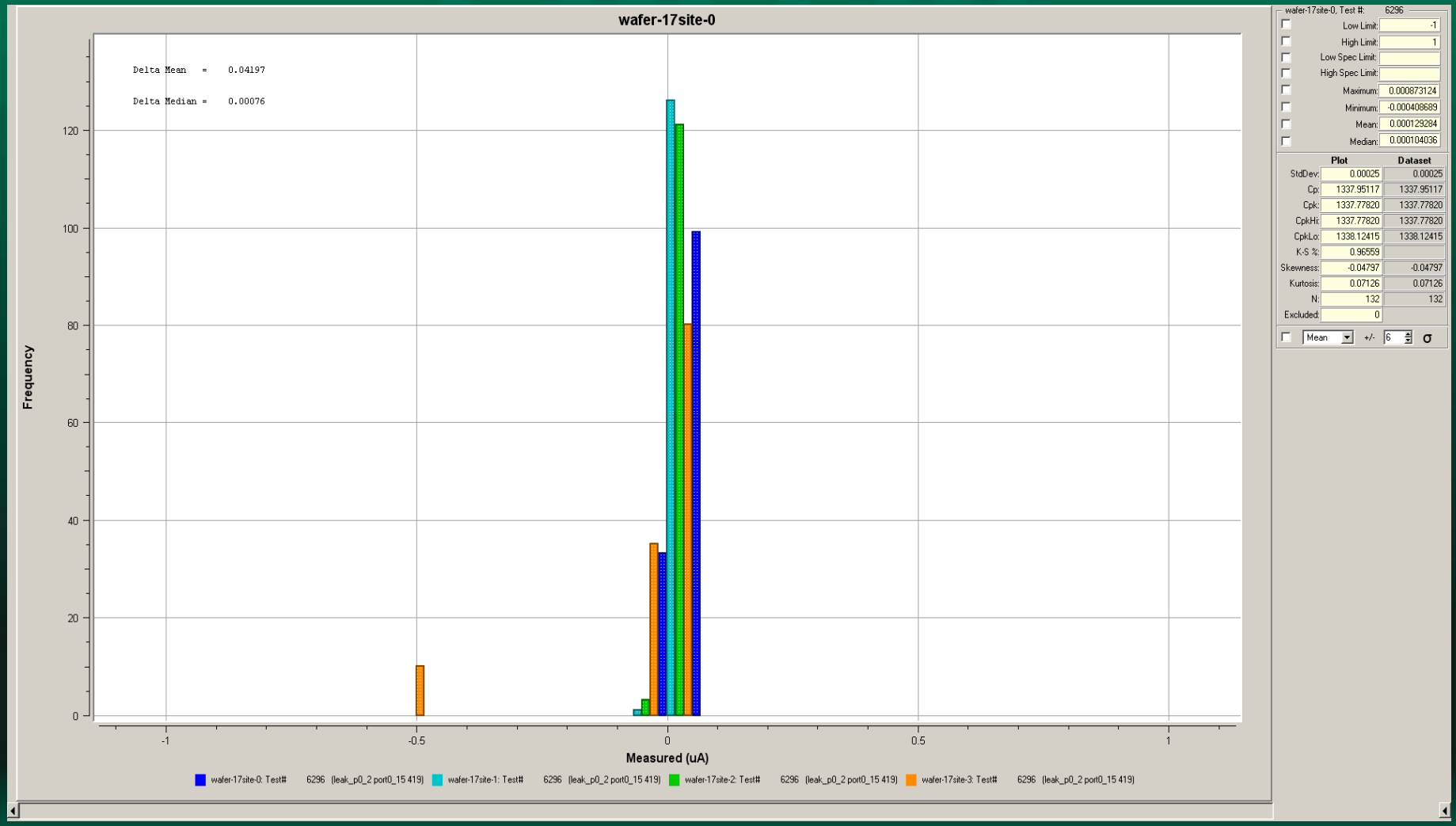
Automatic Z-height correction

- **First contact – full contact**
  - At initialization raise chuck slowly until first needle contact the die.
  - Then raise further until all needles are contacting the die
  - Difference in z-height between first and full contact indicate probe-card/set-up planarity
  - Limits on z-height difference protect the set-up against extensive probe mark damage (cantilever cards)
- **First contact – full contact measured under different conditions (temp) at different locations (on the chuck) will indicate your probe-card deflection**

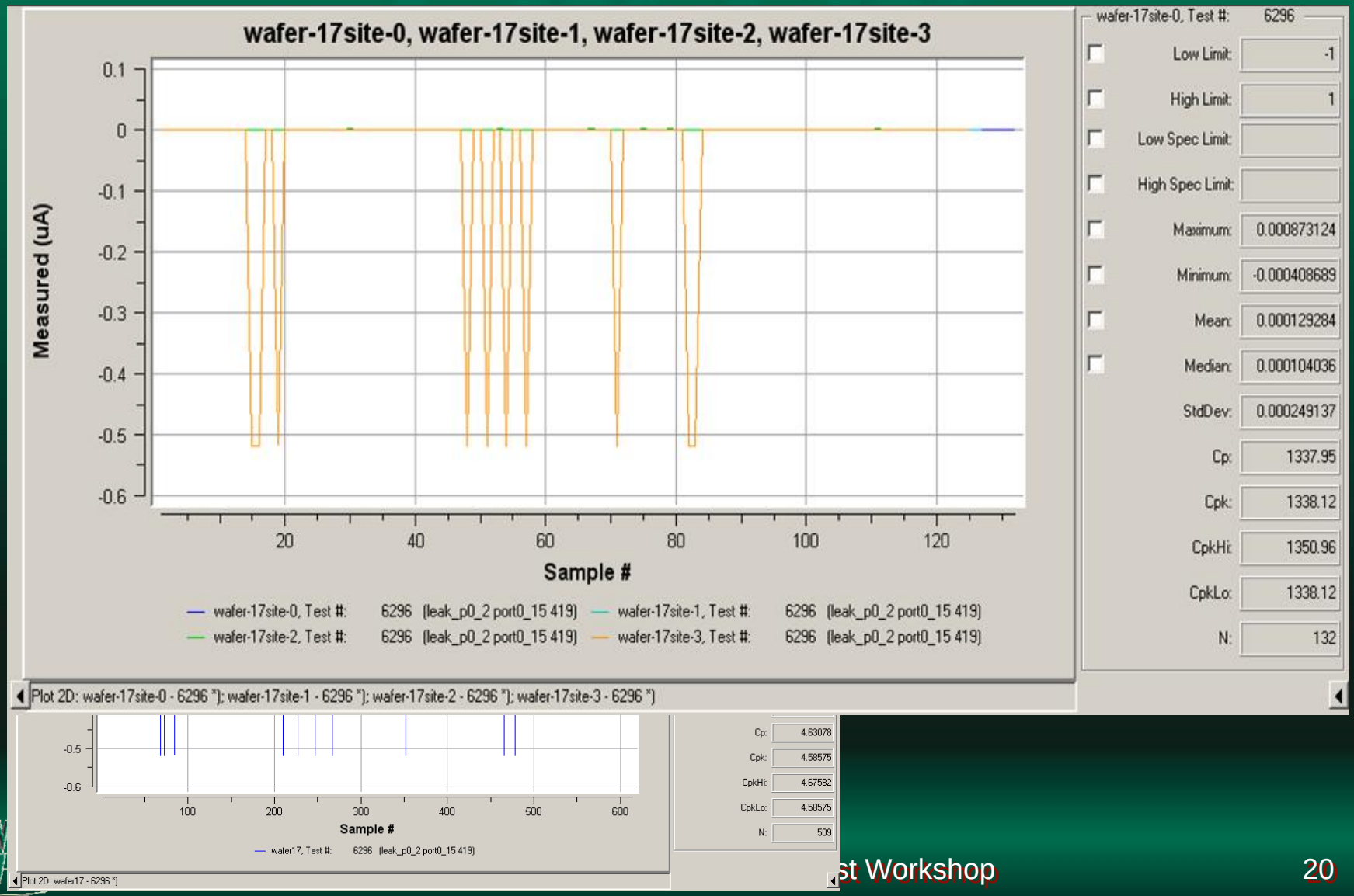
Test variance & Multi site probing

- **At multi-site probing not all site are equal**
  - Probe-card layout (site variation)
  - Tester resources
- **Site related test-data issues**
  - Just look at pass fail nothing to worry about, but looking closer you can detect parametric problems in real time
- **Extensive Site to Site R&R is required!**
  - Verify if all “test-positions” deliver same test results
  - To do this on the prober is difficult (time consuming)

Multi site example



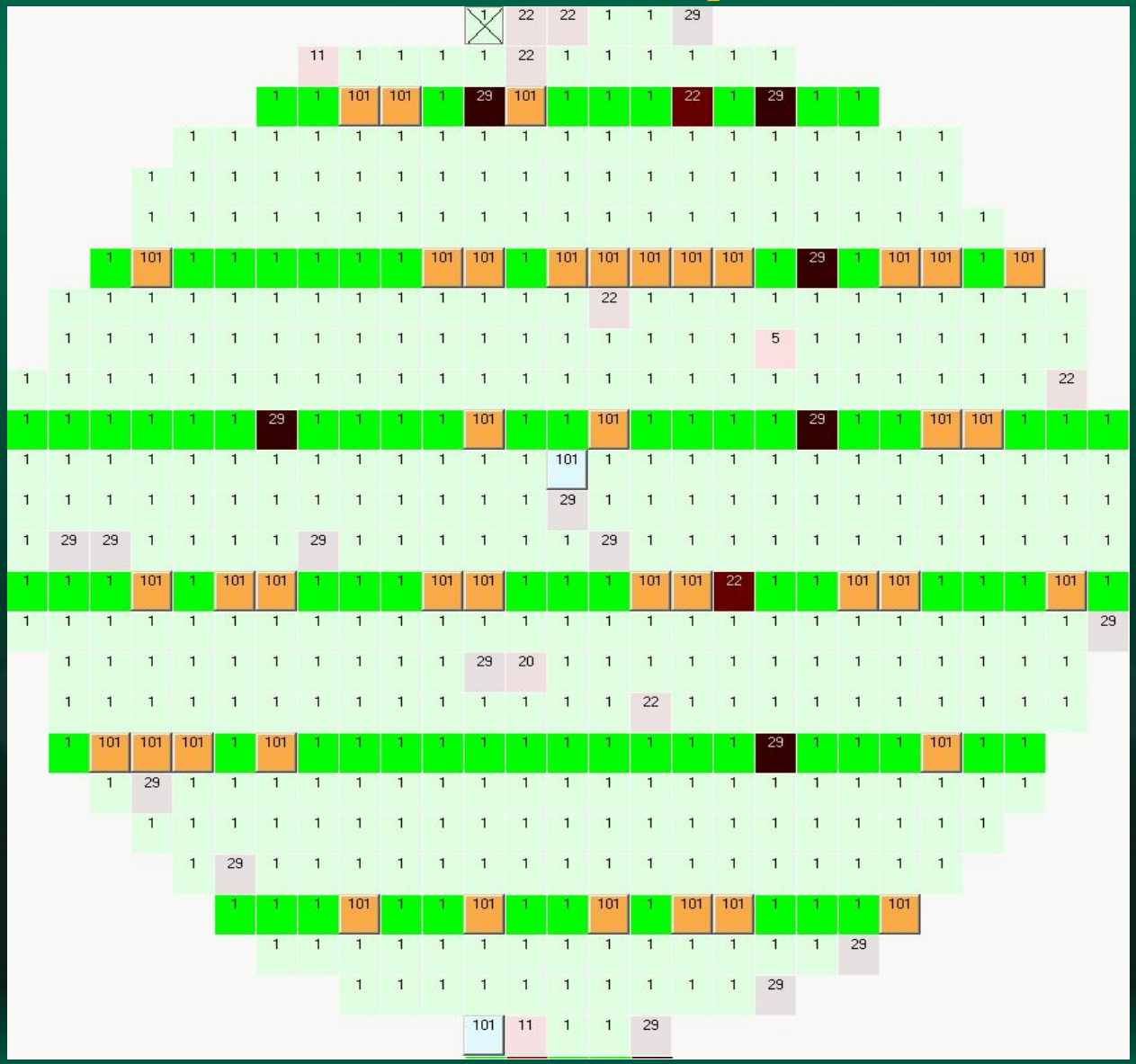
Production results



statistics

- **Wafer 17; the Cpk was suddenly getting down**
  - separating the sites learned; site-3 was way off
    - site 0,1,2 where Cpk value within expectation range
    - site 3 Cpk value was much lower
- **Looking at pure pass/fail level site-3 was best yielding site over the entire lot.**
- **Looking at outlier results, site-3 had a serious test issue**
- **off-line analysis process can detect this, but its too late!**
- **Real-Time Monitoring Cpk make sense to detect a test issue.**
  - Note: For this test; Cpk is relatively high

wafer-maps

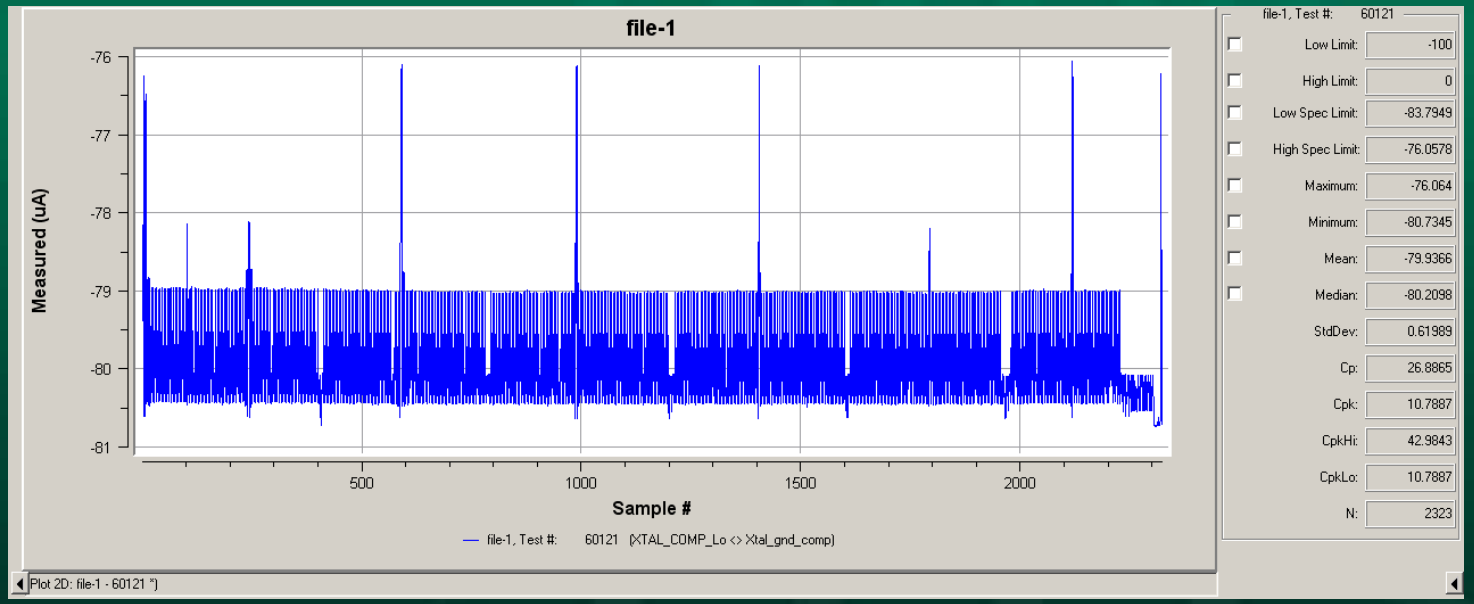


original total yield 94.25%

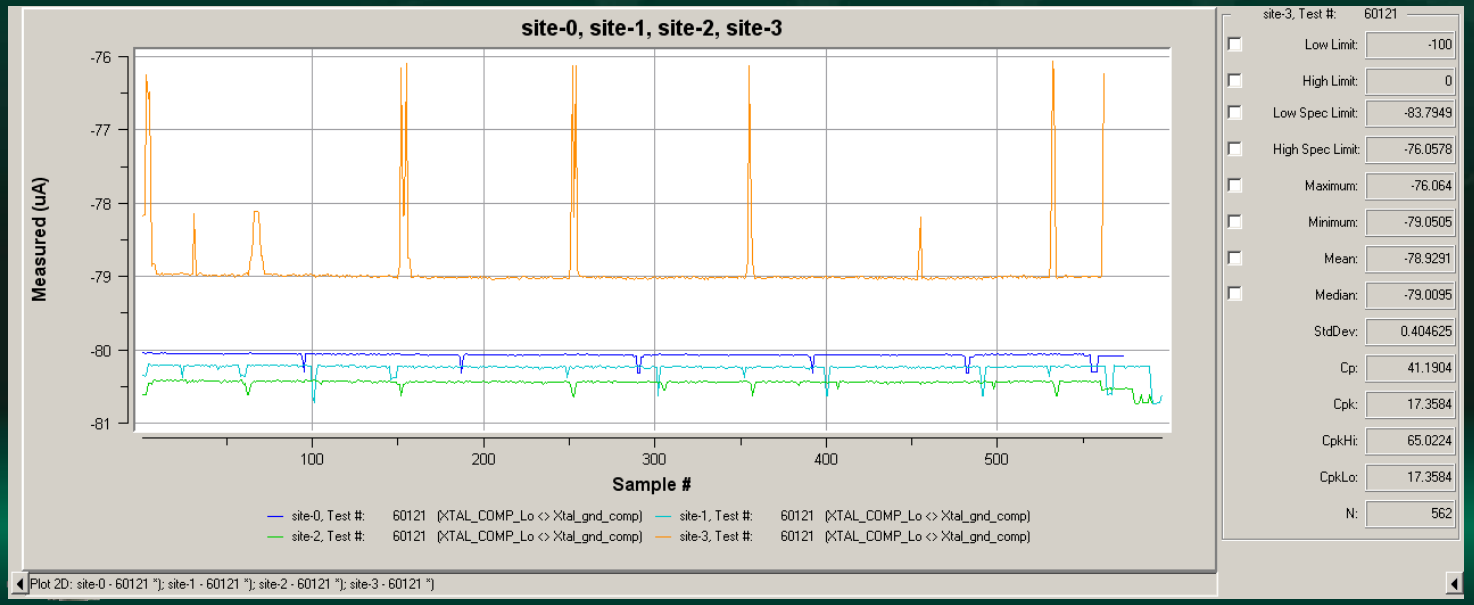
PAT-map total yield 86.64%

site-3 causes 95% of the total 7.61% PAT-yield loss

An other example of a “site-problem”



Test data for 1 Test, all 4 sites



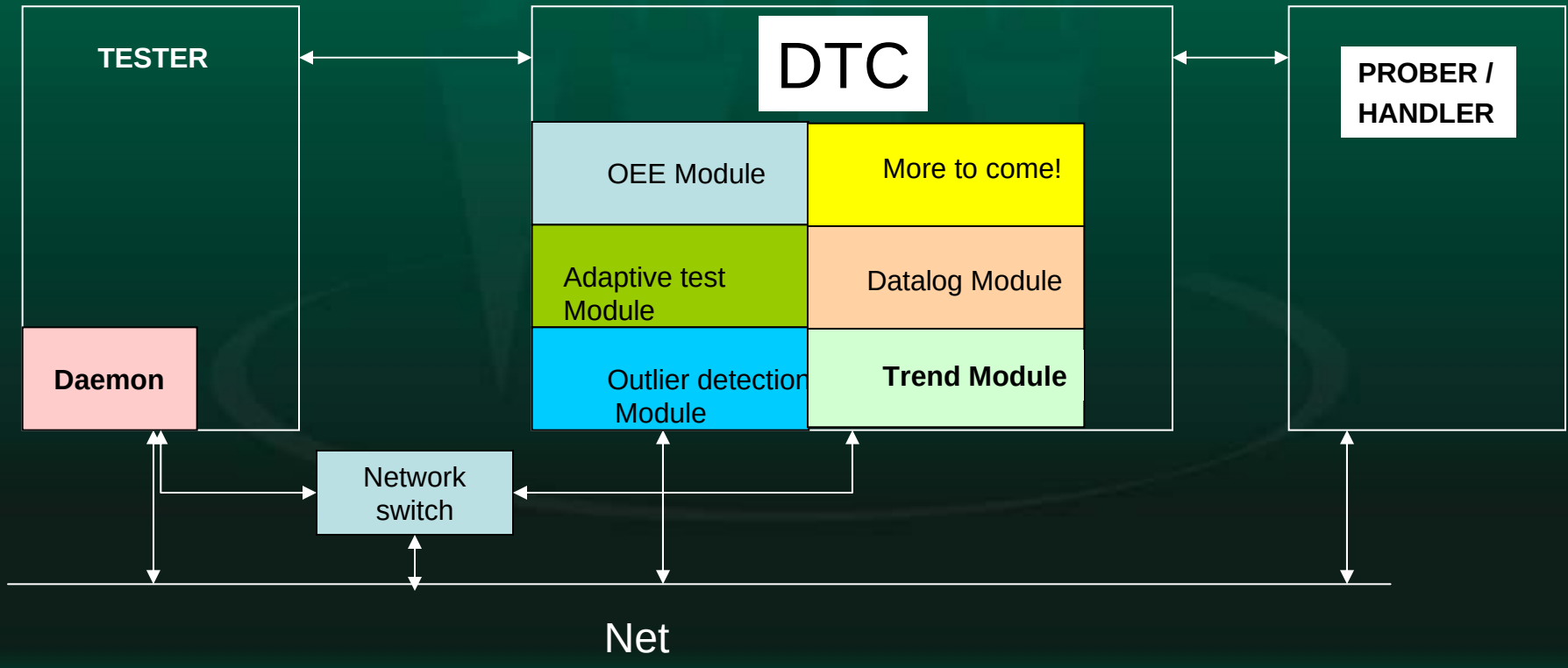
Same data but With separation Of the sites

Control test data quality; Make it more ROBUST!

- **Automatic verification of test related problems**
  - Test-cell controller shift probe pattern to detect if “suspected value” move with the site or stay with the die.
  - – Dynamic clean
    - Clean only then when needed, accepted degrading of data.
  - – Watch-dog test (critical test)
  - – RT SPC (values within expectation)
  - – Correlation
  - – Trigger tester calibration
- **Nice; but how?**

DTC

From SE-PROBE to a **D**ynamic **T**est-cell **C**ontroller



Dynamic Test-cell Controller

- **Tester daemon**
  - Provide in real-time parametric data
  - No overhead (save time)
  - Software on tester workstation
- **Data-log module creating the test-data-log**
- **Trend module will monitor selected test(s)**
  - Dynamic clean
  - Detect parametric value getting out of control (RT-SPC)
  - Initiate a calibration on the tester
- **Prober control**
  - Control over-travel
  - Control movements

Adaptive test

- **Result driven test-flow switching**
- **Based on Cpk, yield, hard/soft bin fail rate**
- **Multiple area's with multiple criteria**
- **Watch dog test(s) switch back to full flow when test data is not according expectation.**
- **Tracking and traceability**
  - Know what, where, when, how
  - Multiple pass bins representing test-flow used

Zero defect

- **On-line Screening**
  - Part Average Testing
  - Nearest Neighborhood Residual
  - Good die in bad neighborhood detection
  - Data integrity

results

- **More robust test data**
  - Clean on demand
  - Reliable data for adaptive testing
  - Problem detection when it happens
    - Stop/pause production ask for assistance
    - Auto correct
  - Actively correct; over-travel
  - Higher Cpk value compared to no test-cell controller
  - Data-log for on-line and off-line screening

conclusion

- **More robust test-data**
  - Reduce and control the test-variance / artifacts
- **Detection of test-variation influence on-line**
  - Off-line detection is too late and can result in retest!
- **Automatic correction before it result in rejects**
- **Better data integrity**
- **First-time-right approach**
- **Field proven solution**

Acknowledgments

- Paul van Ulsen, CEO Salland Engineering
- Salland Engineering DTC development team
- Several customers shared their findings
- Hilary; for posing “at the edge”