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Optical SerDes Test Interface for High-Speed and Parallel Testing

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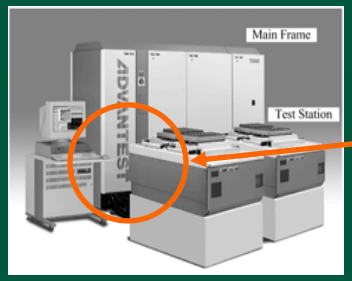
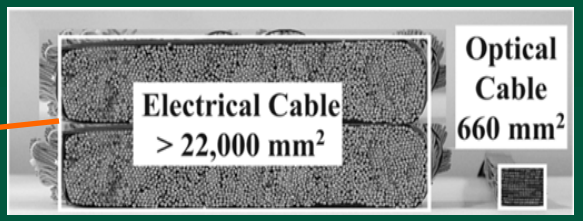
Why Optical Interface ?

- High speed up to 10GHz, Significant scalability



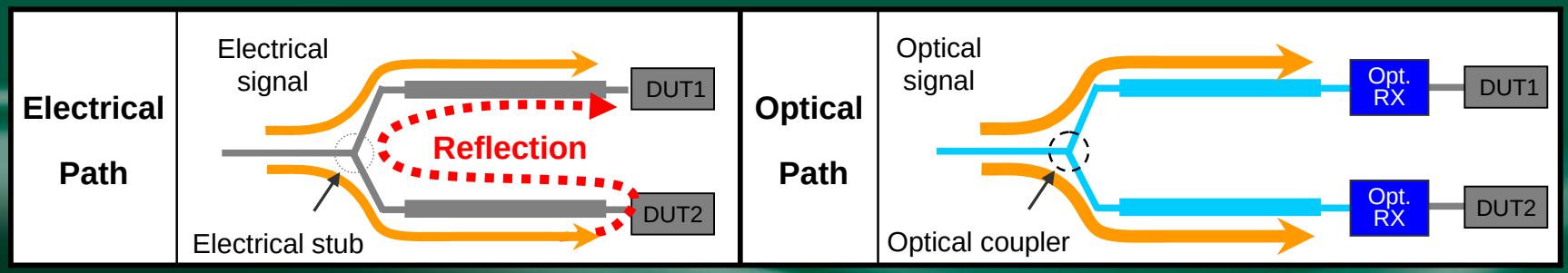
- Smaller cross-sectional area than electrical cable or trace.





[T. Okayasu, et al., JLT, vol. 22, no. 9, Sept. 2004]

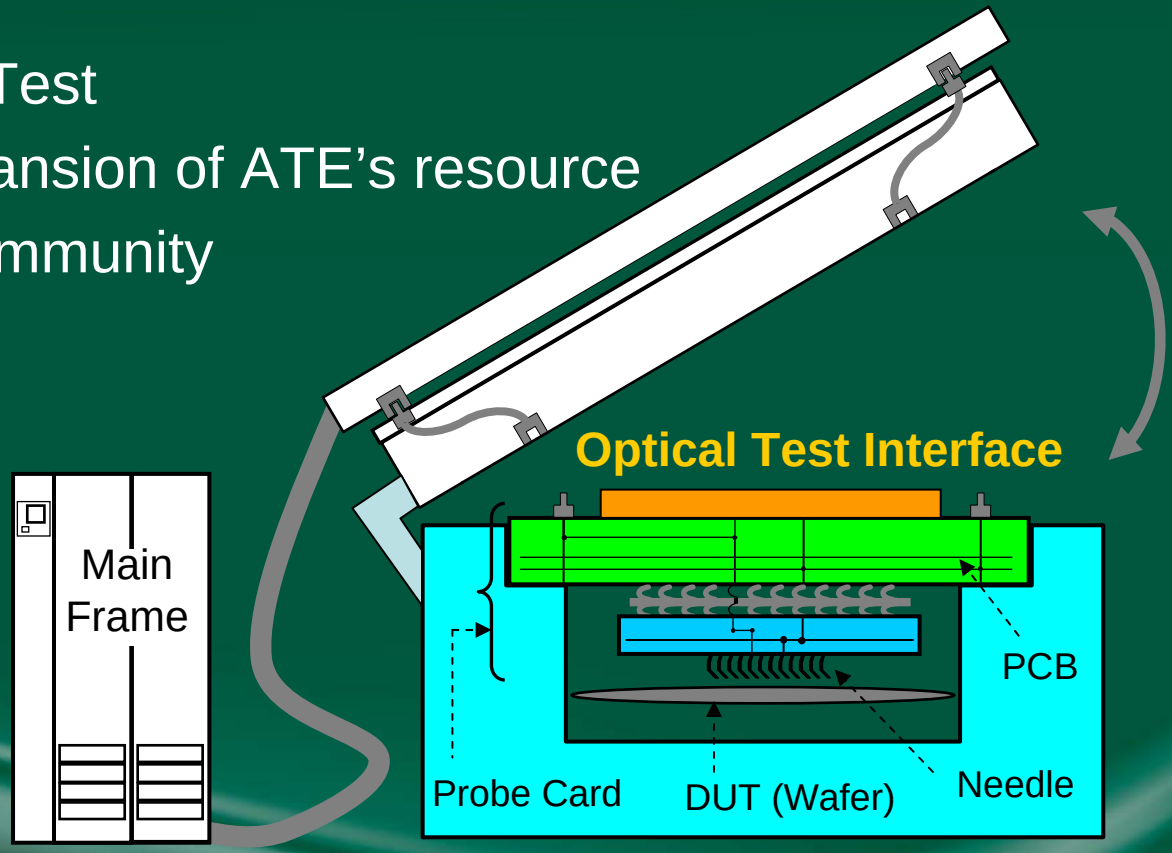
- Immune to electromagnetic interference → Impedance matching not needed



Contents

Introduction

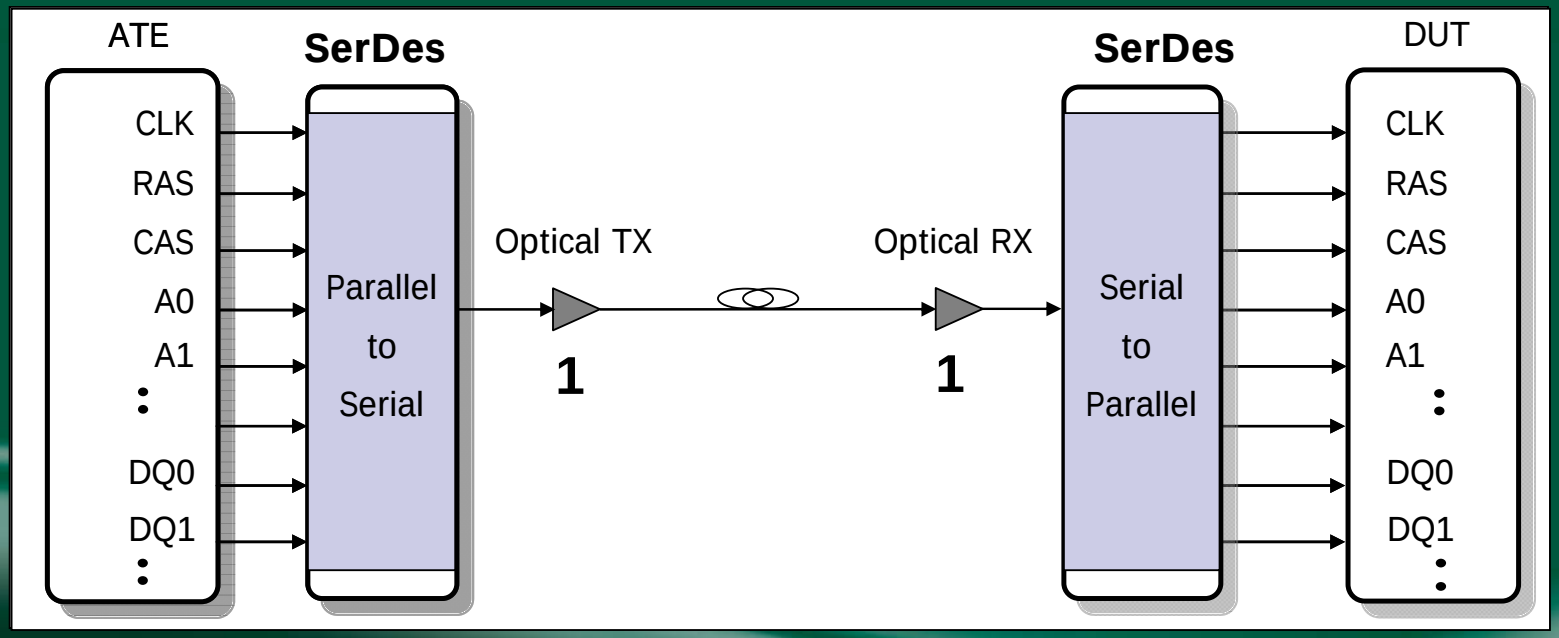
- **Basic concept**
  - Optical Interface is applied onto PCB of Probe Card
- **For what ?**
  - More high-speed Test
  - Scalability for expansion of ATE's resource
  - Good PCB noise immunity



Optical Issue in Test Interface (1)

- **Many of optical modules required (Optical TX/RX + Fiber)**
  - Total of about 80 optical modules including transmitter and receiver when evaluate a single memory chip with only write operation.

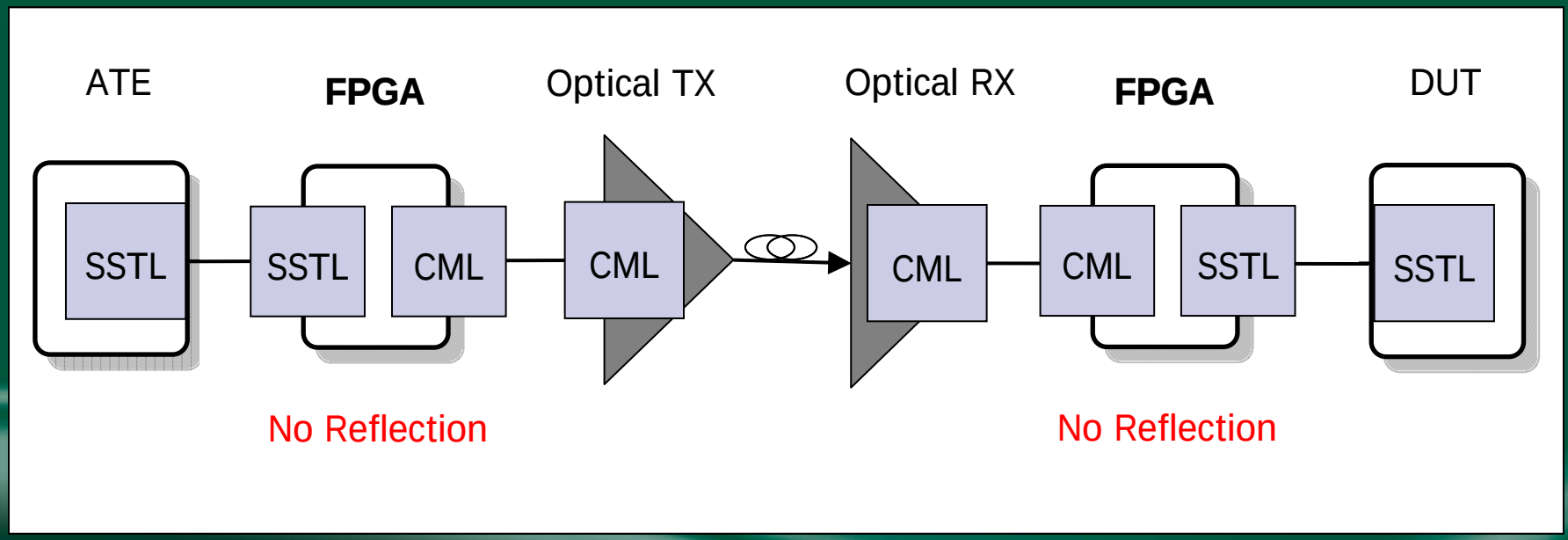
➡ **Solution: SerDes (Serialization/De-serialization) technique**
which combines 8 electrical channels into 1 channel



Optical Issue in Test Interface (2)

- **Interface mismatching**
  - Different I/O interface standards between ATE/DUT and Optical TX/RX
    → Signal Reflection and degradation

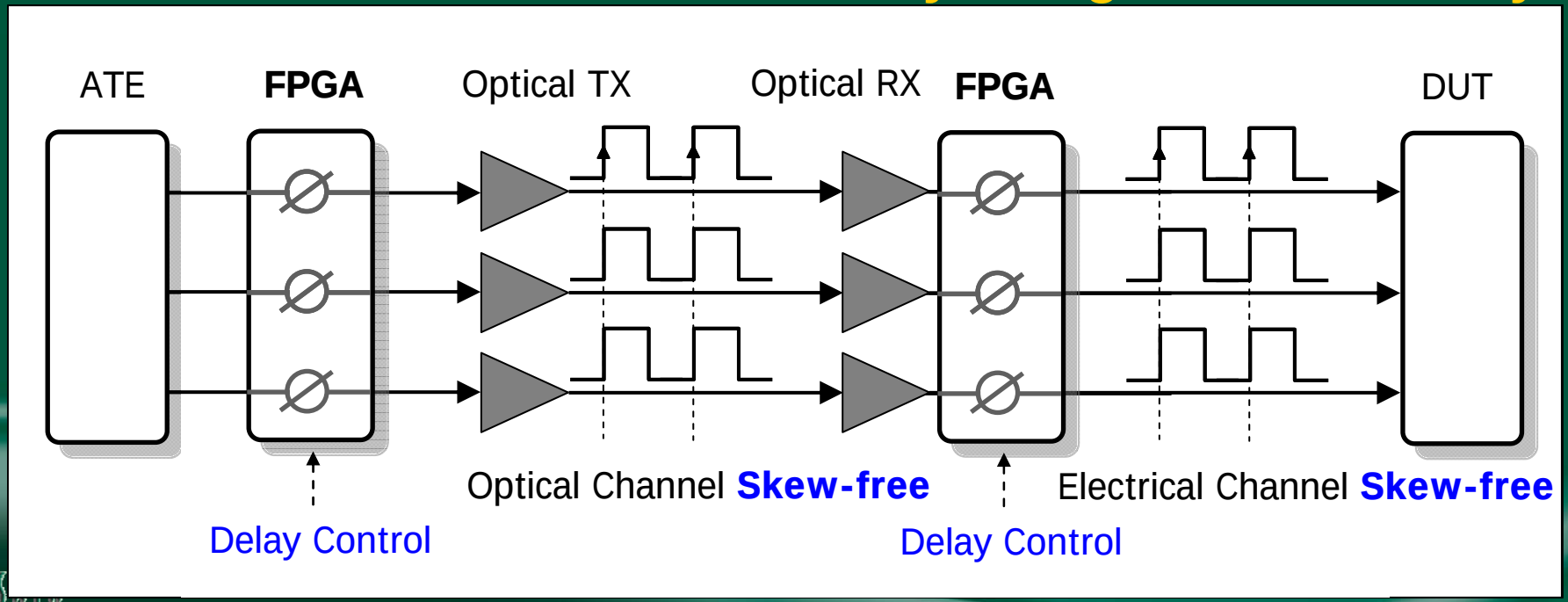
➡ **Solution: Signal level conversion using FPGA logic for the same interface standards**



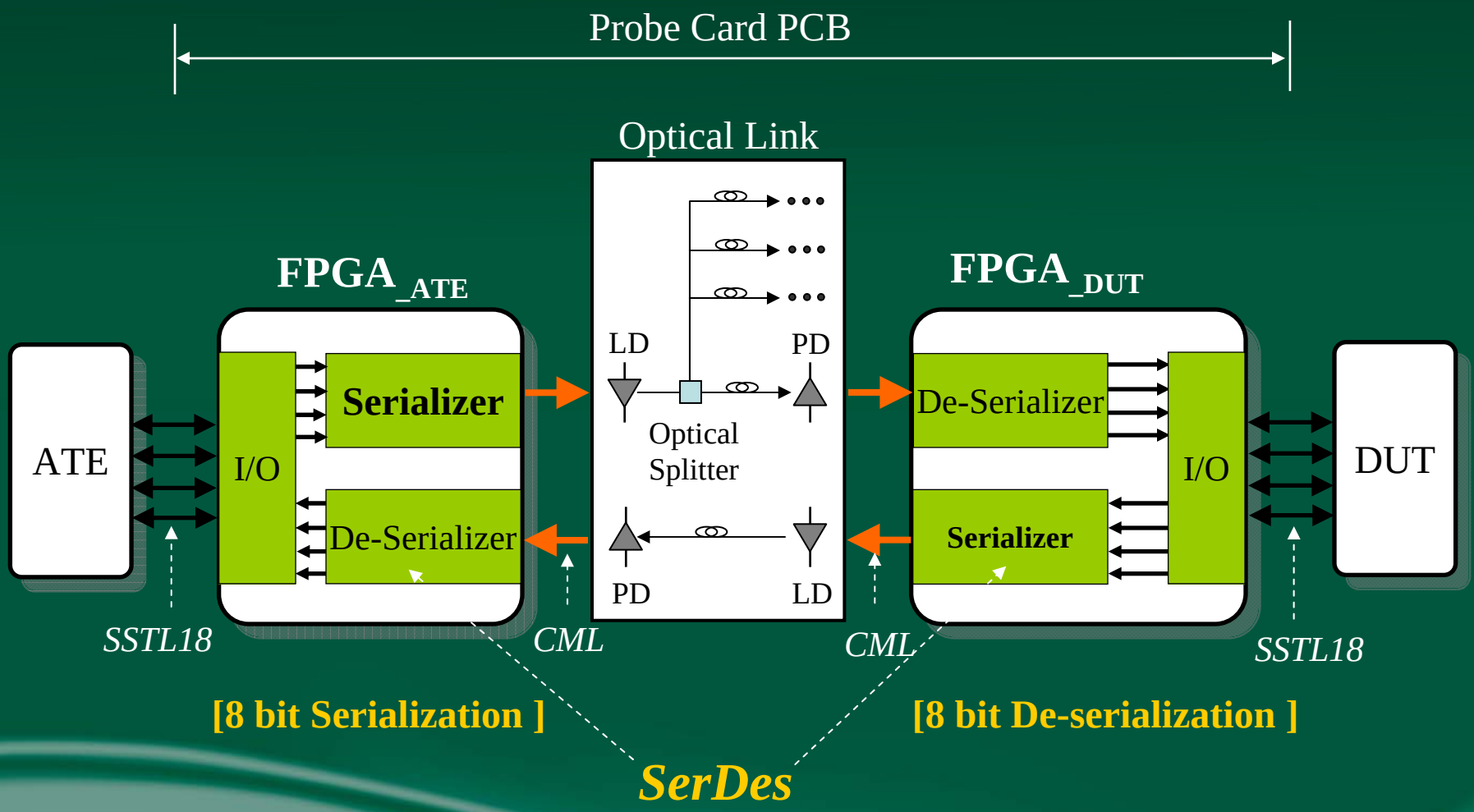
Optical Issue in Test Interface (3)

- **Signal skew in multi-channel interconnects**
  - Impossible to calibrate skews because the optical modules inserted into the electrical path.

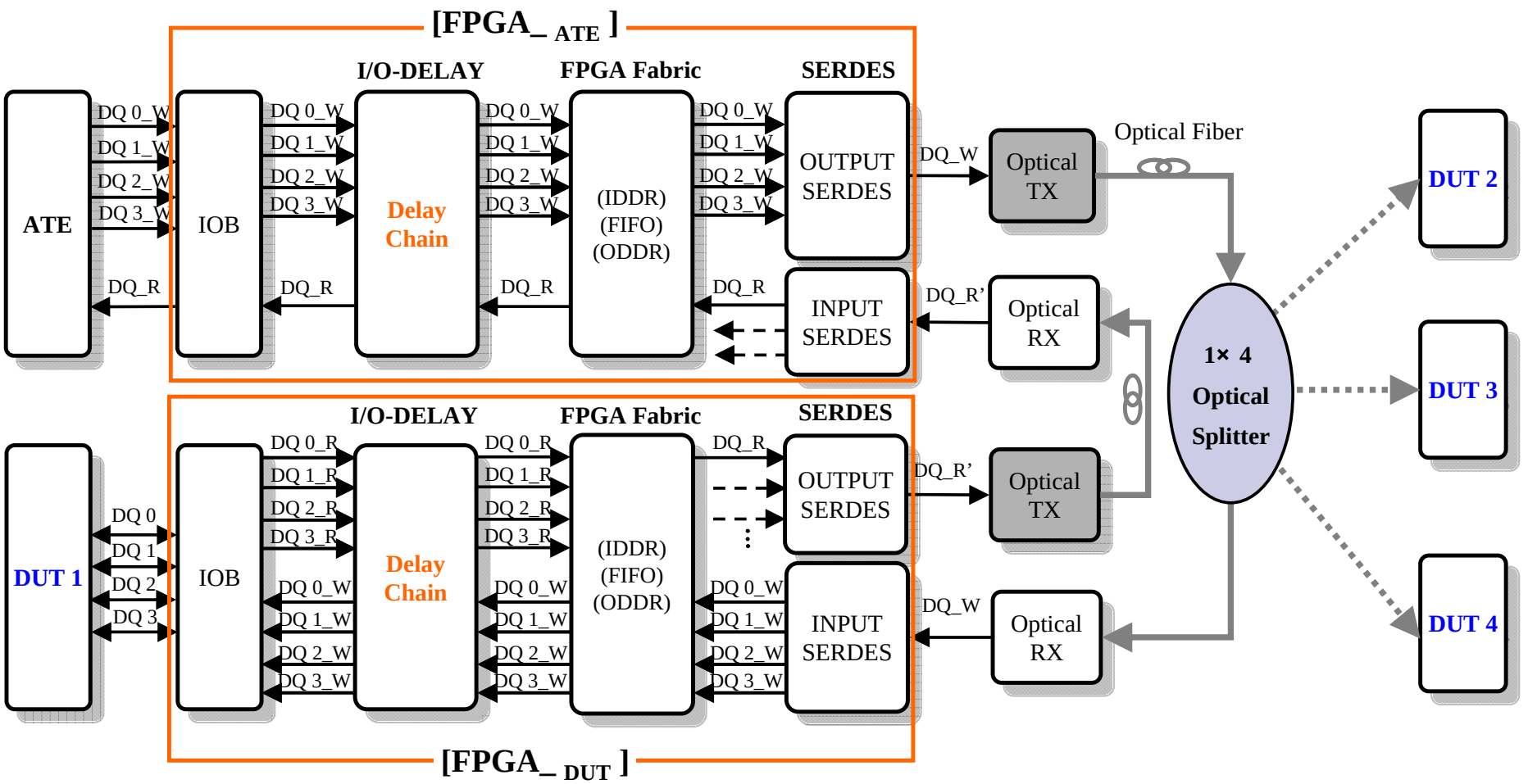
➡ **Solution: Simple skew adjustment technique in optical & electrical channel by using FPGA I/O delay**



Proposed Optical SerDes Interface



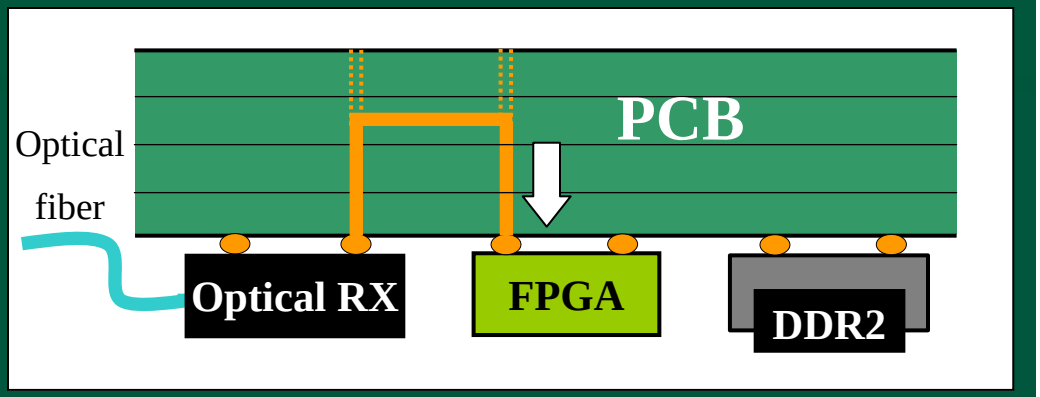
Details

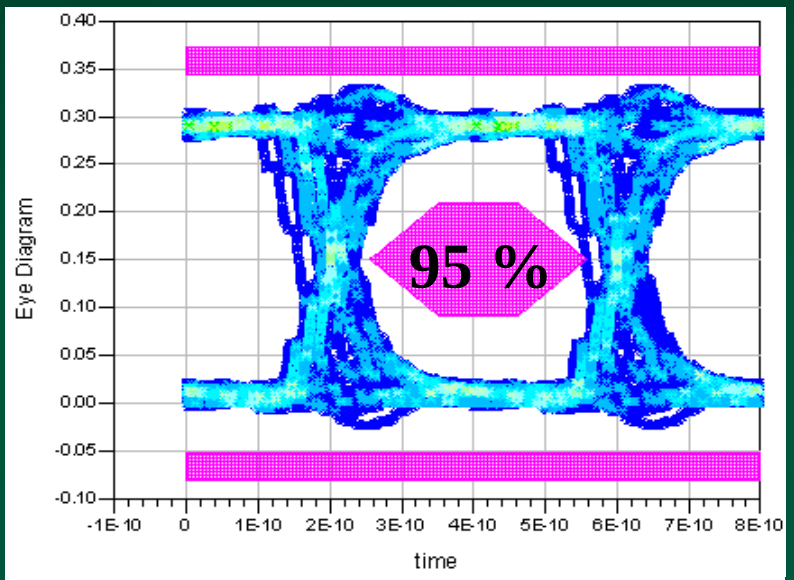

[FPGA_ ATE]
I/O-DELAY
FPGA Fabric
SERDES
ATE
DQ 0_W
DQ 1_W
DQ 2_W
DQ 3_W
DQ_R
IOB
Delay Chain
(IDDR)
(FIFO)
(ODDR)
OUTPUT SERDES
INPUT SERDES
DQ_W
DQ_R'
Optical TX
Optical RX
Optical Fiber
1× 4 Optical Splitter
DUT 2
DUT 3
DUT 4
DUT 1
DQ 0
DQ 1
DQ 2
DQ 3
[FPGA_ DUT]

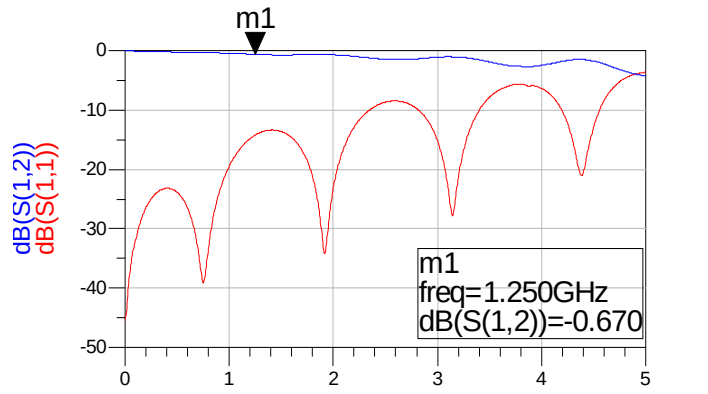
3D Electromagnetic Board Simulation

Serialized 2.5 Gbps Performance

- **FPGA Input Signal (2.5 Gbps)**
  - Differential Line
  - Back-drilling at all DQ via channel



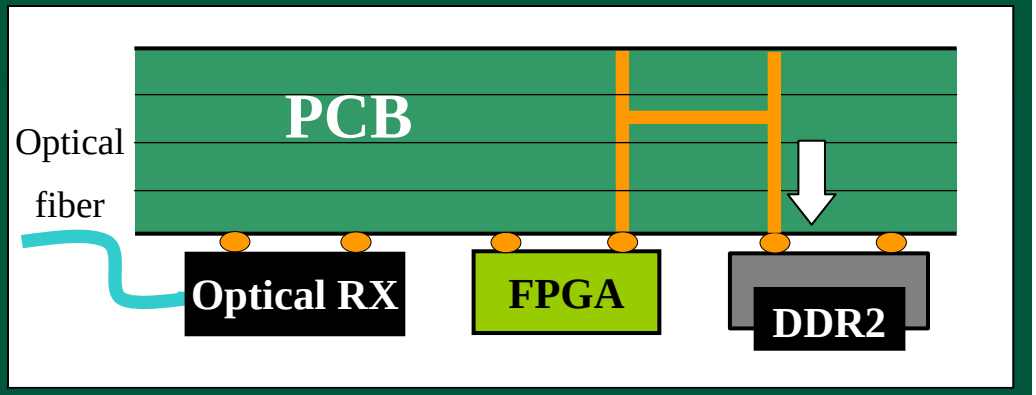


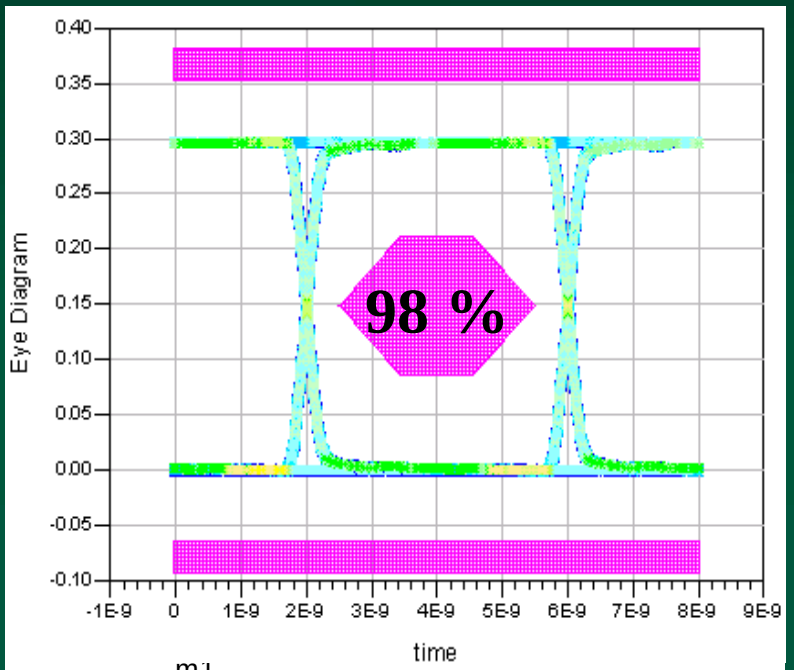


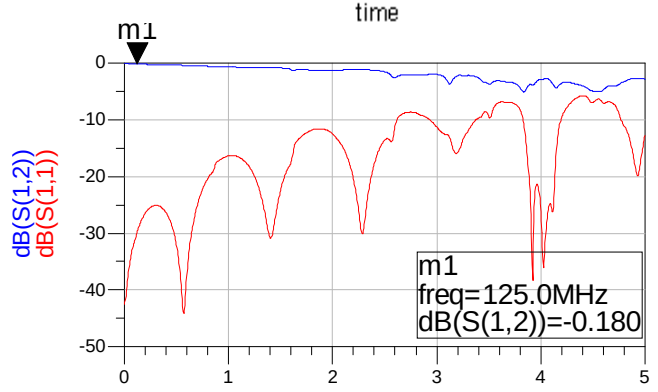
Voltage of 7 % decreases

Write Signal 125 MHz Performance

- **DDR2 Input Signal (125 MHz)**
  - Single ended



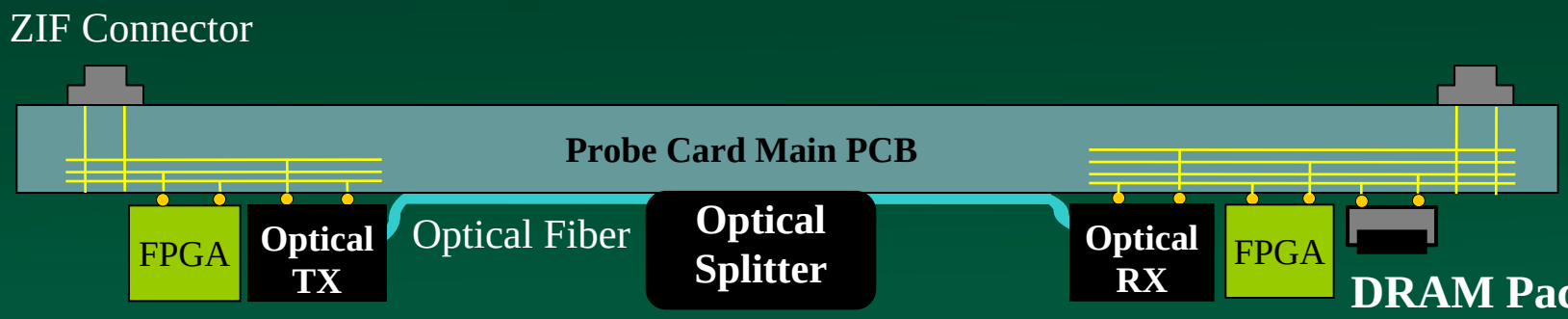


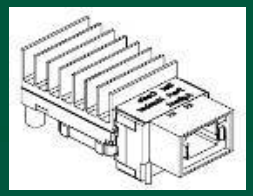


Voltage of 2 % decreases

Measurement and Analysis

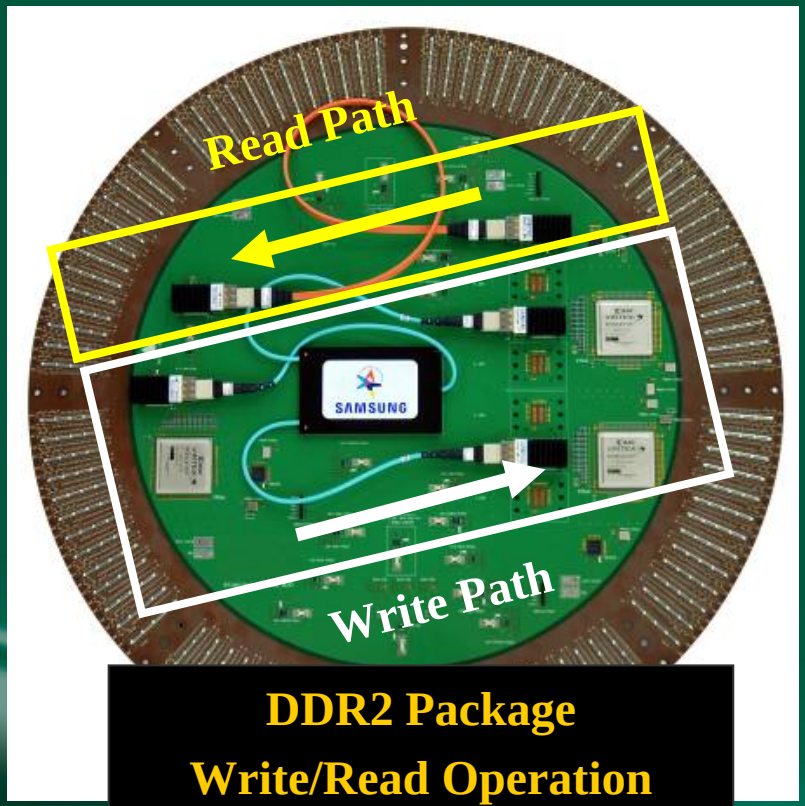
Structure & Operation



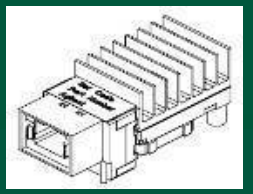


Multi-Channel Optical Module (Transmitter)

1×4 Optical Splitter



DDR2 Package Write/Read Operation



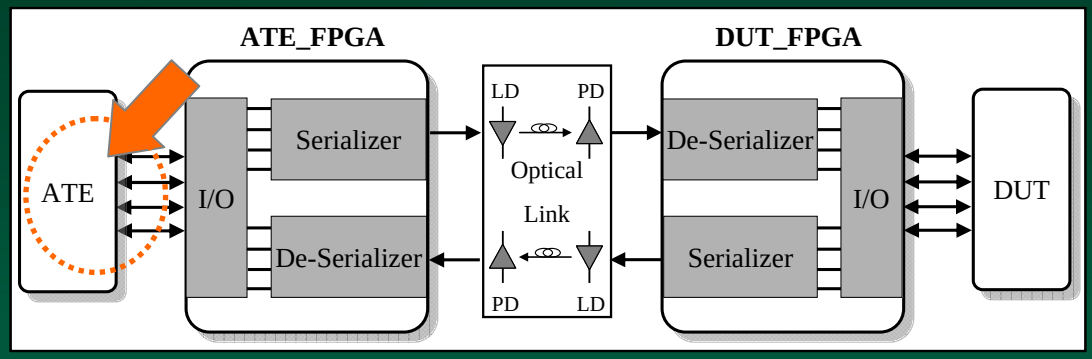
Multi-Channel Optical Module (Receiver)

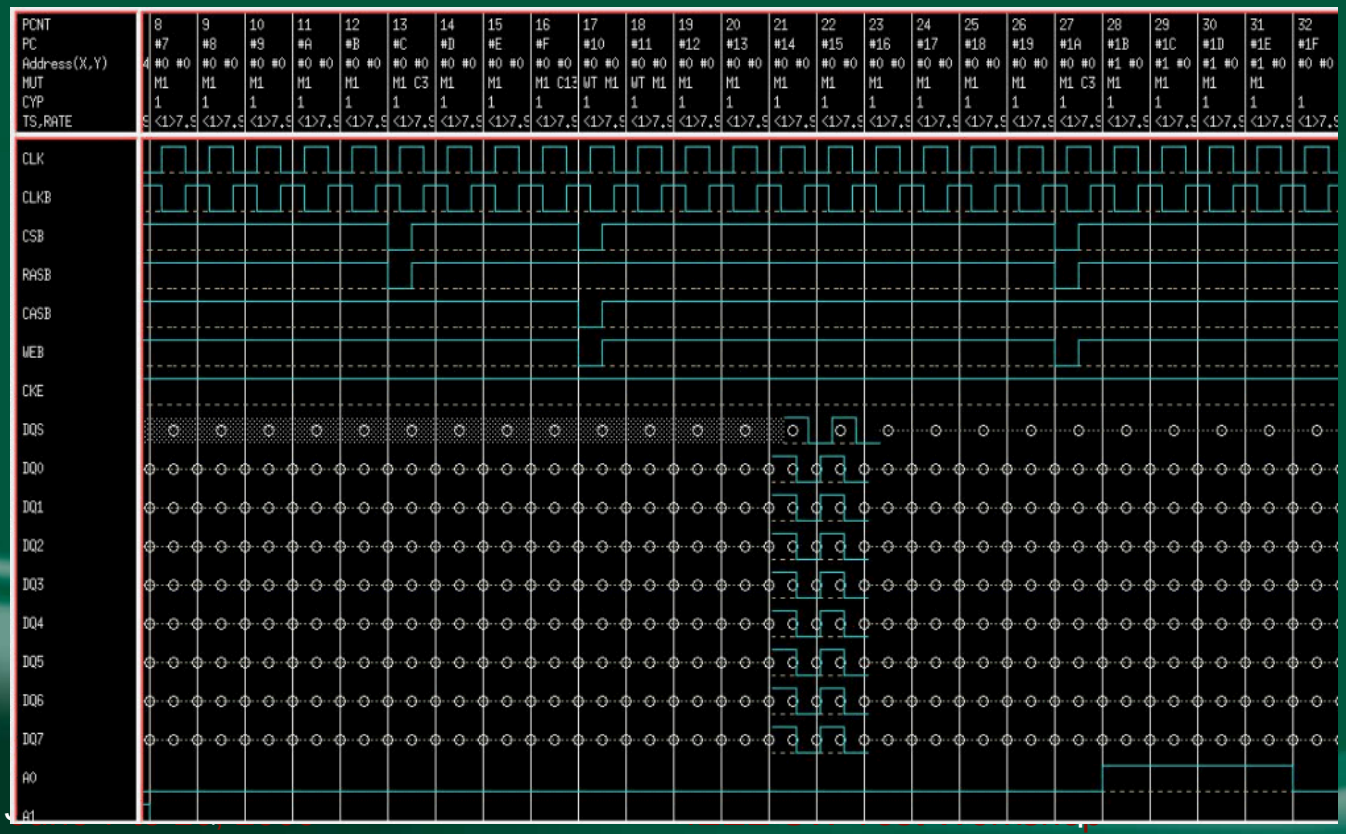
FPGA

Experimental Setup

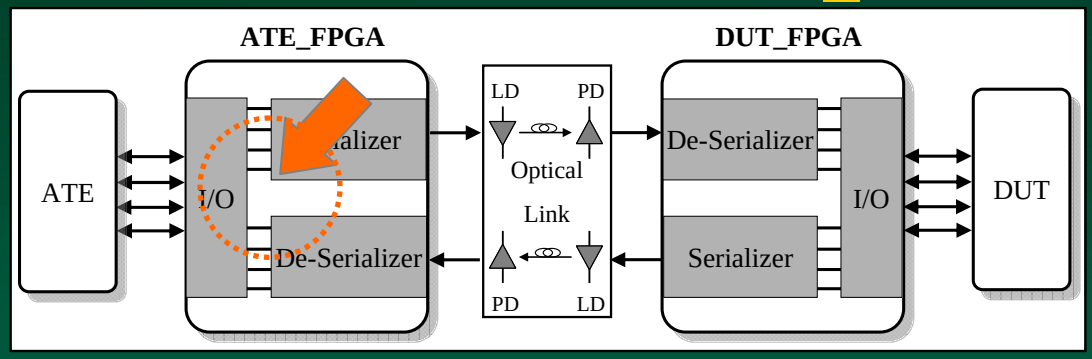
Items	Specification
DUT	• DDR2-533 (60 BOC)_4ea
Optical TX/RX Module	• 5 ea (12 optical channel / Module) • Bandwidth: 2.7 Gbps
Resource Expansion	• × 4 Expansion using Optical Splitter
Transmission	• SerDes (2.5 Gbps)
Test Condition	• X-March Pattern • tRCD = 4 • CL = 4 • Speed = 125 MHz (8 ns) • Background Write/Read

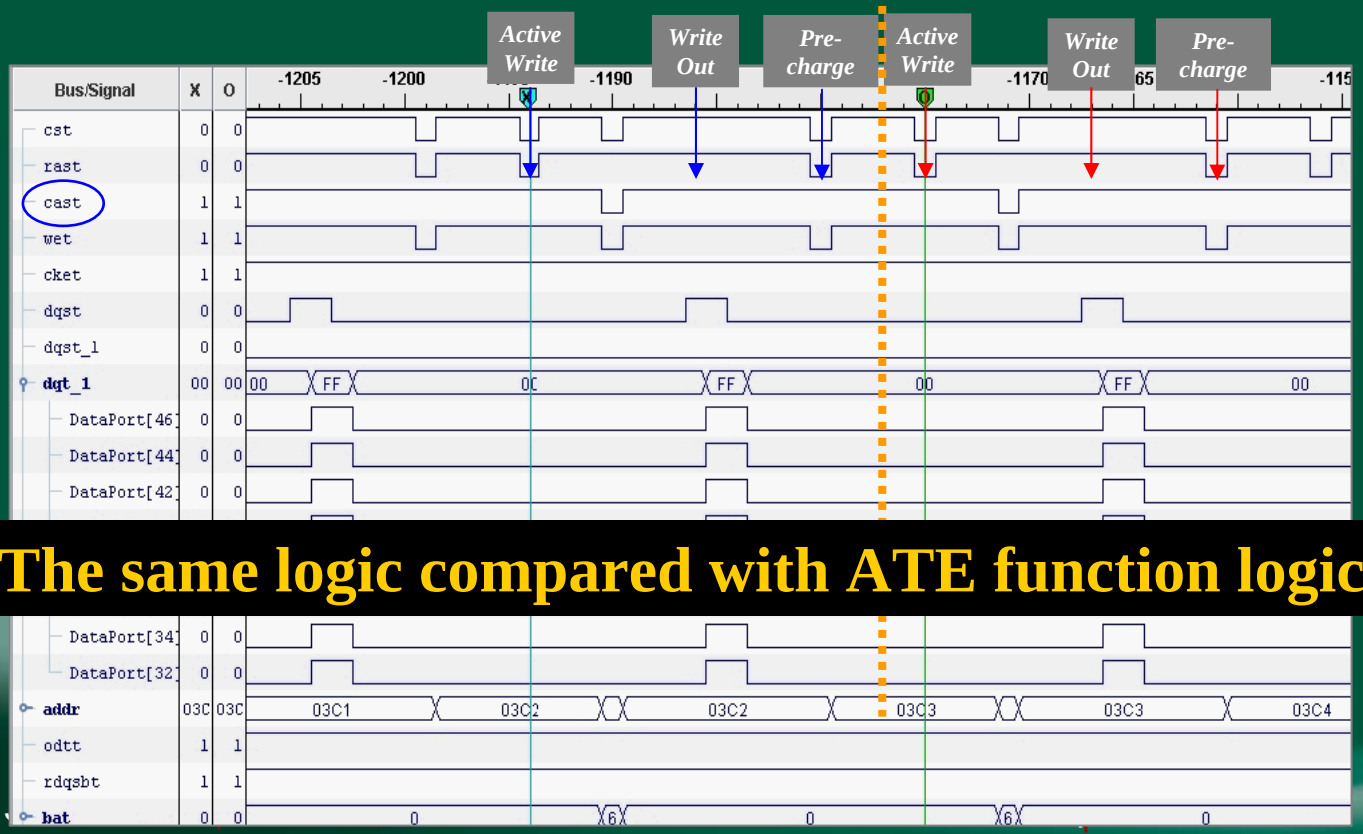
ATE Output Write Signal (125 MHz)





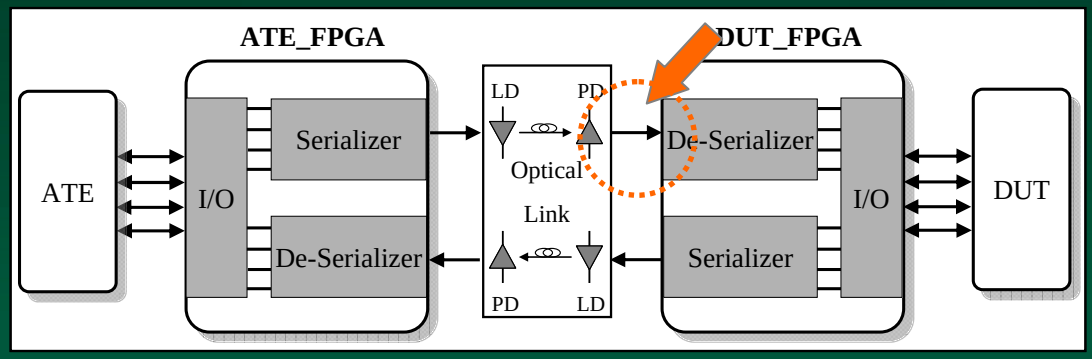
Input Signal into FPGA_ATE (125 MHz)



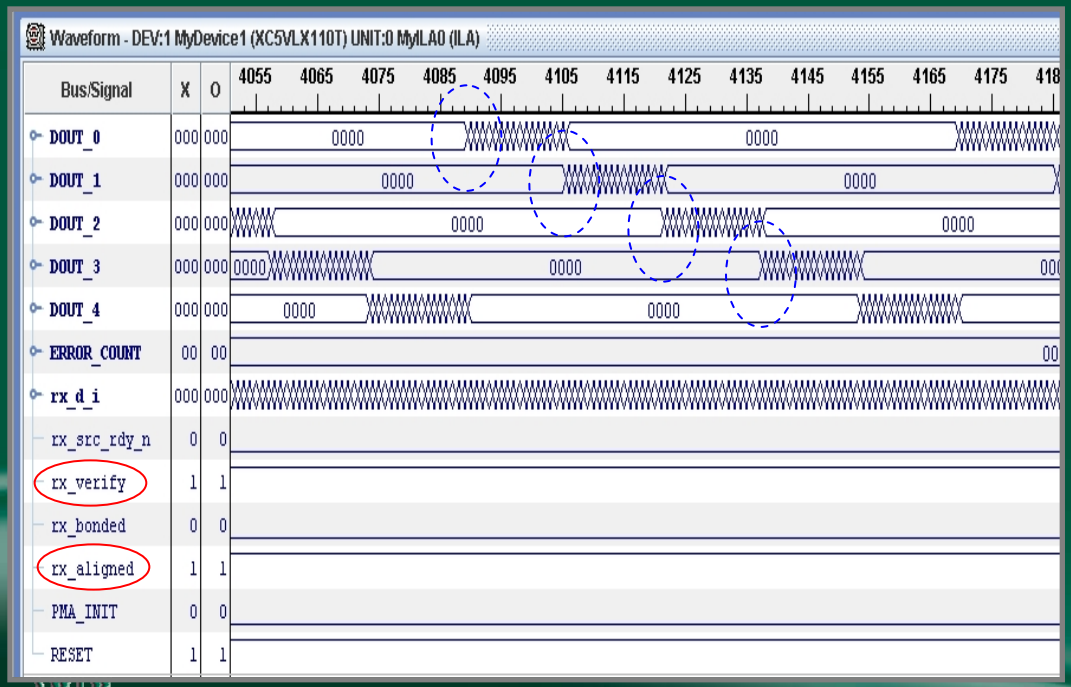


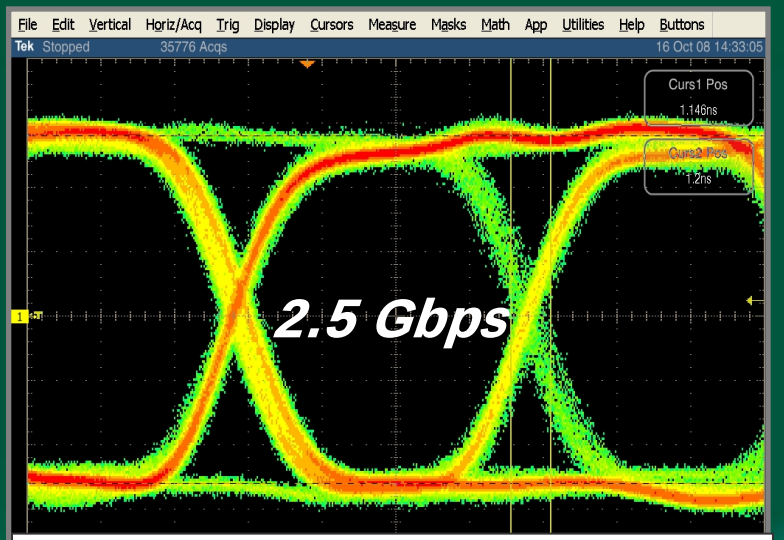
- The same logic compared with ATE function logic

Received Serialized Signal (2.5 Gbps)



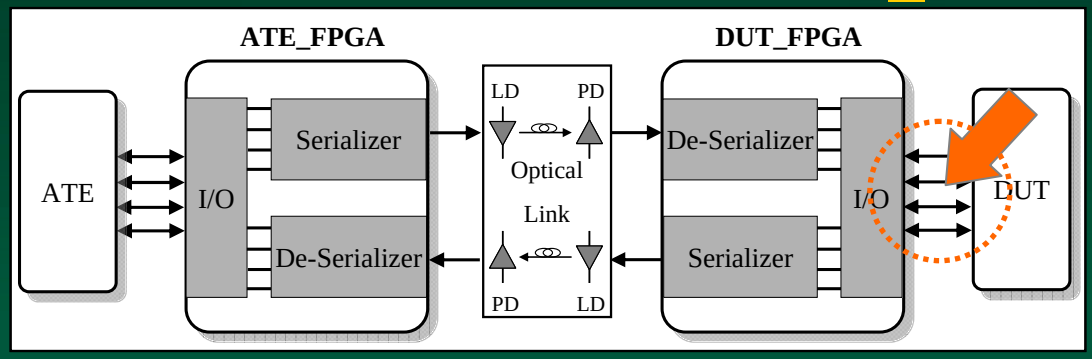
Using Oscilloscope



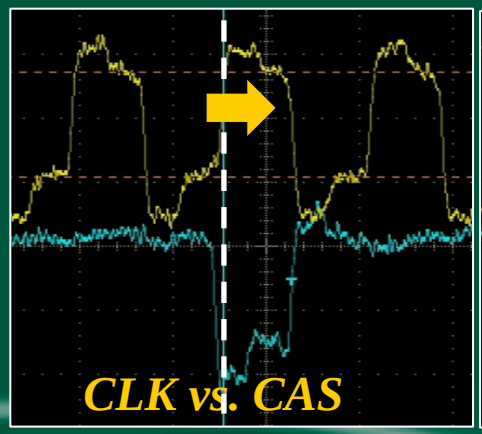


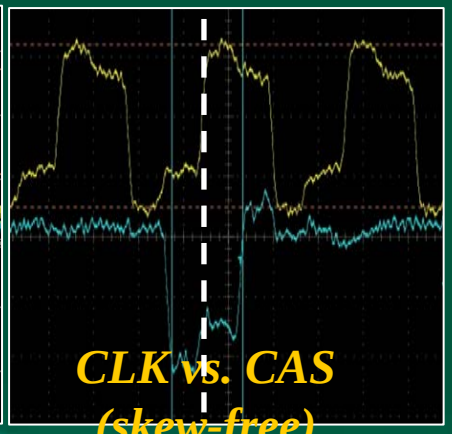
- Amplitude = 270 mV • Jitter = 54 ps
- tR/tF = 180 ps/164 ps

DUT Input Signal at FPGA_DUT (125 MHz)

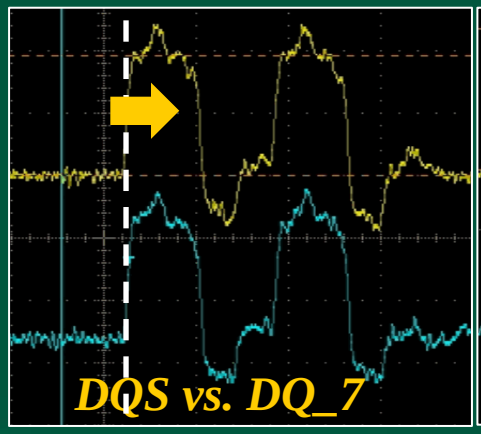


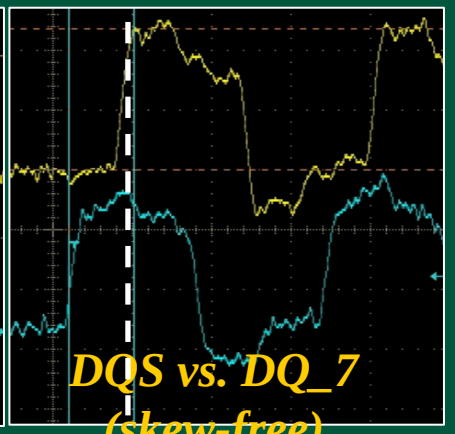
[Skew Control using FPGA IO-delay]





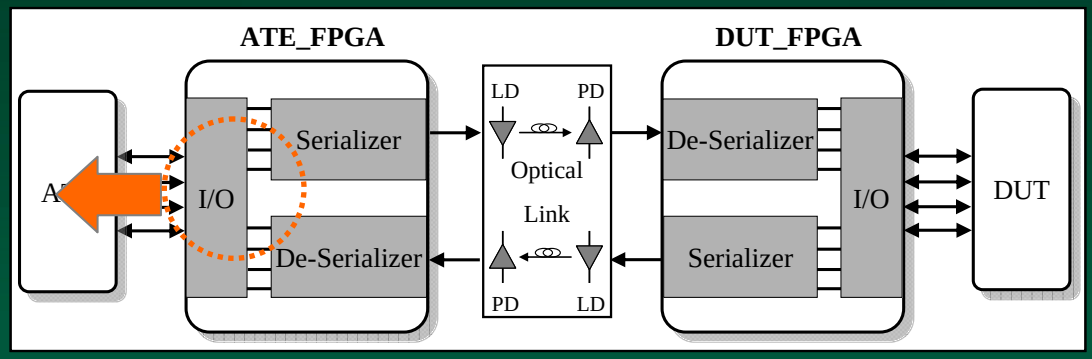
CLK = 2 ns Delay

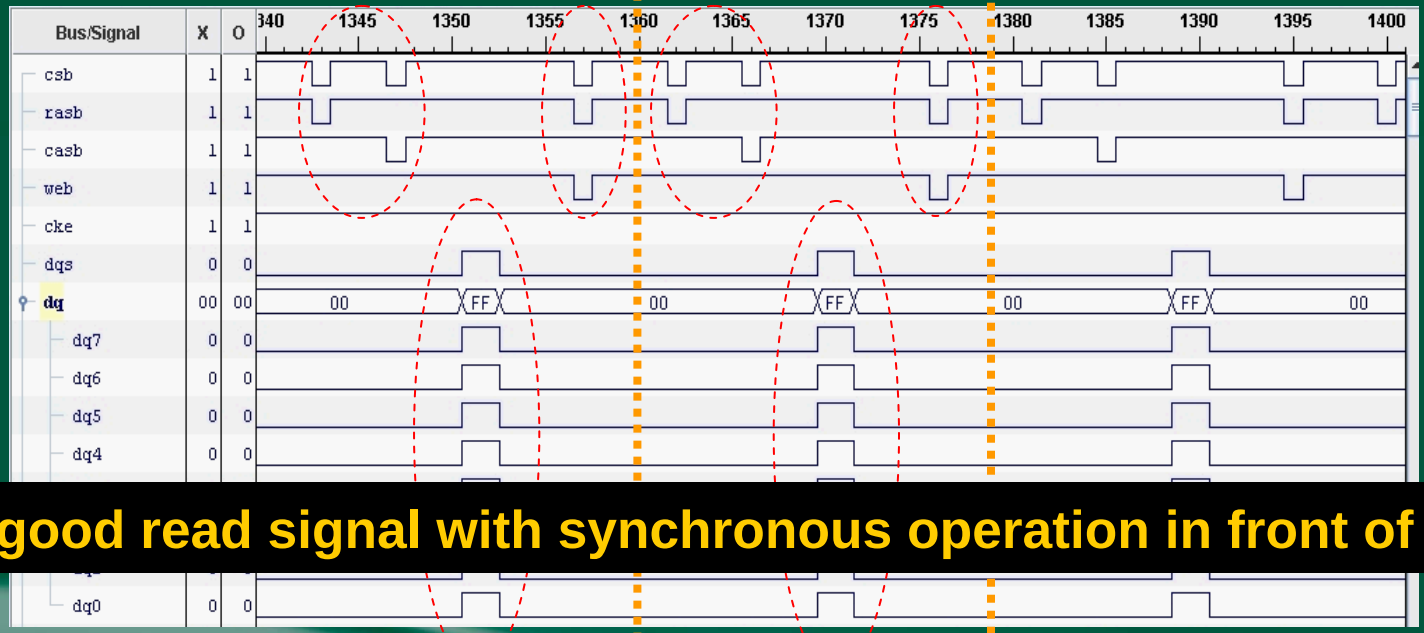




DQS = 2 ns Delay

Read Signal into ATE Comparator





All good read signal with synchronous operation in front of ATE.

Hardware Performance

Performance \ Type	Conventional System	Optical SerDes System	Advantage
# of Optical fiber for 1 DUT	40 ch	5 ch	1/8 reduction
# of Optical Module (TX and RX)	80 ea (only write-mode)	2 ea (Parallel modules used)	1/40 reduction
ATE channel expansion	Not expanded	by Optical Splitter	4 times expansion

Summary

- **Optical signal 4 times splitting scheme and SerDes techniques for a multi-parallel high speed memory test**
- **An actual write/read optical memory test operation**

- **Optical fiber channels of 87 % and Optical module of 95 % are reduced dramatically, compared to a conventional optical interface**

- **Further, this scheme, with proper modifications and optimizations in terms of size and power, might be applied for CPU-memory optical interconnects in the future computing environment.**