IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Overcoming challenges of high multi-site, high multi-port RF wafer sort testing

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Worldwide RF Semiconductor Market Trends: Strong Growth and integration into almost everything

7,000,000
6,000,000
5,000,000
4,000,000
3,000,000
2,000,000
1,000,000
0

Capacity increase

2001 2002 2003 2004 2005 2006 2007 2008 2009 2010 2011

Total
Cellular Handsets
Cordless Phone
WLAN
Bluetooth
GPS
UWB
WiMax
DVB-H & T-DMB
Zigbee

Source: Gartner, iSuppli (2007)

RF Unit Volume

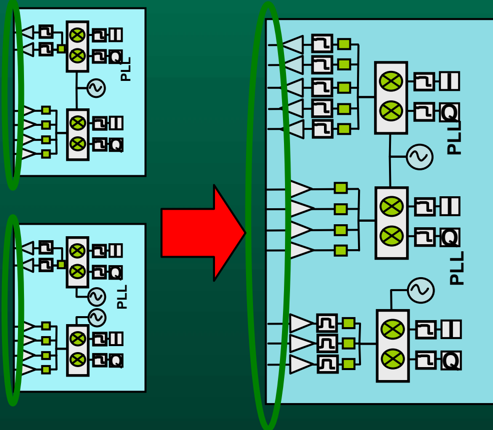
Device Complexity*

Product Life Cycles

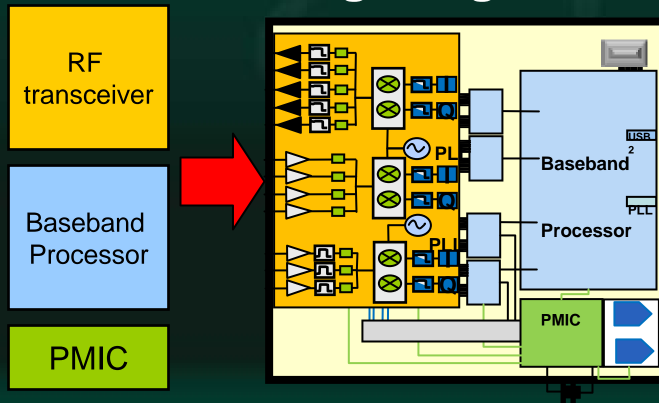
ASP

Increasing Device Integration in RF and Digital impose design constraints

Multi-mode Transceivers, MIMO



RFSOC – Single Chip Radio & Analog Integration



Complexity Impacts

- RF Port Count ↑
- Parallelism ↑
- Package Size ↓
- Digital Baseband ↑
- High Speed Serial ↑
- Test Time ↑
- ASP ↓

Interface Design Challenges

- Increased Applications Space
- Higher RF mating forces
- High Digital Pin Force
- Signal Integrity
- Current Prober Capabilities
- COT - Leverage existing interface technology
- COT - Minimize interface circuit board cost

What do we mean by high multi-site, high multi-port RF wafer sort testing?

High Multi- Site:

- Above x2
- Up to X8 (and to X16 future)

Digital Pins

- Greater than 2000 signal pins

Multi-Port RF:

- Up to 16 RF Ports per device
- Low density = 24 RF Ports total
- Medium Density = 64 RF Ports total
- High Density = 96 RF Ports total

Essentially, get 10 pounds of Wafer S#!T test into a 5 pound test interface bag…

Look at the entire RF interface as a system – define what is important so Intelligent Tradeoffs can be made…

RF Probe: Criteria Weighting

Criteria	Weighting
Bkwrd Compatibility	3%
COGS	6%
Compatible High Speed Digital	10%
Applications Space	11%
Signal Integrity	11%
Digital Signal Pin Count	13%
RF Port Count	14%
Schedule	14%
Reliability/Lifetime	16%

Applications Space – Some Applications can require more space than is available with 300mm hardware

Space Constraints:

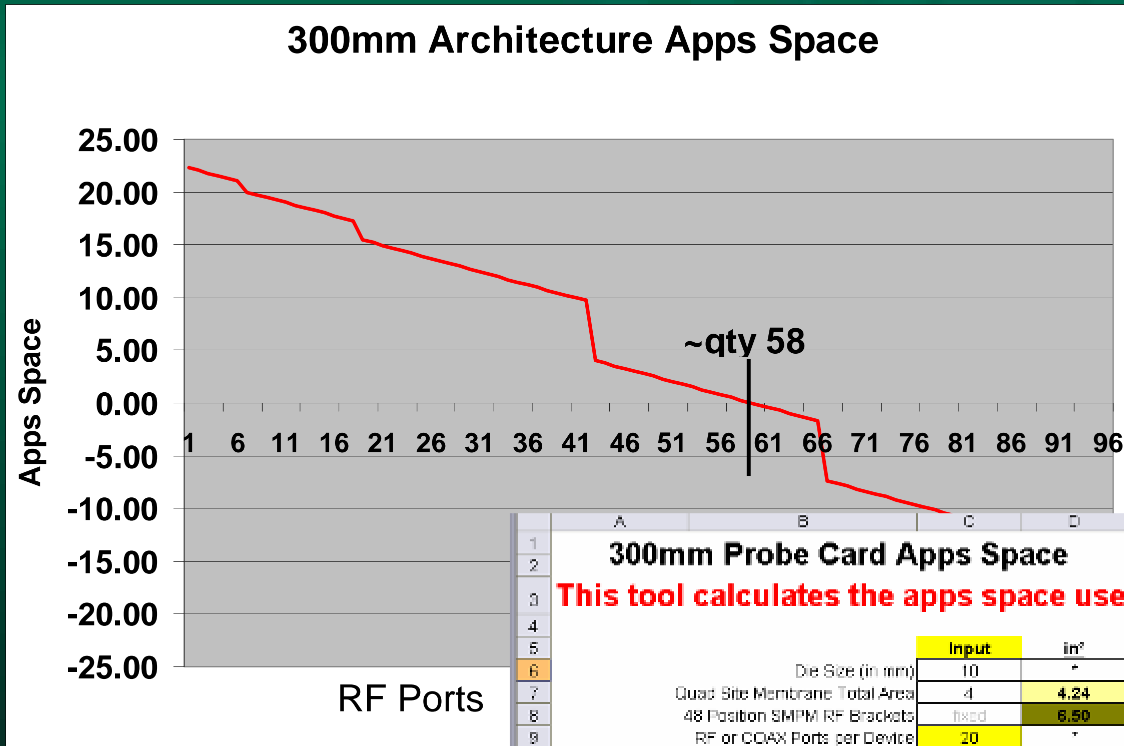
- PC size = 100%
- Stiffener 21%
- Traces 20%
- Digital Pins 19%
- Components 16%
- RF Hardware14%
- RF connector 10%
- Contactor -5%

Design Tradeoffs:

- 300/440 hardware
- Deflection
- RF vs. Digital Pin Count
- Cable Routing and bending
- Signal integrity
- Component placement

RF Interface Forces Can overload interface components

Managing Applications Space



Build mathematical models of your applications space

- Stiffeners
- Traces
- Digital Pins
- Components
- Contactors
- Etc…

300mm Probe Card Apps Space

This tool calculates the apps space used for RF

	Input	in²	
Die Size (in mm)	10	*	
Quad Site Membrane Total Area	4	4.24	
48 Position SMPM RF Brackets	fixed	6.50	
RF or COAX Ports per Device	20	*	96
SMPM Thru-Board and R/A connector .16" x .46"	fixed	9.14	13.72
Total RF ports per probe card	64	*	
0402 Components Qty	20	0.016	.04 X .02
0603 components Qty	20	0.036	0.06 X .03
Other Components Qty			Need Size Data
Other Components Qty			Need Size Data
Traces, fencing vias, etc		0.000	Need Apps Data

3.141592654	
radius	1
circular area	3.14
Apps space used by RF	19.94 in sq
300	11.81102362

Signal Tower	Available Tower Apps Space	Probe Area Apps Space (in²)	Total Pins	Force (lbs)
Signal Tower Type	29.43	9.49	3,600	630

300mm Application

Applications Space

SMPM Right Angle Connector

SMPM RF Bracket

Include variables to manipulate the apps space tool for various what-if scenarios…

Evaluate tradeoffs.

Managing Applications Space

Consider the Transition to 440mm Interfaces

*may require capital $

Space Constraints:	Design Tradeoffs:
PC size = 100%	300/440 hardware
Stiffener 22%	Deflection
Traces 20%	RF vs. Digital Pin Count
Digital Pins 13%	Cable Routing and bending
Components 10%	Signal integrity
RF Hardware10%	Component placement
RF connector 6%	
Contactor 2%	

Managing RF Interface Forces

Model and Understand the tradeoffs required to meet force constraints

300mm Prober Forces - RF Ports vs Signal Pins Tradeoff

Prober Forces Available

Qty Signal Pins: 0, 200, 400, 600, 800, 1000, 1200, 1400, 1600, 1800, 2000, 2200, 2400

Qty RF Ports: 0, 8, 16, 24, 32, 40, 48, 56, 64, 72, 80, 88, 96

1513

1436

1153

PROBER1 PROBER2 PROBER3

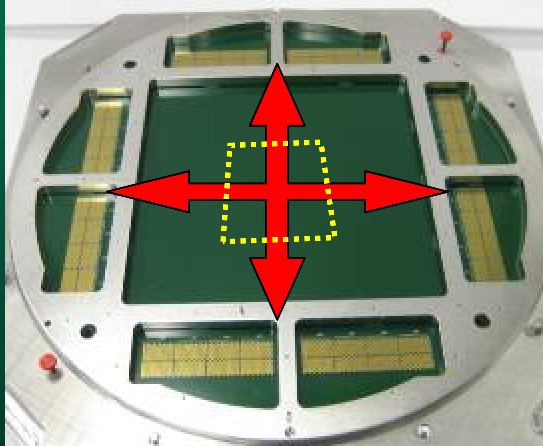
Design Tradeoffs:

- Top Load vs. Bottom Load Interface Systems
- Bottom Probe Card Changer capacity
- Tester docking capacity
- Deflections
- RF vs. Digital Pin Count
- Don't forget un-mate forces…

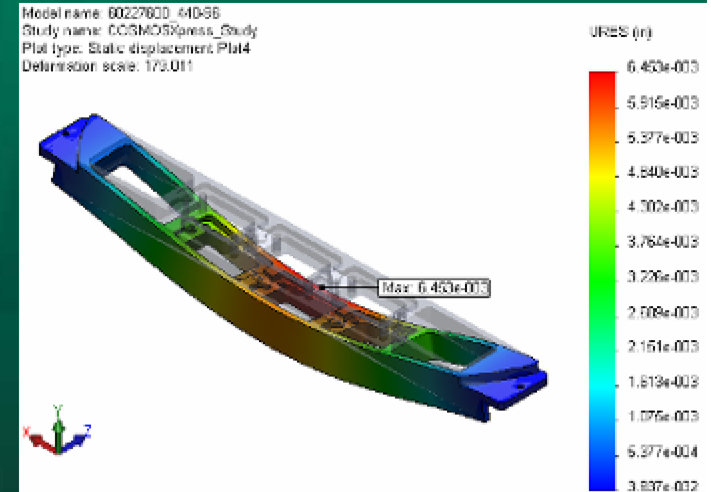
Managing RF Interface Forces

Maximizing applications space and minimizing probe card deflections

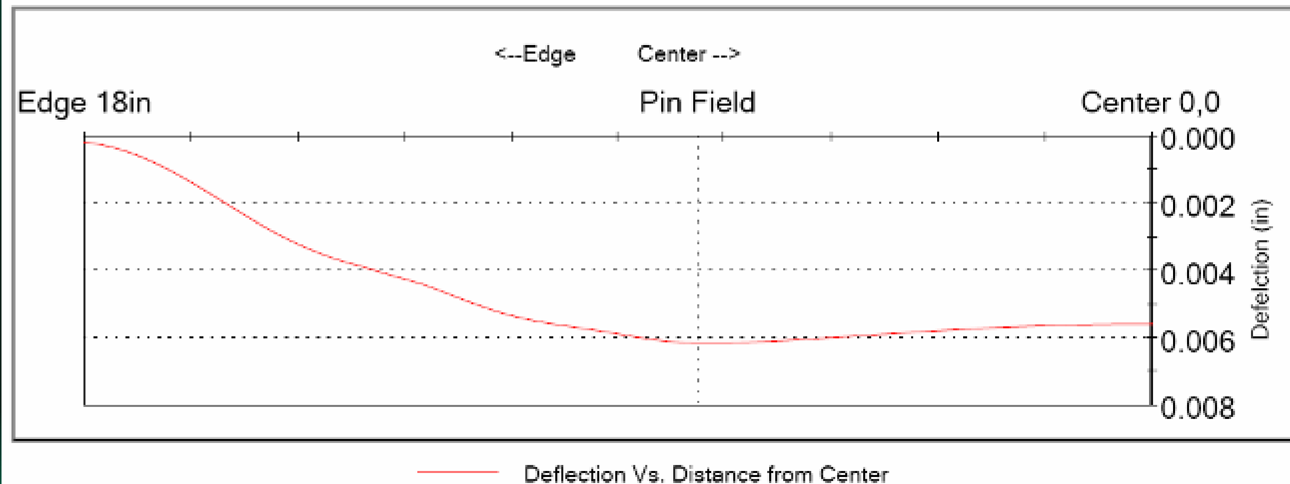
440mm Probe Card Stiffener



- Digital pins and RF connections at perimeter
- More apps space
- More structure to minimize deflection



440mm Probe Card Deflection Profile



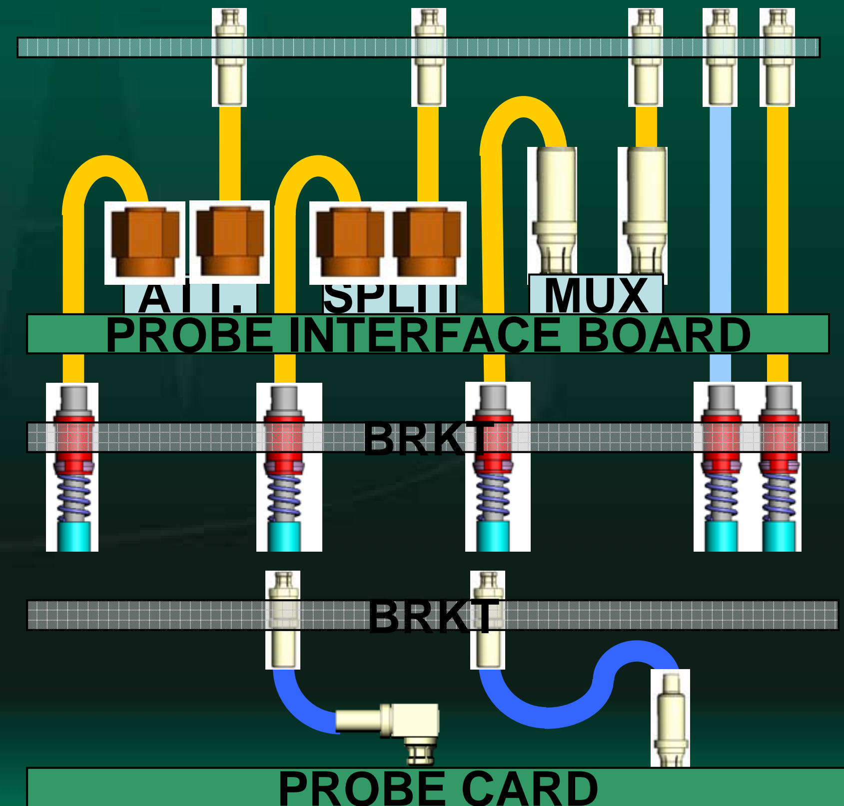
440mm 96 Port RF hardware Deflection Study

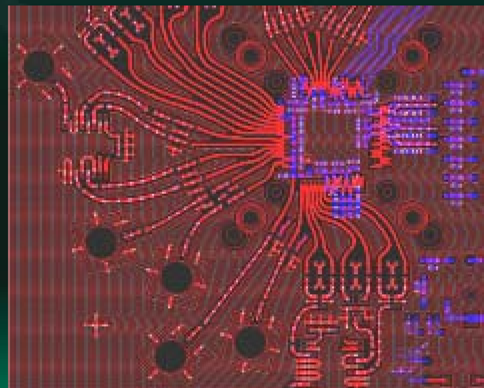
Maintaining RF Signal Integrity/Reliability

<u>Leverage existing technologies</u>:

- Integrate with cable vendors to maximize performance while supporting required bend radii, cable diameter, connector options, etc…
- RF connector types (custom SMPM) have

  Proven signal Integrity, reliability
- Multiple connector styles allow application flexibility
- Support muxing, splitting, attenuation, etc.
- Allow active/passive component placement as close to DUT as possible



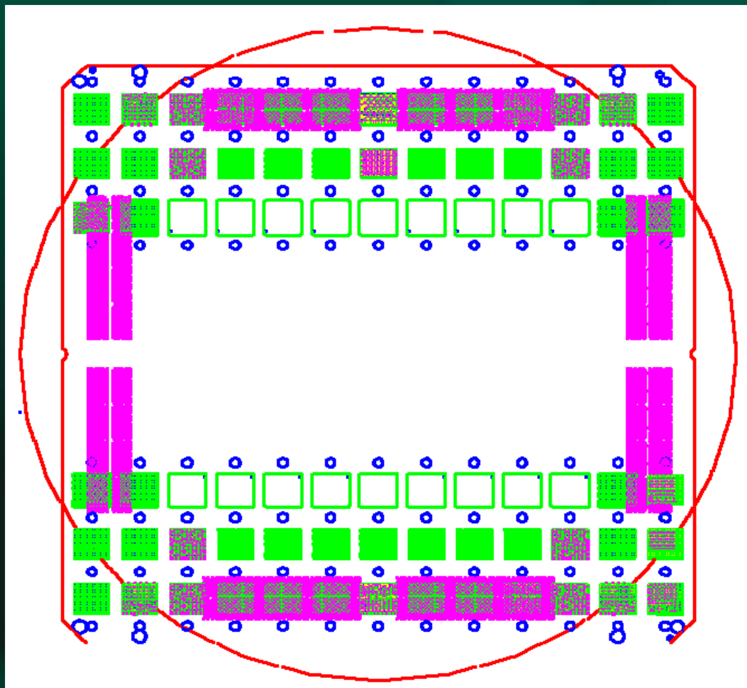


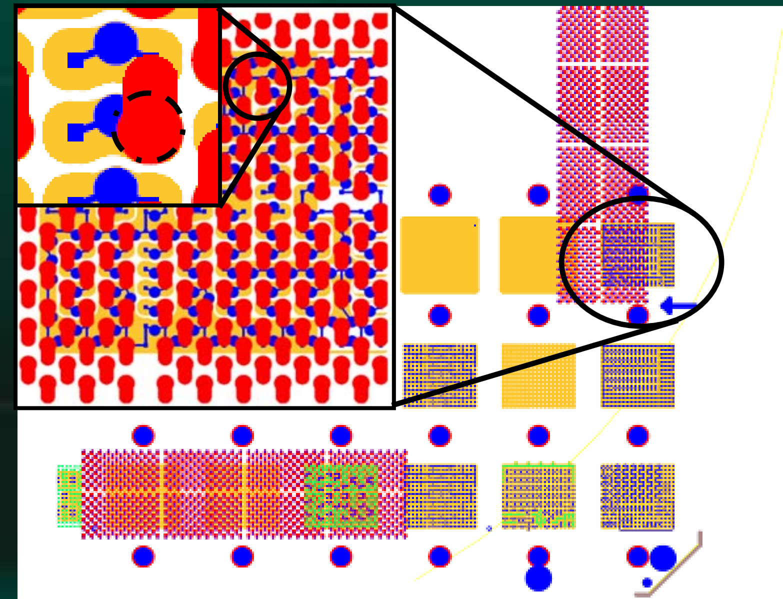
COT – Managing Interface Circuit Board Design

Plan the board design with signal tower, apps space, and board routing integrated early.

Careful design and routing can facilitate pass through connections.

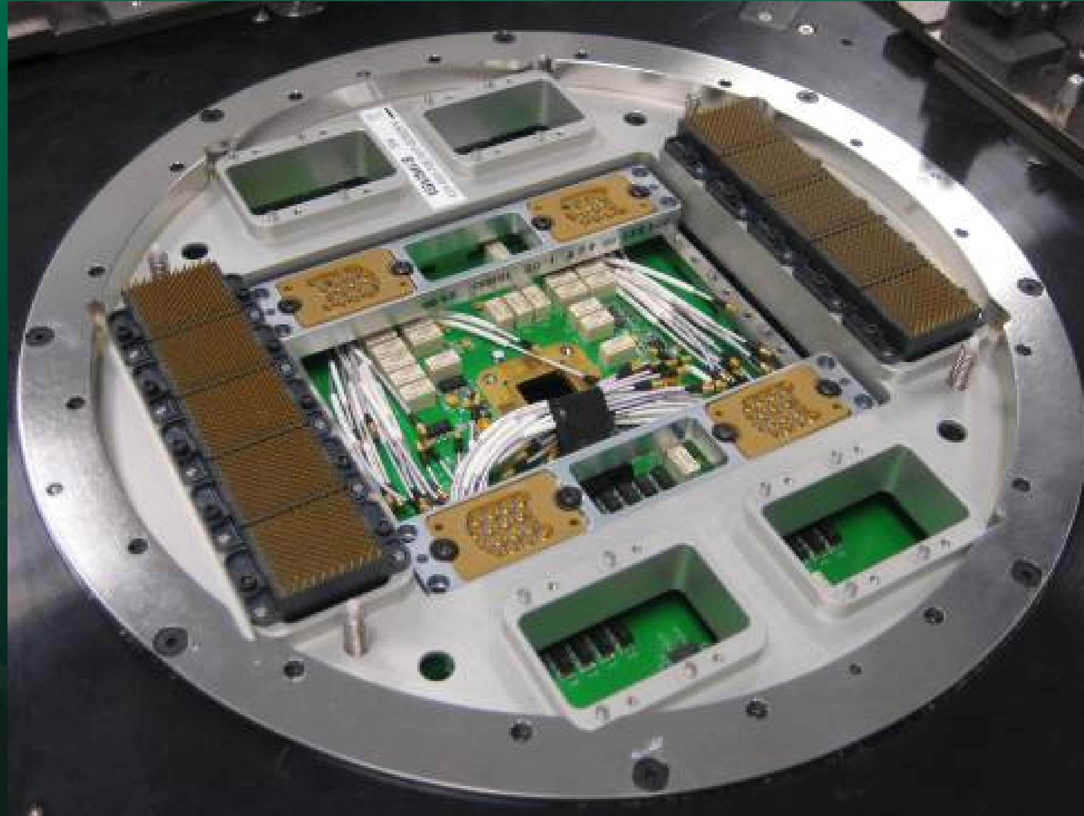
Avoid Blind Vias
Avoid Multi-layer Construction
} **Potential $30% Savings**





Real 300mm RF Hardware

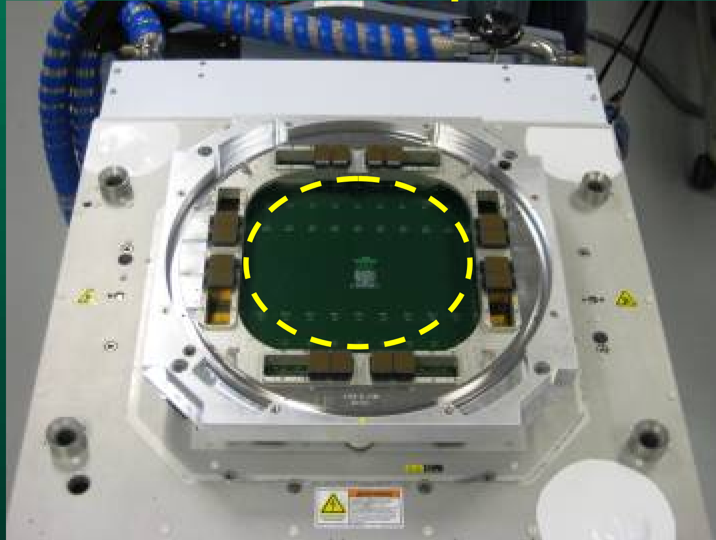
300mm with 64 RF Ports 900 digital pins

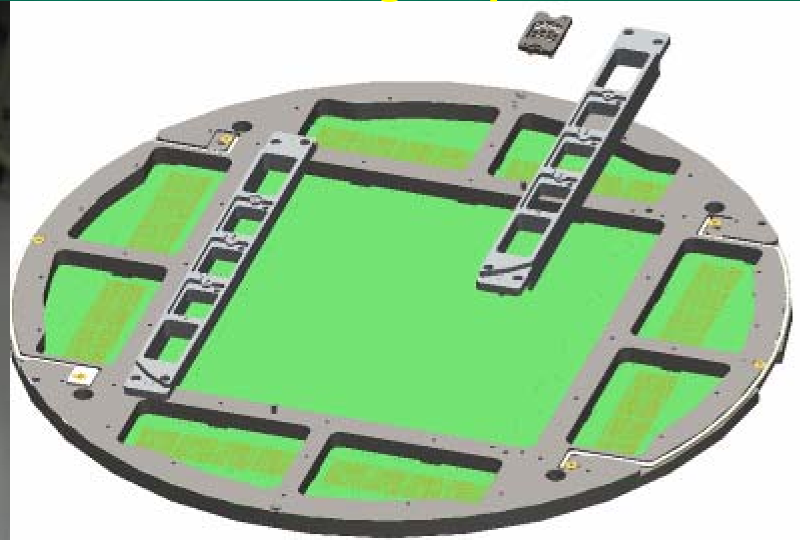


You can still pack a lot of punch into a 300mm interface with careful planning

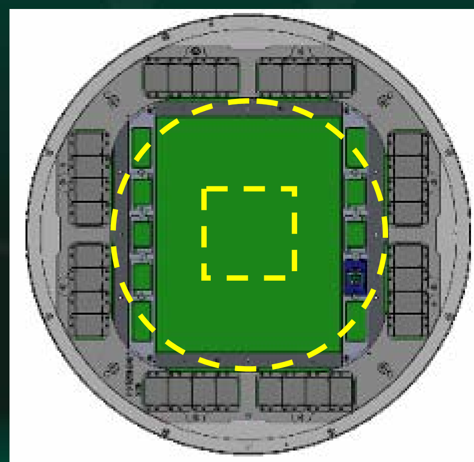
Real 440mm Solutions

440mm Probe Tower and Probe Card
with up to 96 RF Ports and 2880 digital pins





20 inch chrome



20 inch pizza

In Conclusion…

- High density RF interface solutions pose some significant challenges, but are very manageable.
- Teradyne has done quite a bit of work to understand and define these challenges, and managed them to develop solutions that work.
- The key is to think big picture, act as a general contractor or system integrator.
- Learn the capabilities of the existing equipment technologies.
- Build tools that let you evaluate tradeoffs and investigate the variables of what-if scenarios.
- These challenges can be overcome with proper planning and careful implementation!