IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 7-10, 2009
San Diego, CA

High Speed Pre-Probe Wafer Inspection

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INSPECTION INC.

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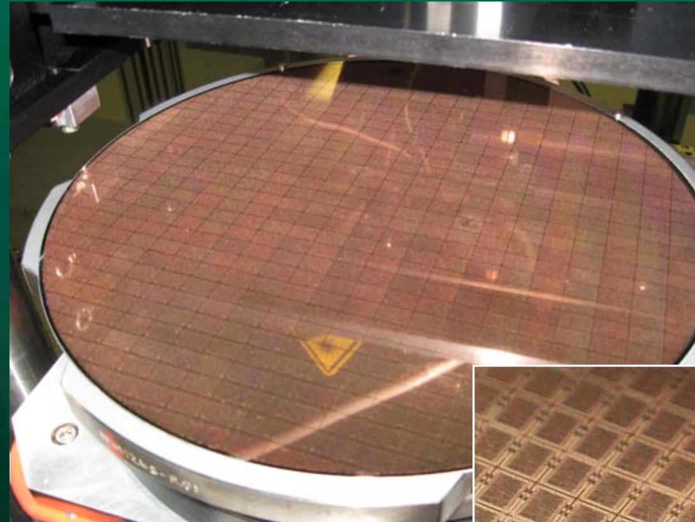
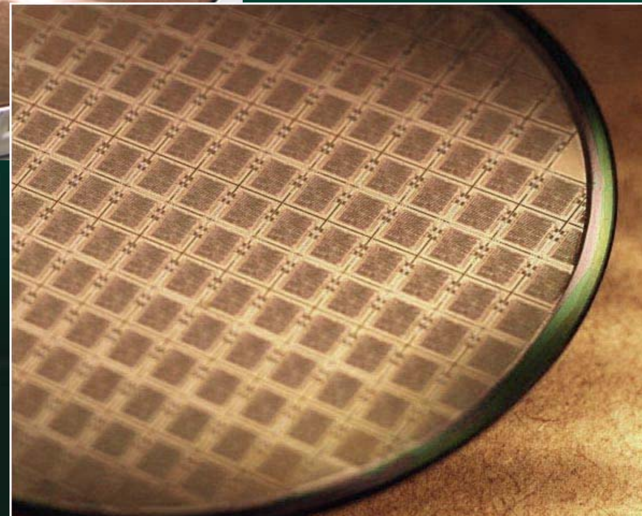
Pre-Probe Inspection
Probe Card Protection





Introduction

- Offering an inspection strategy to enable pre-screening of wafers prior to probing to avoid probe card damage .
- Focus is on MEMS-type of one touch down 300mm probe cards for the memory makers.
- Elimination of costly probe card damage.

Focus →Probe Card Type

- High density DUT probe cards
- One Touch Down probe card
- High parallelism probing
- Costly probes given > 50,000 contacts
- Pad pitches down to 60uM
- → MEMS type card

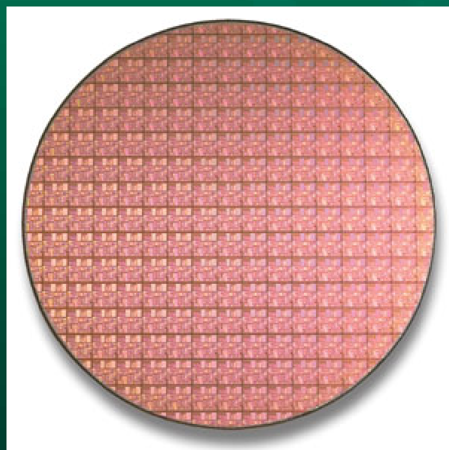
Objective

- Create an alternative inspection process for users of MEMS probe cards enabling process flow throughputs.
- 100% wafer screening while minimizing handling and time out of WIP.
- Mitigating the risk of damaging expensive probe cards caused by interaction with large debris on wafer.

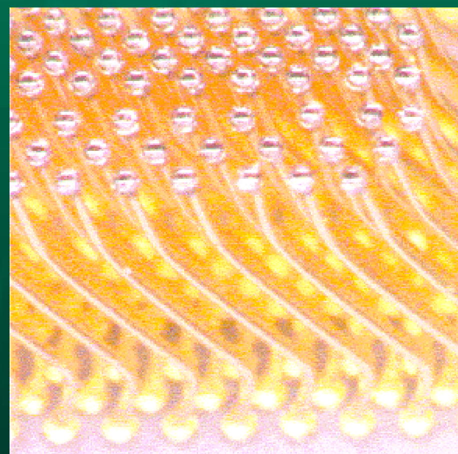
Customer's Challenge

- Memory manufacturing is a low margin high volume manufacturing endeavor.
- DRAM manufacturing is not profitable on wafer sizes smaller than 300mm.
- High throughput and yield are imperative for making profits in memory. One touch down probe cards are the choice for speed and CoO.
- They cannot afford to damage these cards in the testing process. Capital investment is high.

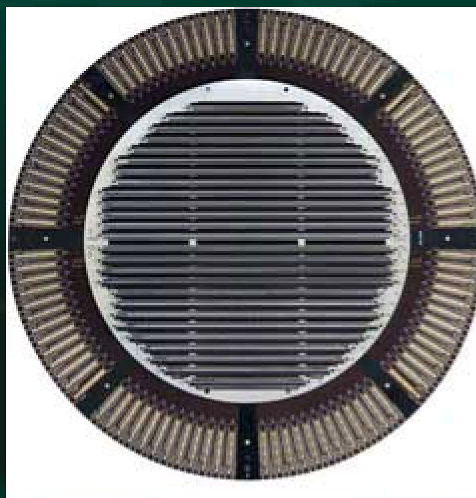
Associated Costs



WIP Loss

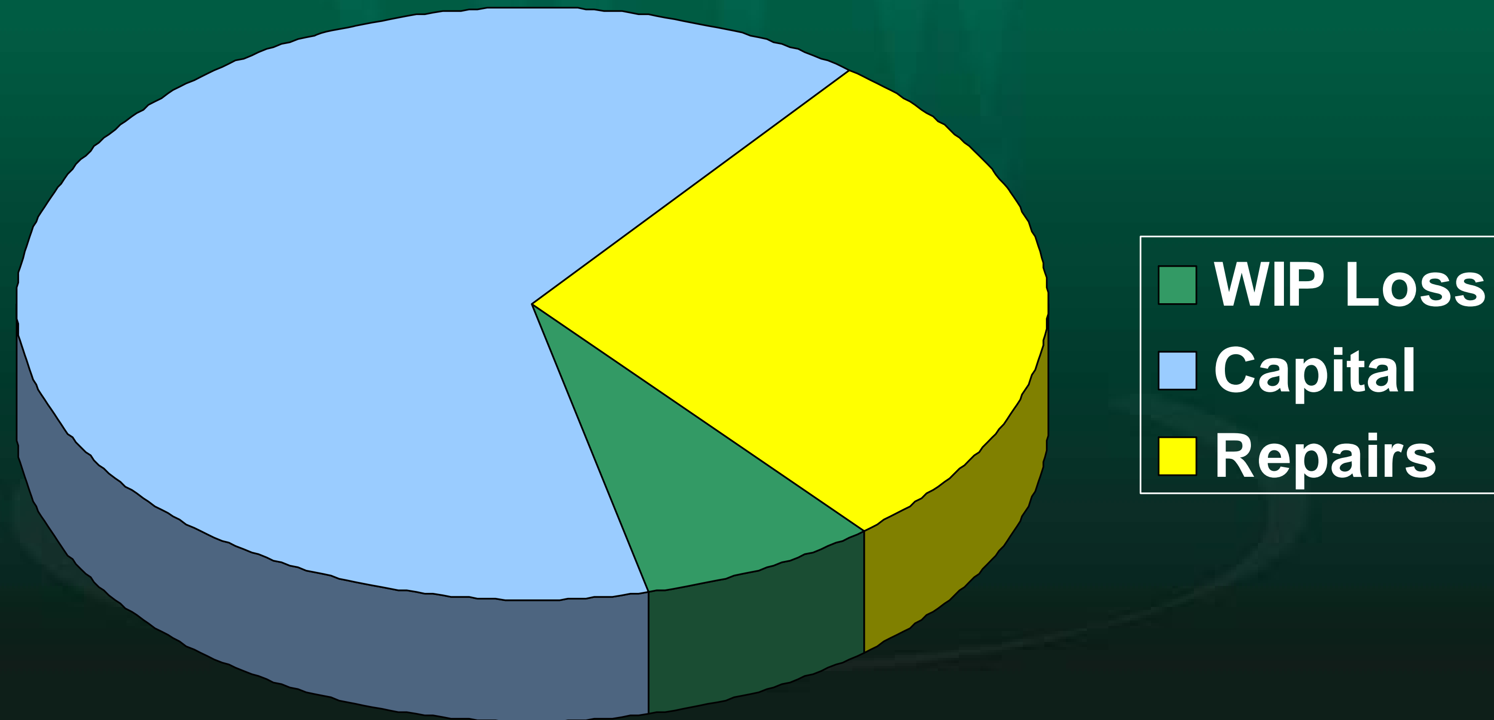


Repair



Capital

ROI Target → Capital Savings



Customer Data

2D Inspection Strategies

- **Die to golden image comparison.**
- **Relatively high speed.**
- **Catches only defects based on X-Y information. No Z information.**
- **Decision process:**
  - Reject if X-Y data shows large defect
  - If defect meets certain X-Y criteria, revisit with 3D inspection to verify defect (debris) is above height thresholds.

2D-3D Methodology

- **Straight down perspective on wafer.**
  - No Shadows; full view of defect
- **No moving parts on inspection head.**
  - High reliability
- **Simultaneous 2D and 3D measurements.**
- **High speed low resolution inspection for screening, row / column re-inspection for high resolution characterization of suspect debris.**

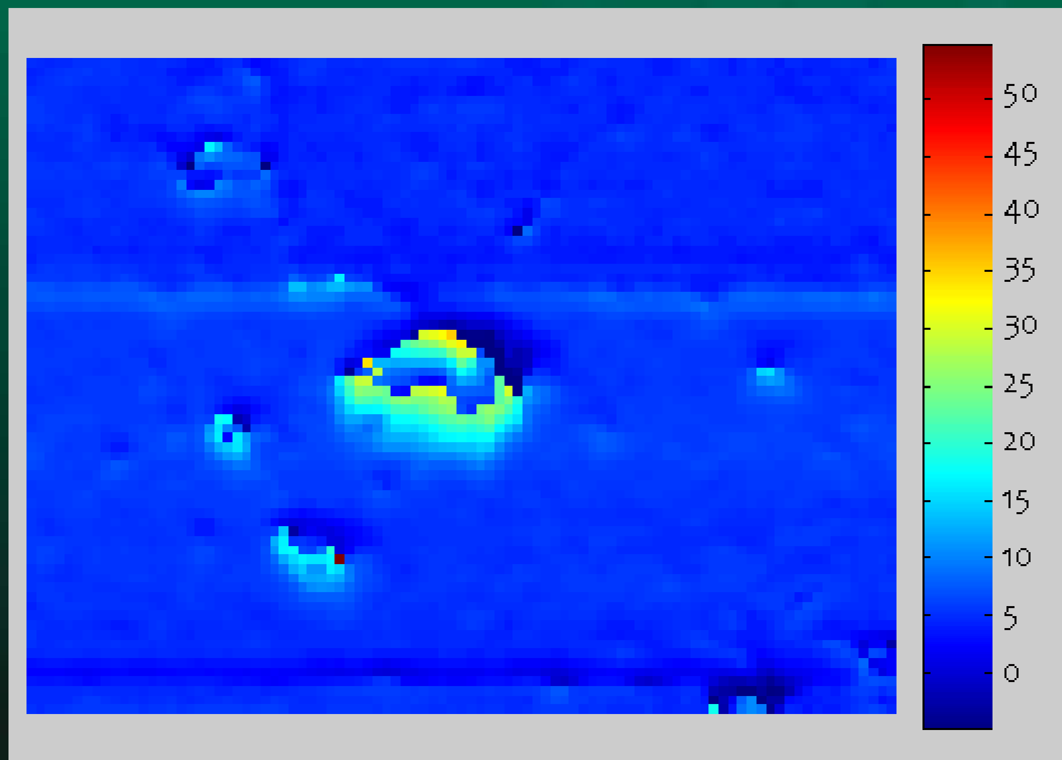
2D-3D Metrology Methodology

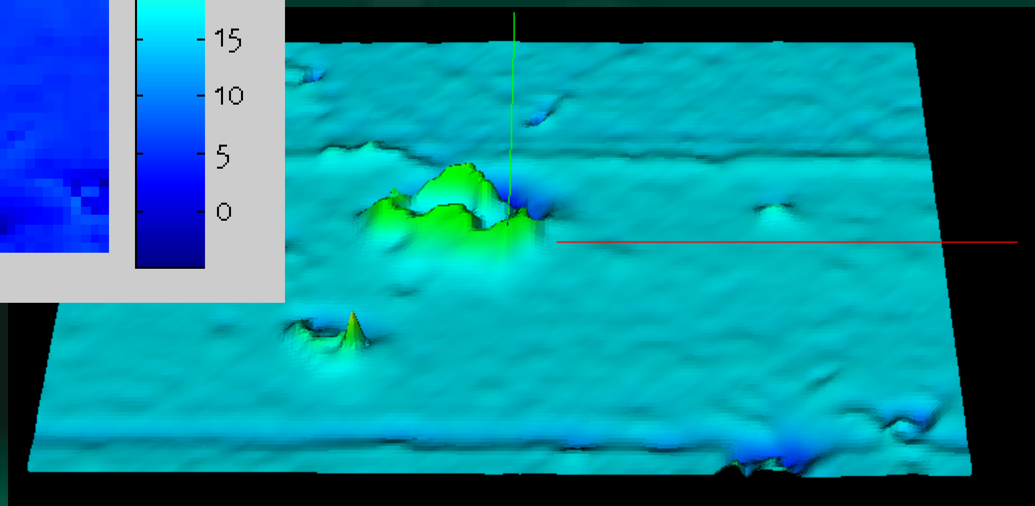
High Speed Low Res
Serpentine Pass

High Resolution
Repeat Pass

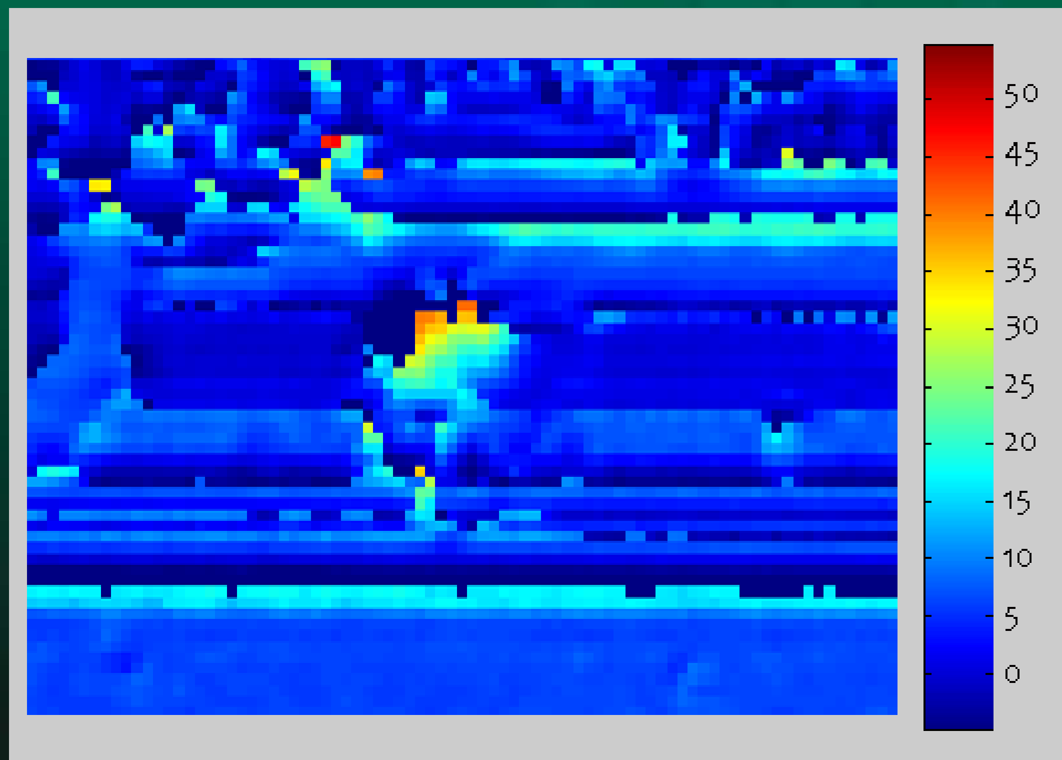
7uM x 7uM X-Y Pixel
Height Resolution – 150nm

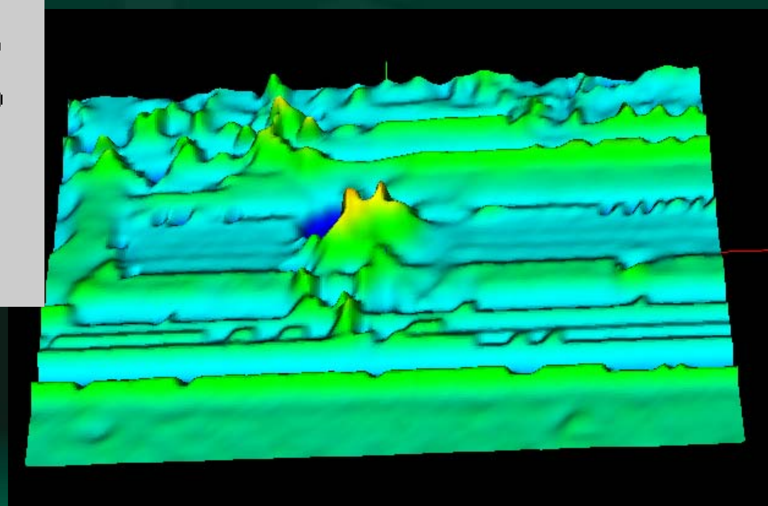
Inspection Metrology / Images





Inspection Metrology / Images





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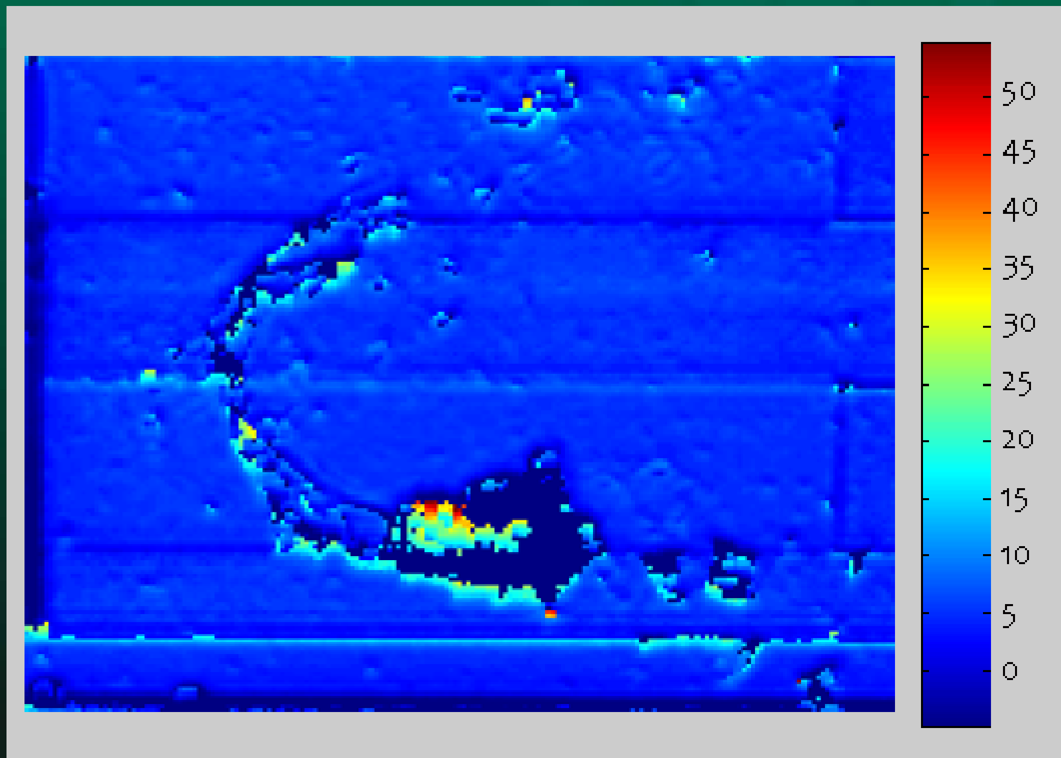
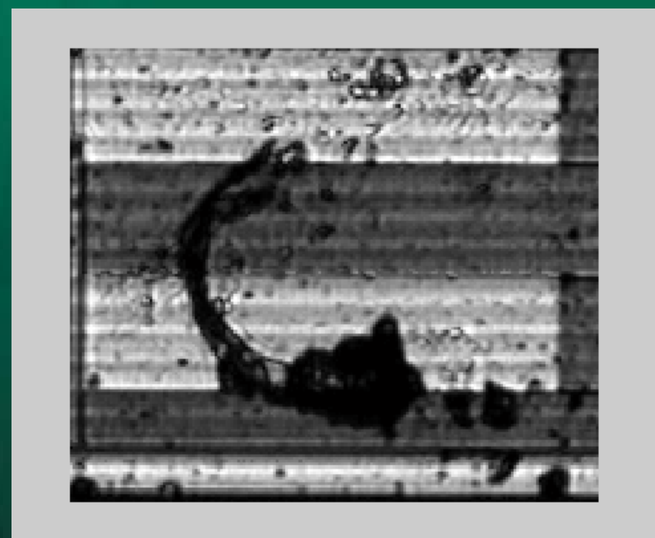
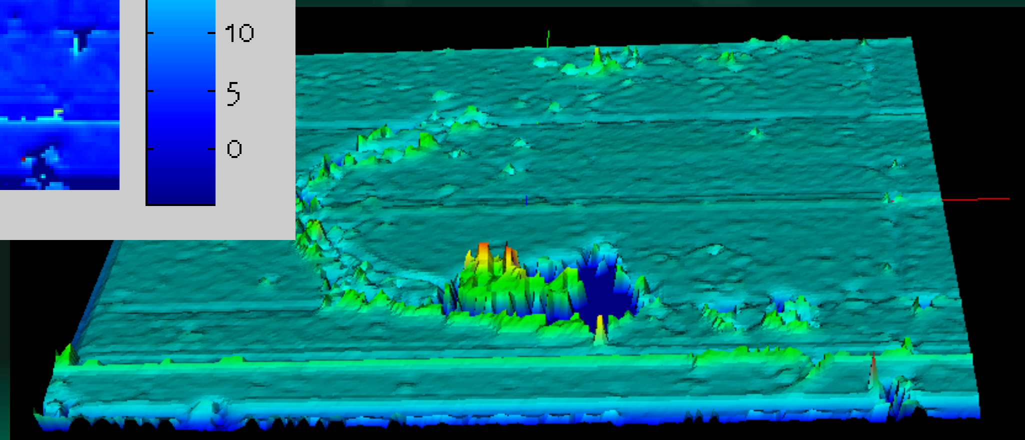
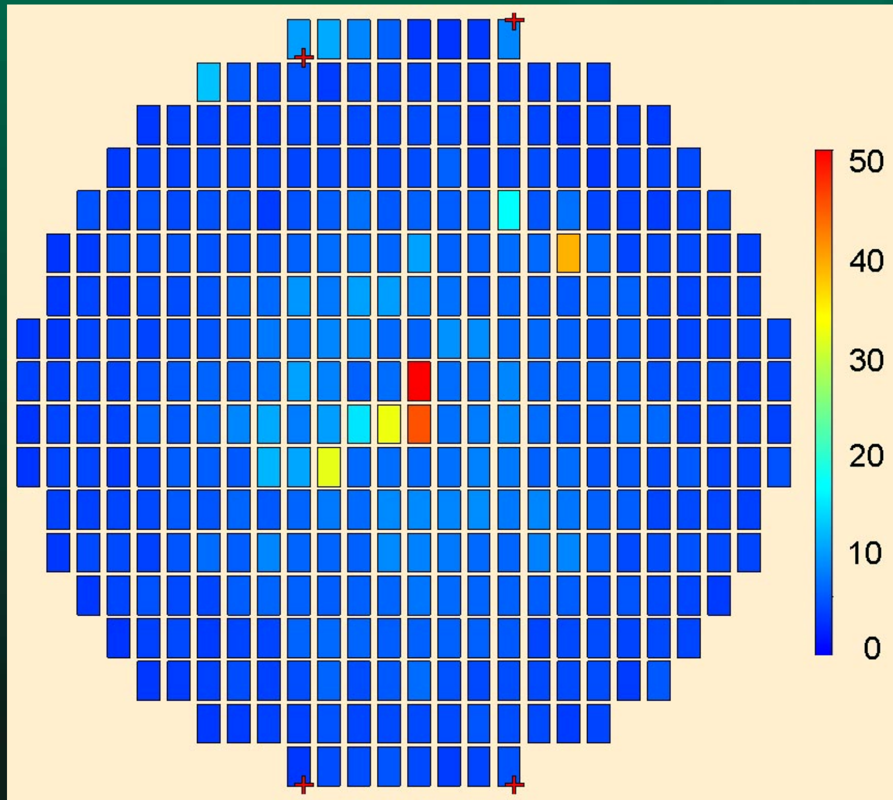


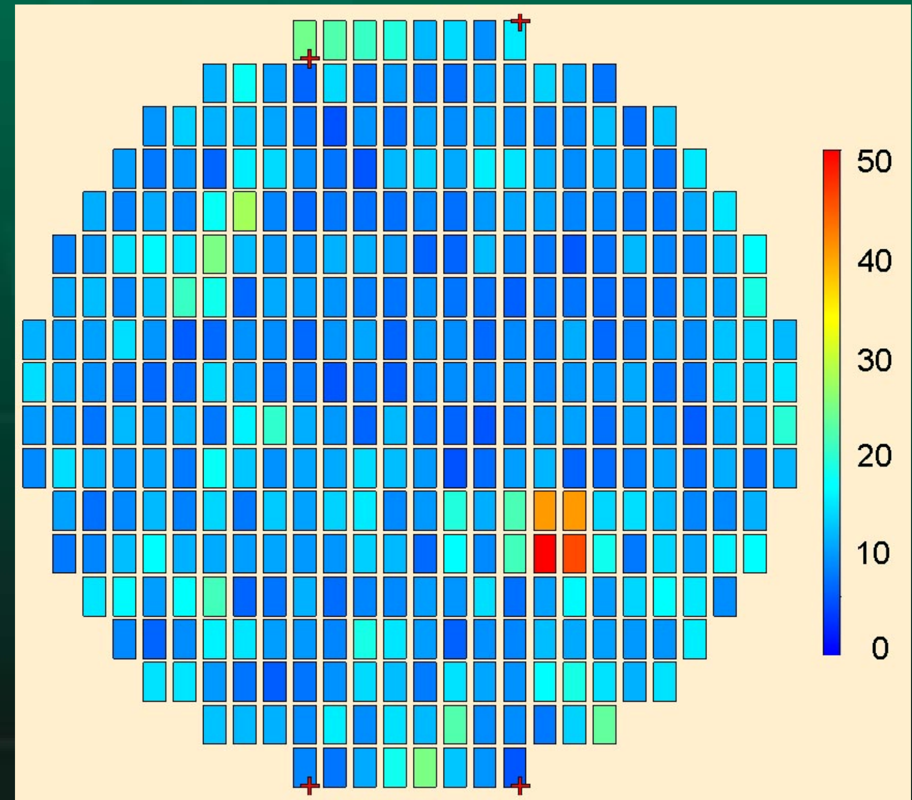




Inspection Metrology / Images

Particle Height Wafer Maps





300mm Memory Wafer Die Map showing Max Particle Heights (uM)

Strengths / Weaknesses

- **This is a solution to eliminate the risk of damaging probe cards which can be expensive.**
- **Capital outlay for this 2D-3D inspection solution is >$750k. ROI could vary in time significantly depending on fab methodology.**
- **Throughput for this application:**
  - 300mm wafers
  - 100% inspection with up to 20% high resolution 3D revisit
  - 100+ WPH
- **System would be configured for pre-probe inspection only. Other applications would require H/W changes and optional S/W.**

Thank You