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50um In-line Pitch Vertical Probe Card

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Agenda

- Introduction
- Scope
- Test Set-Up
- Test Method
- Evaluation Parameters
- Summary
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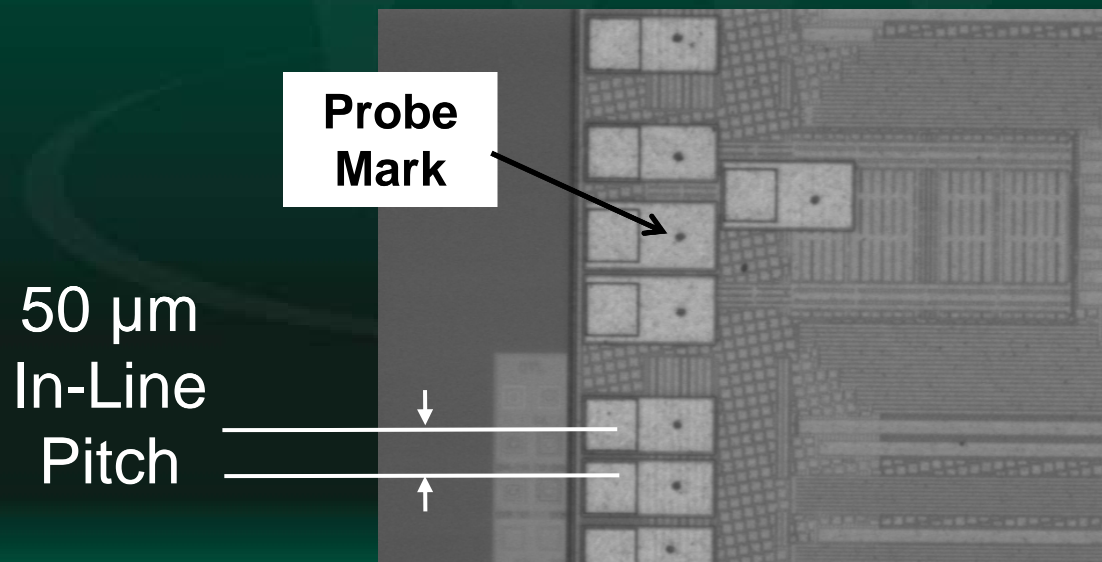
- Acknowledgements

Introduction

- TI fabricates devices with ever increasing test point densities at periphery and core, multi-site (x8…x64) tester capabilities and thermal requirements; thus driving the need for advanced probe card technologies.

- For example, TI devices such as embedded processors OMAP® have test pads spaced at 50 µm.

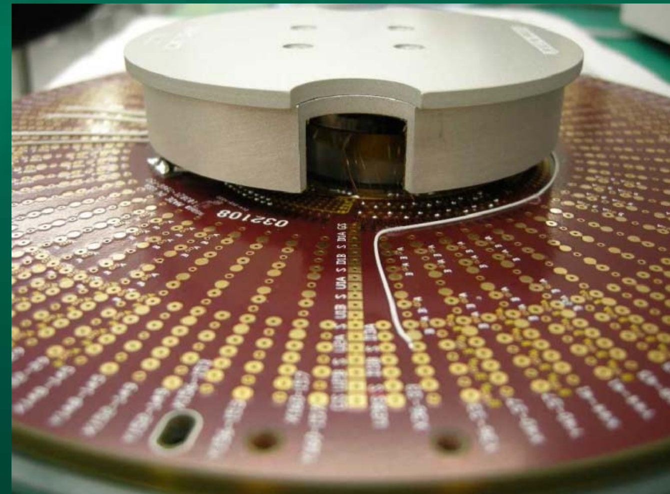


Scope

- TI Test Operations and Make Test performed a feasibility or "pathfinding" study of next generation vertical technologies manufactured by MJC.
- This evaluation was performed to understand if the current state-of the art technology (~70um) could be tasked to perform at the next density level (~50um).
- Moreover, the evaluation focused on thermal performance of this technology for the effect of both High (140°C) as well as cold temperature (-40°C).

Test Set-Up

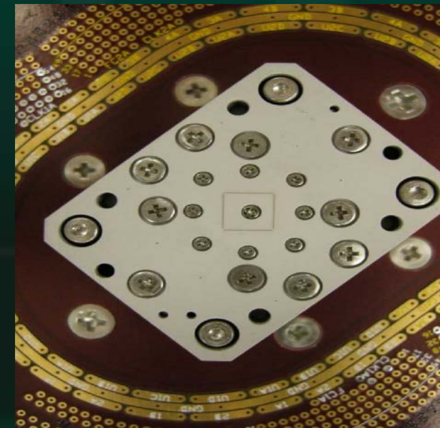
TI-VLCT X1 TESTER /
TSK UF3000



MJC VP50 WT Probe Card
(Tester Side)

Probe Card Characteristics:

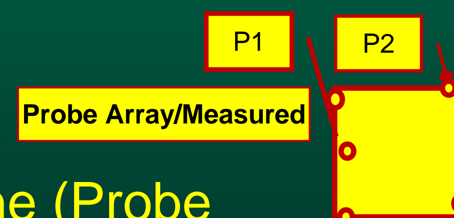
- VLCT Single Site 8” Probe card
- Needle Diameter : 25um (1mil)
- BCF : 2.8+/-1g (80um O/D)
- X Y position: +/-10um Planarity : <30um
- Total Pin counts : Single-Site 315
- Minimum pitch 50um (82 pins/315)



MJC VP50 Probe Head
(Wafer-Side)

Test Method

- A single site probe card was fabricated using MJC VP50 technology with Type 1 or hand-wired interconnect technology for a MCT 62 Test Chip Device.
- 5 of the 315 probes from this probe card were selected to be characterized.



- After initial device parameters of interest were characterized at TD = 0 condition, either off-line (Probe Card Analyzer) PCA or on device (tester/prober) the card was then cycled on an Al-wafer for 10 K TDs under power/current.
- After 10 K TDs, the card was again characterized or tested off-line (PCA) and on the device in its test cell.
- This testing and measurement process was repeated every 10 K TDs until 140 K TDs were reached.

Evaluation Parameters

- Lifetime (Wear Rate)
- Alignment (X,Y)
- Planarity (Z)
- CRes
- Leakage
- Yield
- Thermal Performance (-40/140C)
- Scrub Mark Area
- Stepping-Off Wafer

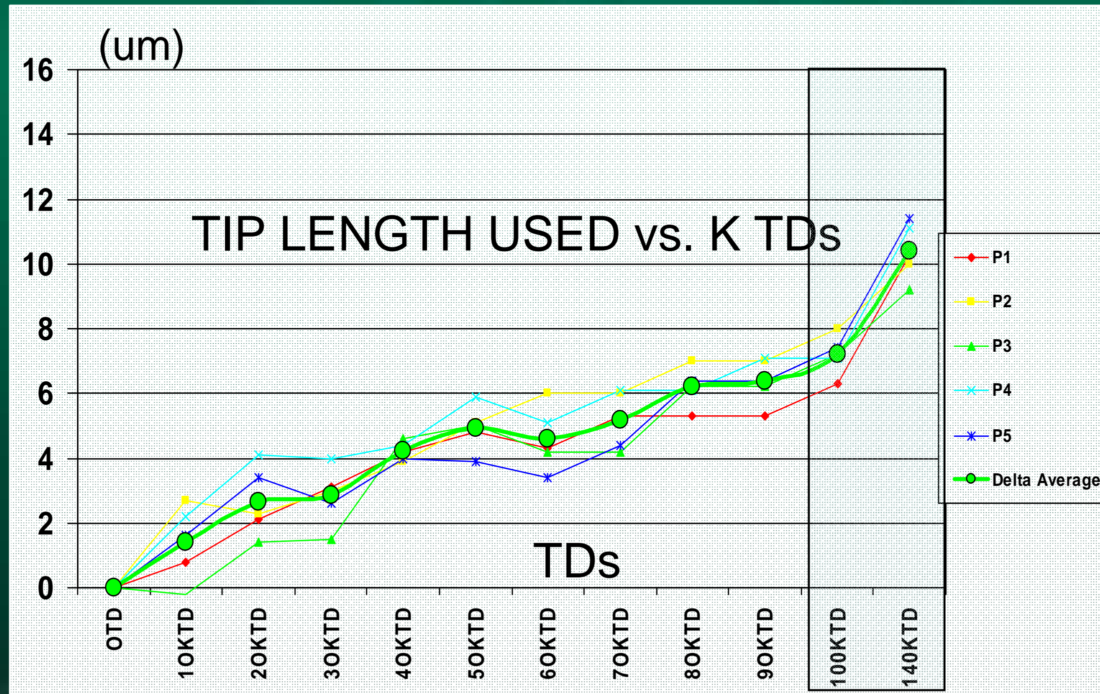
TIP LENGTH METROLOGY

Probe Tip

10K P1 LENGTH=208.6UM

Tip length metrology measurement system using a custom SerTek ® optical microscope with Z-focus vs. height (TPL) measured w/ automated capability.

WEAR RATE: 0 TD-140KTD at 140C

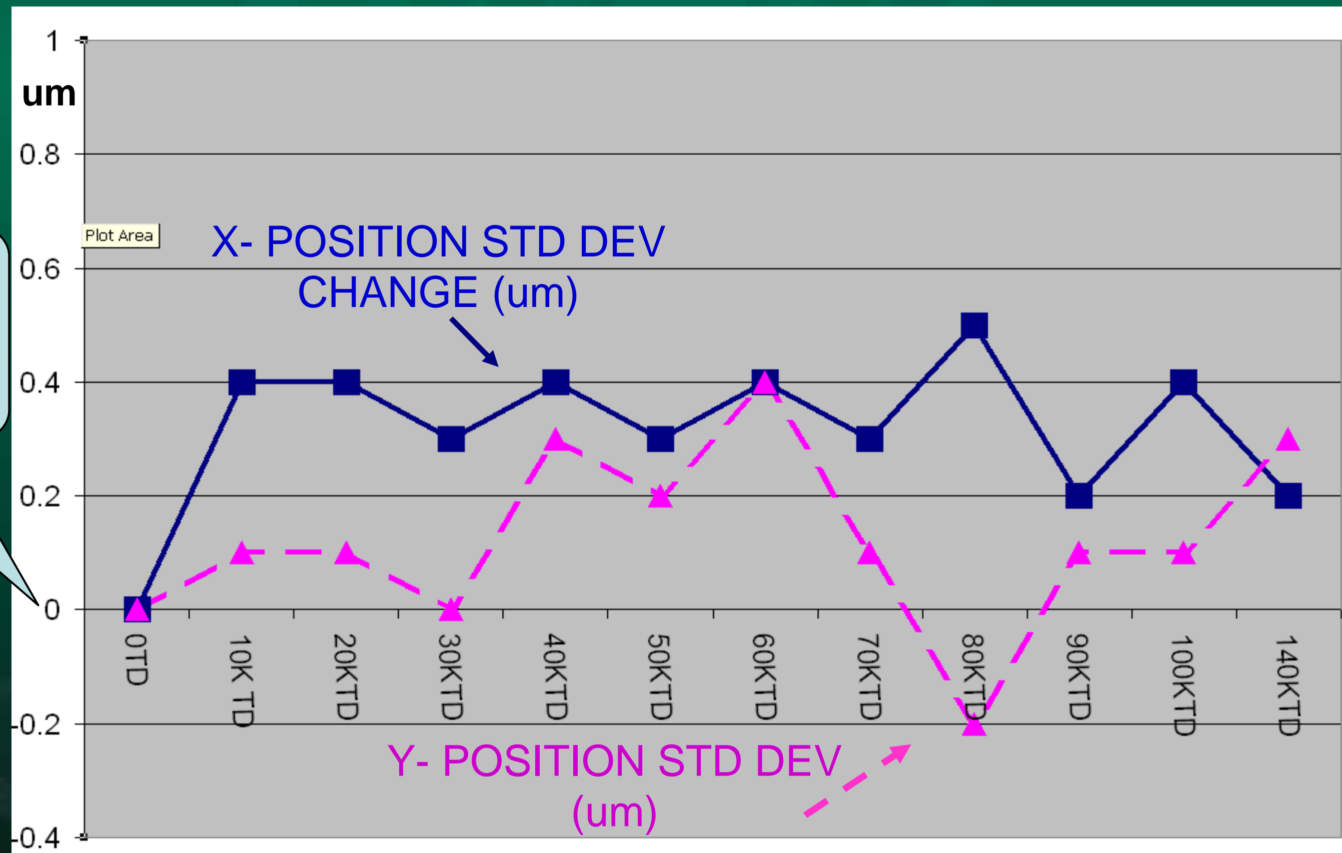


Graph above shows how much actual TIP LENGTH is consumed; measured at intervals of 10K TDs for a total of 140K TDs performed.

WEAR RATE about 0.0010725um /TD. With 120um of available tip length, this projects to a lifetime of about 1.725M TDs.

PROBE ALIGNMENT CAPABILITY

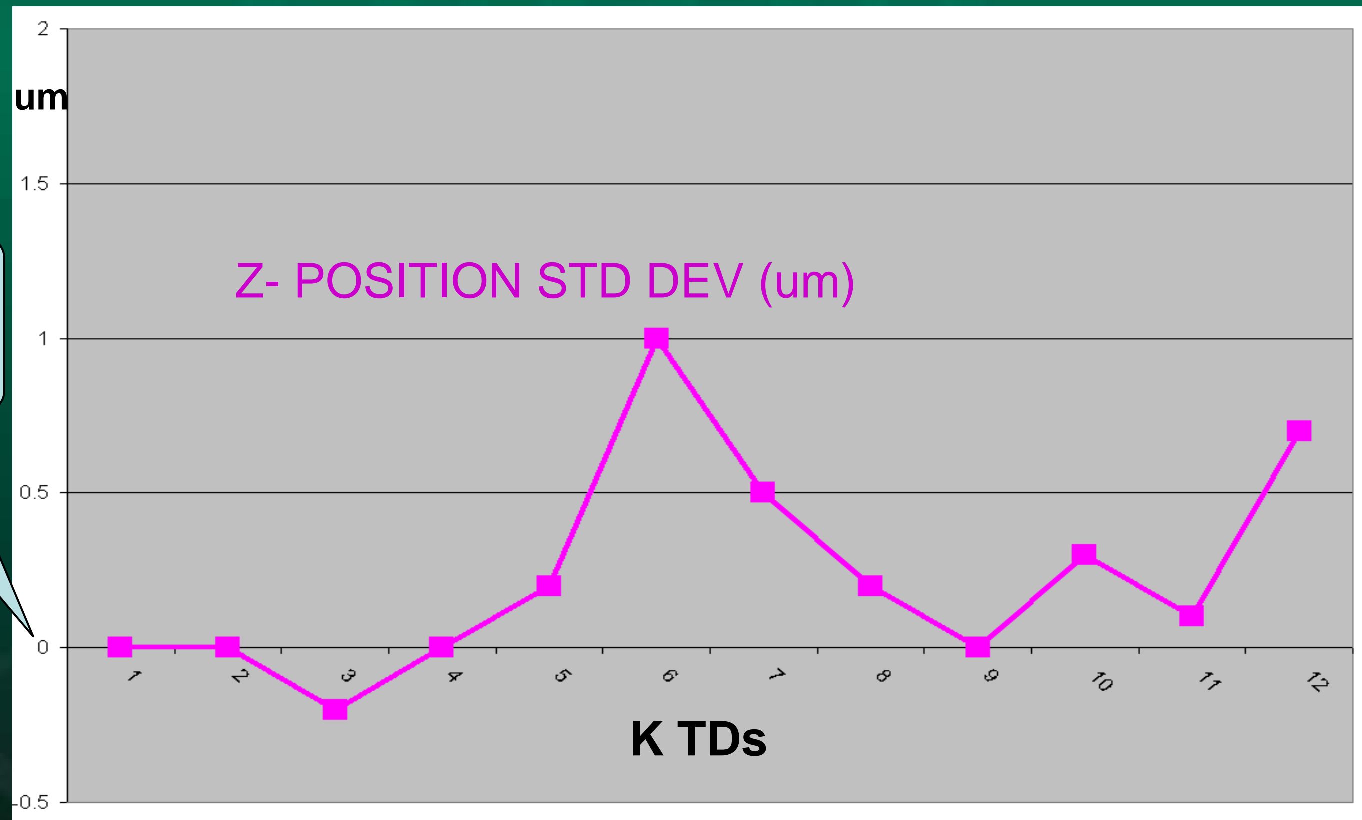
Zero equals 3.3 um from 0TD start for STD DEV



Graph above shows the probe X and Y positional consistency or STD DEV to be < 0.6 um measured with respect to position at 0 K TDs during probing up to 140 K TDs at 140C.

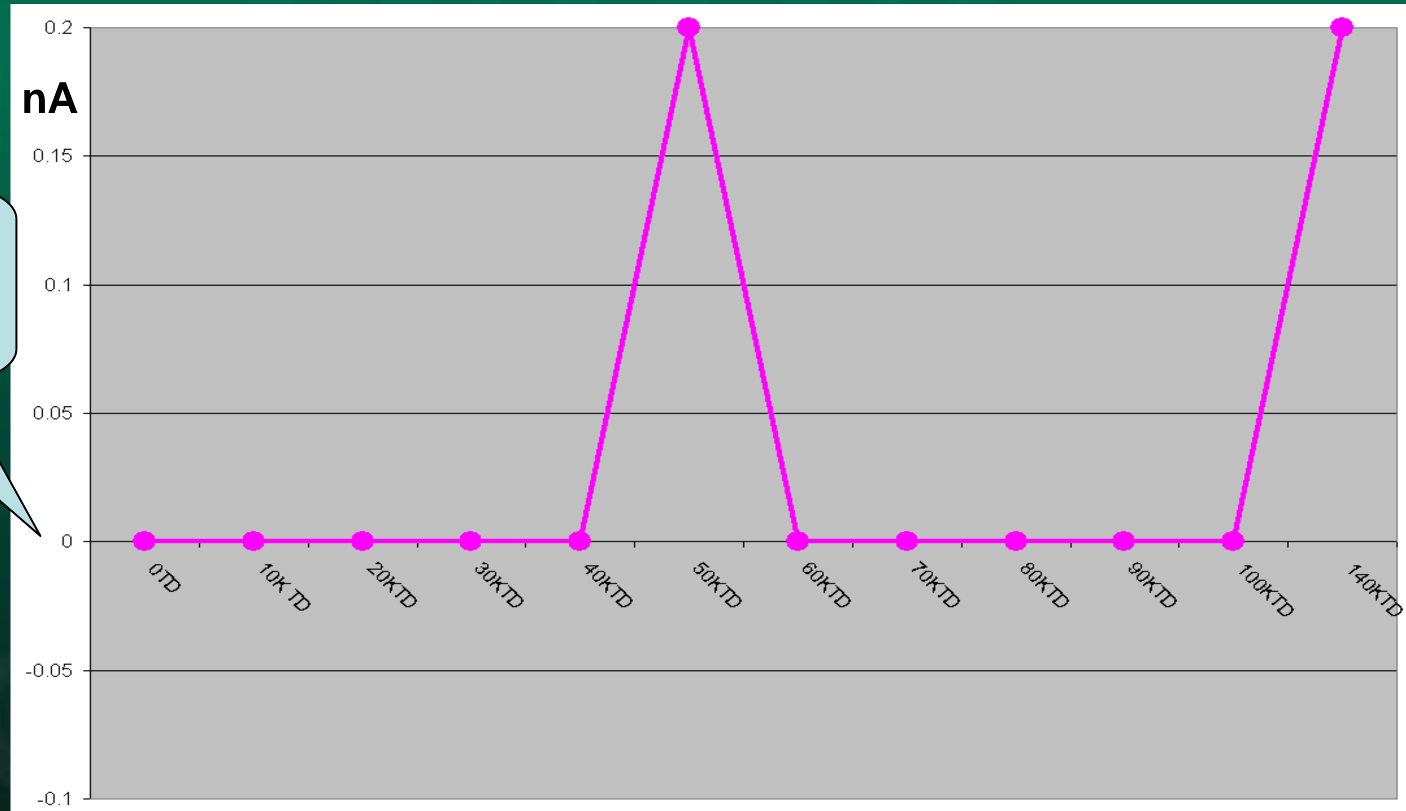
PROBE PLANARITY CAPABILITY

Zero = 12.6 um from 0TD start for STD DEV



Graph above shows the probe Z or planarity consistency or STD DEV to be < 1.0 um measured with respect to Z position at 0 K TDs during probing up to 140 K TDs at 140C.

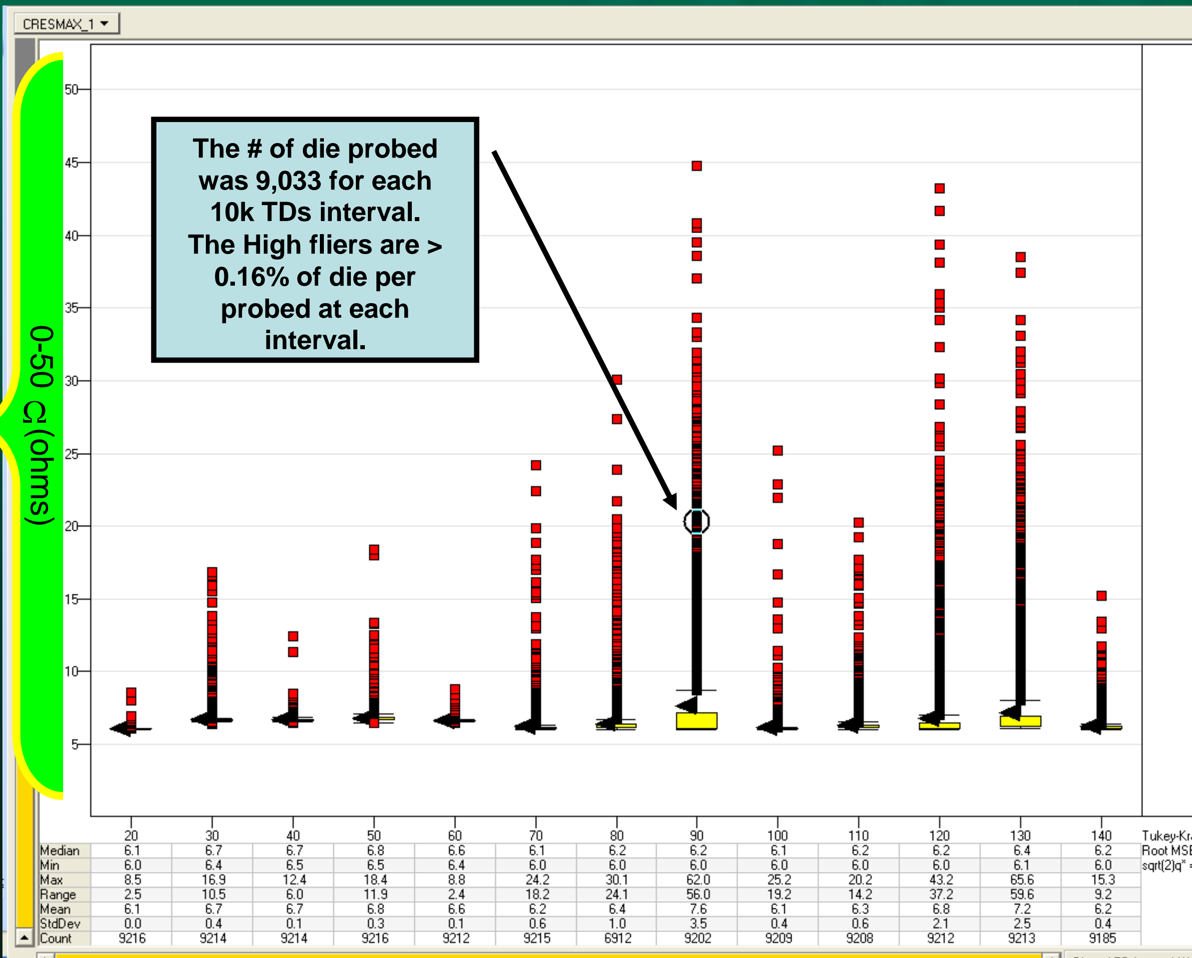
PROBE LEAKAGE



Zero = 0.5 nA from 0TD start for STD DEV

Graph above shows the probe card leakage consistency or STD DEV to be no more than 0.2 nA as measured with respect to leakage observed at 0 K TDs during probing up to 140 K TDs at 140C.

VLCT TESTER CRes (140 C)

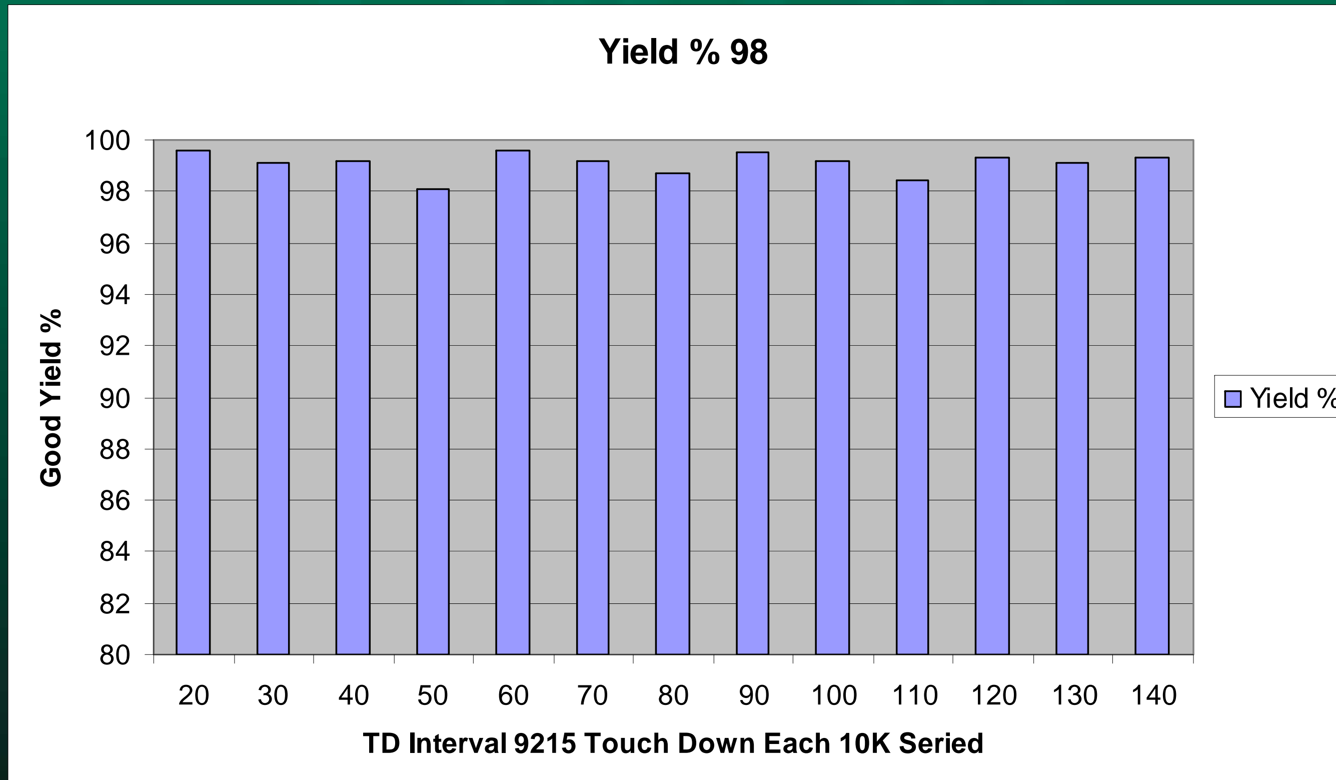


	20	30	40	50	60	70	80	90	100	110	120	130	140
Median	6.1	6.7	6.7	6.8	6.6	6.1	6.2	6.2	6.1	6.2	6.2	6.4	6.2
Min	6.0	6.4	6.5	6.5	6.4	6.0	6.0	6.0	6.0	6.0	6.0	6.1	6.0
Max	8.5	16.9	12.4	18.4	8.8	24.2	30.1	62.0	25.2	20.2	43.2	65.6	15.3
Range	2.5	10.5	6.0	11.9	2.4	18.2	24.1	56.0	19.2	14.2	37.2	59.6	9.2
Mean	6.1	6.7	6.7	6.8	6.6	6.2	6.4	7.6	6.1	6.3	6.8	7.2	6.2
StdDev	0.0	0.4	0.1	0.3	0.1	0.6	1.0	3.5	0.4	0.6	2.1	2.5	0.4
Count	9216	9214	9214	9216	9212	9215	6912	9202	9209	9208	9212	9213	9185

Test Program Max Cres Limit 40Ω before failure

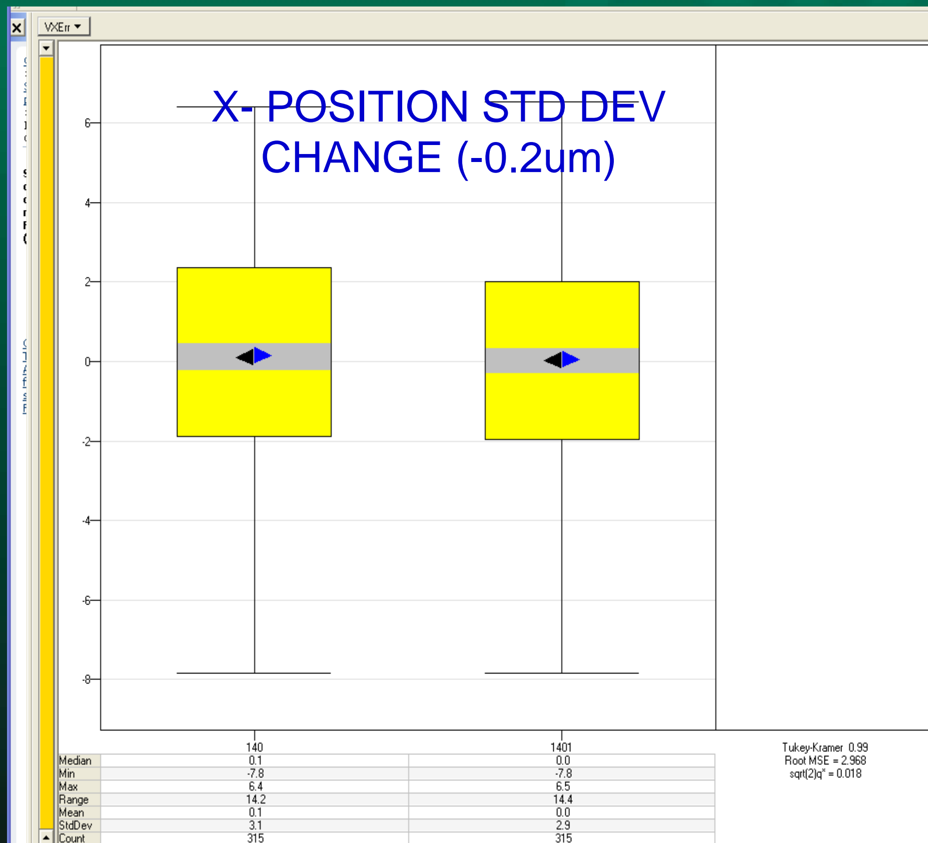
TDs (1000)	CRes STD (Ω)
0	0
20	0
30	0.4
40	0.1
50	0.3
60	0.1
70	0.6
80	1.0
90	3.5
100	0.4
110	0.6
120	2.1
130	2.5
140	0.4

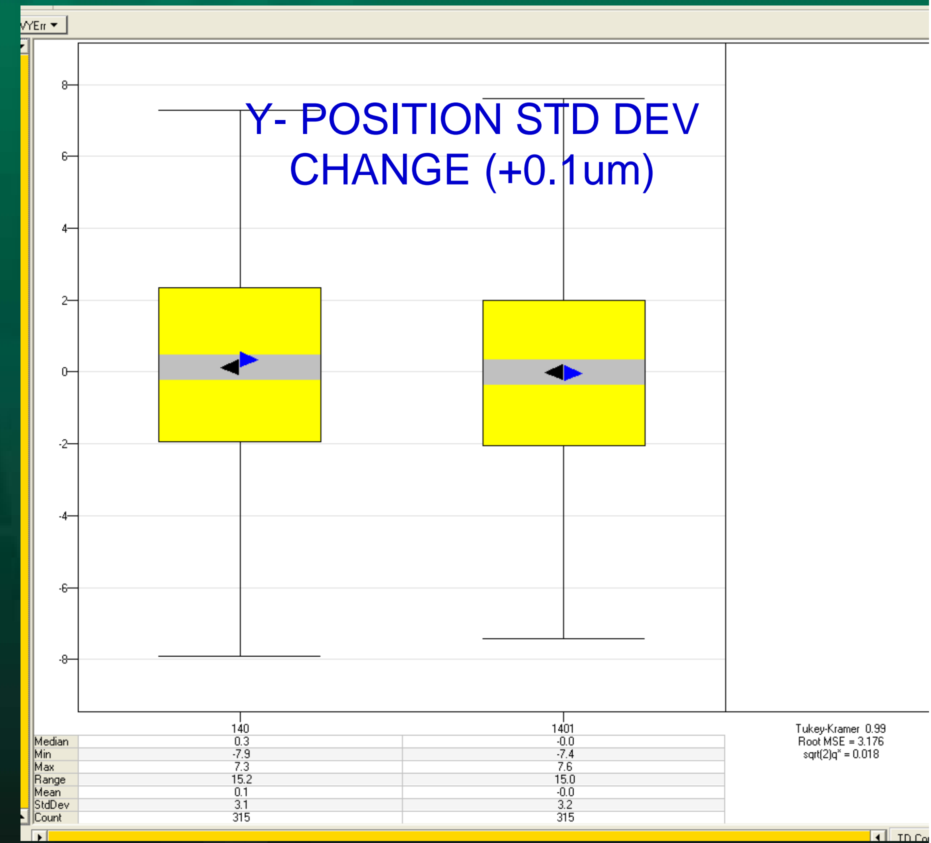
Yield Data in Production Runs (140C)



Graph above shows the wafer test YIELD consistently > 98%.

Cold Temp Probe -40C API X/YE Err

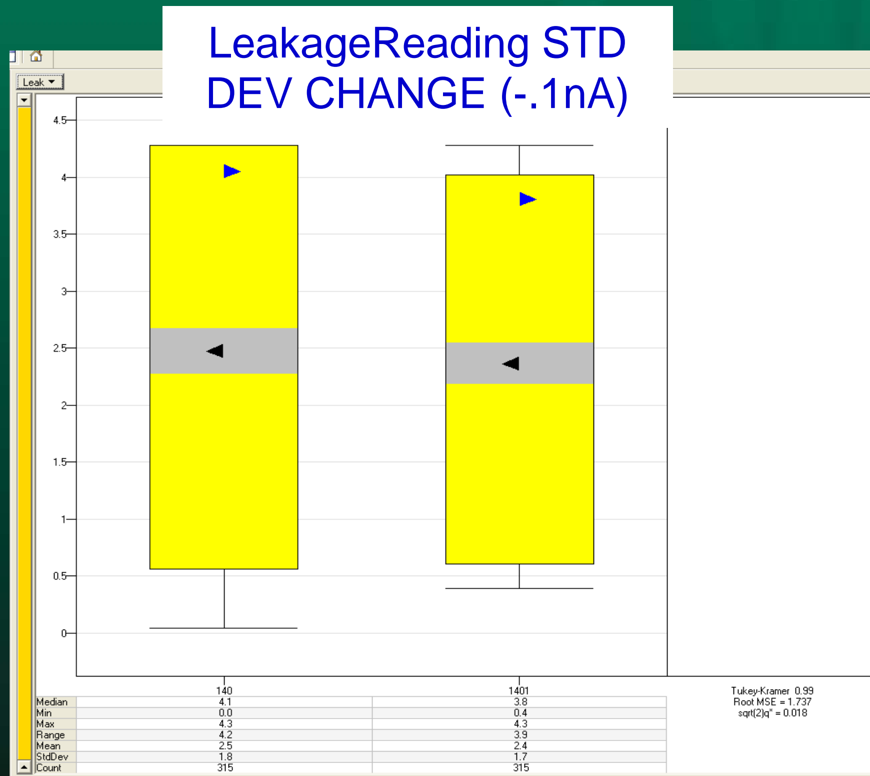


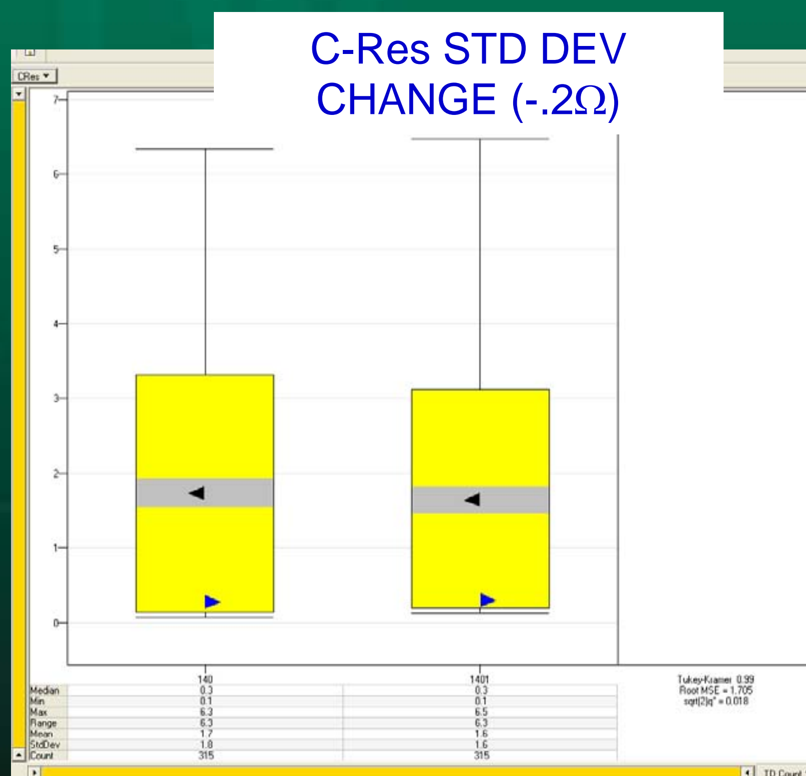


Graph above shows last 140K API run at 140C to API run after -40C wafer run! XErr API VX3

Graph above shows last 140K API run at 140C to API run after -40C wafer run! YErr API VX3

Cold Temp Probe -40C API Cres and Leakage at OT

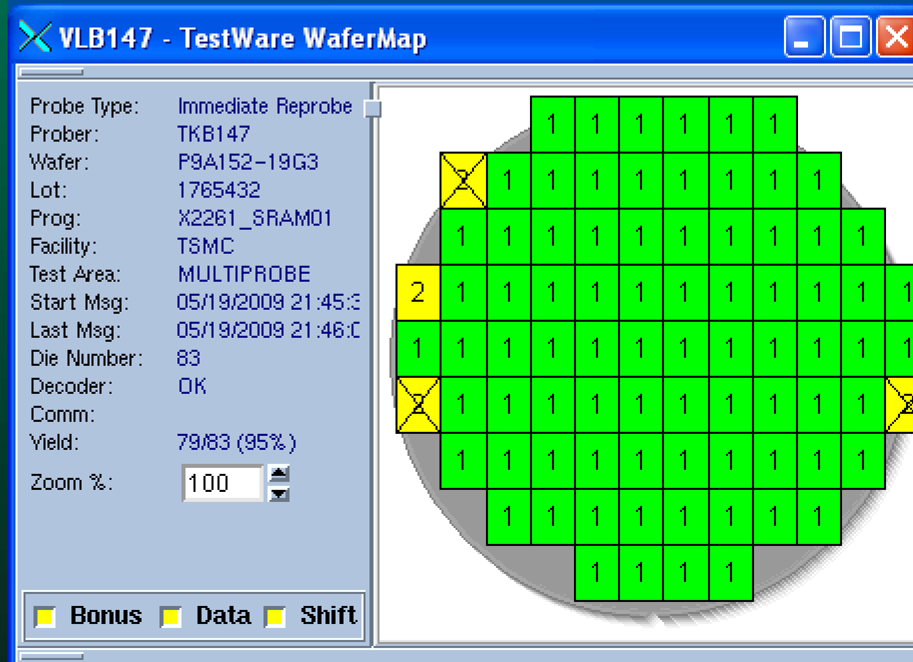




Graph above shows last 140K API run at 140C to API run after -40C wafer run! Leakage API VX3

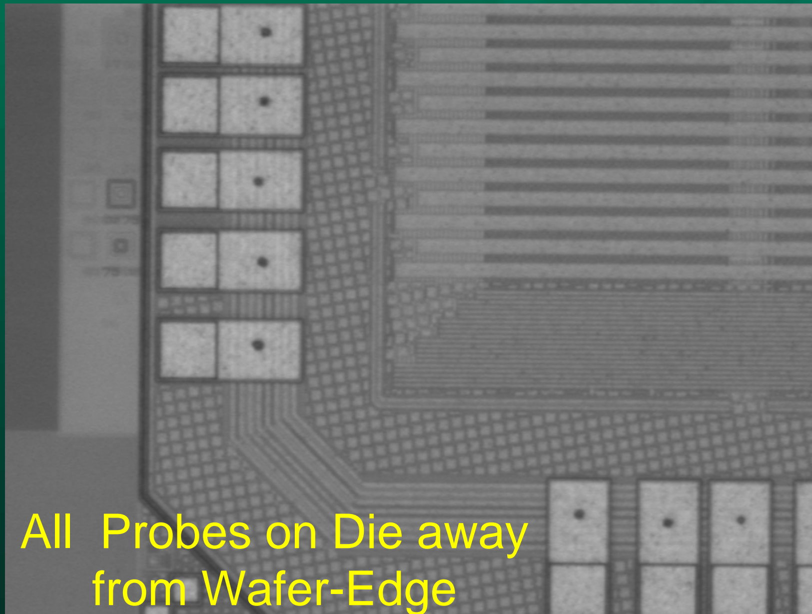
Graph above shows last 140K API run at 140C to API run after -40C wafer run! Cres API VX3

Cold Temp Probe -40C Test Data



For Cold Temp wafer yield above the 96% mark. One open Bin during probe! During debug showed icing on the wafer causing a false open fail.

Stepping-Off Wafer Capability



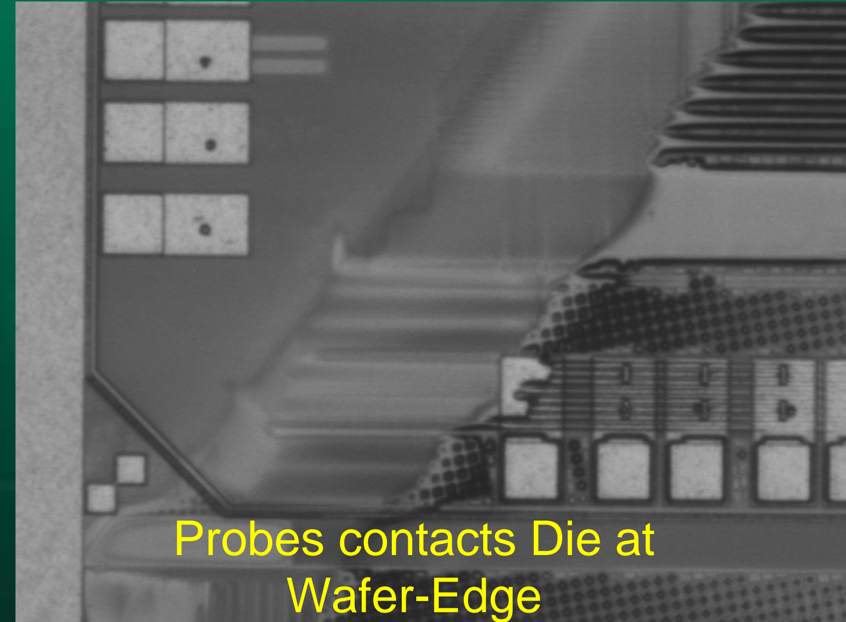


Figure shows the relatively very small probe marks < 80um^2 and that the probes can "step-off" the wafer without affecting the position of adjacent probes, i.e., minimal "mechanical crosstalk"

SUMMARY

WEAR RATE: ~ 0.0010725um /TD or~ 1.725M TDs / PC.

ALIGNMENT: X and Y positional drift < 0.6 um Std Dev

PLANARITY: Probe Z ht . Std Dev to be < 1.0 um

LEAKAGE: Probe card leakage no more than 0.2 nA

YIELD: Wafer yield consistently observed > 98%

CRES: Contact resistance Std Dev < 0.6 ohms

THERMAL: Capability demonstrated at HT and CT

PROBE MARKS: Al pad scrub mark areas < 80 um^2.

STEP-OFF: Capability of stepping-off wafer demonstrated.

NEXT STEPS

MJC VP50 probe card technology demonstrated capability and feasibility for next generation "fine-pitch" wafer level applications.

To be recommended for the next phase of advanced vertical probe card INTEGRATION or technology and production qualification on actual devices.

Acknowledgements

John Hite

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END