IEEE Semiconductor Wafer Test Workshop

June 7 to 10, 2009 in San Diego, CA

Submitted by Jerry Broz, Ph.D., General Chair of SW Test Workshop.

The 19th Annual IEEE Semiconductor Wafer Test Workshop (SW Test) was successfully held at the Paradise Point Resort in San Diego, CA, from June 7 to 10, 2009. This yearly workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. The SW Test 2009 agenda consisted of a technical program, supplier exhibits (which **ARE NOT** open during the technical sessions), and a Casino Royale Social Event as well as plenty of time for informal interaction and networking with colleagues. The total conference and EXPO attendance was 175 with approximately 15% international attendees representing a total of 12 countries. Unfortunately, due to the H1N1 pandemic alert level, many of the usual international attendees were restricted from travelling to the United States.

The workshop began with a Sunday afternoon tutorial session organized by Technical Program Chair Brett Crump in conjunction with Darren James and Jeff Greenberg of Rudolph Technologies. This excellent three part tutorial provided new and experienced technologists key insights into many of the metrology problems facing the wafer test industry. Topics included an introduction into applied metrology concepts; a series of case studies focused on metrology tool capability assessments; and wrapped up with a practical discussion on the metrology approaches used to fix wafer sort floor problems.

After the welcome reception, Jerry Broz, Ph.D., SW Test General Chair, gave a short, "Probe Year In Review" presentation which set the stage for the Keynote Presentation, entitled, "Test Economics Driving Test Technology", made by Risto Puhakka, President of VLSI Research, Inc.

Mr. Puhakka discussed the key metrics tracked by VLSI which showed that the overall semiconductor industry was relatively healthy as the global recession began. Interestingly, these metrics demonstrated that half of the global chip recession was caused by overspending within the Taiwan memory sector. VLSI's global chip making climate trend index showed that the semiconductor industry has started slowly moving out of the "deep freeze". The data provided also showed that the general semiconductor business and capacity utilization rates are basically returning to normal but at an overall lower operating level.

The probe card market experienced a reduction in revenue of approximately 30% from 2008; with the most dramatic changes occurring in the advanced probe card technologies primarily used for memory test. FormFactor, Micronics Japan (MJC), and Japan Electronic Materials (JEM), respectively, remained as the top three probe card suppliers world-wide; however, the rest of the top ten saw a major reshuffle. Mr. Puhakka stated that VLSI has already seen that the back-end consumables and materials are bouncing back and expects the probe card and socket businesses to recover sooner than ATE. ATE is forecasted to remain less than half of total test hardware spending. Overall, VLSI's outlook for the semiconductor industry was very positive for the rest of 2009 and into 2010. Risto's keynote presentation will be available on the SW Test website (http://www.swtest.org) in July; in the meantime, it can be downloaded from the weSRCH.com website at http://electronics.wesrch.com/pdfEL1SE1ZTZAAXK.

The 2009 SW Test technical program began on Monday morning with the Welcome session by Dr. Jerry Broz. Dr. Broz gave a positive update on Bill Mann, Chair Emeritus, who is battling

cancer and recognized the passing of long time SW Test contributor and Steering Committee member, Frank Pietzschmann (Qimonda-Dresden). Dr. Jerry Broz, Ph.D., was selected as a recipient for the IEEE Computer Society's Golden Core award, given for long-standing service to the society. Each year the IEEE Awards Committee selects up to a maximum of 50 recipients out of the more than 100,000 current IEEE Computer Society members and permanently includes the names in the Golden Core Member master list. The Golden Core is the highest level of membership designation in the IEEE Computer Society.

The next two and a half days were filled with a wide variety of technical presentations covering every facet of the wafer test process from *Large Area Array Probing Challenges* to *Damage Control and Low Force Probing*. Some individual highlights from the technical program included Michael Huebner, Ph.D., (FormFactor) and Scott Lindsey, Ph.D. (Aehr Test), discussing the future of increased pin counts and two different full wafer probing methods. The importance of consistent and accurate data tracking methods in the sort environment was detailed by Mark Winn (Intel) and Rob Marcelis (Salland Engineering). Jan Martens (NXP-Hamburg) discussed contact mechanisms behind copper metallurgy effects for sort process and cleaning performance. The technical hurdles experienced during an RF-probe card and ATE hardware qualification were discussed by Mike Slessor, Ph.D., (MicroProbe); Mark Roos (Roos Instruments) with Roger Hayward (Cascade Microtech); and Daniel Watson (Teradyne). Several other presentations, such as those by James Tong (Texas Instruments) and Gordon Vinther (Ardent Concepts) reviewed the use of standardized methodologies within the development environment and transitioning to a production test floor. Overall, the technical program had 29 podium presentations with 65% from suppliers, 15% from semiconductor manufacturers, and 20% collaborative presentations from both manufacturers and suppliers.

Best Presentation was awarded to the collaborative team of Yuan Huang, Gary Liu, Thompson Hsu (United Microelectronics Corp.) and Wensen Hung, Cahris Lin, Dean Yang (MPI–Taiwan) for their comprehensive work on vertical cobra probing on low-k wafers; ***Best Data Presented*** went to the technical team of Wolfgang Schaefer, Ph.D. and Gunther Boehm (Feinmetall GmbH) that discussed various aspects of high temperature probing; ***Best Presentation, Tutorial in Nature***, went to Gert Hohenwarter (GateWave Northern) for his overview on key issues for power delivery verification; the ***Most Inspirational Presentation*** was awarded to Jason Mroczkowski and Ryan Satrom (Everett Charles Technologies) for their detailed work on wafer level test hardware using a signal integrity simulation; and although there were many eligible candidates for the infamous "***Golden Wheelbarrow Full of Crap for the Poorest Disguised Sales Pitch***" this award was not inflicted. All the presentations (including the tutorials, keynote, technical program, and posters) from 2009 as well as previous workshops (1993 to 2009), are available on the newly redesigned SW Test website (http://www.swtest.org).

Technology EXPO 2009 had a total of 31 industry exhibitors and five Corporate Supporters (Advanced Probing Systems, BucklingBeam Solutions, Electro-Scientific Instruments, International Test Solutions, and JEM). During the EXPO, all aspects of the wafer sort industry and associated infrastructure suppliers were represented with twelve probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo pin suppliers, and a variety of other probe related service providers.

The 20th Annual SW Test Workshop and EXPO will be held June 6 to 9, 2010, at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for podium and poster presentations will be open starting January 1, 2010.

Images from IEEE SW Test 2009 …

Technical Program	
	

Technology EXPO