IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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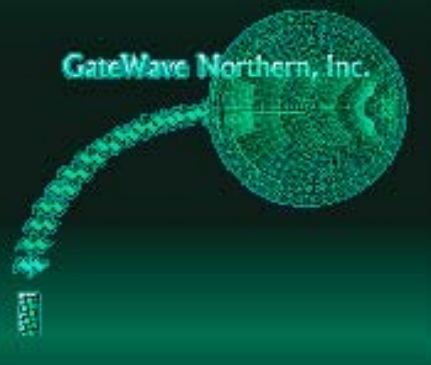
Hidden Performance Limiters in the Signal Path



June 6 to 9, 2010

San Diego, CA USA

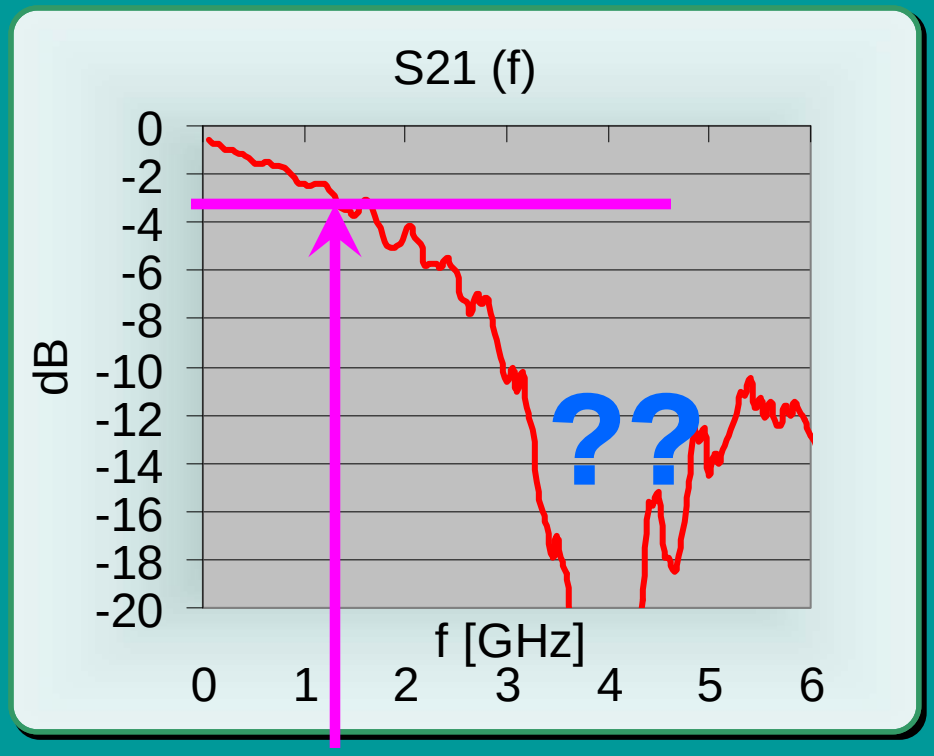
Objective

Identify potential sources for hidden contributions
- parallel lines on PCBs
- wiring harnesses
- interposers
- short coupled sections of multiple transmission lines
- unused, unterminated or improperly terminated transmission lines

Examine impact of examples for these contributors
- Coupled lines
- Interposer
- Faulty contacts
- Power delivery system design and components

Provide guidance for detection and remedy of problems

Problem:



Target value: -3dB at 2 GHz

But - 4 GHz fres. Who cares?

Potential problem areas

- Coupling
  - Adjacent signal lines
  - Adjacent power lines
  - Adjacent sense lines
- Mismatch
  - Unterminated/lightly terminated DUT
  - Unterminated tester (power/sense)
- Resonances
  - Interposer pin assignments
  - Ceramic/DUT arrays
  - PCB
- PDS connections and component locations

- Discontinuities

-Vias

-non-50 Ohm sections

- interposer

- PCB loss

- DUT input

- contacts

Problem manifestations

- Resonances
  - Reduced bandwidth / operating speed
  - Reduced switching margins
- Crosstalk
  - Increased noise levels
  - Reduced switching margins
- PDS ‘weakness’
  - Reduced operating speed
  - Reduced switching margins

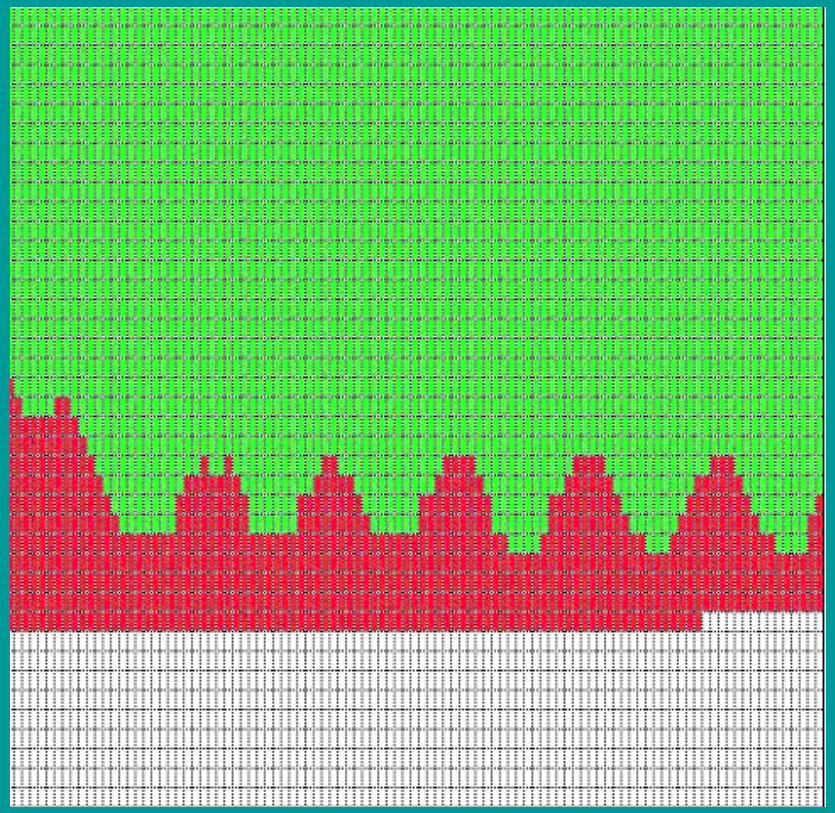
Consequences range from none to reduced test yield and complete probe card failure

-> loss of a sale -> loss of customer

Example problem 1:

Wikipedia:

....a **shmoo plot** is a graphical display of the response of a component or system varying over a range of conditions and inputs.



Measured shmoo plot reveals periodic structure in the yield (red=fail, green=pass) as a function of one parameter

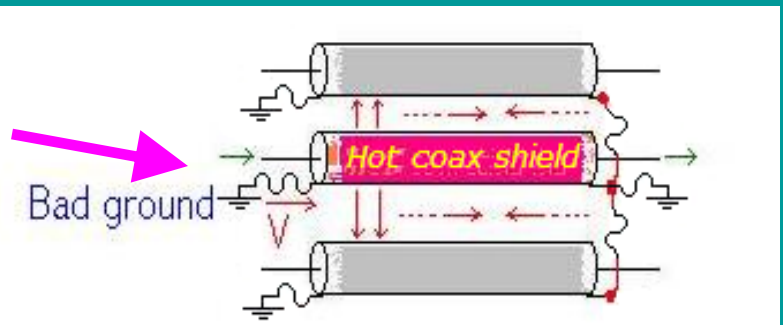
Observed:

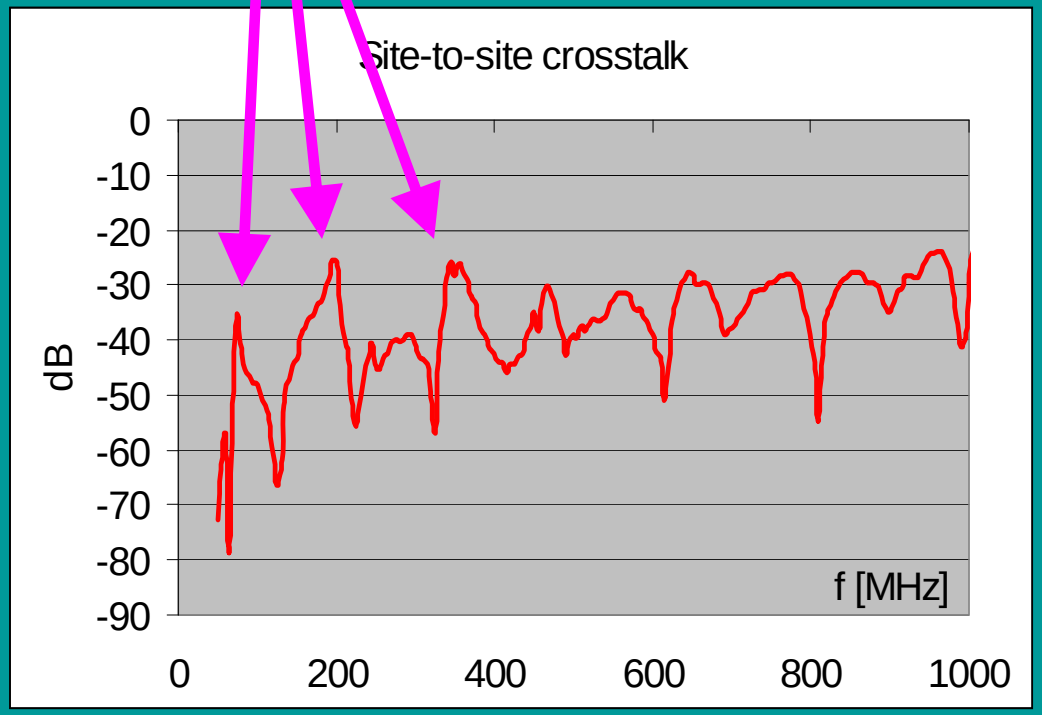
Peaks in Crosstalk

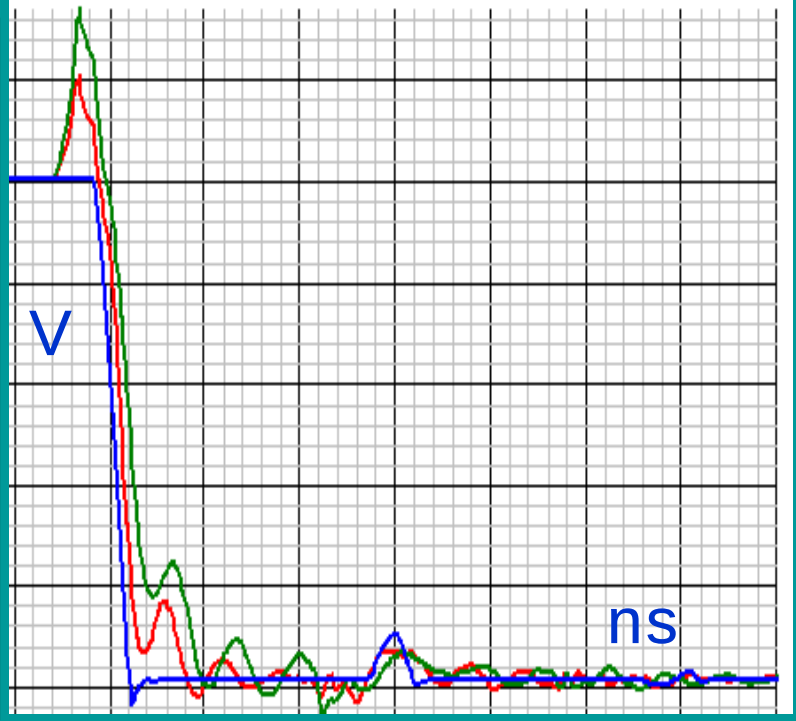
?

Cause:

Inductance in ground path

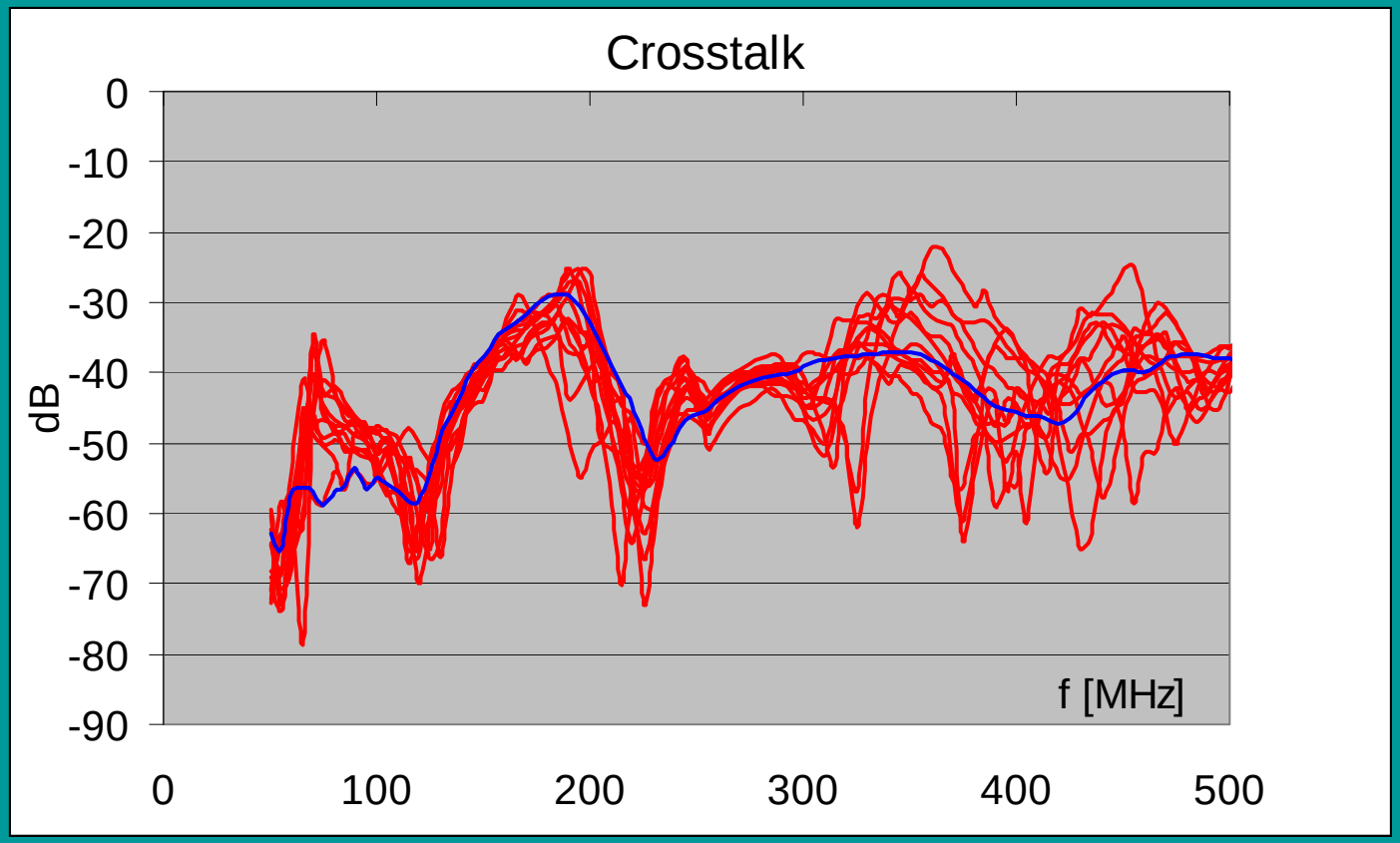






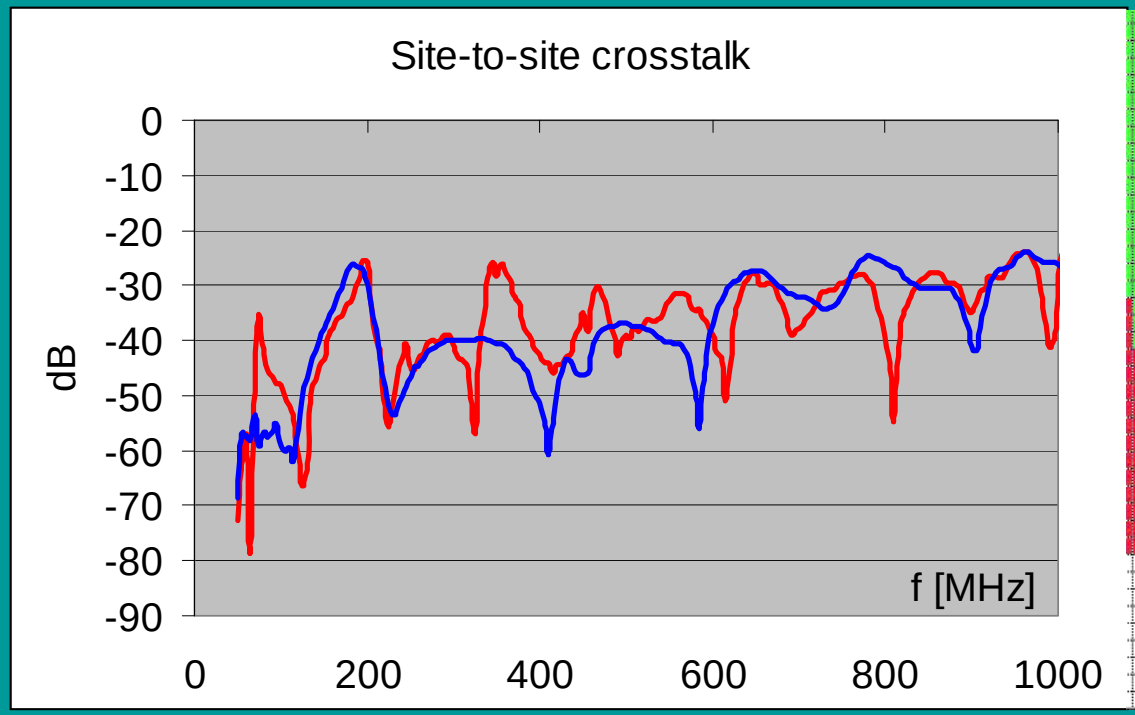
Line to line crosstalk and step response plot
(blue line = without crosstalk)

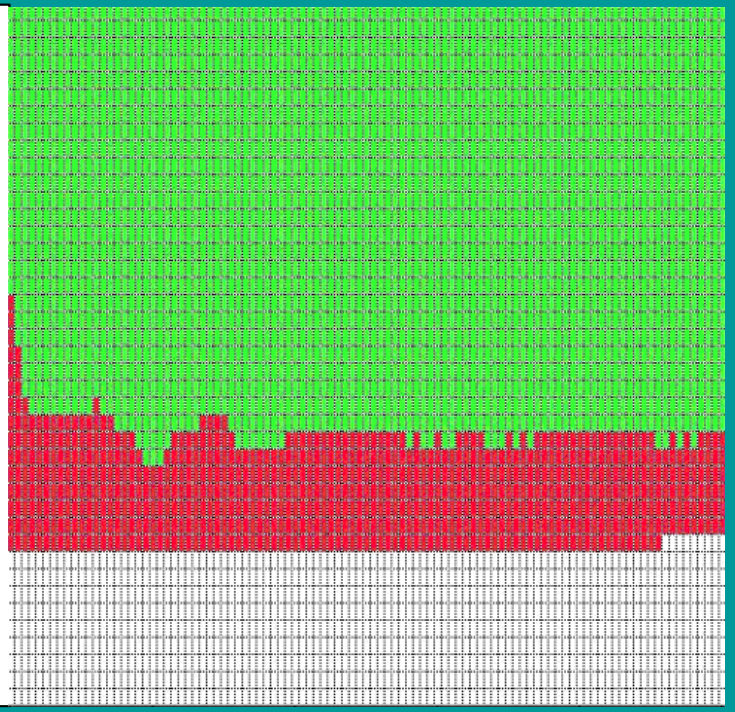
Common mode coupling



Line to line crosstalk impact is increased from multiple aggressors

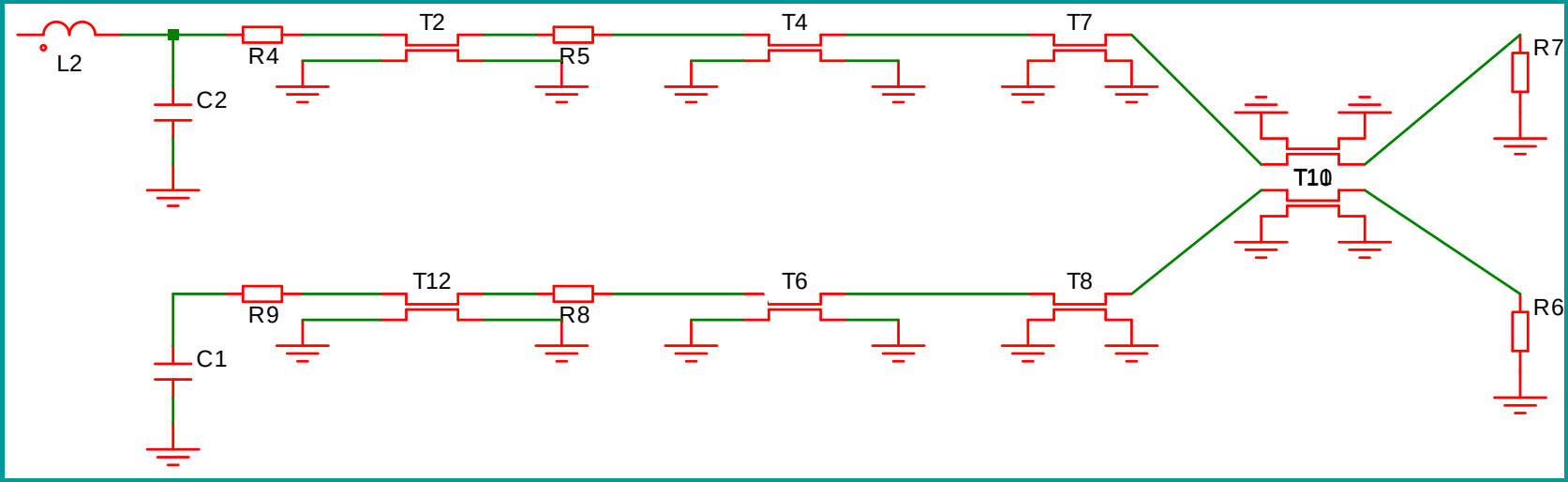
Common mode coupling





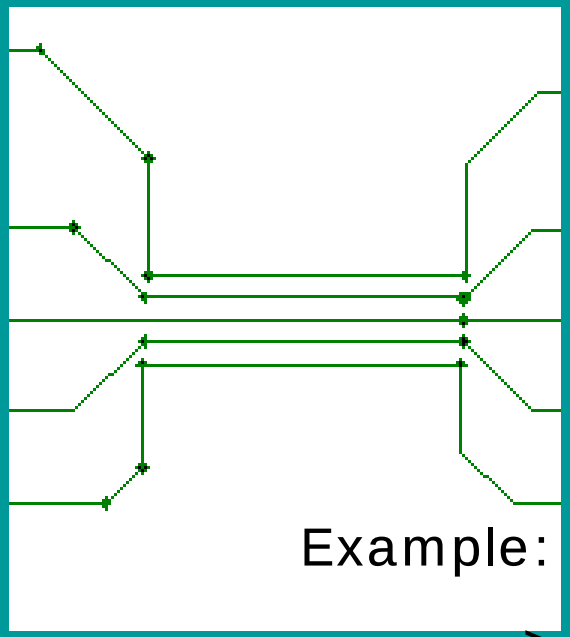
Line to line crosstalk and shmoo plot after design changes (blue curve)

Coupled lines



Tester PCB Interposer Ceramic DUT

Most likely locations for inadvertent coupling are the PCB, the interposer and the signal distribution on the space transformer (ceramic)



Example problem 2: Short coupled lines on the space transformer

Example: Coupled length = 1 cm

-> free space wavelength at ~33 GHz

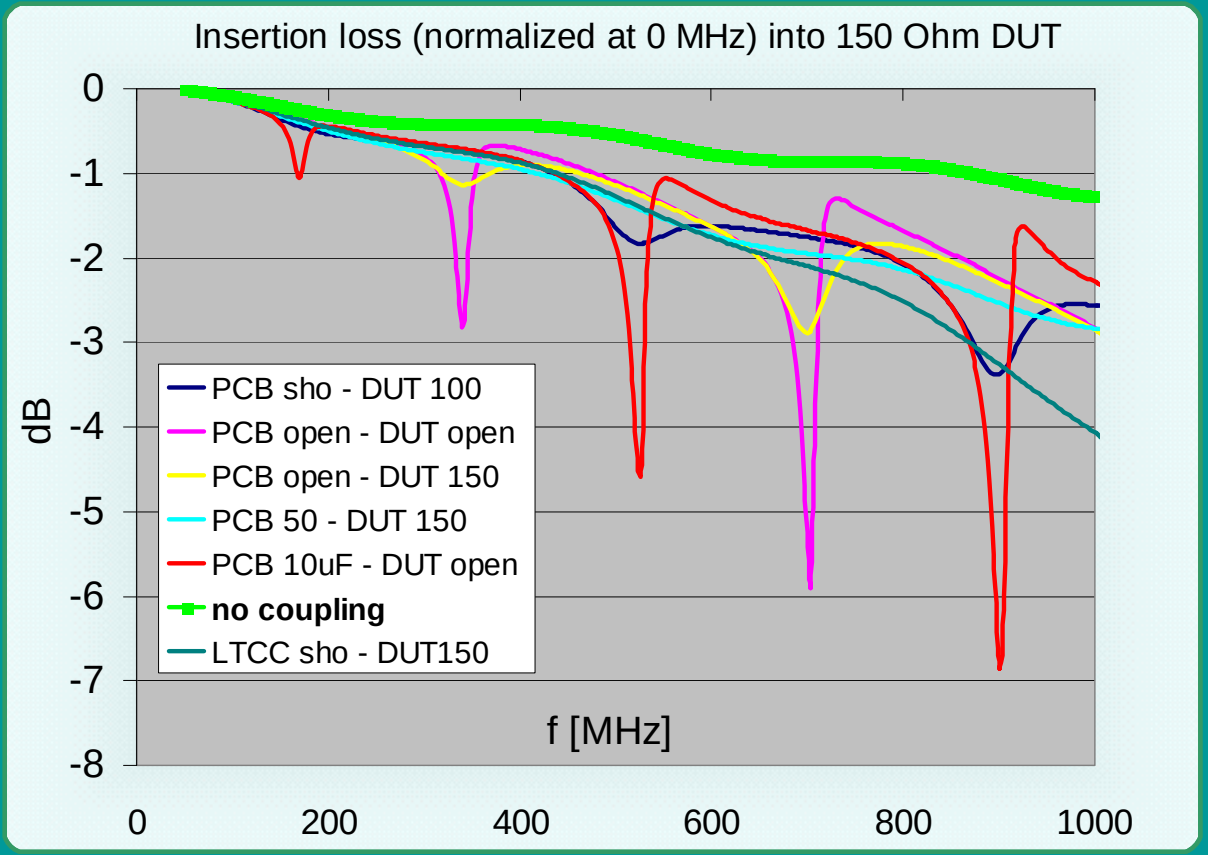
-> on Alumina at ~10 GHz

o> quarter wavelength at ~2.5 GHz

guard trace

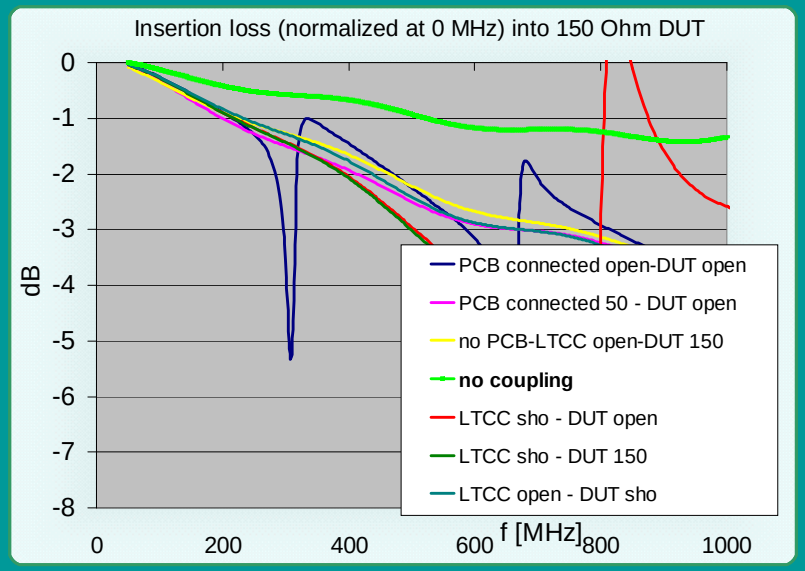
Should I worry ?

Coupled lines SPICE models

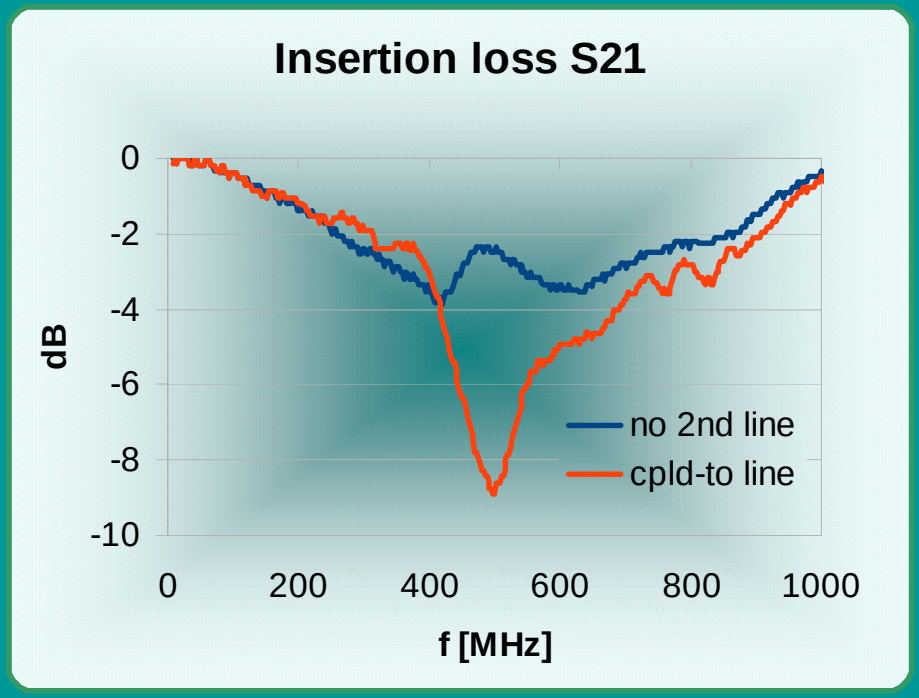


1) Resonances appear upon coupling
2) Increased insertion loss – energy is taken away
3) Point 2 also equates to increased crosstalk

Coupled lines model and measurement

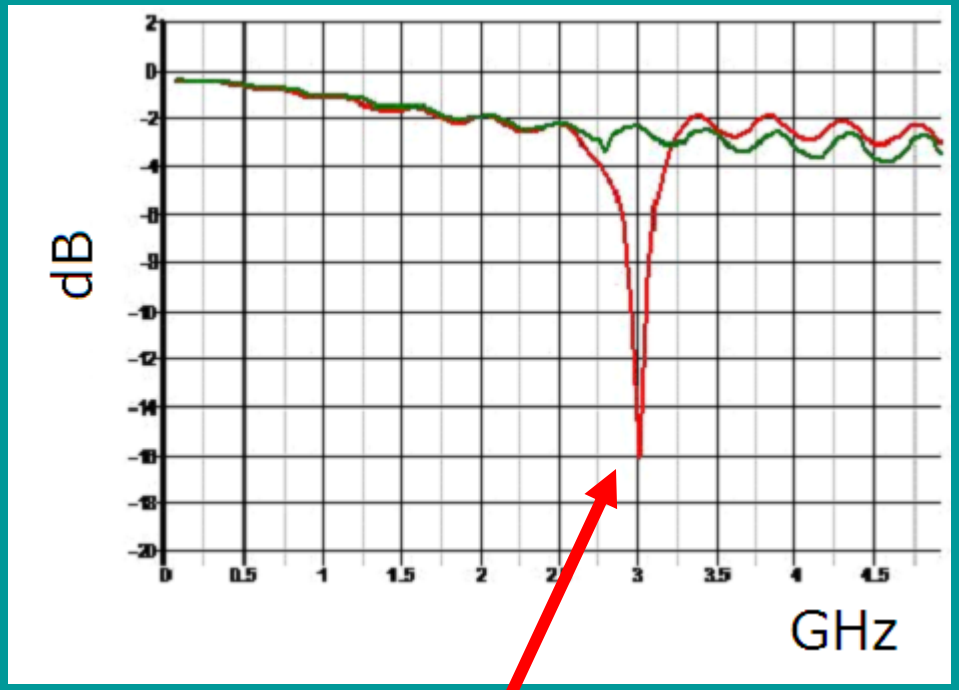


Matters get worse with increasing coupling length

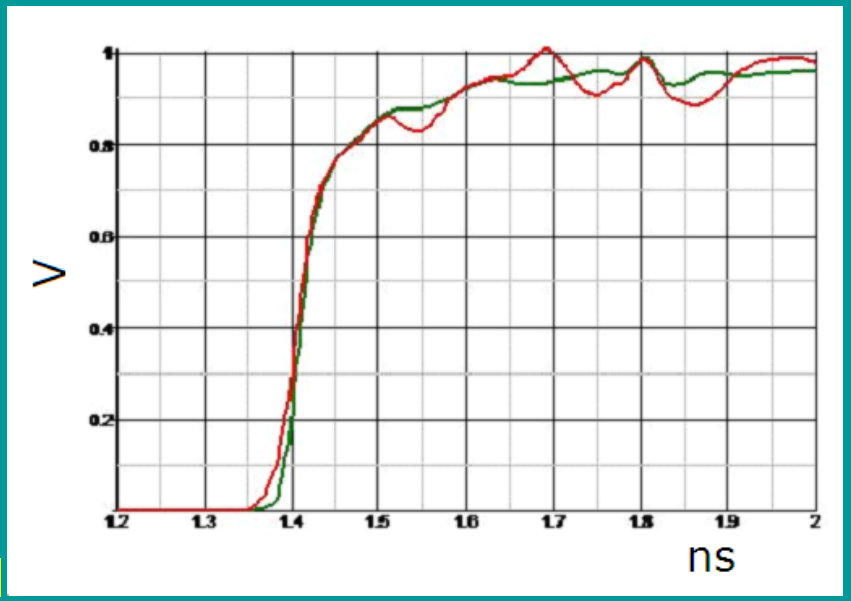


Probe card measurement (scale model) demonstrates impact of coupled line on insertion loss measurement

Impact of resonances on time and frequency domain performance



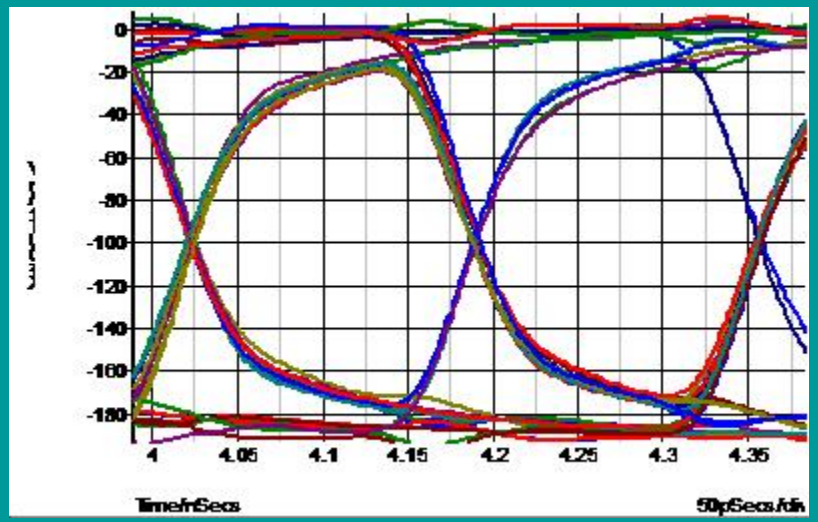
Insertion loss model

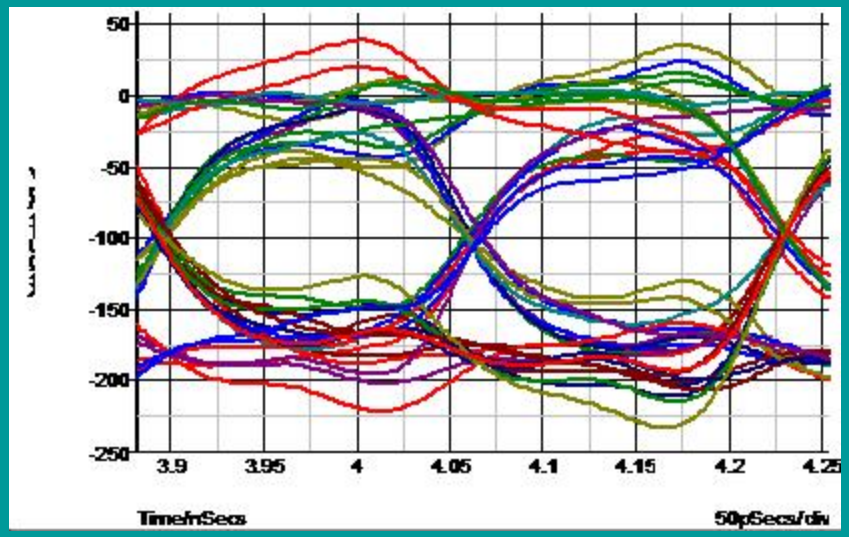


Transmitted step model

While the frequency domain response shows a strong resonance, the voltage step has only small aberrations, but.....

Eye diagram change due to an adjacent pin open/short resonance





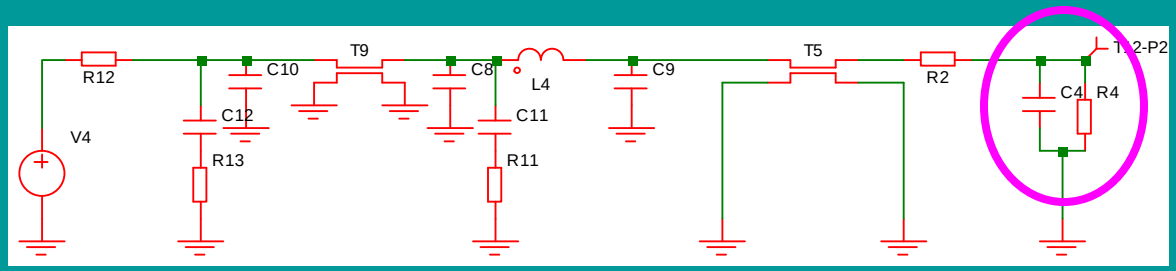
no resonance

resonance

Noticeable degradation of an eye diagram at 6Gbps from a 3 GHz resonance*

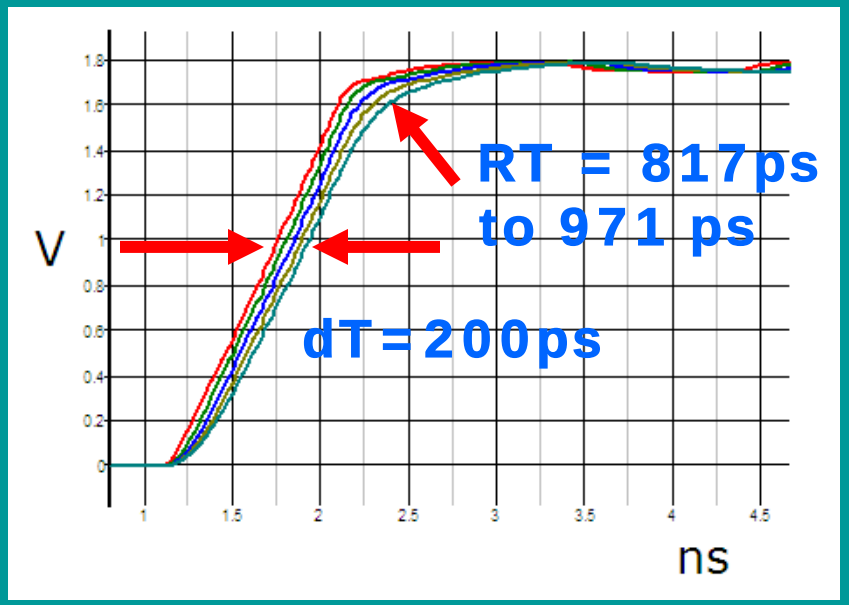
**For resonances at lower frequencies data rates scale accordingly to lower values*

Capacitive loading from devices



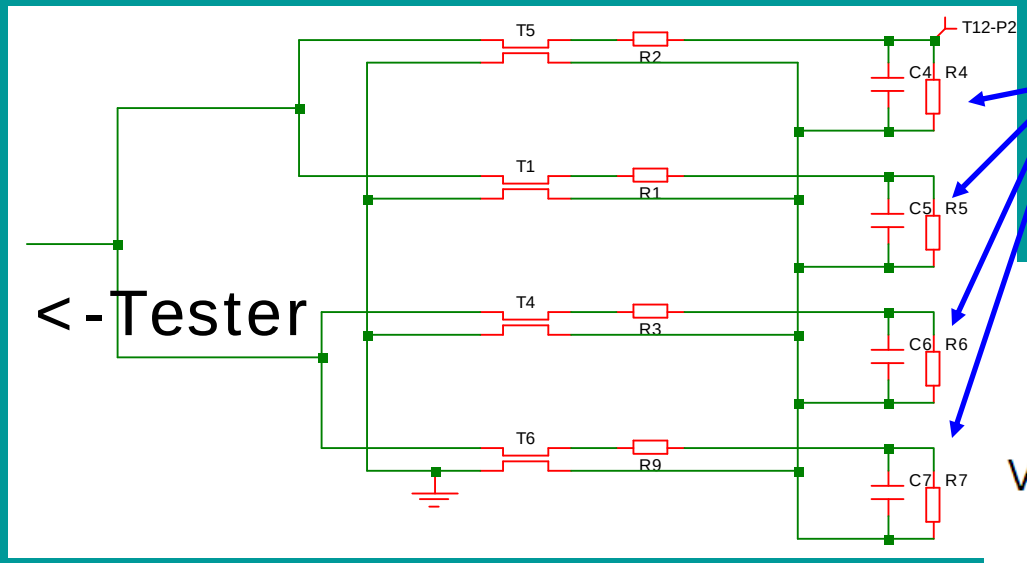
Device inputs often have pF level capacitances

Graph shows simulation results for a representative selection of DUT input capacitance values

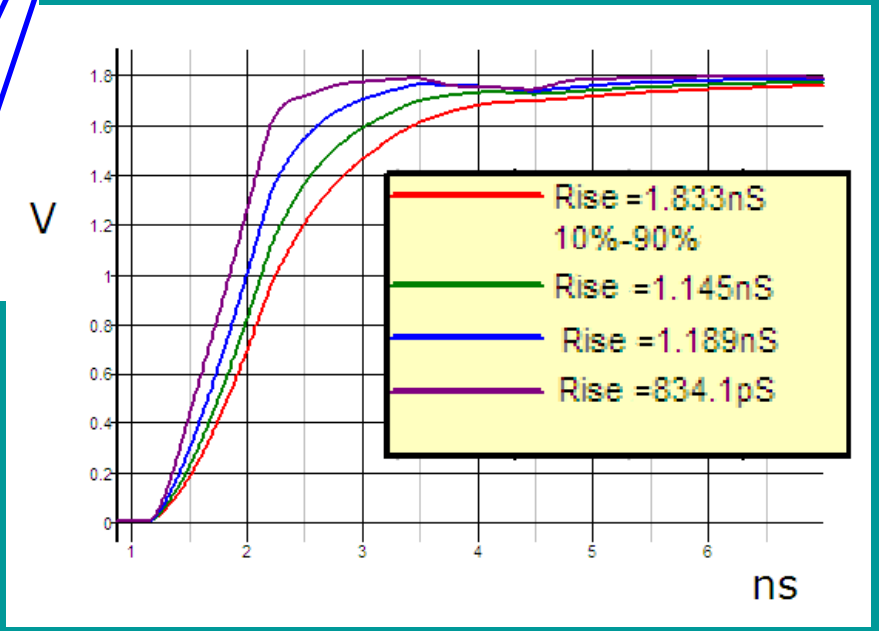


RC time constant and mismatch cause timing shift as well as rise time reductions

Shared resources



Device inputs



Capacitive loading from devices and parallel lines causes timing shift as well as rise time reductions

Example problem 3:
Long coupled lines, PCB

Example: Coupled length = 10 cm

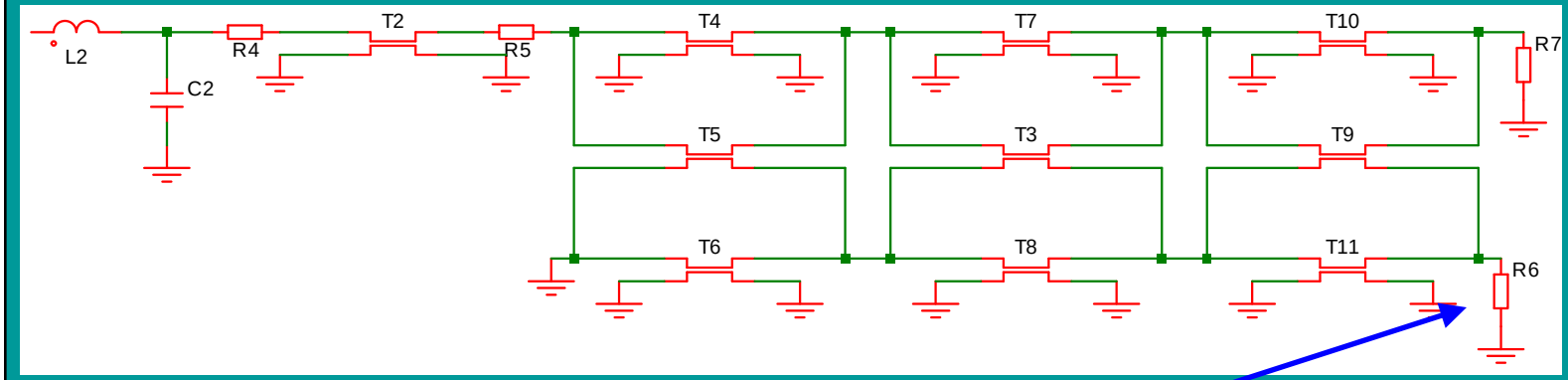
-> = free space wavelength λ at 3 GHz

-> = λ on FR-4 at ~ 1.4 GHz

o> quarter wavelength at 330 MHz

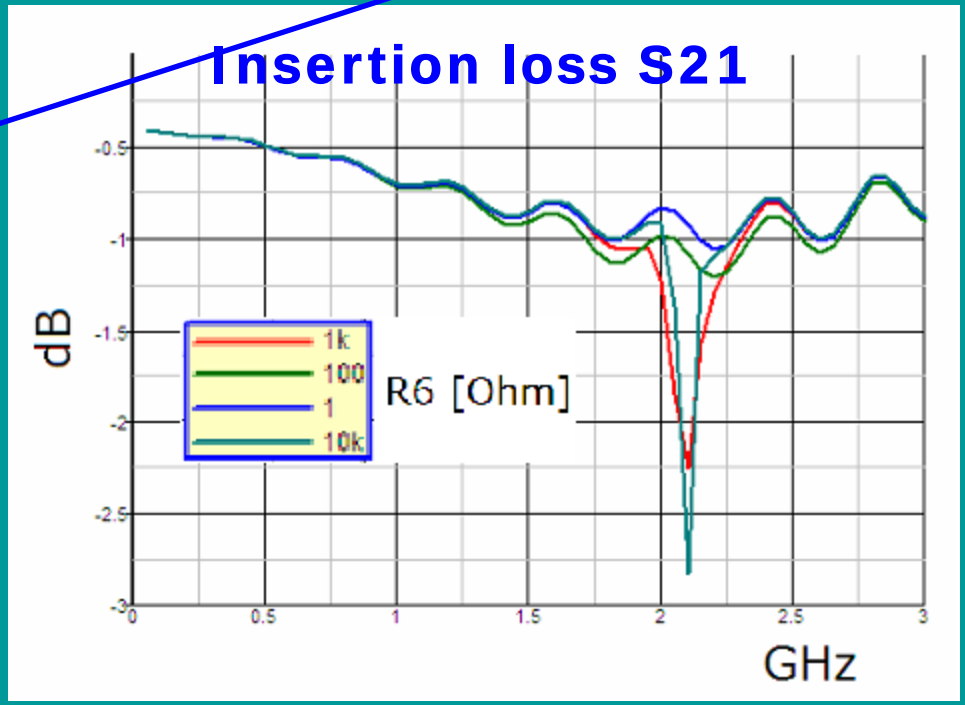
Time to worry !

Coupled lines remedy

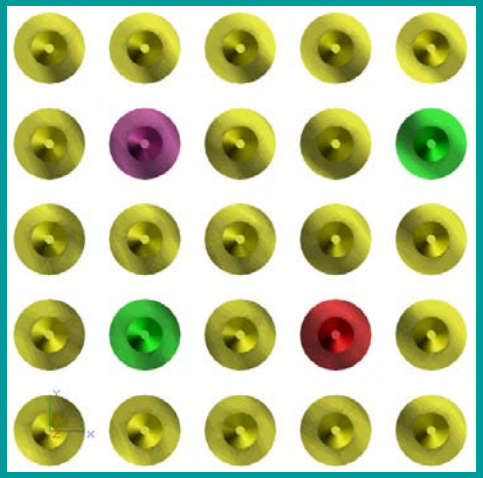


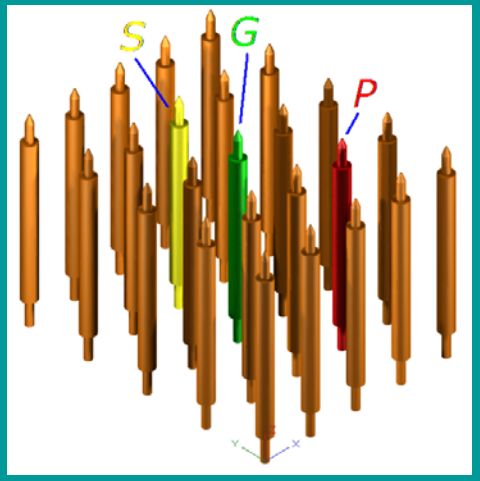
Resonance elimination by resistive loading – even relatively large values can reduce resonance peaks

Loading can potentially be located somewhere along the offending line, not necessarily at the end



Coupled pins





Example: Interposer - coupled length = 3 mm

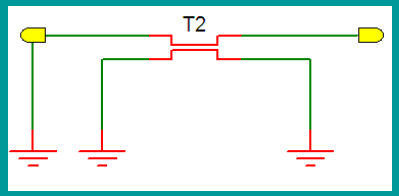
-> = free space wavelength λ at ~100 GHz

-> = λ in typical socket dielectric at ~50 GHz

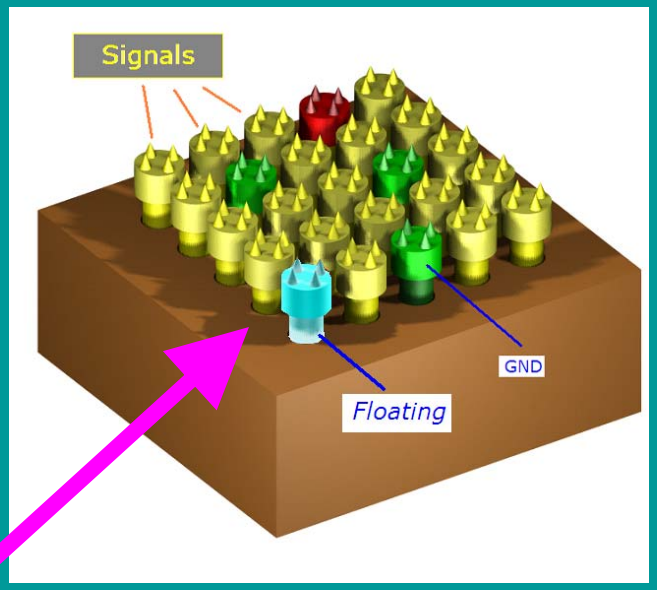
o> quarter wavelength at ~12 GHz

Should I worry ?

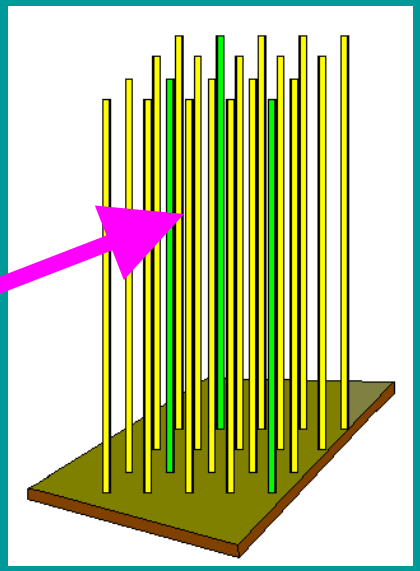
Helmholtz resonator



Transmission line, open on one end, shorted on the other

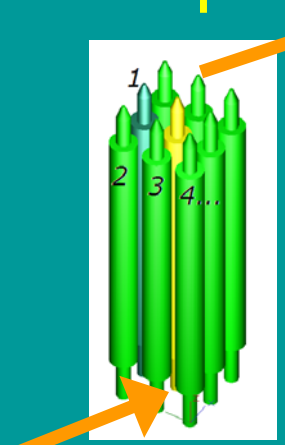


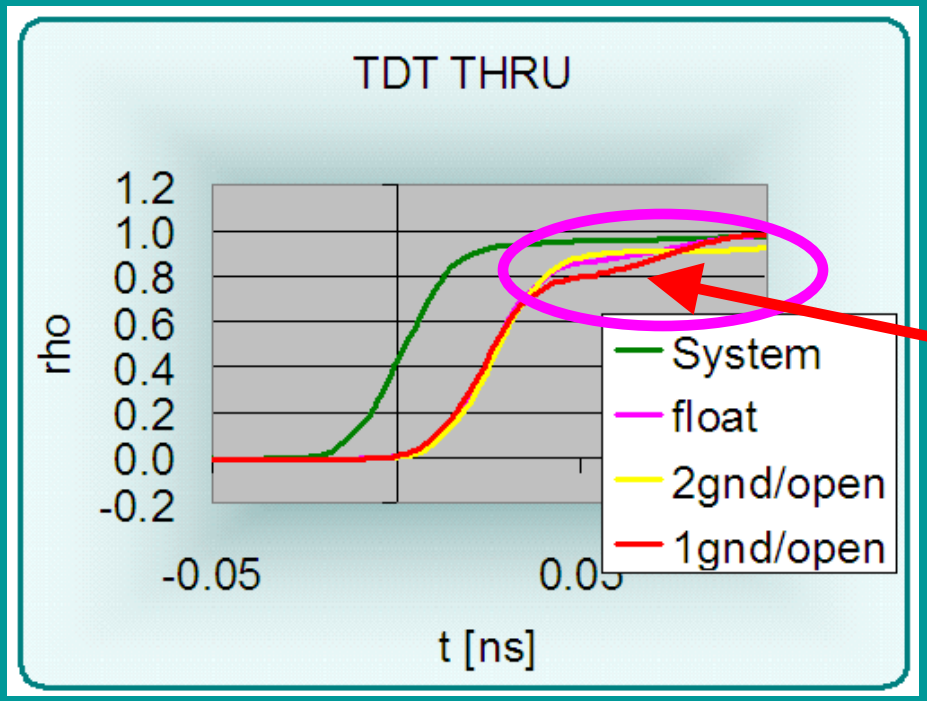
Opportunities for open/short circuited transmission lines exist

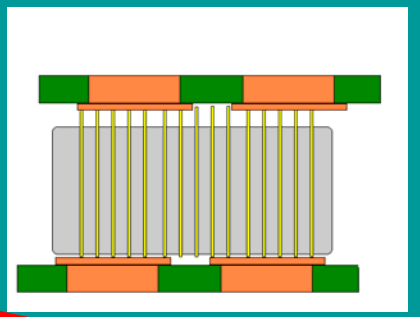


Consequences of an open/short pin

Measured time domain signals sent through a representative contact array (on yellow pin) show some changes as a result of an open/shorted pin (1) in the assembly:



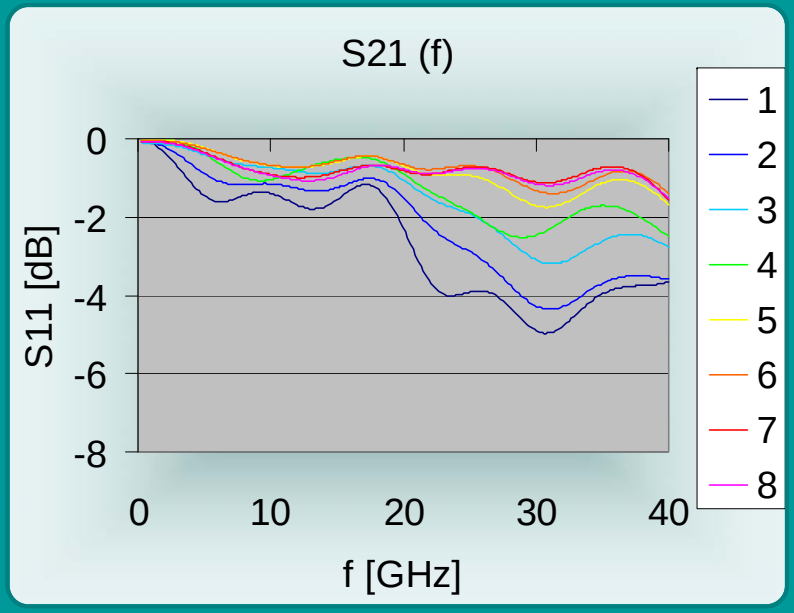


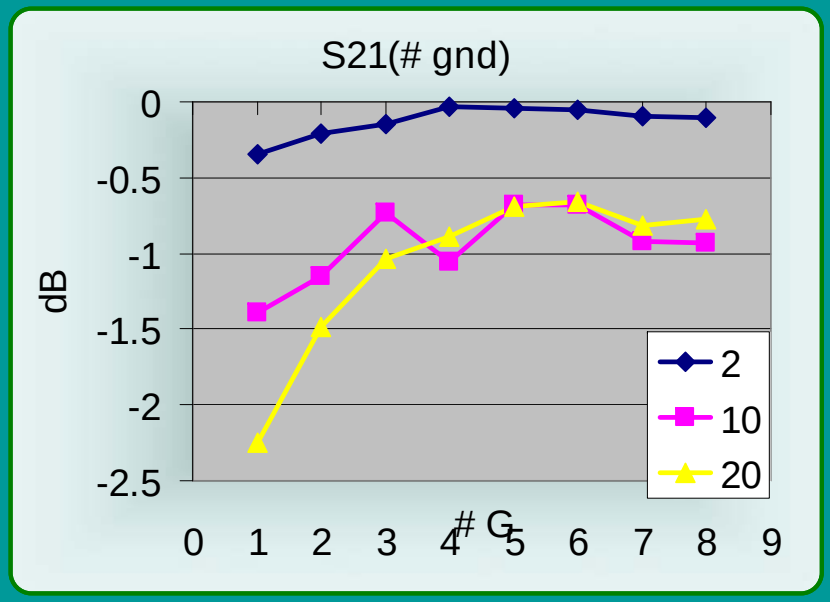


A noticeable timing error results at the 80% level

(red curve)

Insertion loss (S21) performance with varying number of ground connections



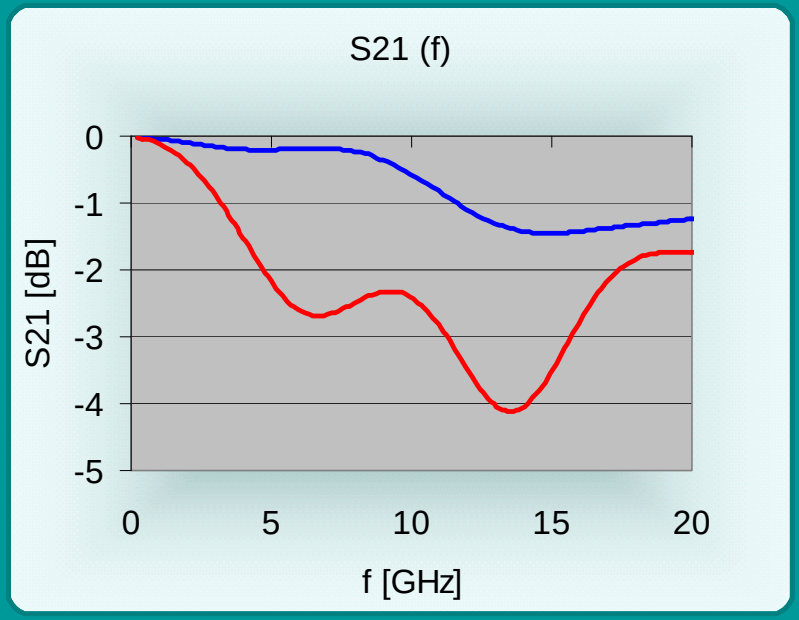


Insertion loss

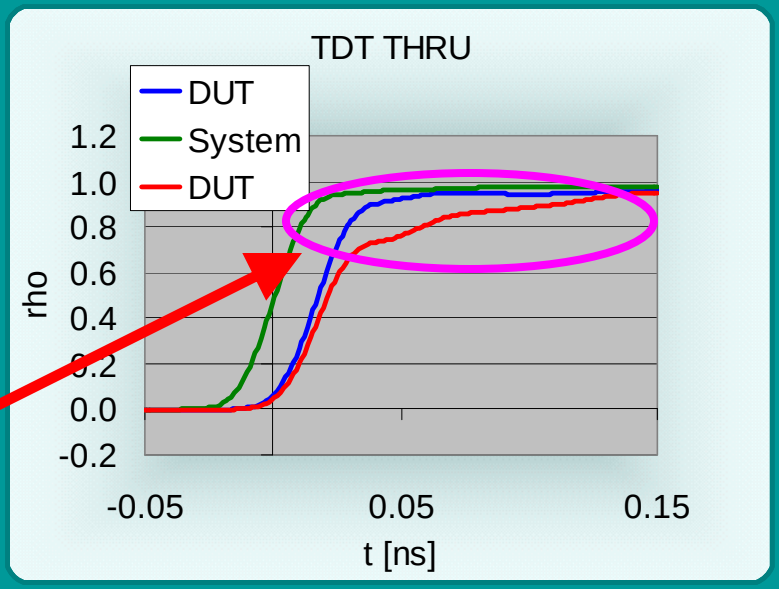
Insertion loss change as a function of #GND at 3 different frequencies

As in the open/shorted pin scenario the impact on timing will again be noticeable

Interposer contact instability



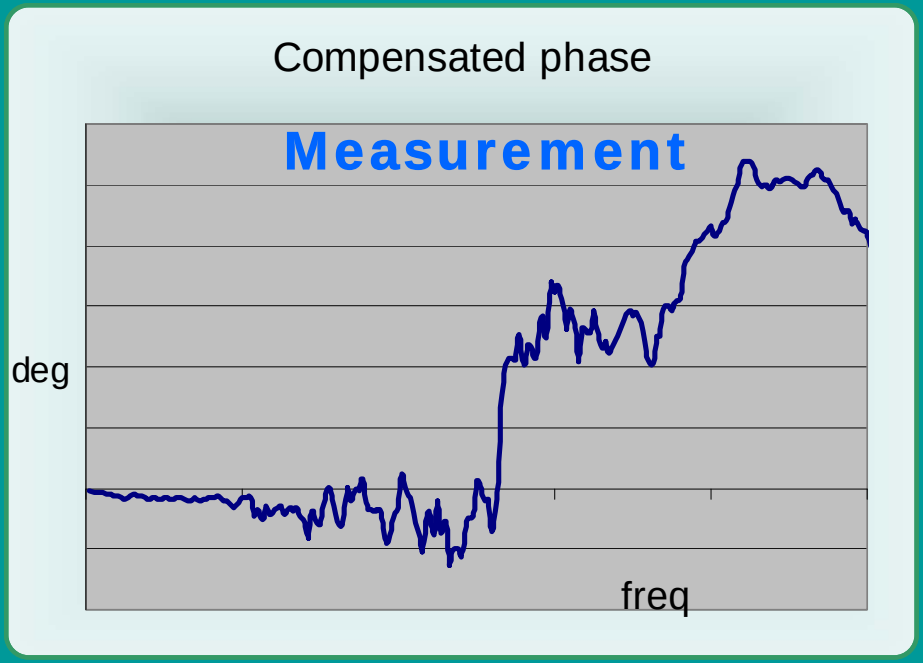
Measured S21 insertion loss and transmitted step signal variations of an interposer contact

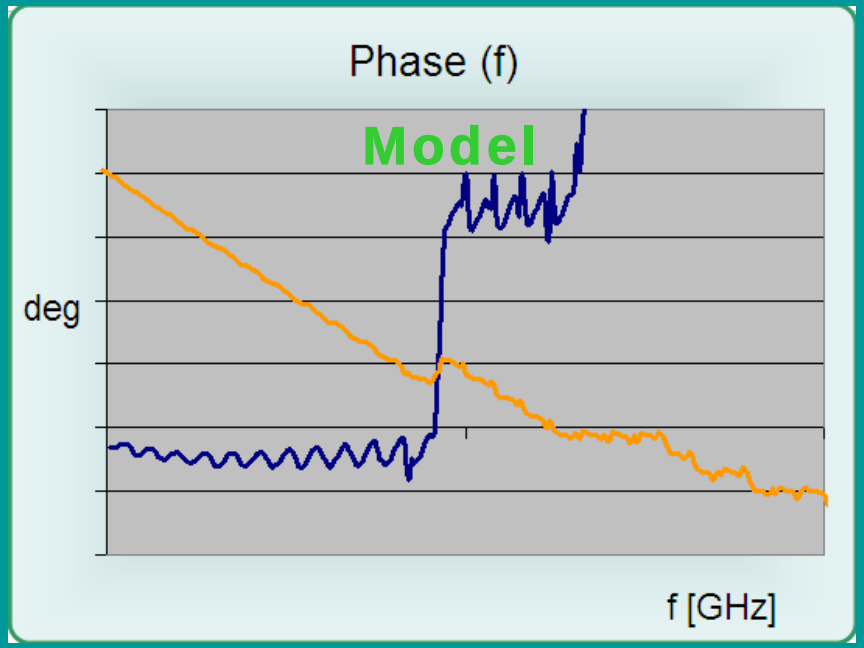


There will be significant timing variations (error) at the 80% signal level

(blue vs. red curve)

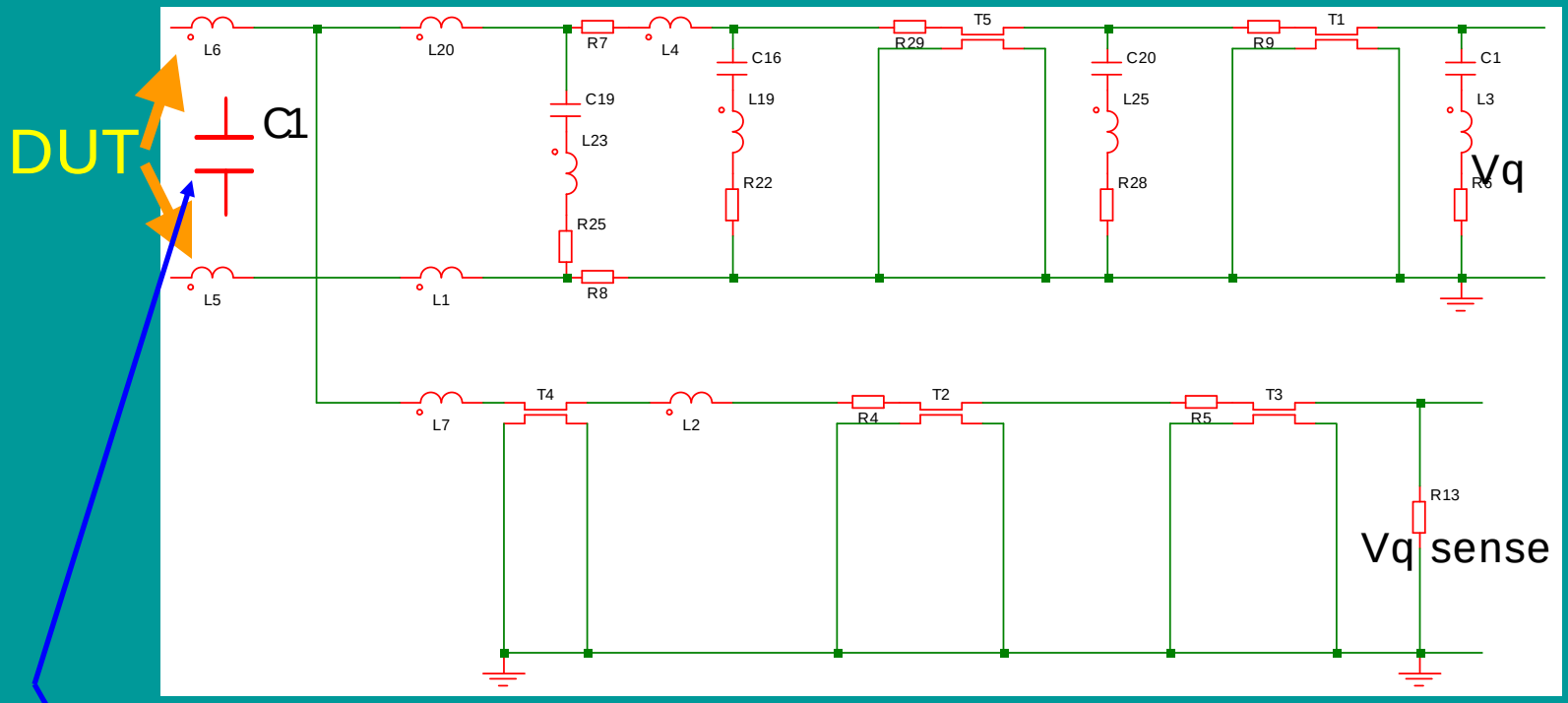
Diagnostics





Phase deviation from linear can be used to examine and visualize signal path quality. It also aids in adjusting models to the measurements.

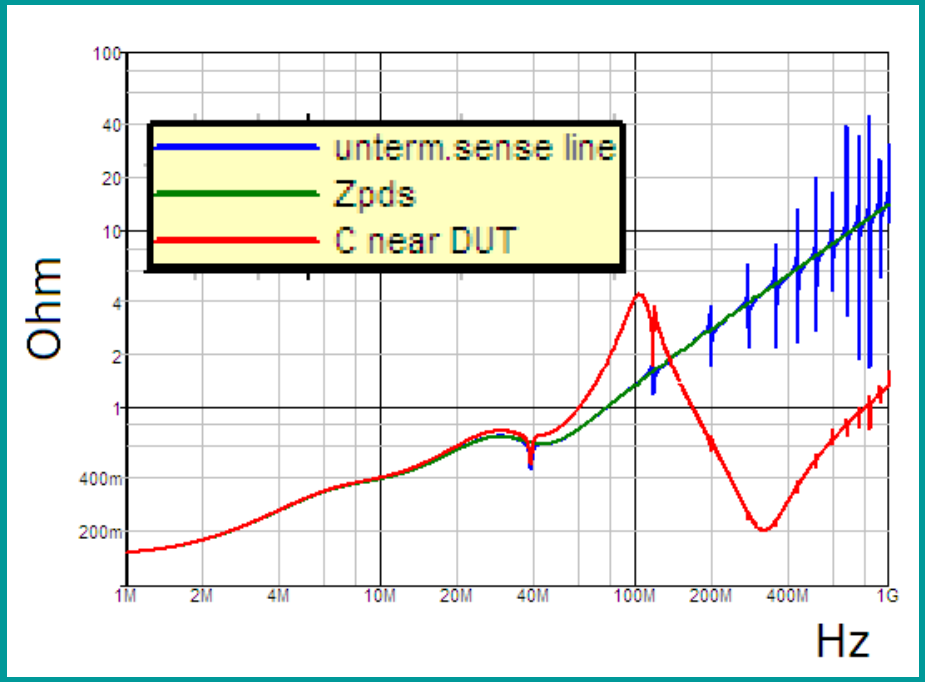
Power Delivery System (PDS)

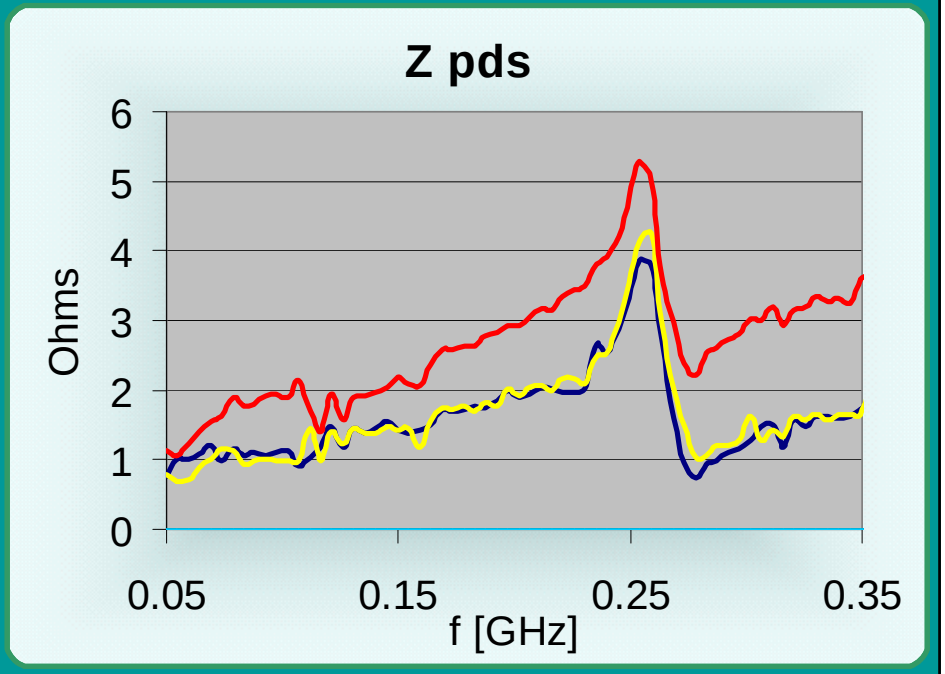


Potential sources of resonances:

- Transmission lines between capacitors
- 'Near'-die capacitance in conjunction with probe card inductance and capacitance
- Unterminated branch and sense lines

PDS resonances





Simplified PDS model SPICE simulation (with power delivery path and unterminated sense path as well as additional capacitance very near active device)

Measured PDS impedance as a function of frequency

(upper curve is for location in center of array)

Where is any of the above an issue ?

- At / near speed test
- Burn-in
  - Increasing speeds
  - Fast devices transmitting back into probe card
  - Power delivery system (PDS)
- Marketing

Conclusion

Examples demonstrate that seemingly insignificant individual effects can compound, thereby reducing performance

Some problems may not be readily apparent during the design phase and show only during verification via measurement or on the test floor

Resonances at high frequencies can have an impact on relatively slow signals via timing errors or ringing

Verification of performance via select measurement techniques can be a valuable tool to spot potential problems