IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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The Importance of the Signal Return Path in Test Applications

CIRCUIT SPECTRUM

MICREL®

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Introduction

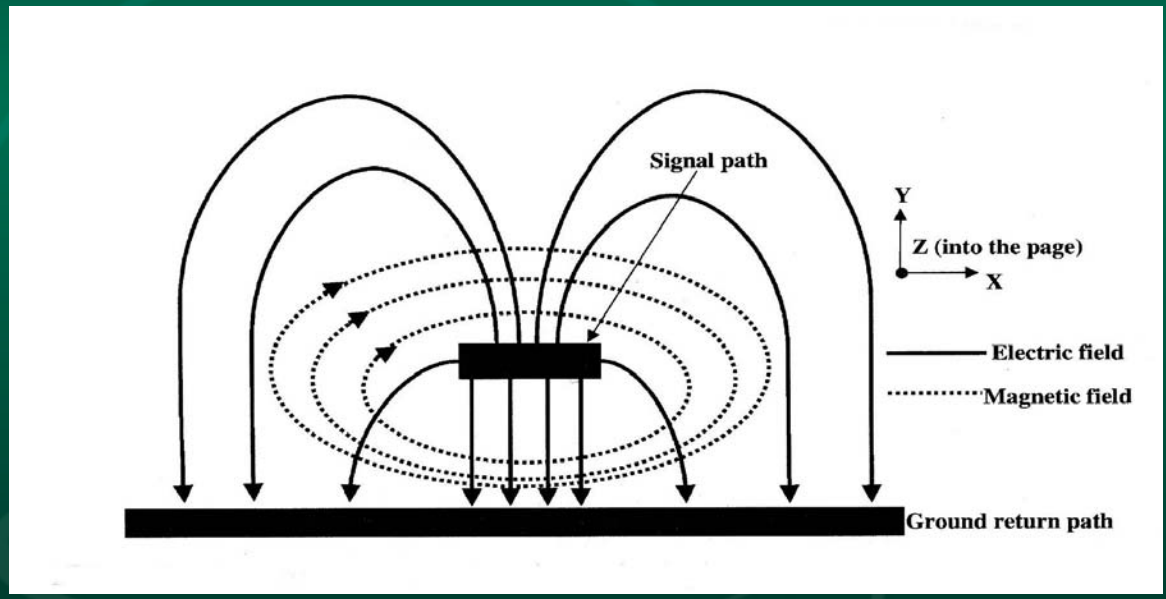
As digital data rates in electronic systems continue to increase, the demands on test professionals and on hardware escalate over the full range from ATE to PCB interfaces and semiconductor device contact mechanisms. Instruments housed in ATE deliver or promise to deliver signals in excess of 10 Gbits per second. Simplified modeling and simulation techniques may fall short of accurately predicting behavior. We hope to demonstrate the value of 3D full-wave electromagnetic solutions as they pertain to the quality of the signal return path.

Outline

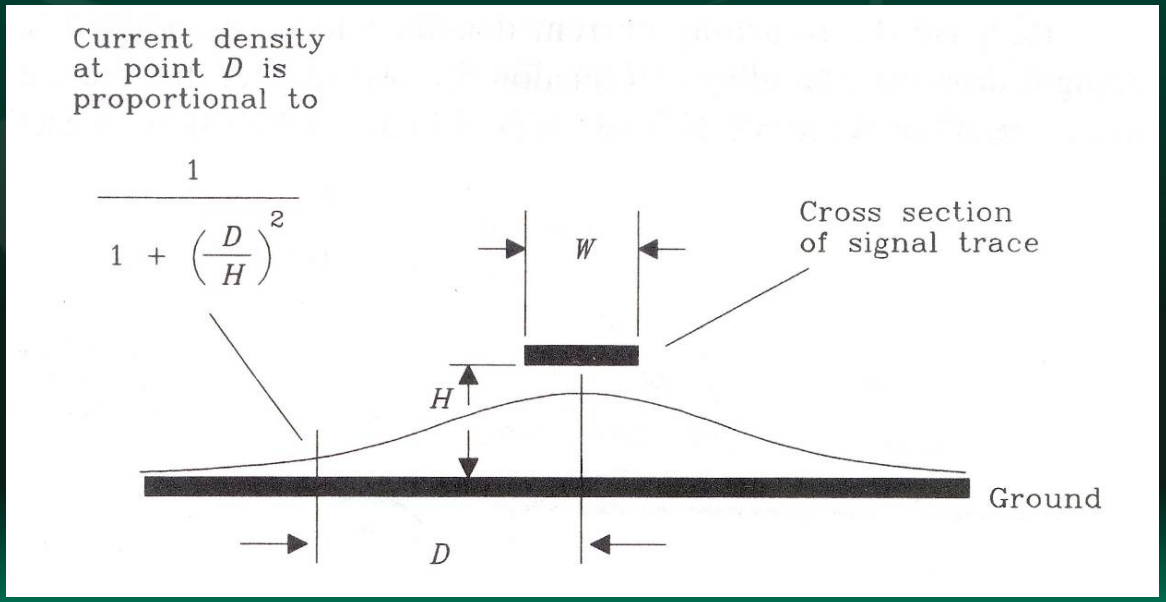
- Contributors to signal degradation at launch and as it propagates along its path in a PCB
- Lossy conductors and dielectric media and discontinuities in the signal or return path
- Use of frequency domain and time domain data to characterize 2-port systems
- Focus on PCB via transitions
- A simple, but important, lesson from an SMA launch
- Correlation between simulation results and empirical data

The Need for 3D Electromagnetic Field Solver

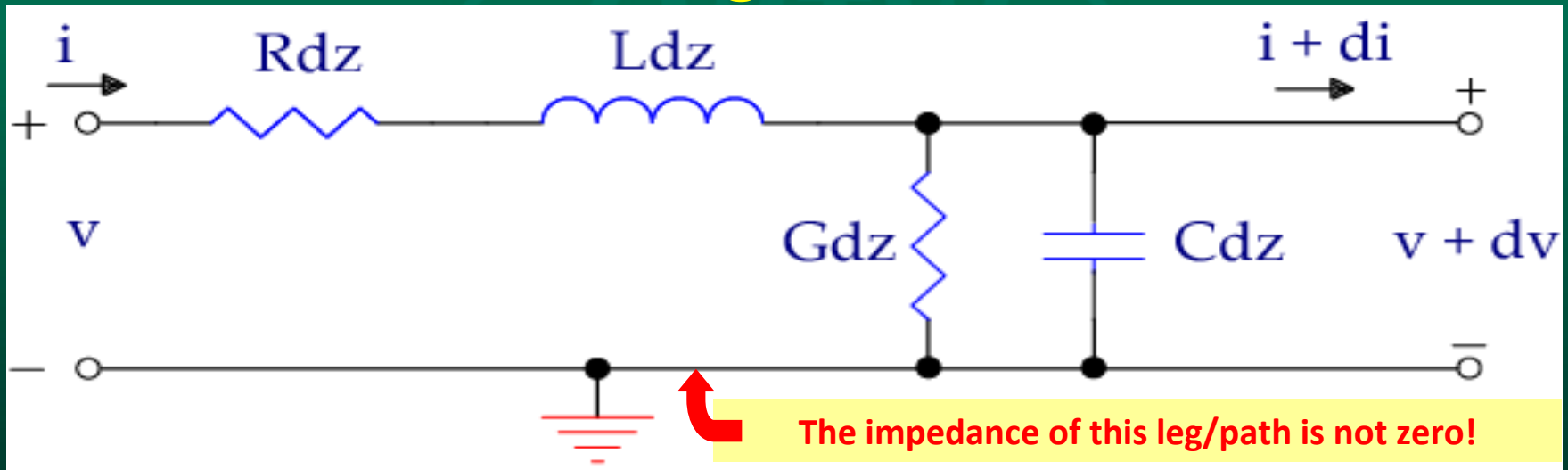
Time-varying electric and magnetic field lines



Current density is 10% at D=3H



RLGC Lumped-Element Model for Incremental Length dz



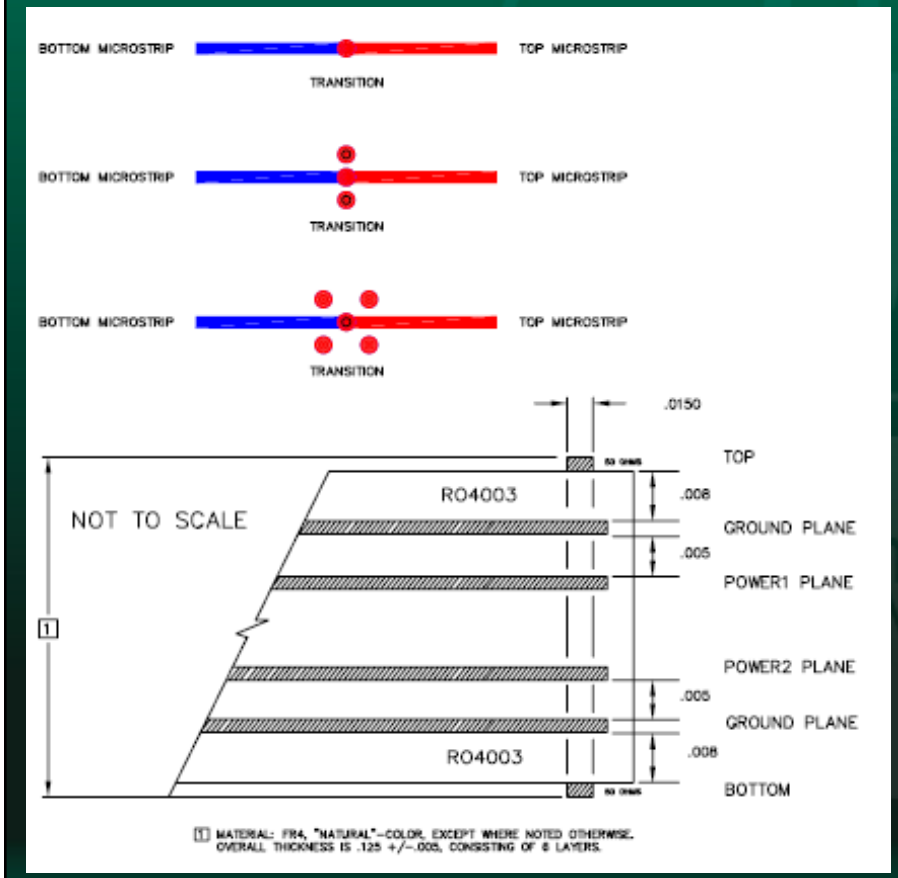
$$\frac{dv}{dz} = -L\frac{di}{dt} - R\,i$$

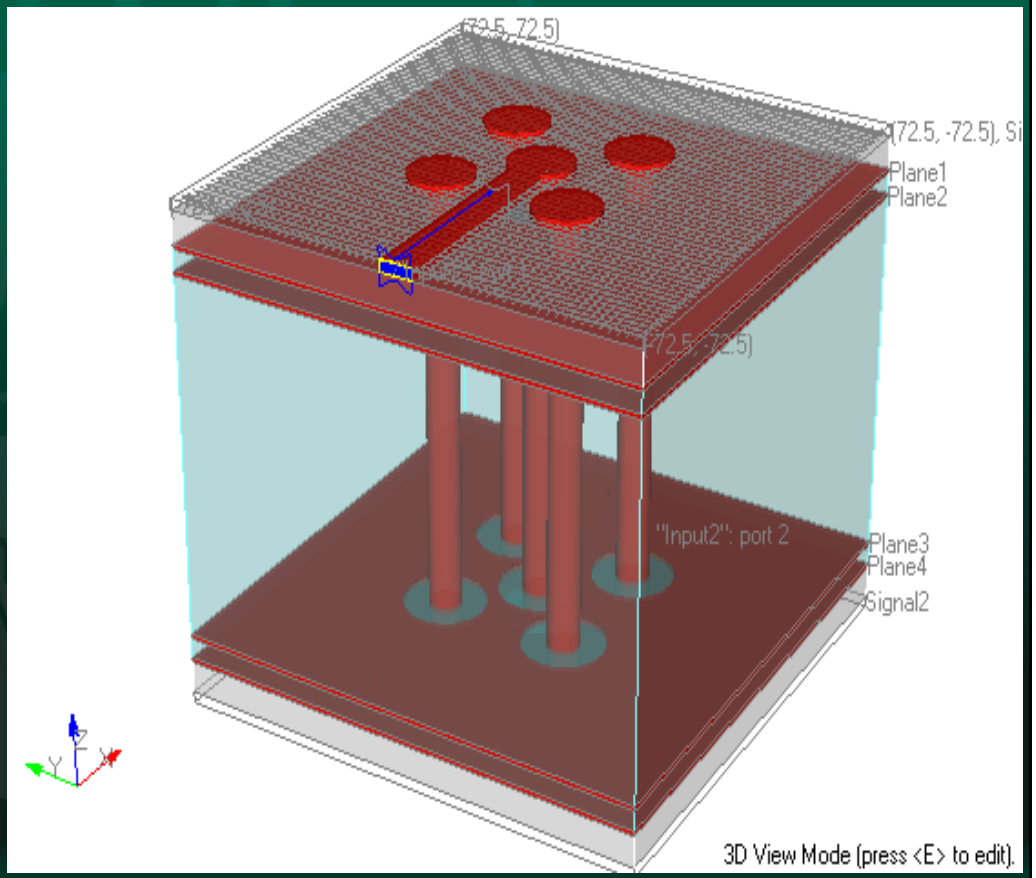
$$\frac{di}{dz} = -C\frac{dv}{dt} - G\,v$$

Microstrip Lines with Via Transitions

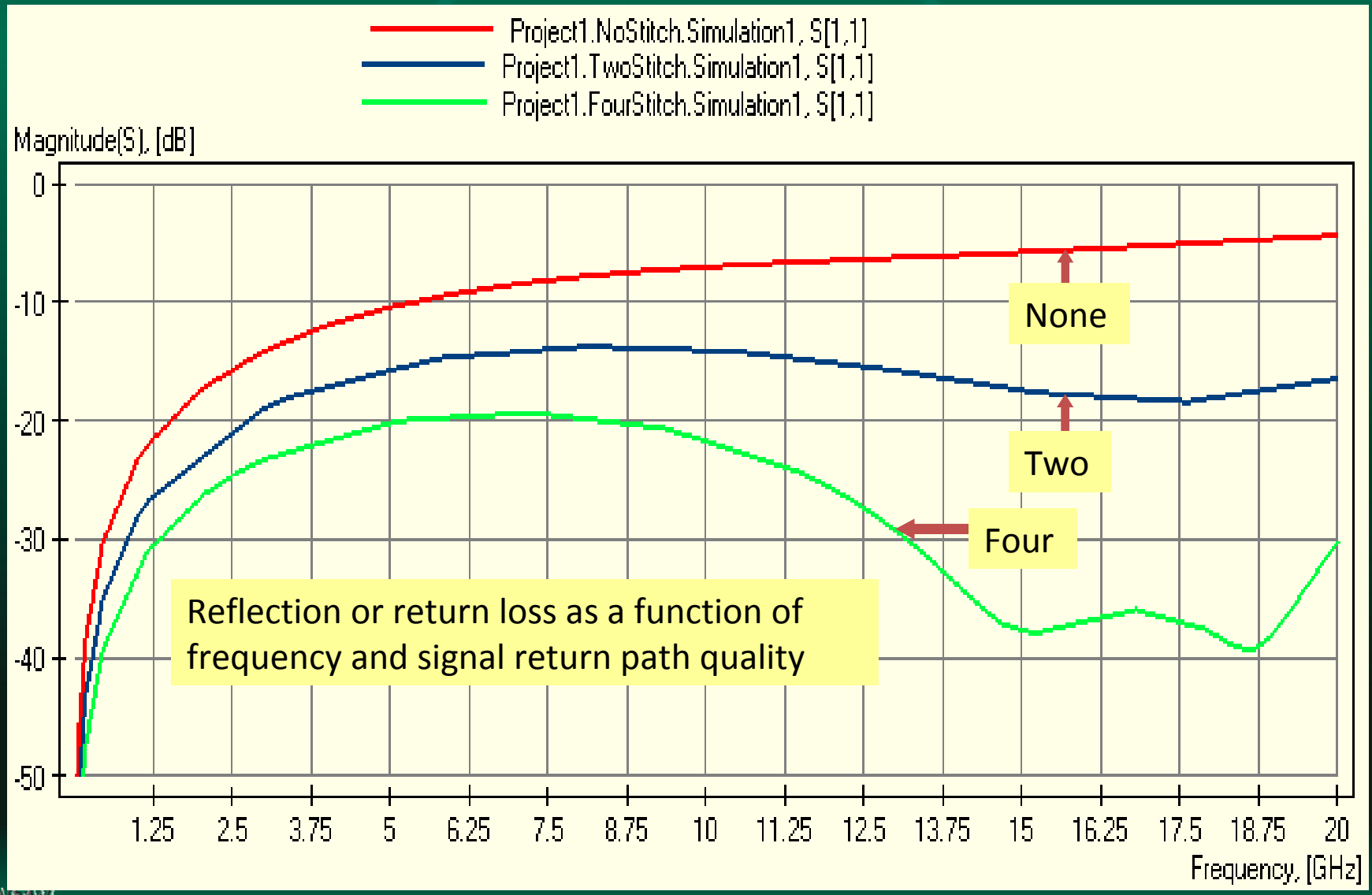
From CAD

Modeling by Simbeor

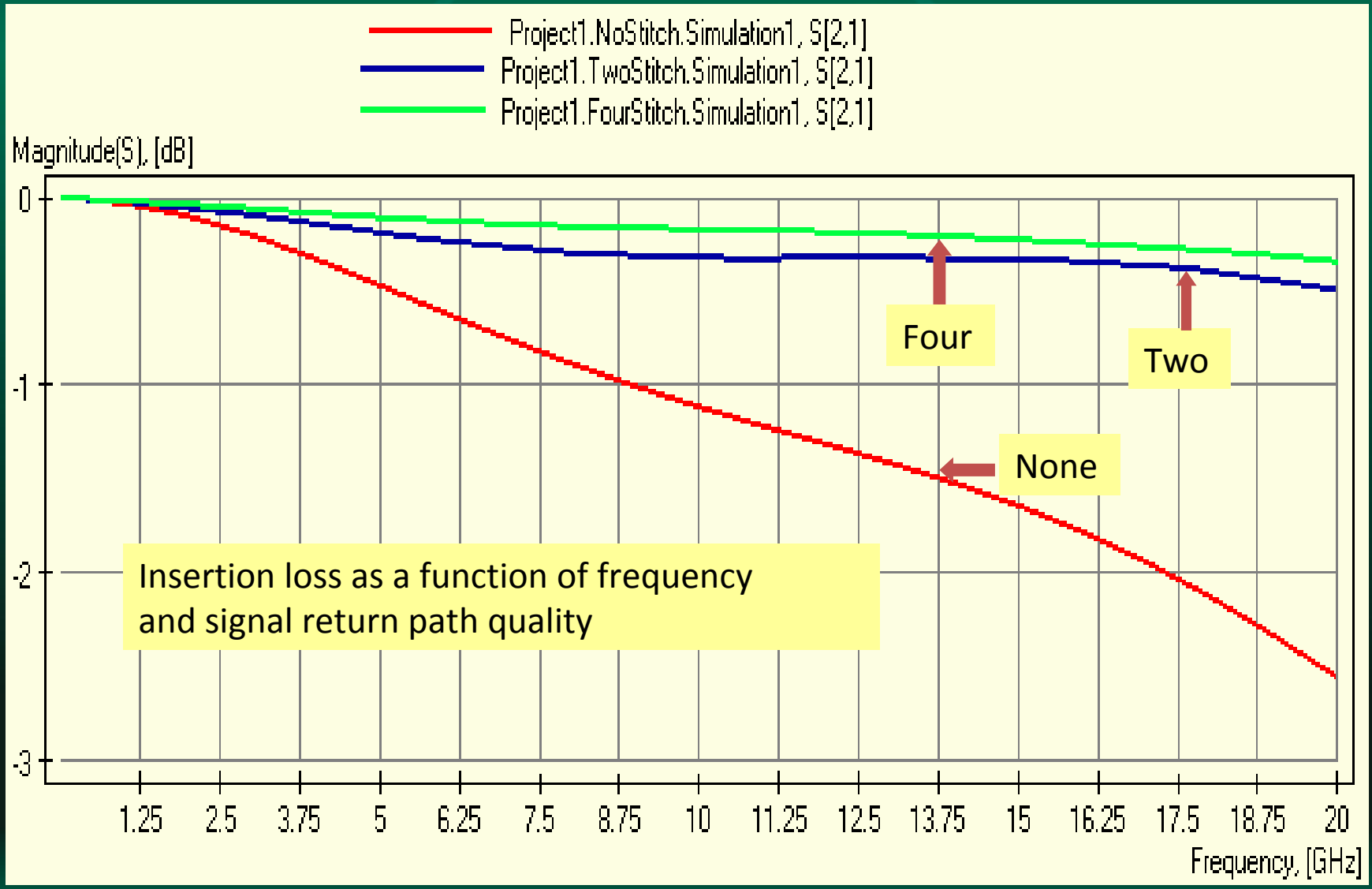




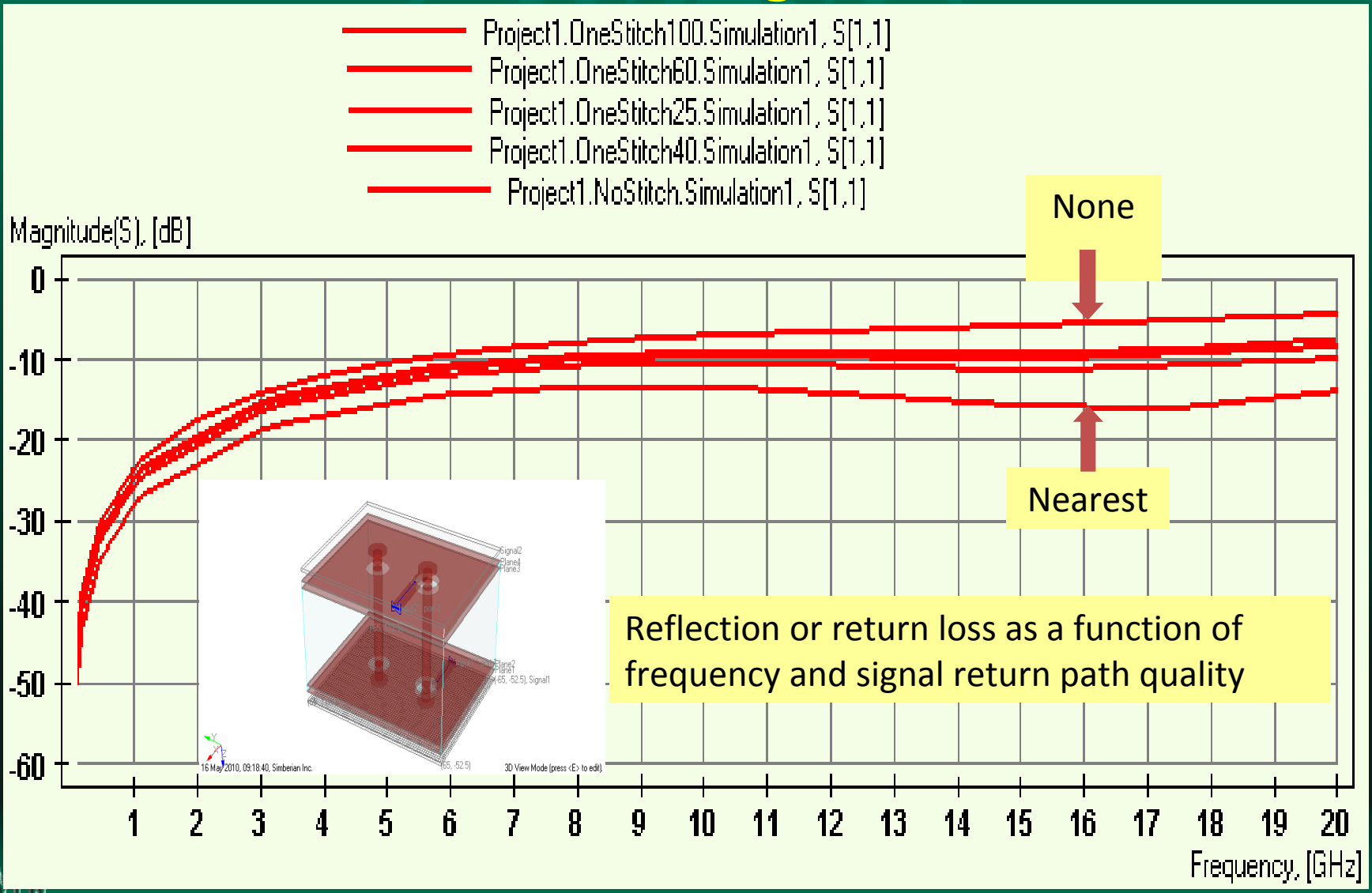
S11 for Three Ground Stitch Patterns



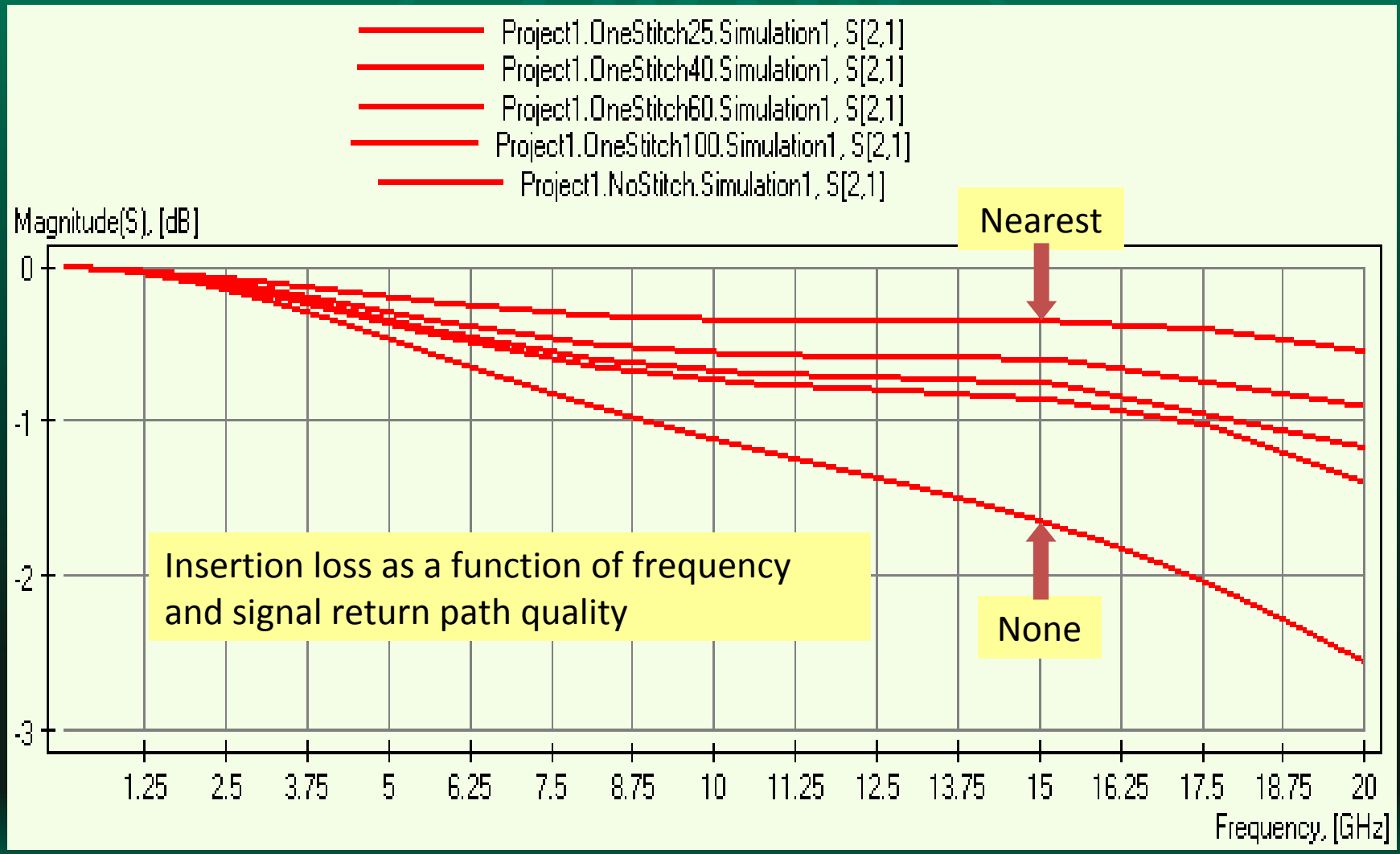
S21 for Three Ground Stitch Patterns



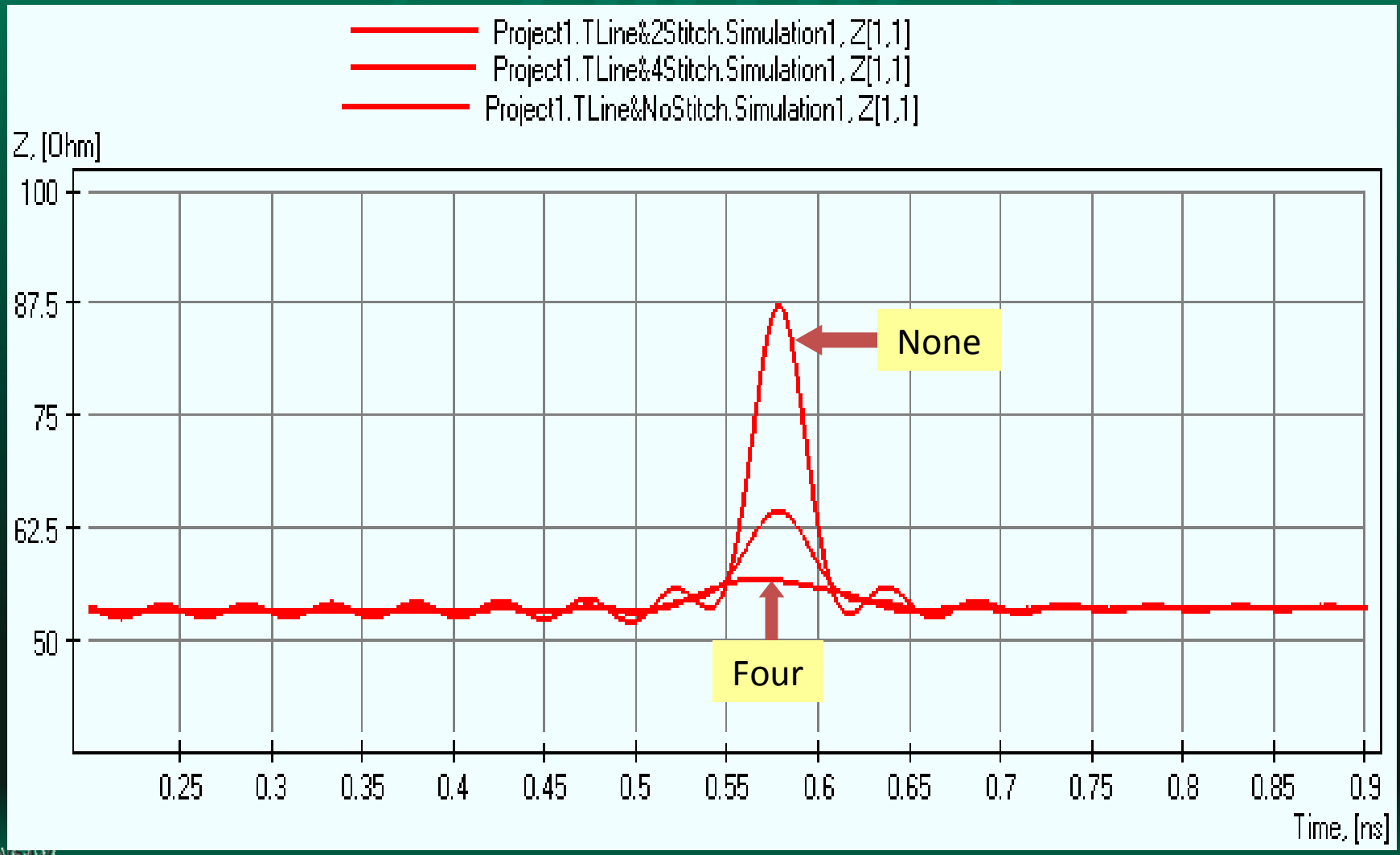
S11 for Varying Distance of Single Ground Stitch from Signal Via



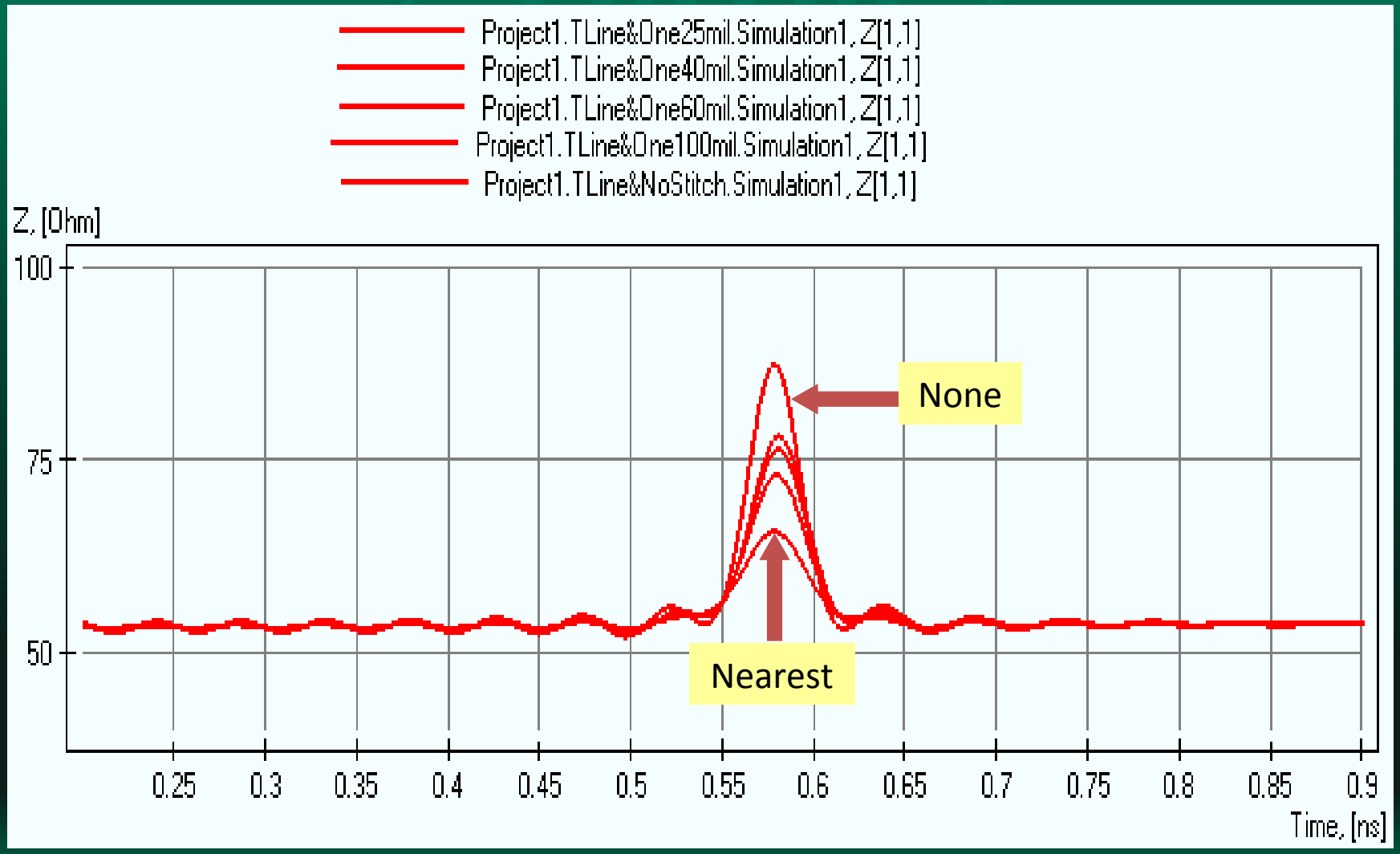
S21 for Varying Distance of Single Ground Stitch from Signal Via



TDR for Microstrips and Three Ground Stitch Patterns around Signal Via



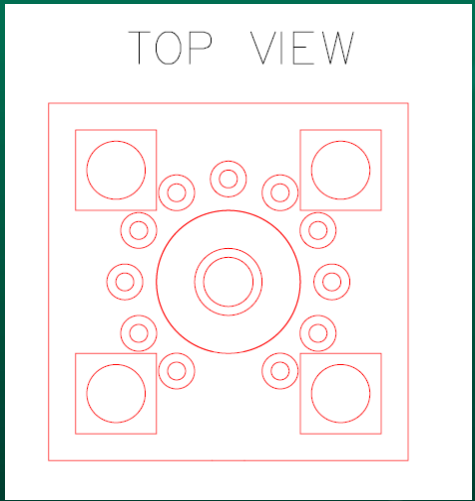
TDR for Microstrips and Varying Distance of Single Ground Stitch from Signal Via

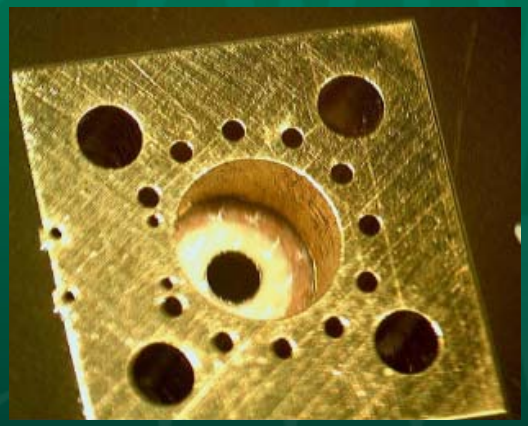


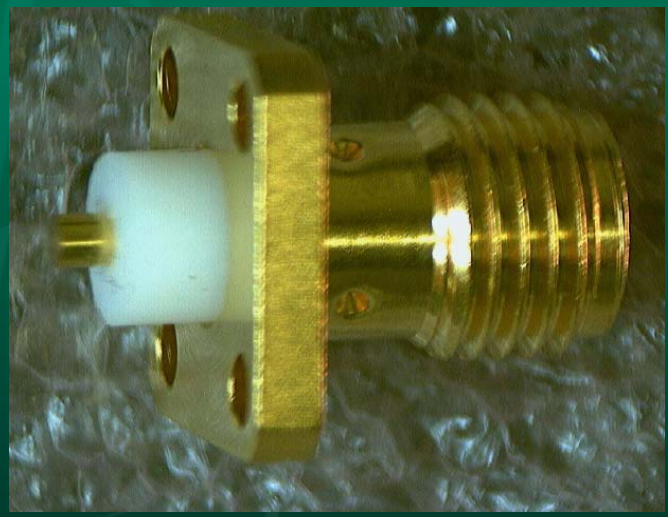
SMA Signal Launch through PCB

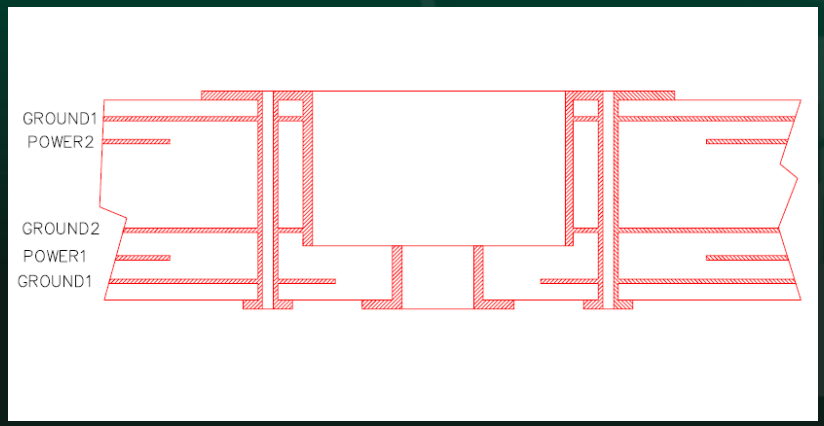
- SMA flange-mount connector launch
- Two cases - one with a poor return path and one with an improved configuration
- Simulation results from a 2D tool
- Simulation results from a 3D EM solver
- Measured data from a test coupon using VNA
- S-parameters show performance versus frequency

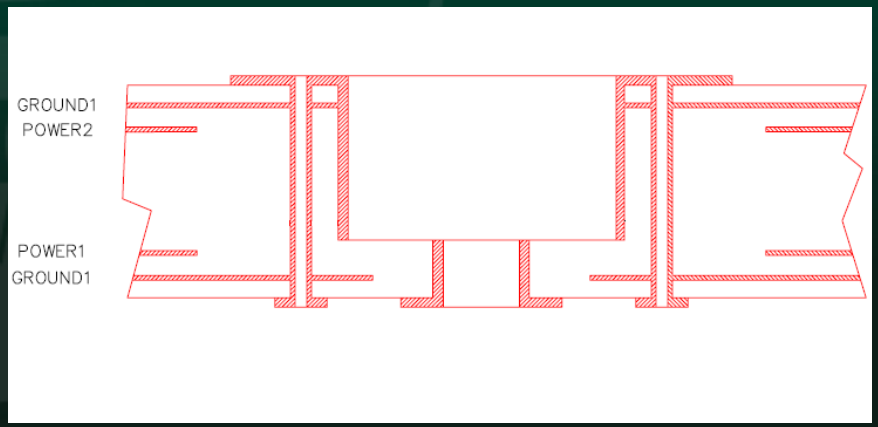
SMA Launch Detail







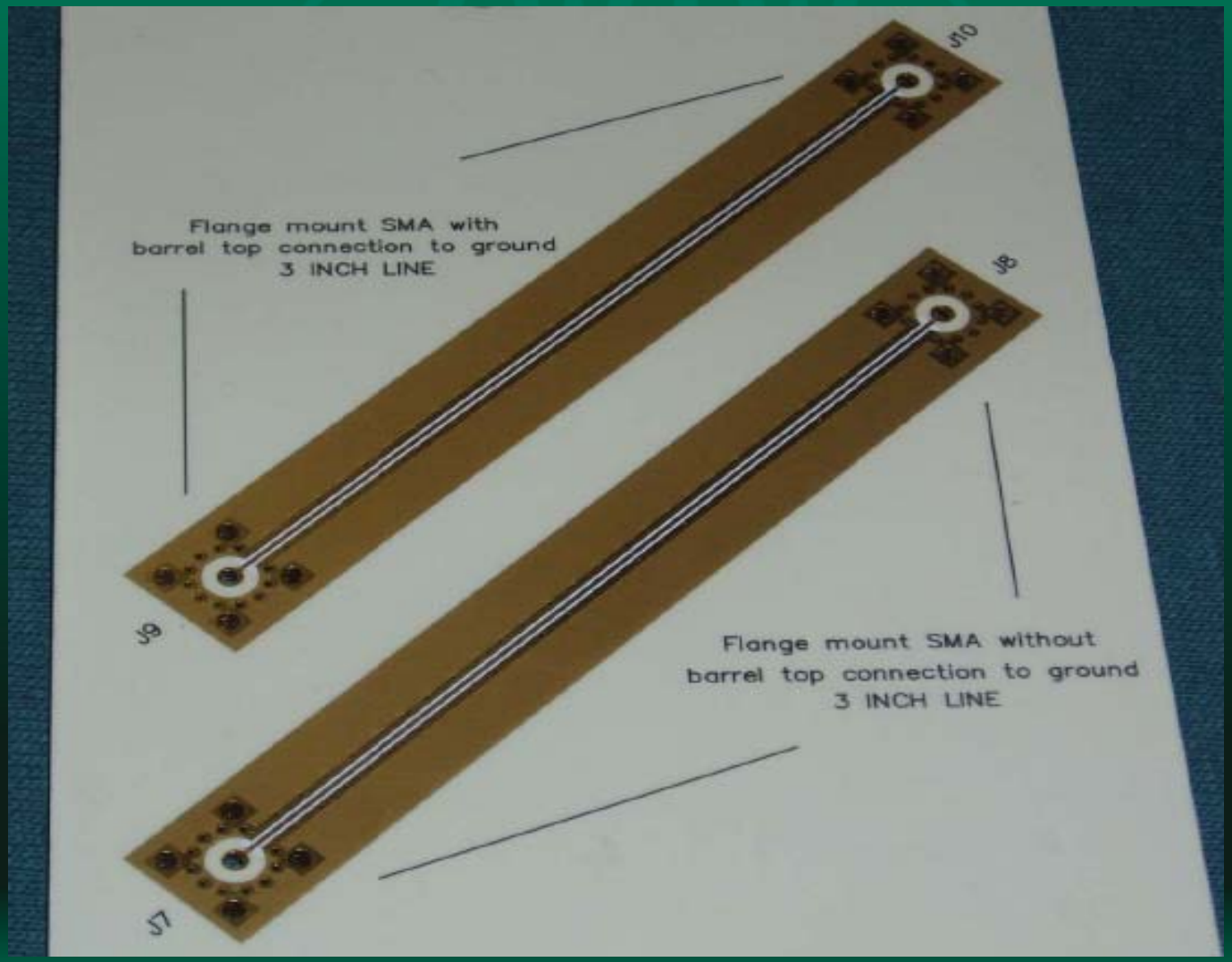




Improved Signal Return Path

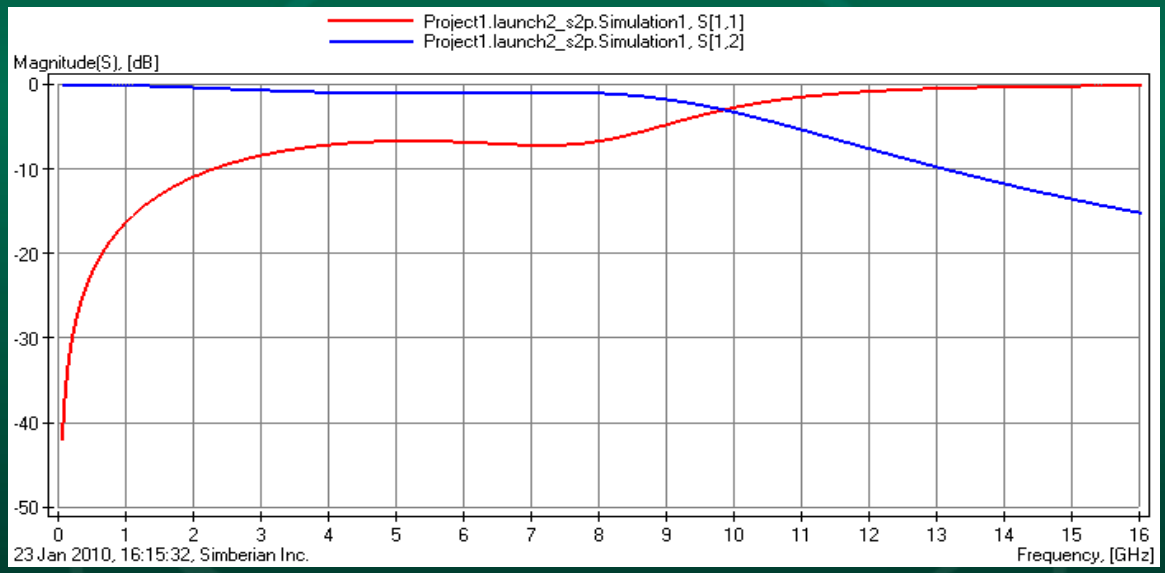
Poor Signal Return Path

SMA Launches with Co-planar Microstrips

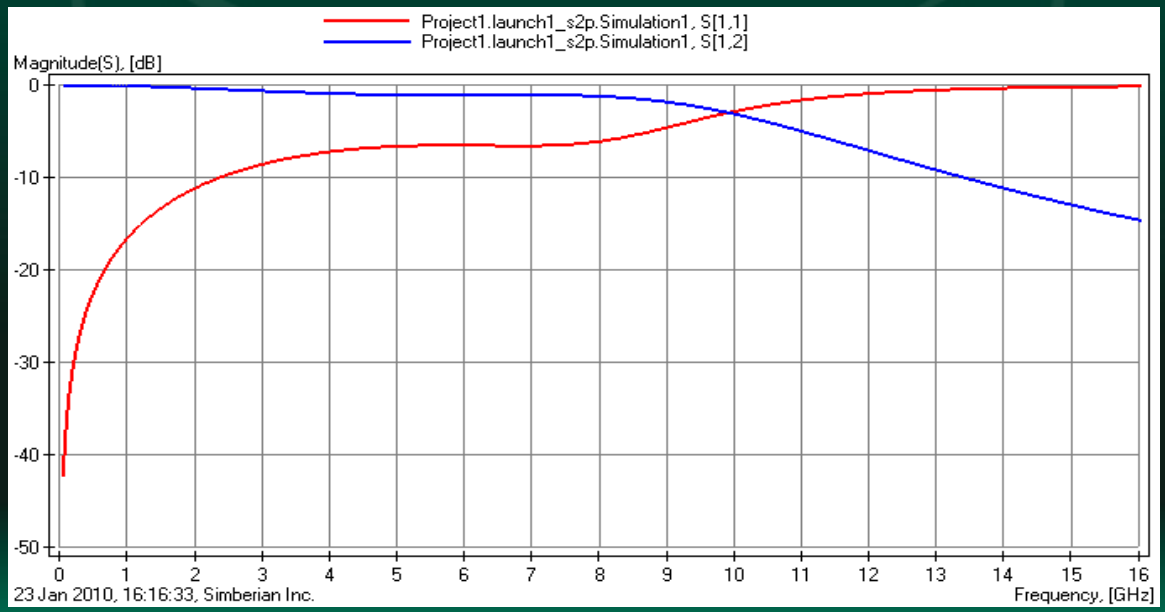


Results from 2D Modeling Tool

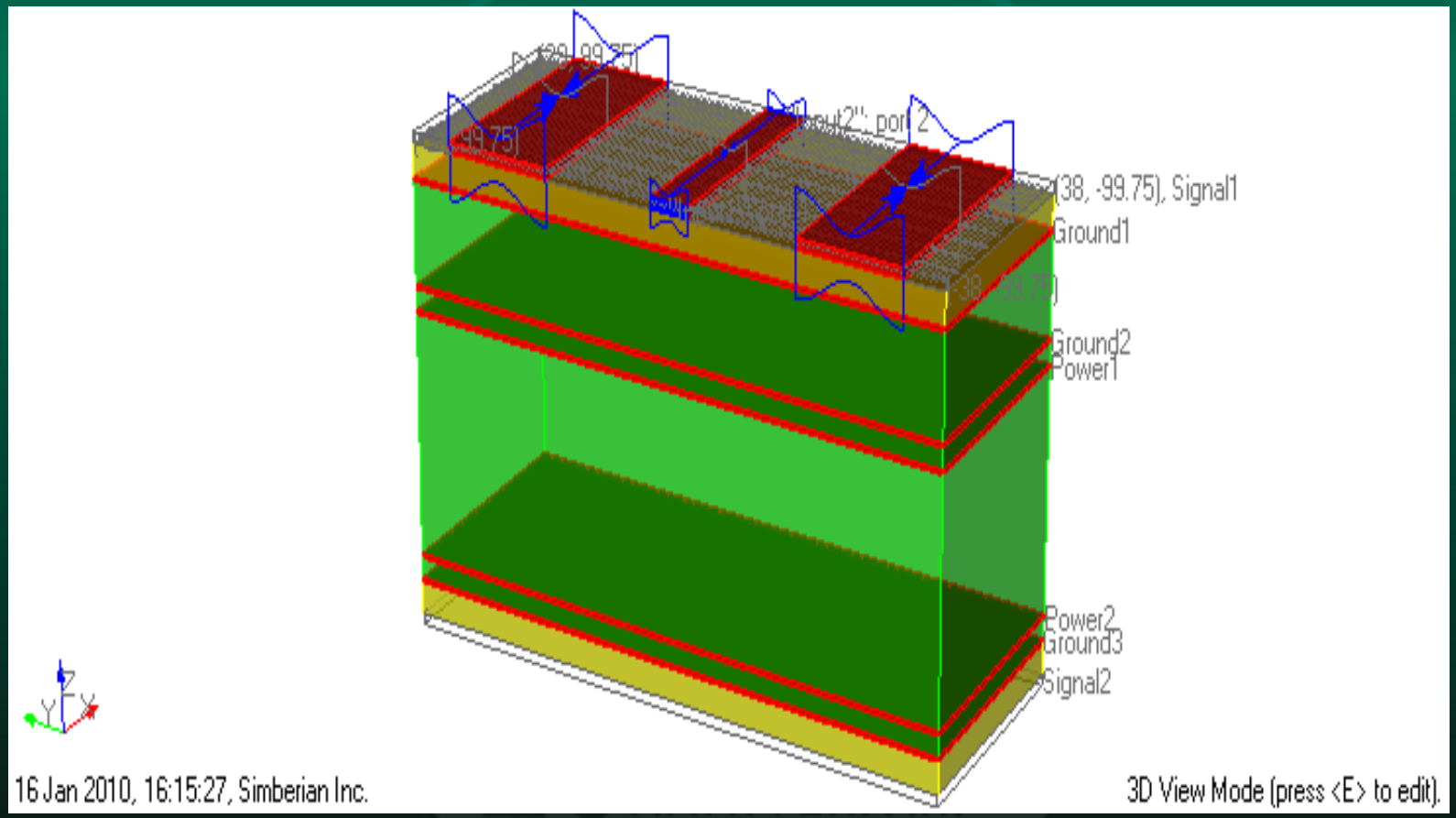
Improved Path



Poor Path

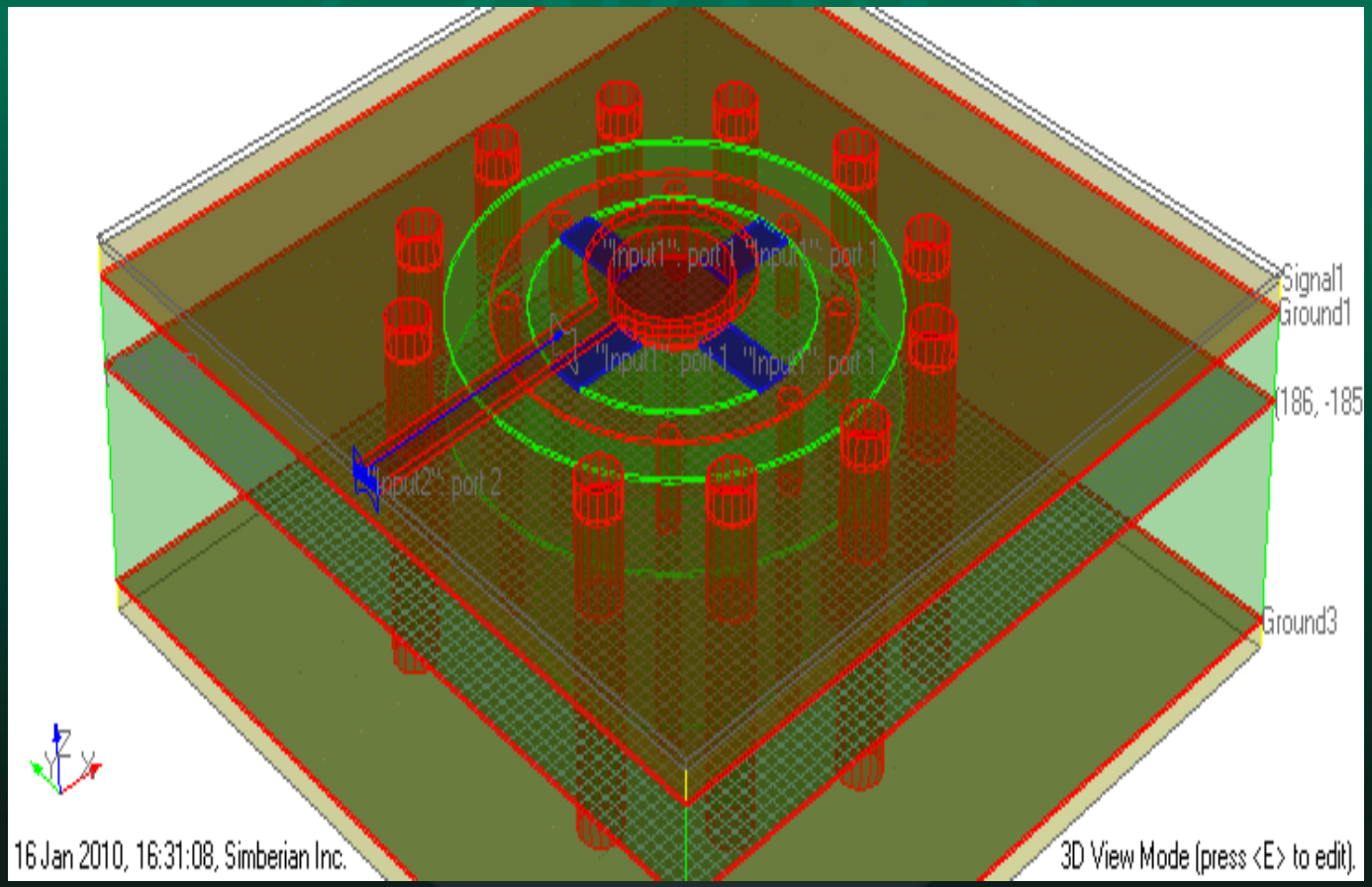


Transmission Line Simulation Geometry



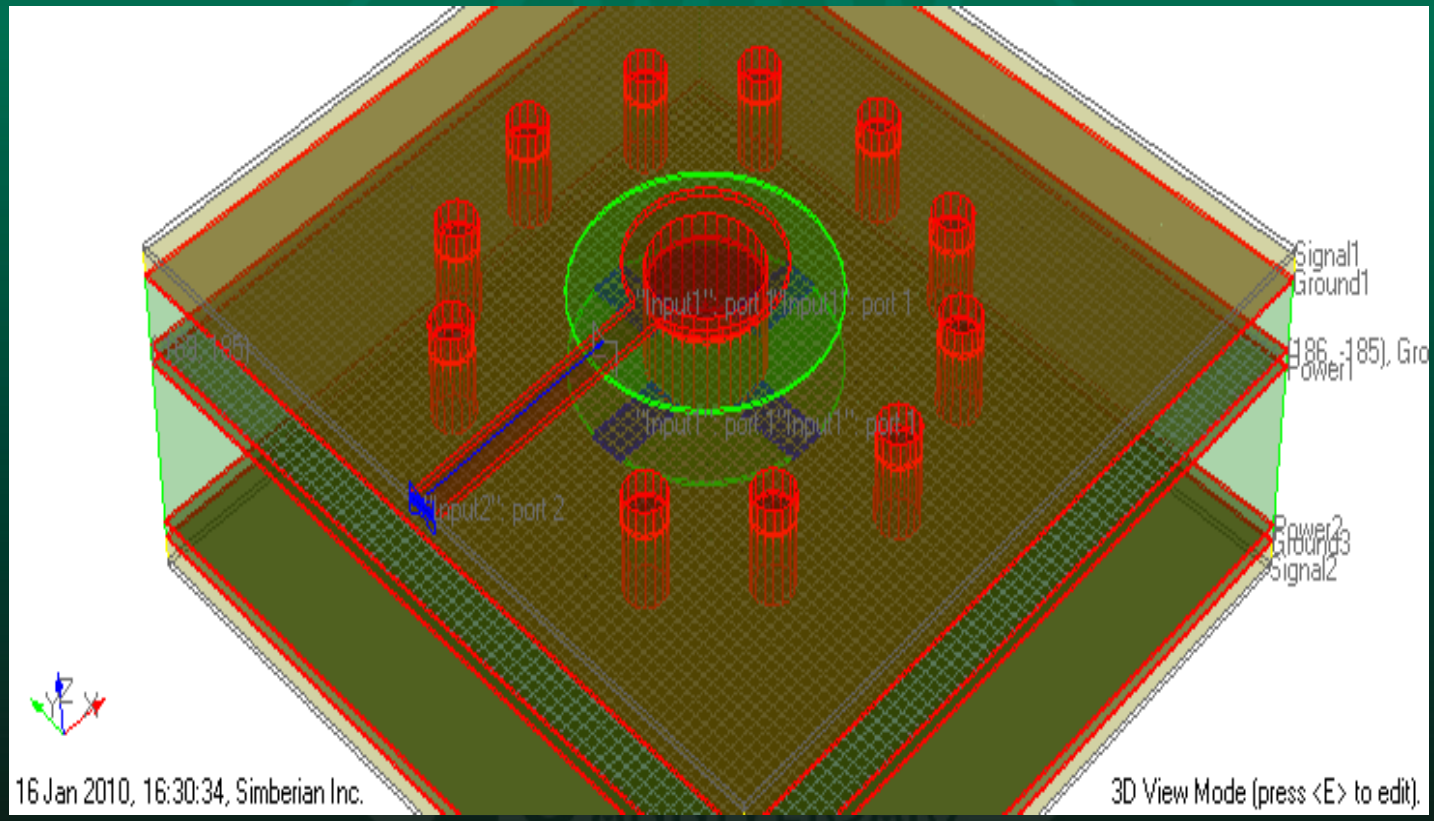
- Microstrip T-line with co-planar ground
- Reduced ground width to minimize simulation

Launch Geometry: Poor Return



Circuitous signal return path

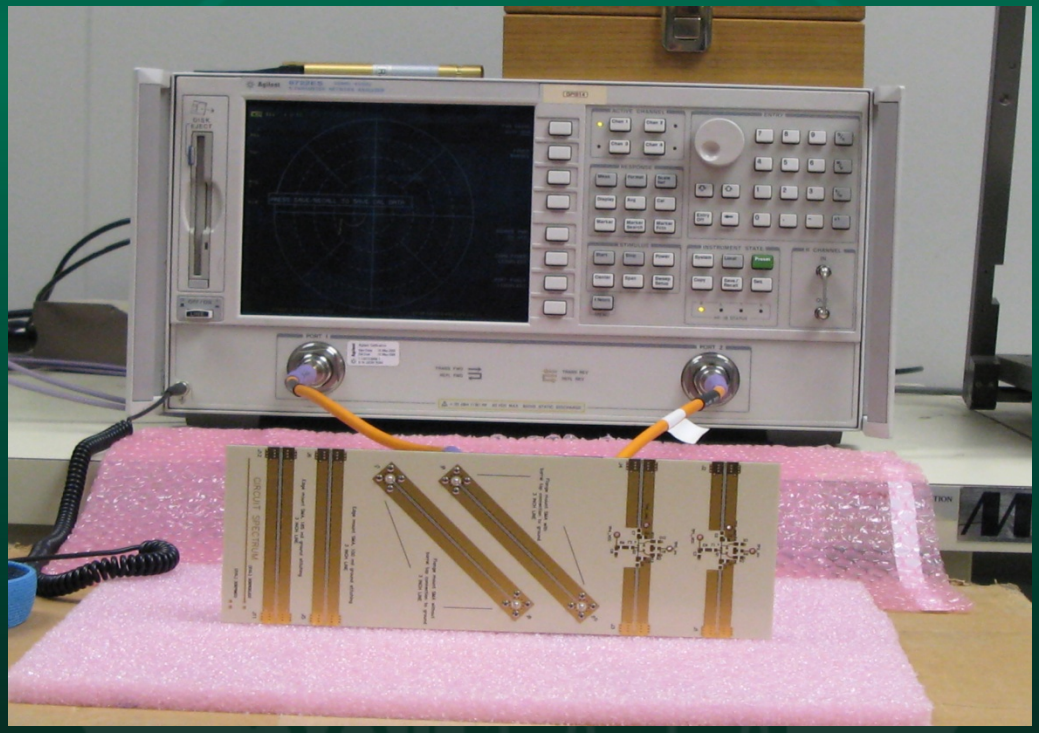
Launch Geometry: Improved Return



Direct path from Ground1 to Ground2 afforded by adding a plane to the design

VNA and Test Coupon

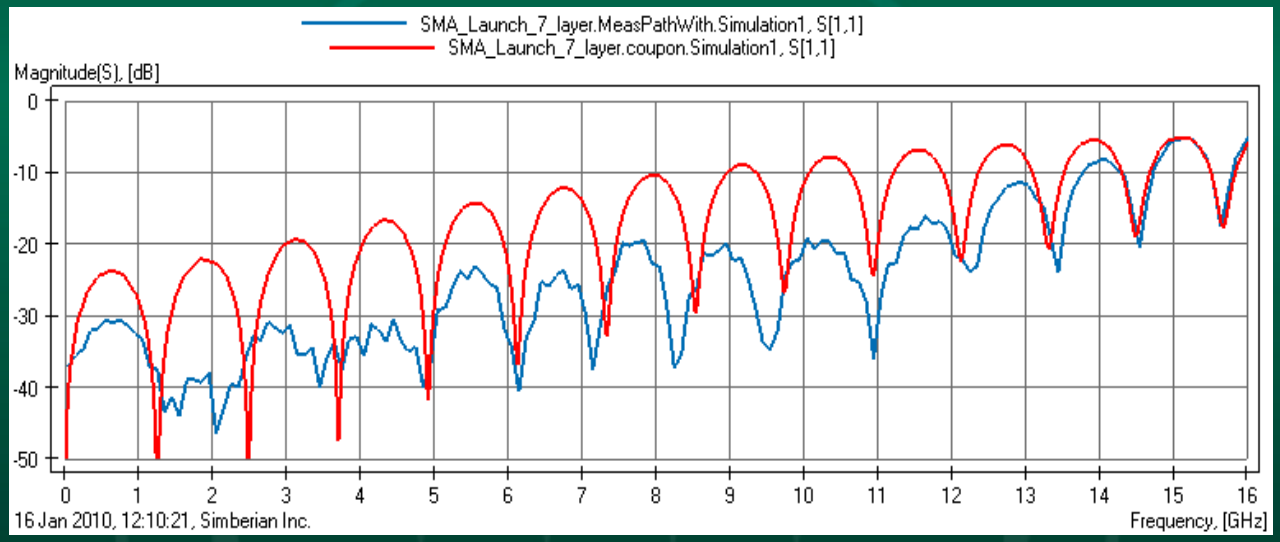
Agilent
E8722ES



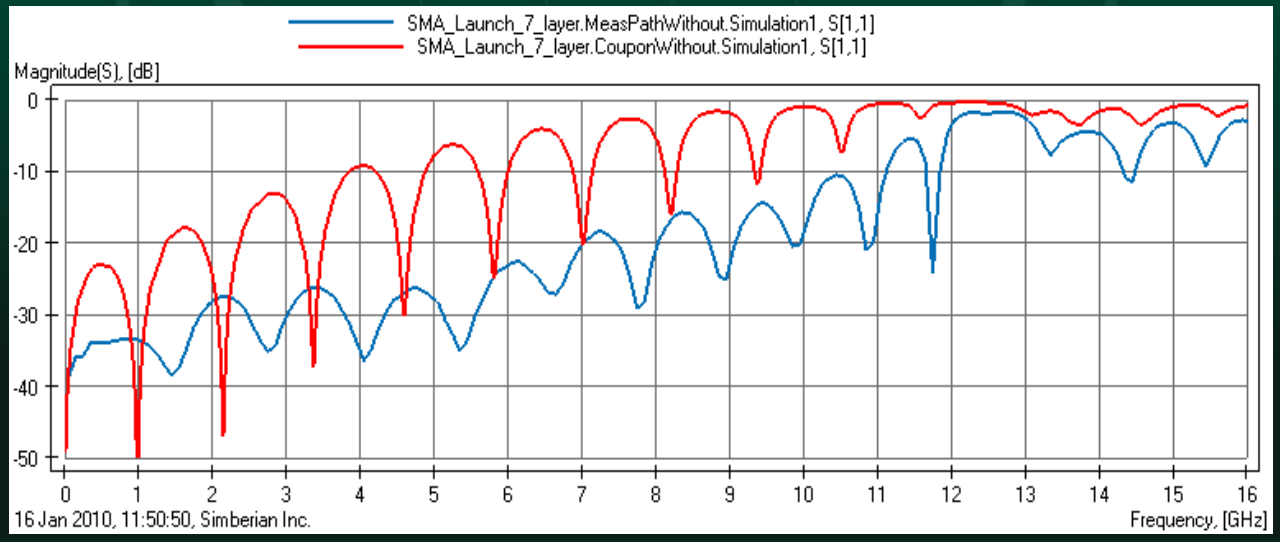
The VNA provides measured responses over a frequency range (S-parameters) that can be saved in a Touchstone file format, allowing importing into a simulator for comparison

S11 - Return Loss

Improved Path



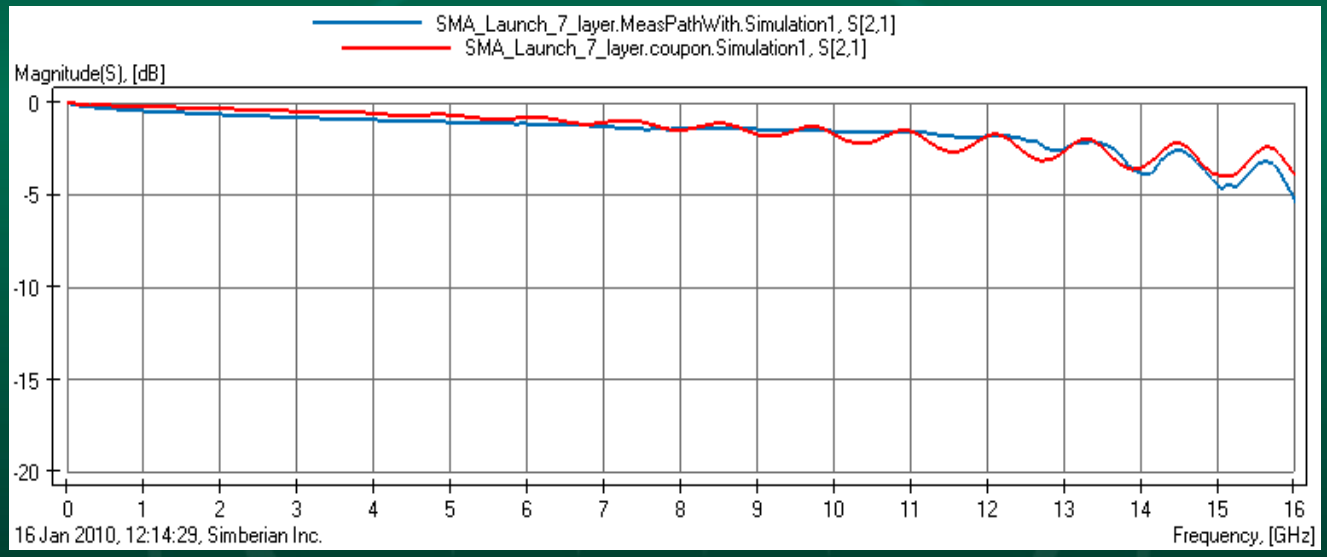
Poor Path



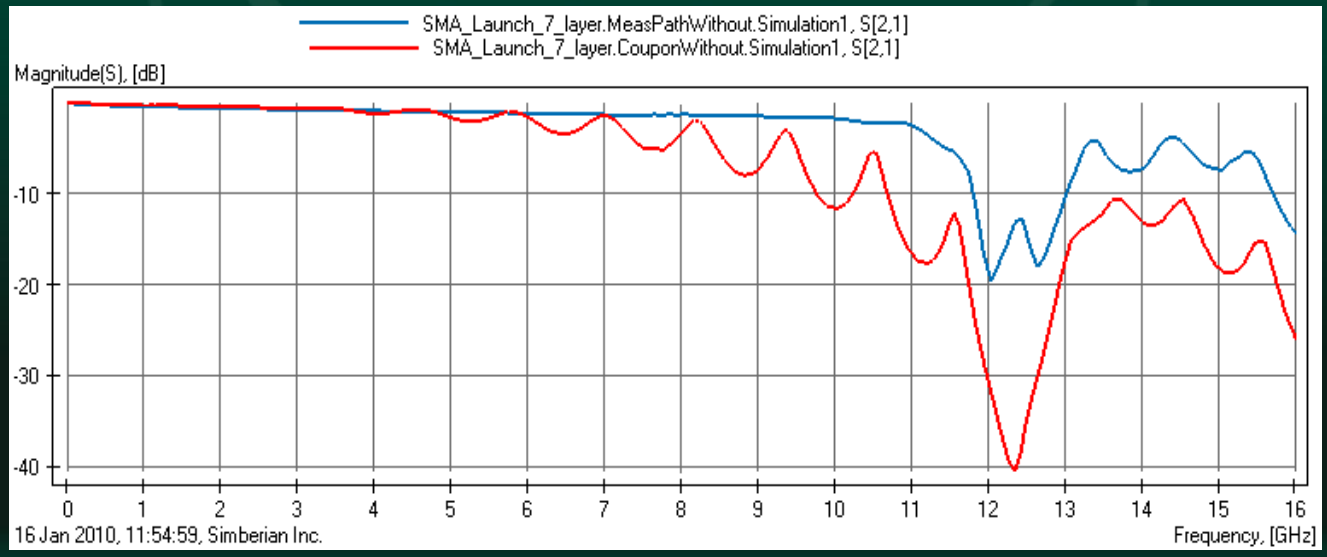
Measured response in blue, simulated in red

S21 - Insertion Loss

Improved Path

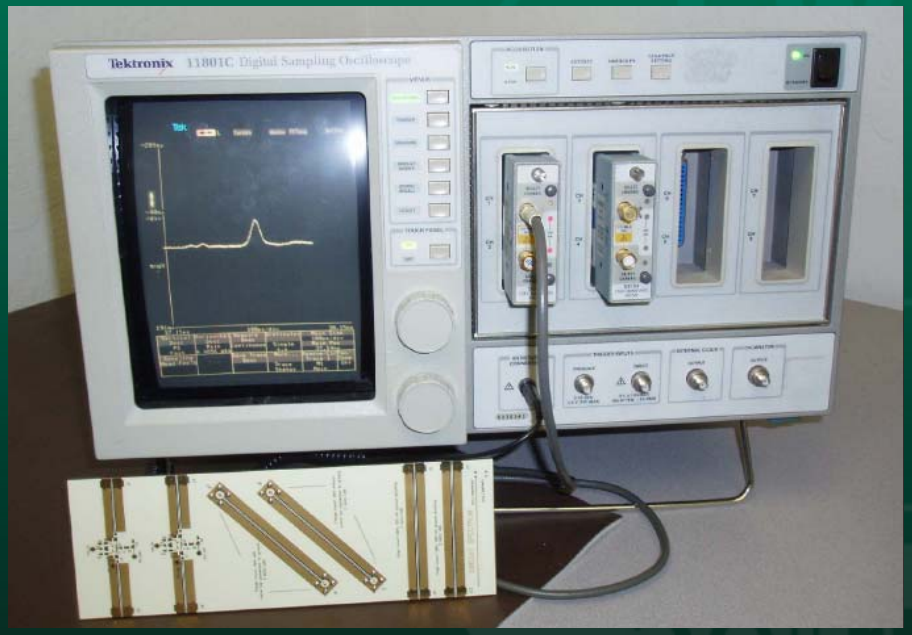


Poor Path

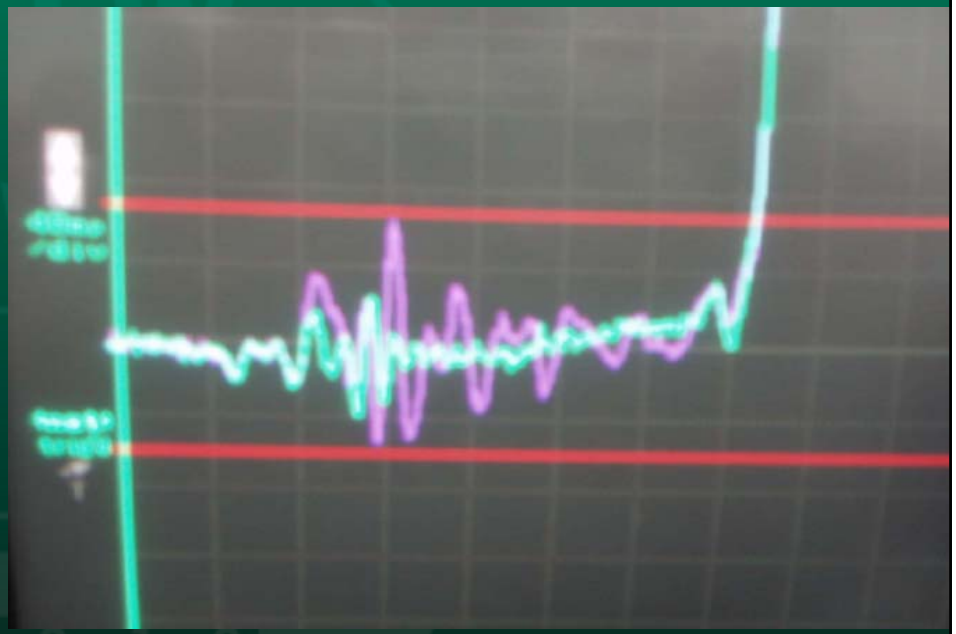


Measured response in blue, simulated in red

TDR Scope and Test Coupon



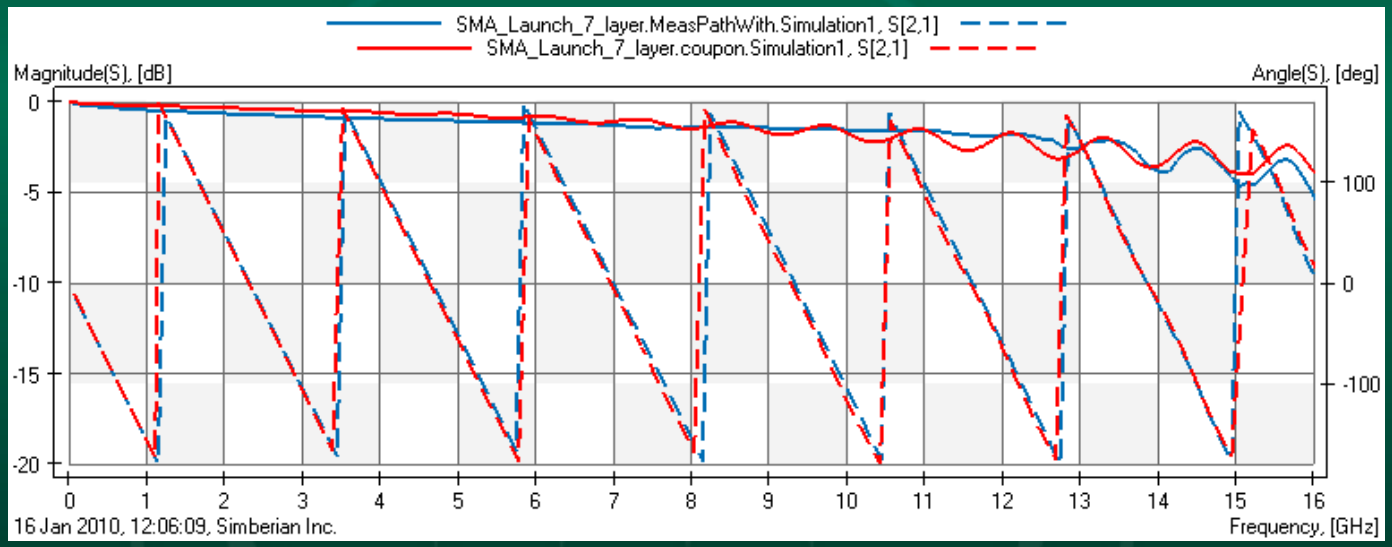
Tektronix 11801C



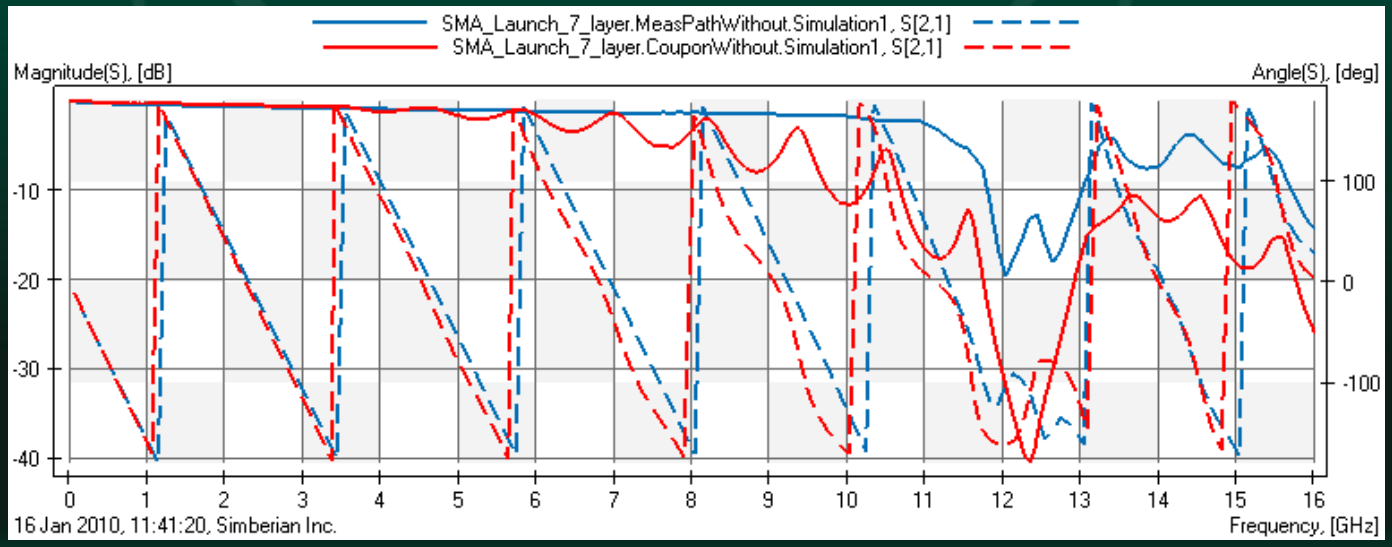
Improved path in green, poor path in purple

S21 - Magnitude & Phase Comparison

Improved Path



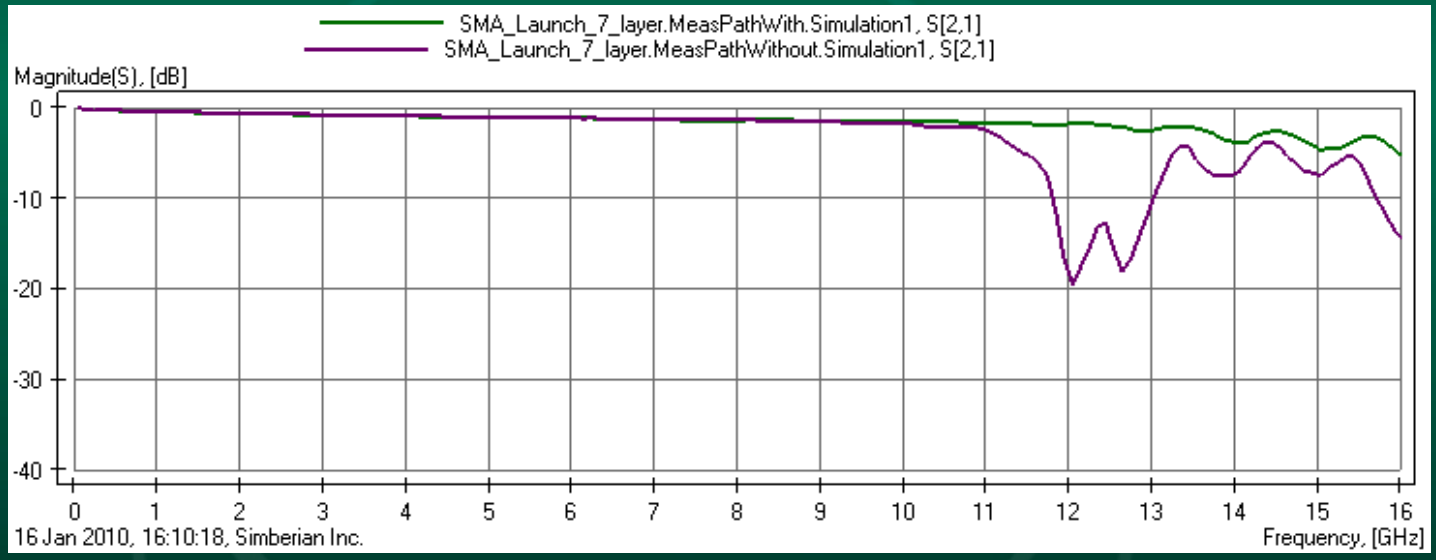
Poor Path



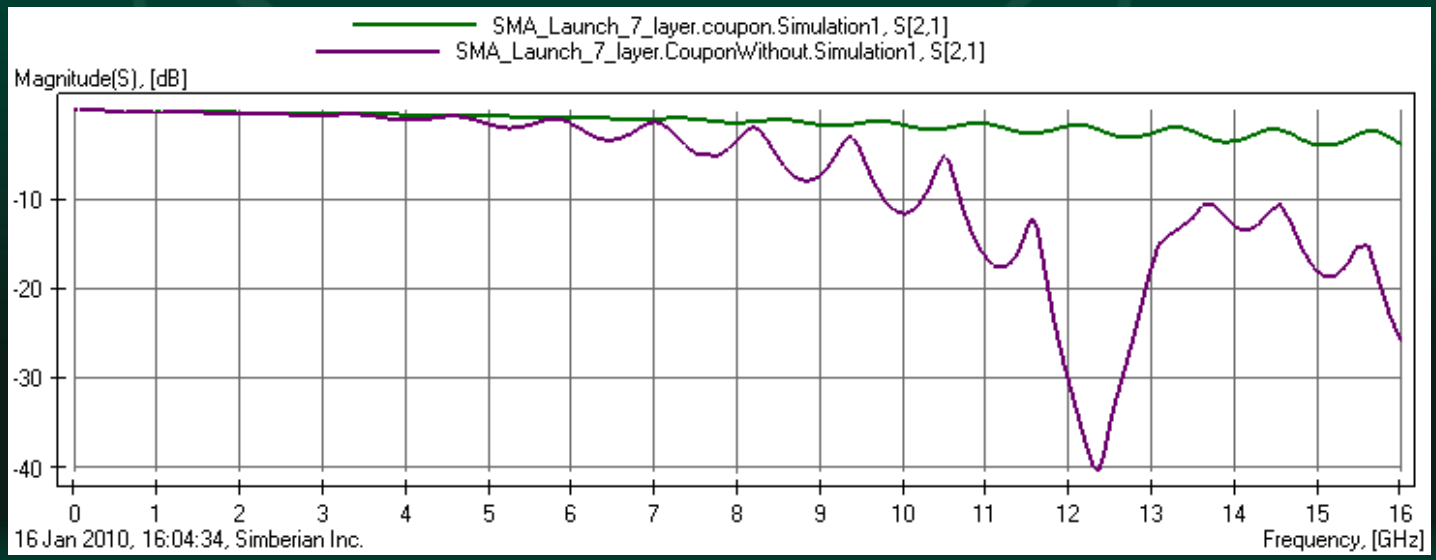
Measured response in blue, simulated in red

S21 - Improved vs Poor

Measured Data



Simulation Data



Improved path in green, poor path in purple

Conclusions

- For signal transitions through a PCB, the nature of the return path will affect performance
- Comparison of simulated and measured results shows good correlation of general behavior
- Improving the return path takes a design that is usable to 3.2 Gbps and extends it to 10 Gbps

Acknowledgement

The authors wish to thank Yuriy Shlepnev, Ph.D., President, Simberian Inc., for his valuable help and generous support throughout the process of creating this presentation.