

**IEEE SW Test Workshop**  
Semiconductor Wafer Test Workshop

June 6 to 9, 2010

San Diego, CA



# Probe Cards with Modular Integrated Switching Matrices



**Authors:**  
Evan Grund  
Jay Thomas

# Agenda

- **Review of Traditional Scribeline Parametric IV and CV Probe Card Requirements**
- **Shift Toward Fast Pulsed Characterization Of 100nS Memory, Power Transistor, and ESD Clamping Devices**
- **Scalable Solution Automates All DC and PIV Tests Within A Scribeline Test Structure**
- **Conclusions**



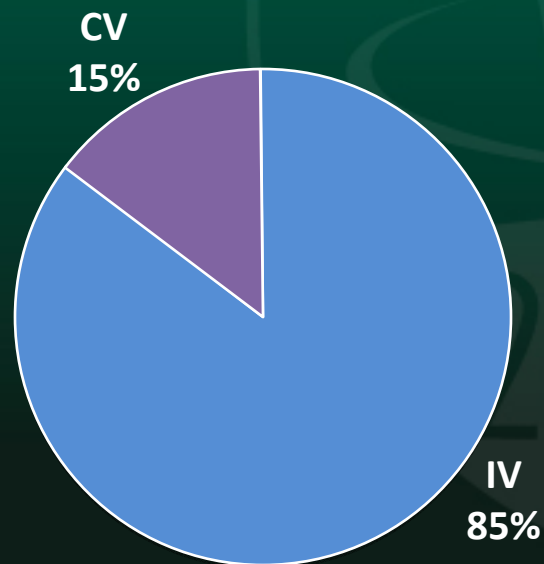
# Traditional Scribeline Probing

- **12 to 32 Pin Complexity**
  - Trend toward fine-pitch in-line structures
- **IV and CV Using a 10 MHz Bandwidth Matrix**
  - External matrix works well for bench top characterization
- **PIV Is Very Limited**
  - Pulse widths to 1uS
  - Pulse amplitude to 40V (high impedance DUT)
  - Pulse power limited to a few Watts

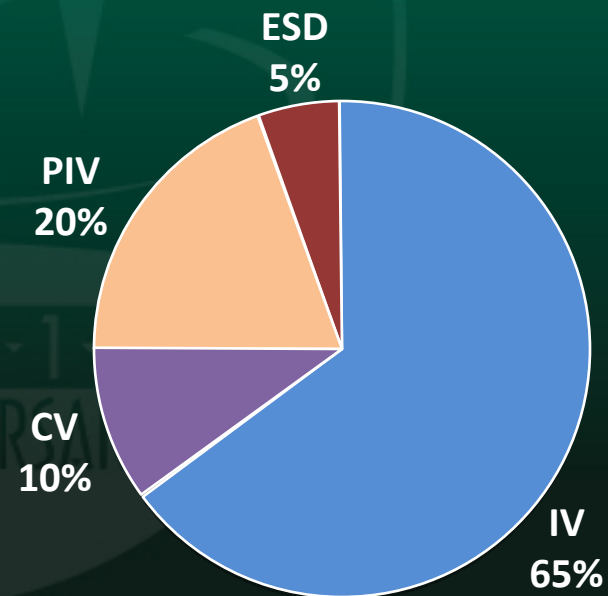


# Evolving Parametric Test

**1990's Traditional DC Para**  
10 MHz Matrix Required



**2010's Expanding to HF Para**  
1 GHz Matrix Required



# Parametric Test Bandwidth

- Matrix is 5x to 10x Bandwidth of Device Test Freq.

Type	Device	Freq	Matrix	Test Name
IV	Transistor	1 MHz	10 MHz	Vt, Gm, Vsat, BV, IDVD, IDVG, Gate & Drain Leakage, V-ramp, J-ramp, TDDDB, HCI, Charge Pump, EM
CV	Transistor Oxide	1 MHz	10 MHz	Thick Gate Tox, Field Tox, Diffusion Profiles, Trapped Charge, Mobile Ion, C-gate, C-drain
HF-CV	Transistor Oxide	100 MHz	1 GHz	Thin Gate Tox, Carrier Life Time, Contamination
PIV	Transistor	200 MHz	1 GHz	Vt, Gm, Vsat, IDVD, IDVG, Gate Charge, Trapped Charge
ESD	ESD structure	200 MHz	1 GHz	TLP, HBM, MM, HMM (IEC 61000-4-2) waveforms, CDM stress pulse failure, PIV & leakage curves
Flash R-ram	Transistor Resistor	200 MHz	1 GHz	State 0-State 1 Programming Current/Time, Read Leakage Current



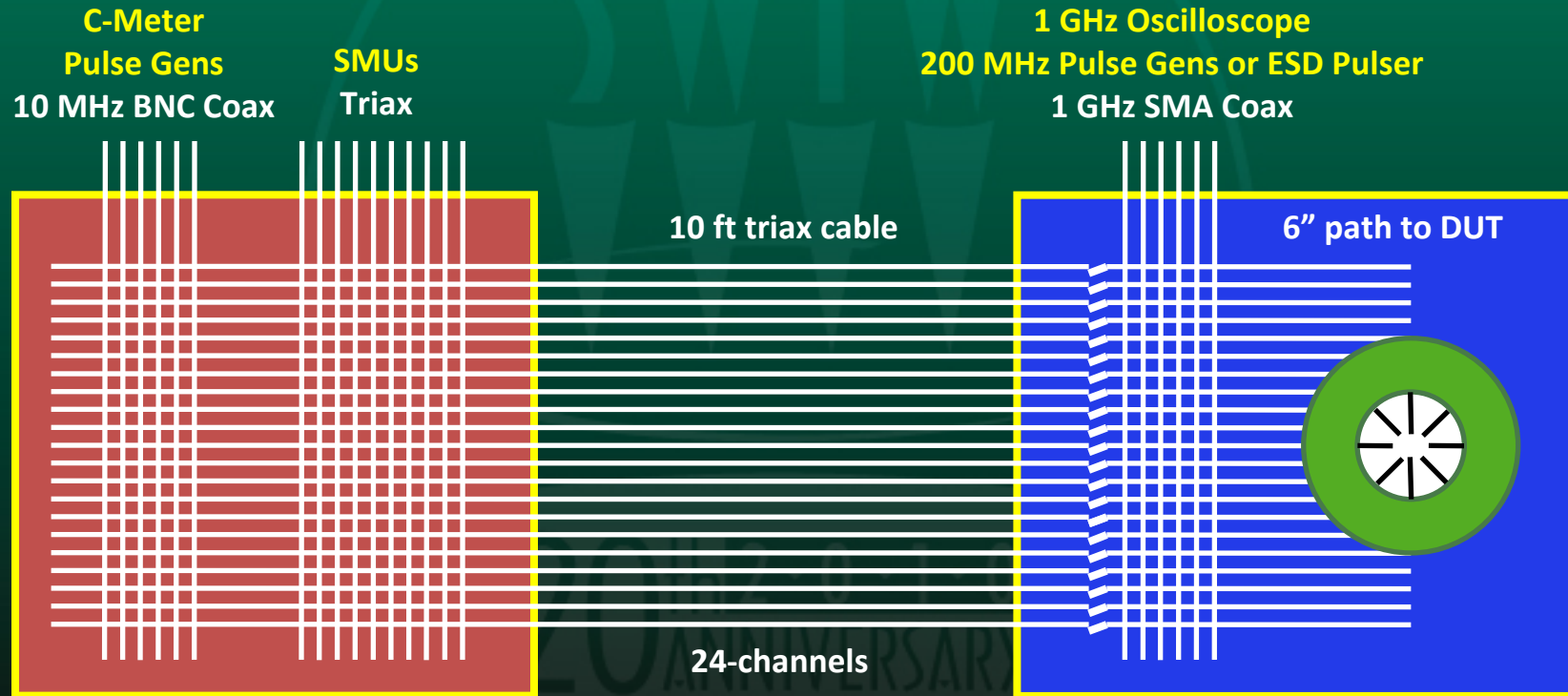
# Wafer-Level 1 GHz Matrix Challenges

- I/O paths needs need to be very short (inches)
- Must easily fit onto standard analytical probers
- AC Kelvin required for high current PIV
- 100 pA-level DC leakage desirable
- All resources should MUX to all TEG pins
- Support of legacy DC Analyzers is important
- High uptime, quickly configurable
- Modular, adaptable, extendable, and reusable



# Genus 1GHz Matrix/Probe Card

- Supports legacy DC; adds short HF paths



**DC Equipment Matrix**  
Keithley K707A  
or  
Agilent B2201A

**GTS Genus Wafer-Level Matrix**  
Integrated Probe Card  
200 MHz using wire needles  
1 GHz using 50Ω ceramic blades



June 6 to 9, 2010

IEEE SW Test Workshop

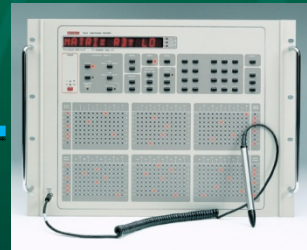
7

# 24 Pin DC + ESD Automation

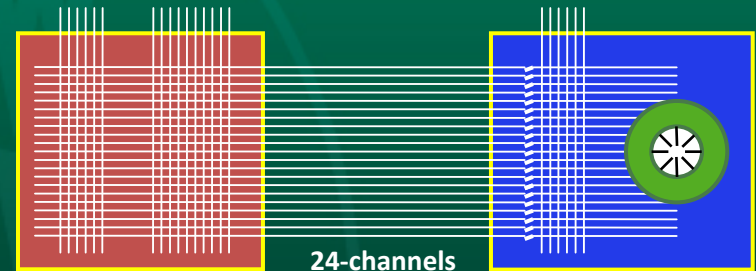
- Leverage Legacy DC Software Platform



Agilent 4156  
Semiconductor  
Parameter Analyzer



Keithley 707 Low  
Leakage Matrix



DC Matrix

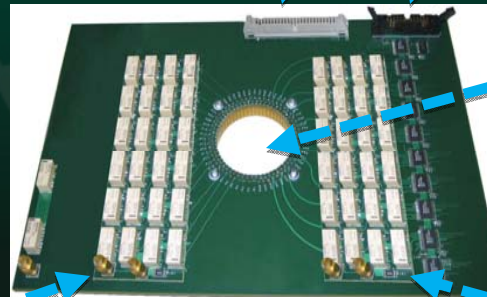
24-channels

Genus

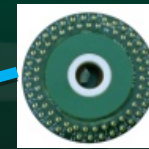
USB Relay Control + Power



ESD Test System

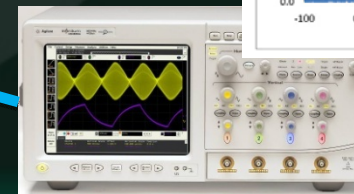
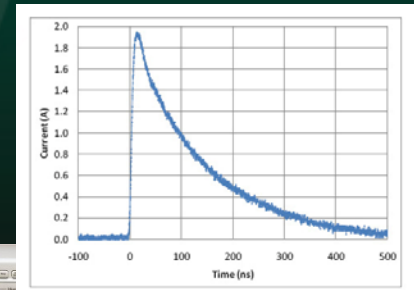


Genus 1 GHz Pin Expander



Low Cost  
Probe Card

2 Amp 500nS  
HBM Waveform at DUT



Agilent  
Oscilloscope



June 6 to 9, 2010

IEEE SW Test Workshop



# 24 Pin DC + PIV + HF-CV Automation

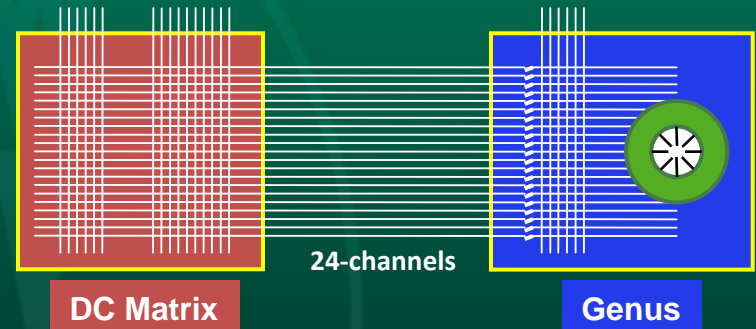
- Leverage Legacy DC Software Platform



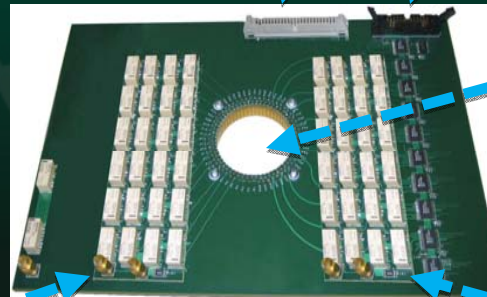
Agilent Semiconductor Device Analyzer



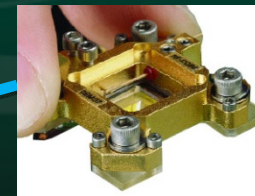
Agilent Low Leakage Matrix



USB Relay Control + Power



Genus 1 GHz Pin Expander



HF Probe Card



HF CV-Meter



Pulse Generator

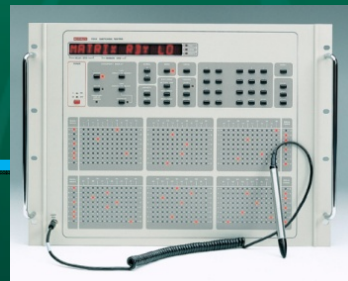


# 24 Pin DC + Power PIV Automation

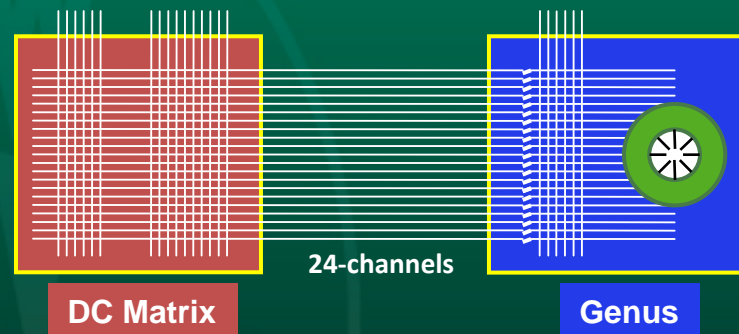
- Pulsing down to 200nS Widths at 10 Amps



Keithley Semiconductor Characterization System



Keithley Low Leakage Matrix



DC Matrix

24-channels

Genus

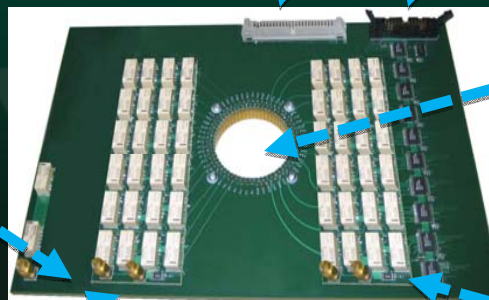
USB Relay Control + Power



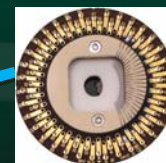
Gate Pulse Generator Avtech 10W-100V



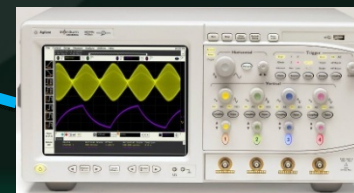
Drain Pulse Generator Avtech 10W-600V



Genus 1 GHz Pin Expander



Celadon High Temp Probe Card



Agilent 1 GHz 4-Chan Oscilloscope



June 6 to 9, 2010

IEEE SW Test Workshop

10

# 24 Pin DC + Memory PIV Automation

- nA level currents using 14-bit AC digitizers



# Feature of Modular Probe Card Switching Matrices

- **Motherboard – daughter board concept**
- **Reconfigurable & expandable daughter boards**
- **Designed to adapt to future test needs**
- **Small foot print for existing probe card holders**



# Motherboard Components

- **Holds the needle assembly and two stacks of daughter boards**
- **Microcontroller for overall control**
- **Interconnects**
  - Standard replaceable probe needle assembly
  - 50-ohm connectors to daughter boards provide high frequency signal paths
  - 12 V DC power routing for relays
  - USB control cable to controlling computer

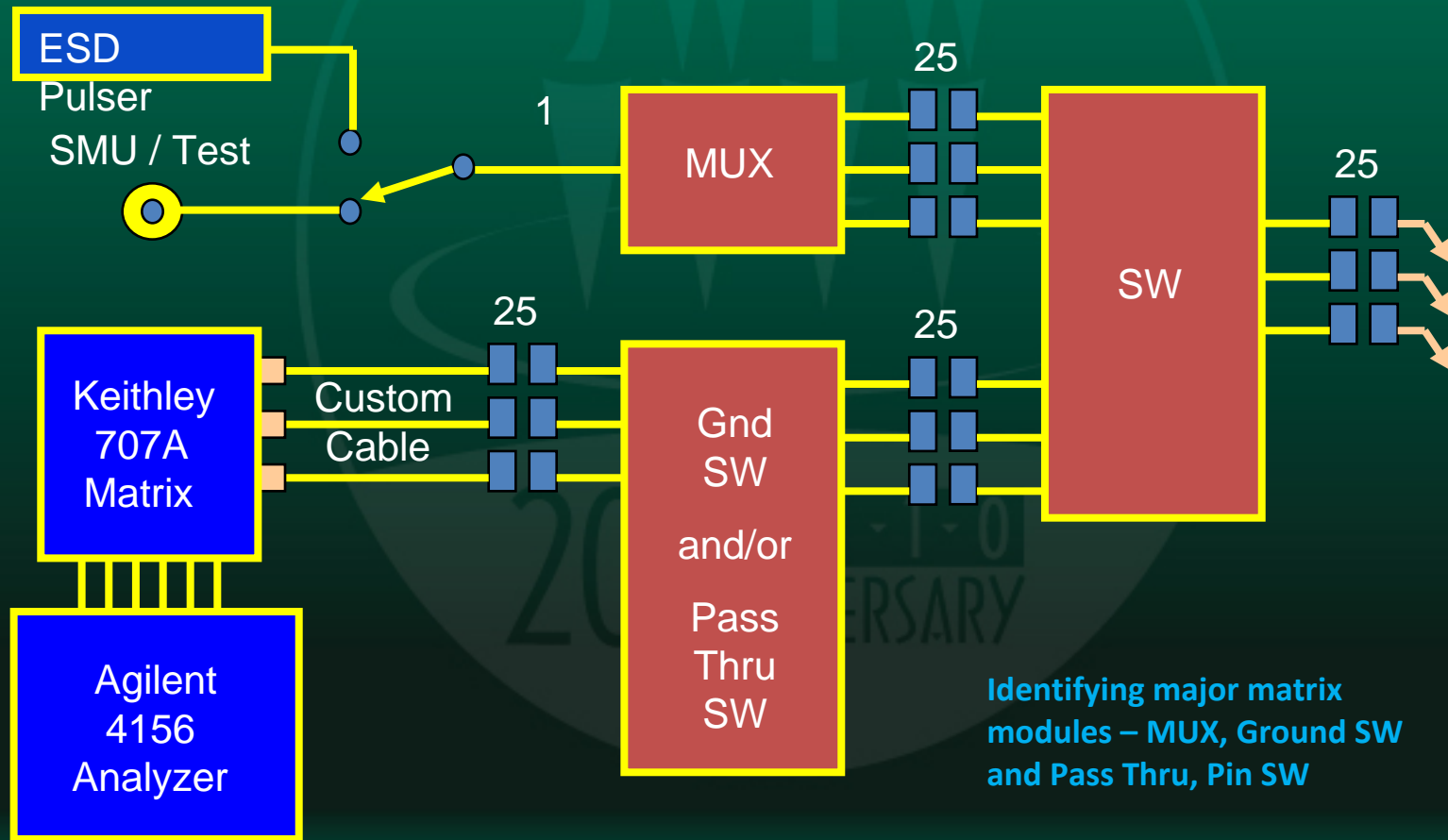


# Daughter Board Components

- **Approximately 25 relays and their drivers**
- **Local Microcontroller**
- **SMA connectors for input/output pulses**
- **Parallel cable connectors for DC signals**
- **Special Connectors**
  - Mechanical support for daughter boards
  - 2 sets of 25 signals  
(allows grouping of daughter boards)
  - Power for relays and electronics

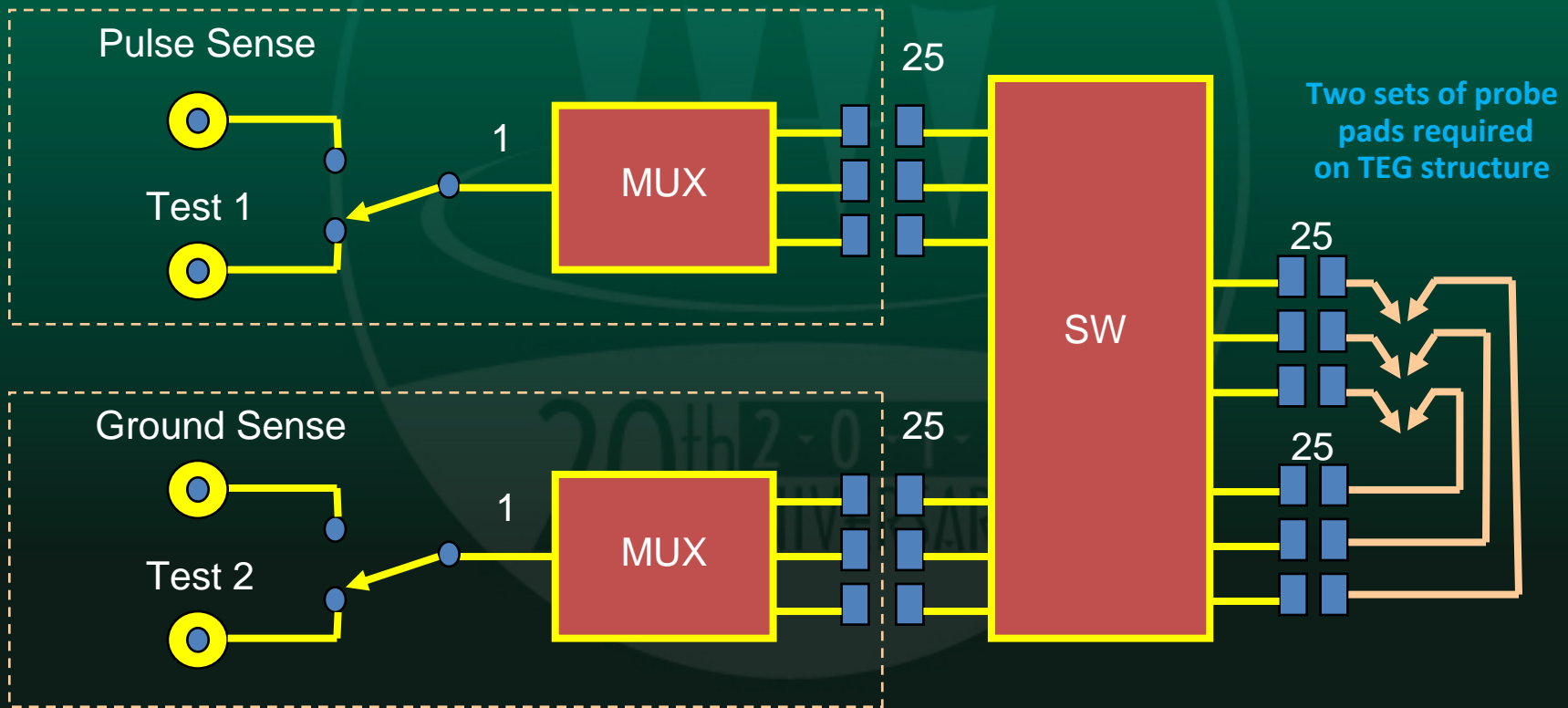


# ESD Pulse Delivery With Full DC Parametric Analysis



# Kelvin Sensing

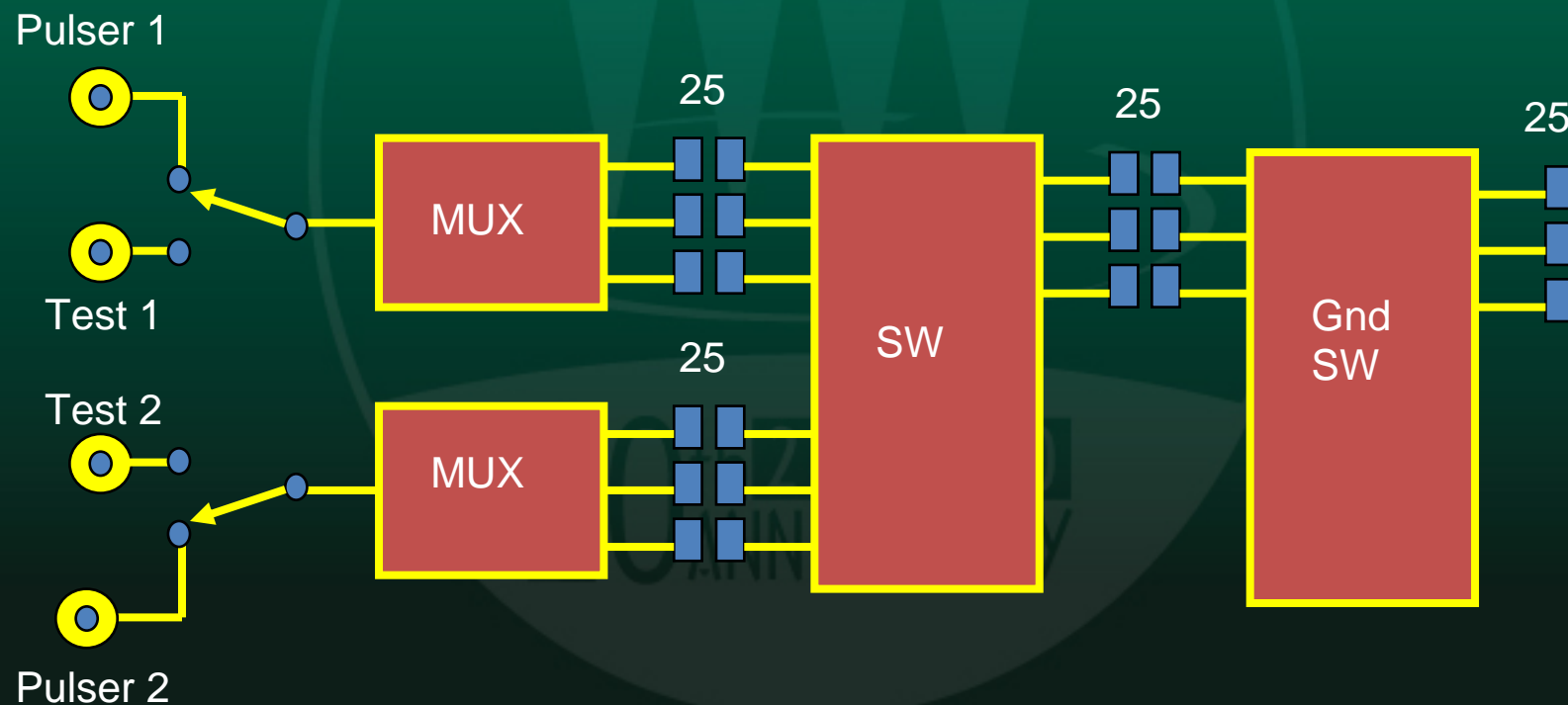
- 2 Daughter Boards Allow AC Kelvin Sensing





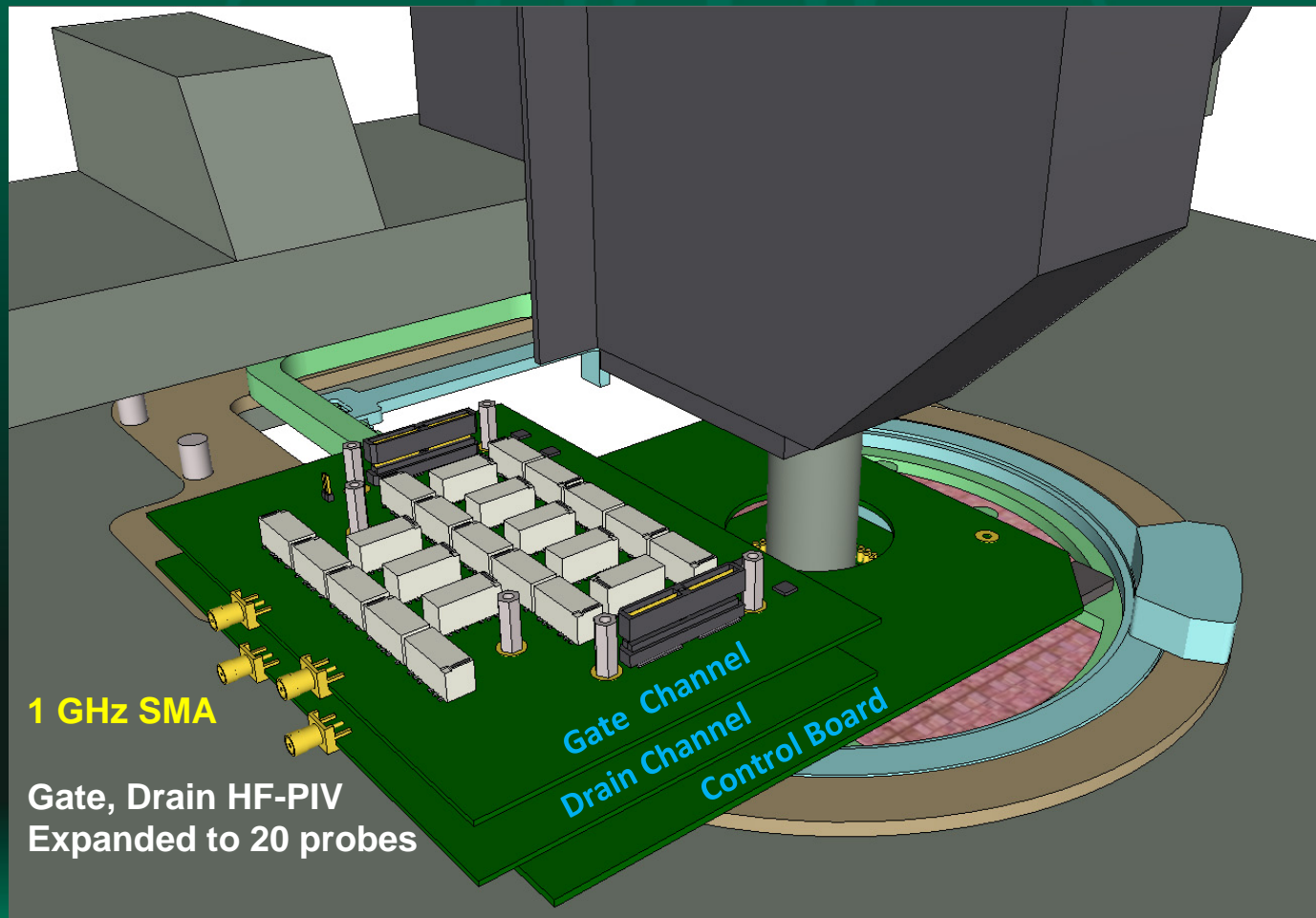
# Expanding Auxiliary Pulsers

- Additional pairs of SW and MUX boards allow expanding the number of pulsers



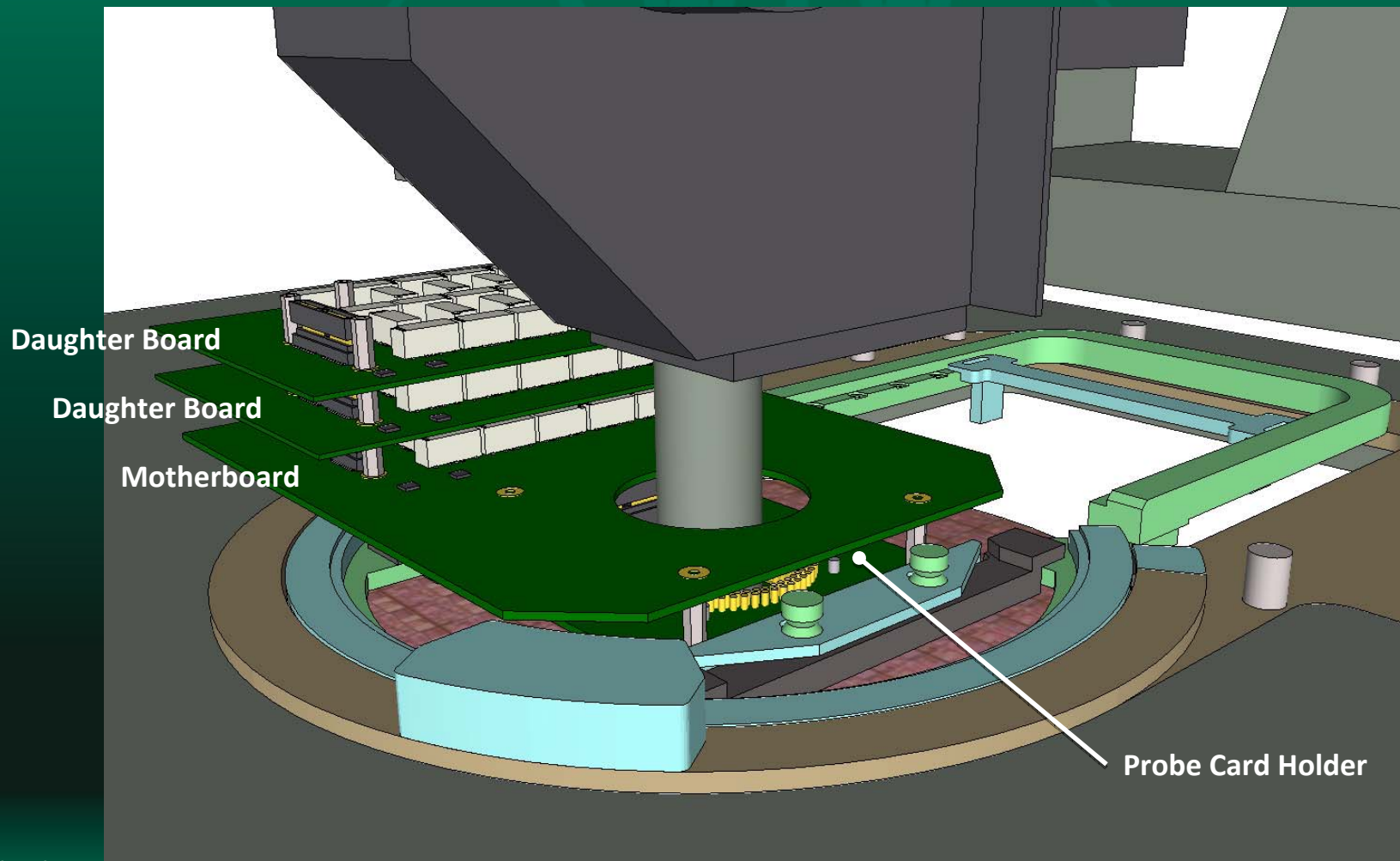
# Genus Modular Matrix Boards

- Transistor PIV example with synchronized gate/drain pulsing
- Add an additional matrix board for AC Kelvin sensing on drain



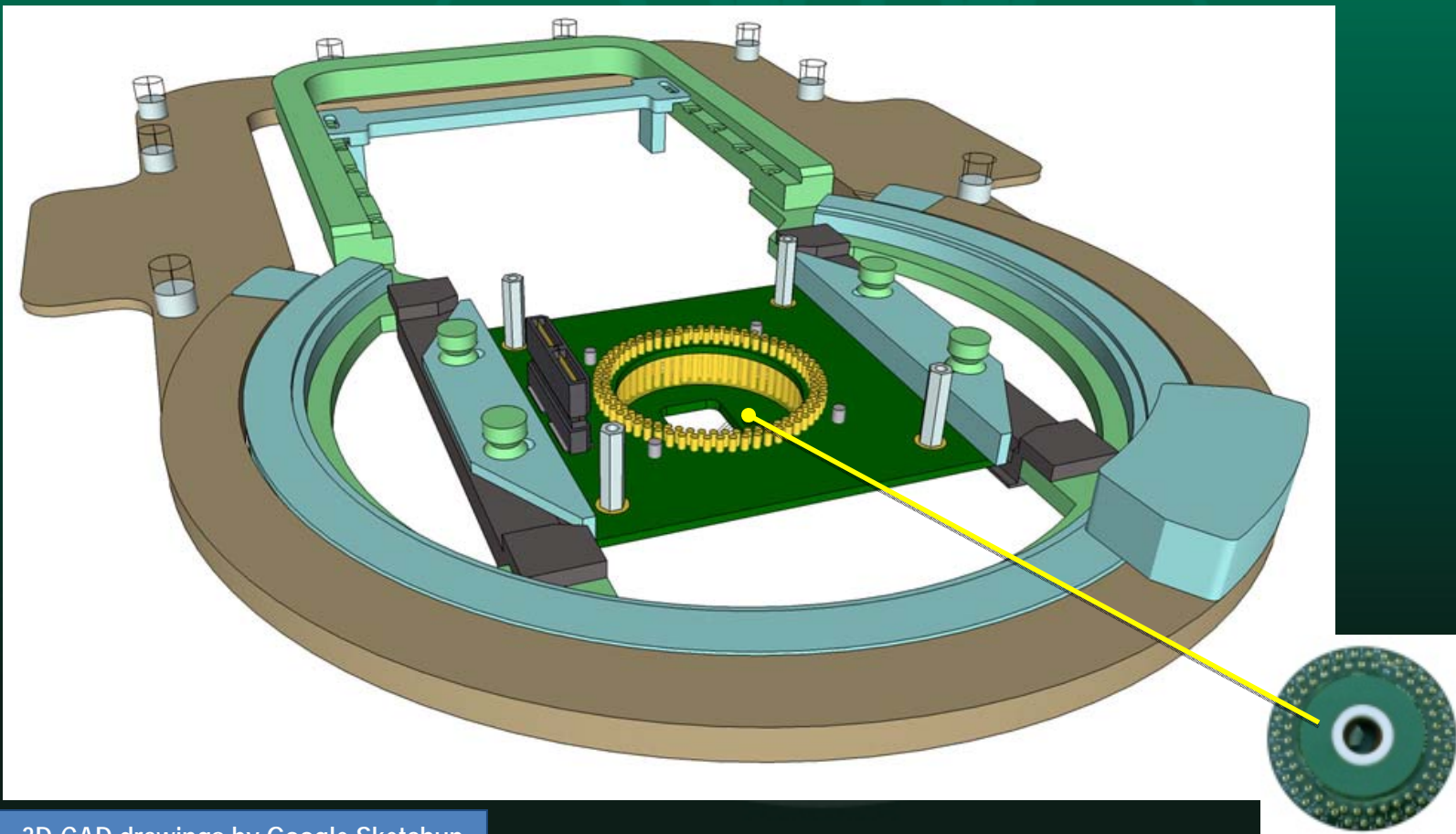
# Genus Modular Matrix Boards

- View showing how the boards stack on top of each other



# Genus Modular Matrix Boards

- View showing donut probe card mounted in card holder



3D-CAD drawings by Google Sketchup

Standard C60  
Donut Probe Card



June 6 to 9, 2010

IEEE SW Test Workshop

20

# Software

- **Genus application SW is developed in Microsoft C#**
- **Can be integrated with Microsoft Languages**
  - C++
  - Visual Basic
  - .NET Framework languages
- **GTS supports popular parametric test shells**
  - Prober control suites such as Cascade Nucleus and Suss Prober Bench
  - Parametric test productivity suites such as Metrics ICV, Keithley ACS, and Agilent Easy Expert
  - Customer's legacy parametric test SW platforms



# Conclusions

- **Scribeline parametric test is evolving toward HF PIV**
  - Many of these tests are not automated for full TEG testing
- **A probe card with integrated and modular switching matrices can address most of the HF PIV challenges**
  - GENUS is a very flexible “next generation” probing system
  - The modular design allows hundreds of configurations
  - Configure motherboards to meet current expected needs
  - Add daughter boards as applications grow

