Backend to the Front Line

Semiconductor Wafer Test Workshop
San Diego
June 12, 2011

William Chen

ASE Fellow

Senior Technical Advisor

ASE Group

CPMT Distinguished Lecturer

Greetings from the IEEE Components Packaging & Manufacturing Technology Society (CPMT)

We wish you great success in the SWTW Workshop

Very best wishes from engineers and scientists at the ASE Group worldwide

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Outline

- History
- Market Landscape
- Game Changing in the Backend
- SIP & 3D
- Food for Thought

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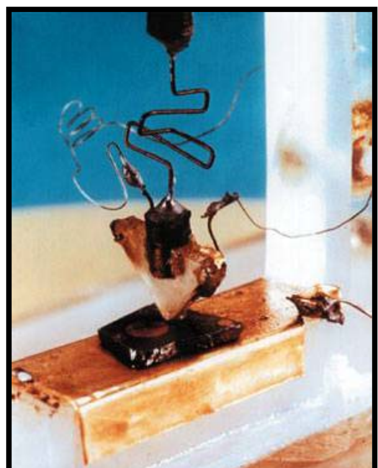
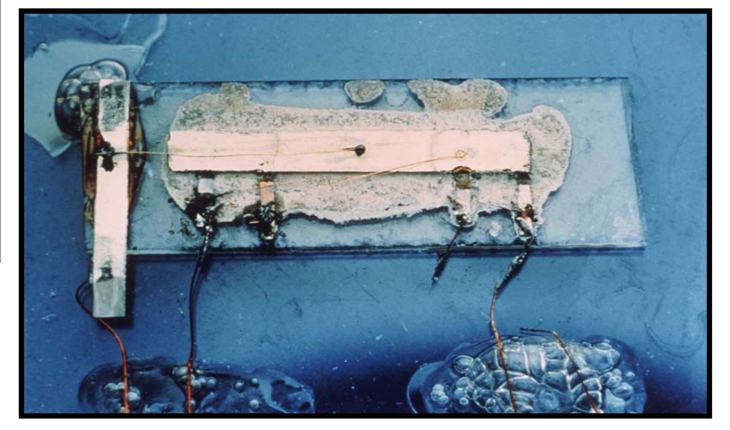
The Early History of the Industry

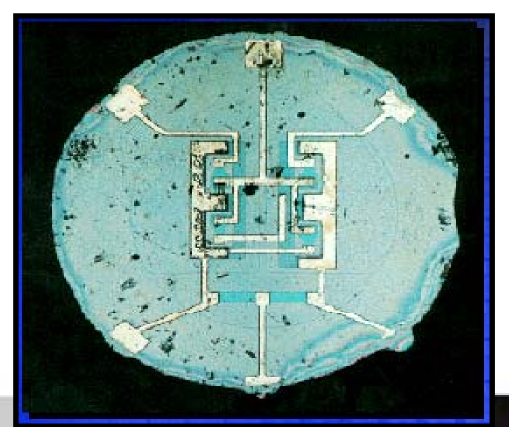


First Transistor
John Bardeen, Walter Brattain, William Shockley 1947



First Integrated Circuit

Jack Kilby 1958



First Planar Integrated Circuit

Robert Noyce 1959

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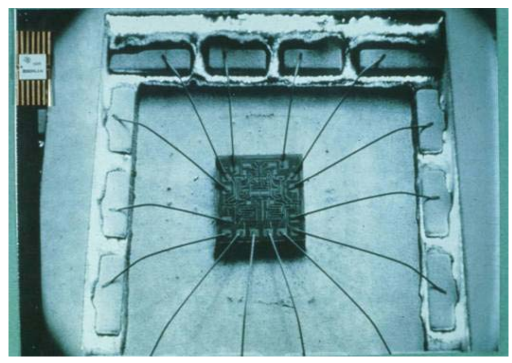
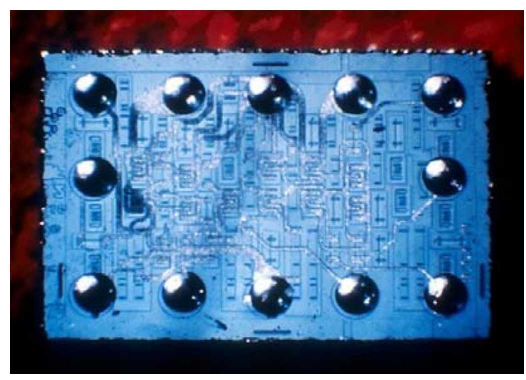
Workhorses for Back End Industry



Au Wirebond – 1967
Source: George Harman



C4 Solder Bump 95/5 Assembly
1970 Paul Totta

Au wirebond and Solder flip chip have been the work horses of the IC packaging industry, since the dawn of integrated circuits.

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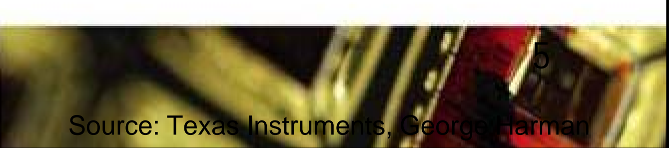
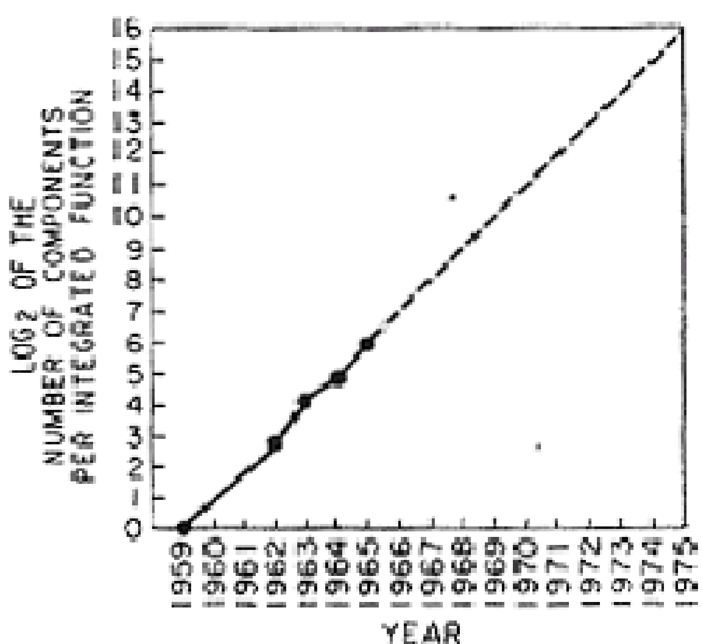


Source: Texas Instruments, George Harman

Moore's Paper

"Cramming more components onto integrated circuits"

Gordon Moore Electronics, Volume 38, Number 8 April 19, 1965



"The future of integrated circuits is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas. "

"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves towards the production of larger and larger circuit functions on a single semiconductor substrate."

Moore's Law

Scaling

Lowering Cost

Driving Innovation

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Moore's Law

Moore's Law is NOT a Law of Nature

It is an Expectation of

Continuity of Innovation & Invention

It is a Promise of the Innovation and creativity of our profession & our industry.

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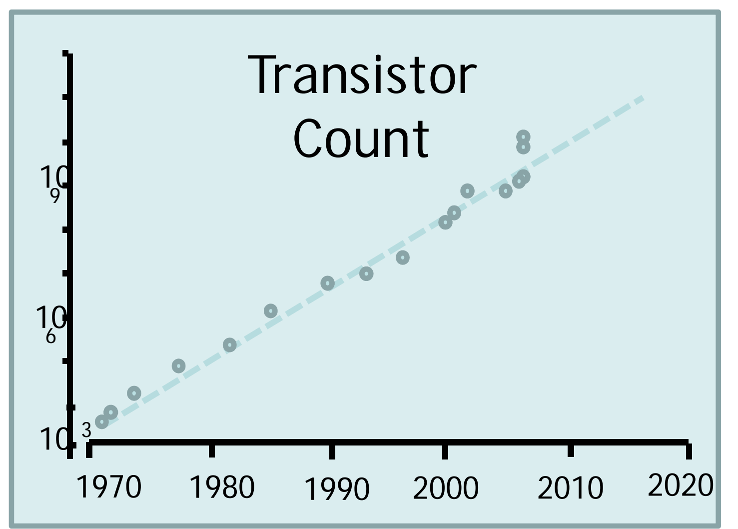
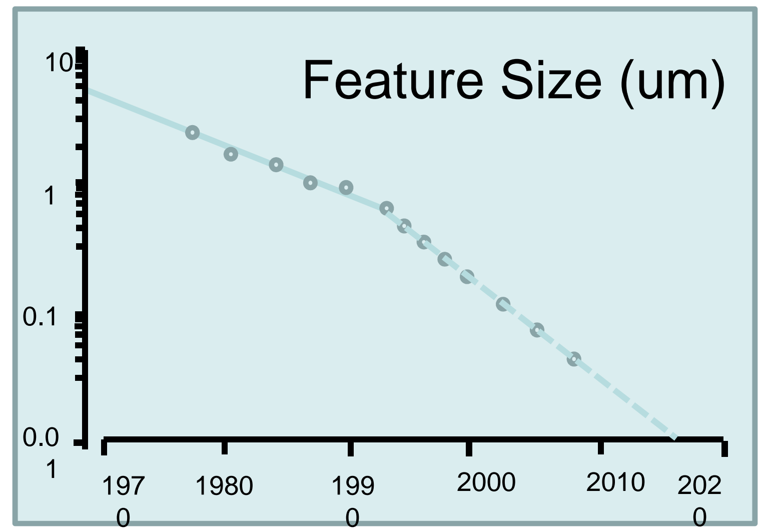
40 + Years of Moore's Law Scaling





We are now at Deep Submicron Era

32 – 22 nm Nodes

Source: Intel

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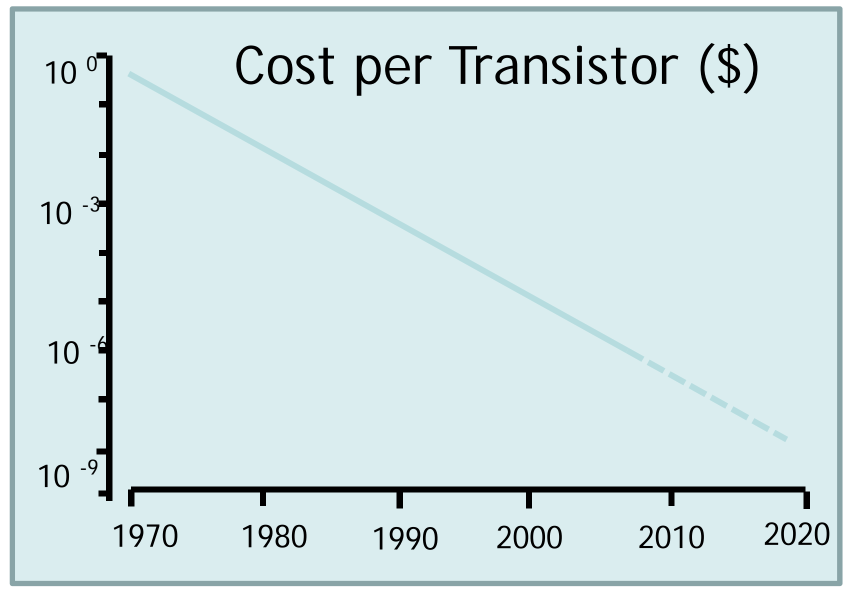
40 + Years of Moore's Law

More than 1,000,000 times of cost improvement



Source: Intel

"100,000 transistors now cost less than a grain of rice"

Geoff Colvin

Fortune magazine Sept 6, 2010 page 64

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For 40 years Progress was in Predicted Directions

- Moore's Law Scaling - we knew what was coming next and the path to progress understood

- IC Devices: focus on Fab and Design
  - Shrink geometries
  - Improve designs for higher density
  - Increase wafer size

- Packaging Interconnect: Au Wirebond & FC Solder Bumps
  - Follow die shrink
  - Signal Integrity
  - Power in - Energy out - Thermal Management ,
  - Mechanical Integrity - Stress Analysis
  - Cost

And together Assembly, Packaging & Test have becomes true Disciplines, recognized Professions and integral parts of the Semiconductor supply chain.

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Semiconductor Life Cycle

Source: Texas Instruments

The first IC by Jack Kilby at Sept 12, 1958

The first transistor by Walter Brattain & John Bardeen's at Dec. 23 1947.

Improvement of Life Experience

Life Sciences?

- Intelligent appliances
- Bio-medical
- Green energy

Information

- Search engine
- Info service
- Machine-to-machine

Communication

- Connectivity
- Bandwidth
- People-to-people

PC

- CPU/GPU
- Memory
- Storage

1980 1985 1990 1995 2000 2005 2010 2015

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Global Interconnection - 2010~12

DeskTop Computer

Laptop Computer

Integrated Network

Growing Bandwidth

Data Center Backbone

Car GPS

Galaxy Tab iPad

Apple TV

Smart TV

iPod / MPG Player

BlackBerry

Cell Phone

iPhone

GPS

Game Consoles

Hand Held Games

2011 Revenue Projections

$ 41 Billion Packaging

$ 314 Billion Semiconductor

$ 1.5 Trillion Electronic Hardware

How much Global GDP is generated by Electronics?

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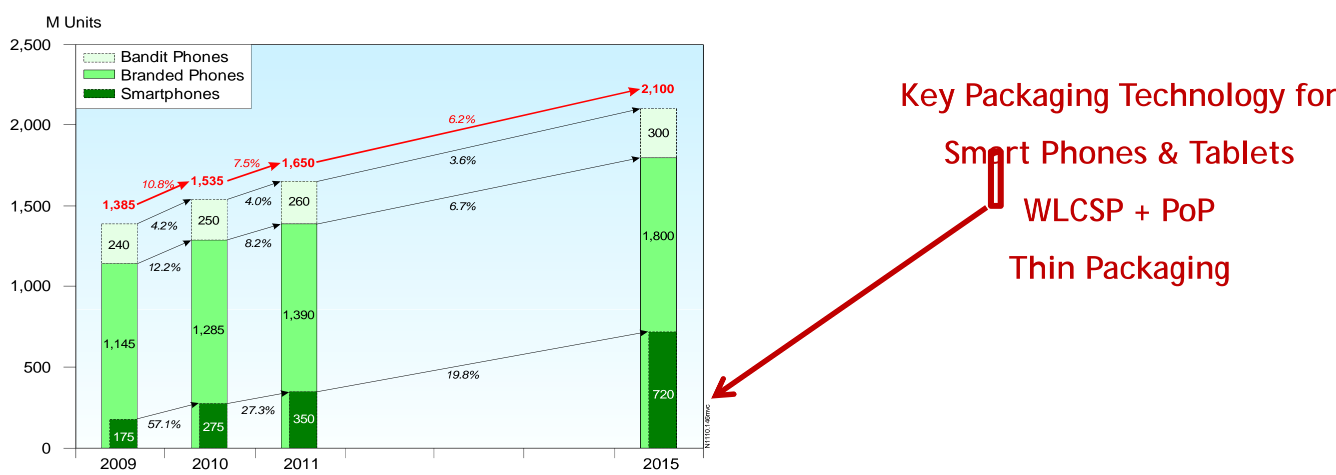
Changing Landscape



Key Packaging Technology for

Smart Phones & Tablets

WLCSP + PoP

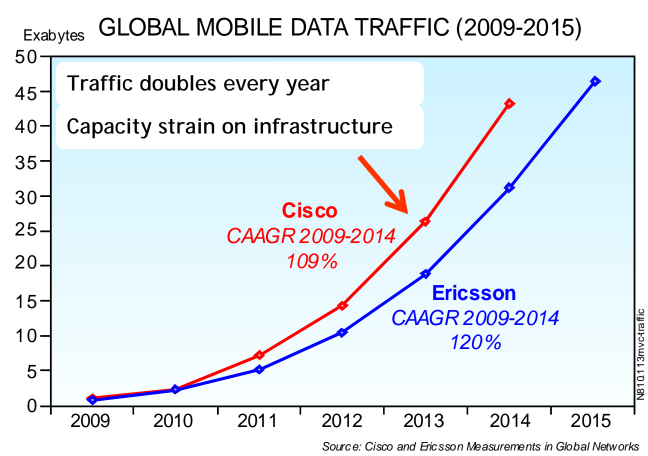
Thin Packaging

Key Networking Packaging Technology

Large Die FC

Ultra Low Alpha

Networking IC Packaging



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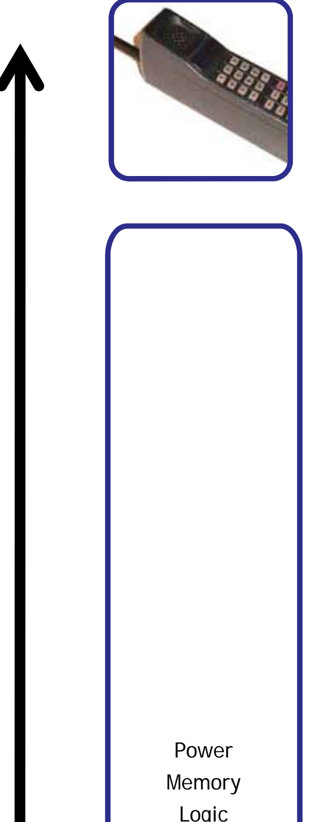
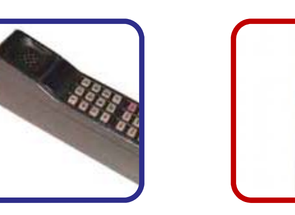
Mobile device D/A/M integration





Power
Memory
Logic
Radio

PDA
MP3
Power
Memory
Logic
Multi-band

Accelerometer
Video
Projector
Touch Screen
Internet
Social Network
Camera
PDA
MP3
Power
Memory
Logic
Multi-band

Microphone
Safety Monitor
Medical Care
Biosensors
Accelerometer
Video
Projector
Touch Screen
Internet
Social Network
Camera
PDA
MP3
Power
Memory
Logic
Multi-band

The Future : engineered by human ingenuity

TIME

We are here

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More Moore and More than Moore

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Source :ITRS

Beyond CMOS

20nm

28nm

40nm

65nm

90nm

130nm

More Moore : Scaling

Baseline CMOS:

CPU, Memory, Logic

Analog RF

Passives

HV Power

Sensors Actuators

Biochips Fluidics

More than Moore :

Functional Diversification

Information Processing
Digital content
System-on-Chip (SOC)

Combine SOC & SiP :
Higher Value System

Interacting with people and environment

Non-digital content

System-in-Package (SiP)

Moore's Law

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What Comes Next?

- What are the Electronic Market and Semiconductor Landscapes in the coming Decade? What type of applications will be thriving?
- What technologies from "More Moore and More than Moore" will come forth to meet the market drivers?
- What are the Difficult Challenges for the Back End Industry ? What are the potential Solutions?
- Important questions for us to consider and to debate.

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Packaging Value

Packaging Game Changers

70%

20%

10%

Cu WB

QFN & Multirow QFN

Discrete & Low IO

- Wire Bond
- Flip Chip/WLP
- Others

PoP

WLCSP & FOWLP

Low Cost FC-CSP

Large Die FC BGA

3D IC Packaging

Si Interposers

Thin – Small Packages

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25+ Years of Semiconductor Packaging

P-DIP
PLCC
SOJ
Enhanced QFP
QFP
LQFP
SOP
TQFP
SSOP
TSOP
Enhanced BGA
Film BGA
BGA
LBGA
uBGA
TFBGA (mini BGA)
BCC
Bumping
FCBGA
FCCSP
COS BGA
LGA
Stacked-BGA
MCM BGA
Finger Print Sensor
VFBGA
WFBGA
QFN
WLCSP
Polymer WLCSP
FC-QFN
Hybrid FC+WB
PiP
PoP
Embedded
RF-Module
FC-PiP
aS³BGA
aQFN
MAP- POP
FC-POP
TSV
Fan out WLCSP
3D-TSV

ASE Begins

Leading edge CMOS node (approx): *0.25um 0.18um 0.13um 90nm 65nm 40nm 28nm*

1985 1990 1995 2000 2005 2010 2015

2011

Sophistication & diversification increasing over time

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Game Changing in Packaging

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Wirebond

- Au to Cu Migration driven by sky high Au price
  - "last frontier" for cost reduction
  - 4 + billion fine pitch wire bond units shipped
  - 18 micron wire diameter for fine pitch pad designs
  - Conversion gaining momentum
- Difficult Challenges
  - High reliability for automotive & networking markets
    - Materials & Process - Cu-PdCu
    - Molding Compound lowering corrosion risk
  - Deep Submicron Technology Nodes - 28 nm - 22 nm ………
    - Pad pitch design & constructions
    - Equipment and Processes for ultra Low k stress compatibility

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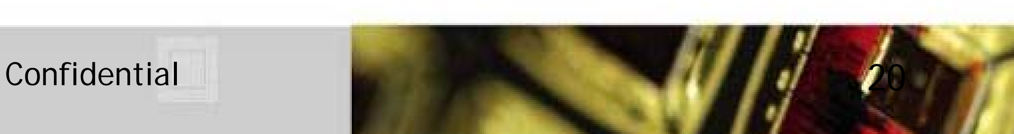

Flip Chip

- From FC BGA to FC CSP & low cost Performance Package
  - PoP package
- Bump materials conversion from high lead/eutectic to leadfree solder to Cu Pillar
  - ROHS legislation
  - Pad Pitch reduction for deep submicron
- Difficult Challenges
  - From lead free to Cu Pillar - UBM structure
  - Underfill materials designed for Cu Pillar
  - Interfacial adhesion
  - Low cost bond - trace (MUF)materials & process system (including substrate)
  - Thin - thin Package

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Packaging Materials Changes

After 40 years or more with only limited changes in materials used, we are now seeing unprecedented changes.

- In this decade, 100% of packaging materials will change
- In the next decade, more than half of materials will change again

Assembly & Packaging

2008 ITRS Winter Conference

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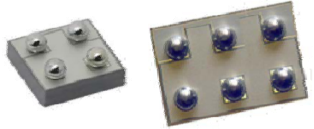
Growth of Wafer Level Chip Scale Packages (WLCSP)

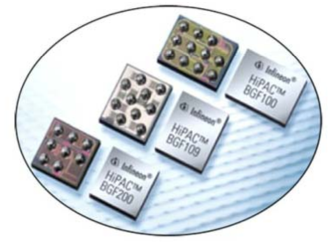
- Year 2000 – WLCSPs were small, low I/O, expensive, and with limited manufacturing infrastructures

On Semi Analog - ASE



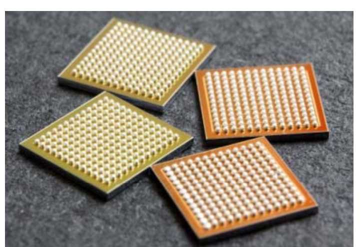
Vishay's Power MOSFET – TechSearch

TI Nanostar Digital - ASE

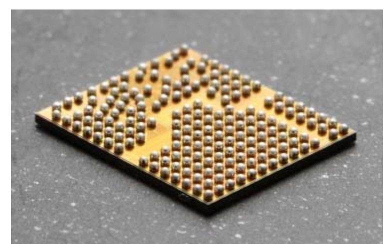


Infineon BAW filters- TechSearch

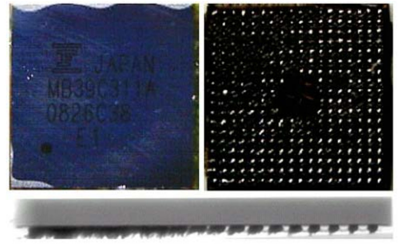
- Year 2011 – Billions shipped, >300 I/Os, Established infrastructure, cost competitive, with high volume manufacturing



Qualcomm 169L WLCSP - ASE



Broadcom 182L 6.5x6.5 WLCSP - ASE



Fujitsu Power Management WLCSP 308 L 7.7x7.7mm -TechSearch - TPSS

361 L WLCSP- ASE

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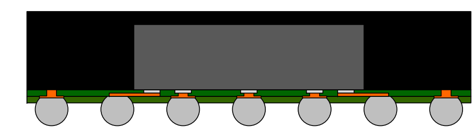
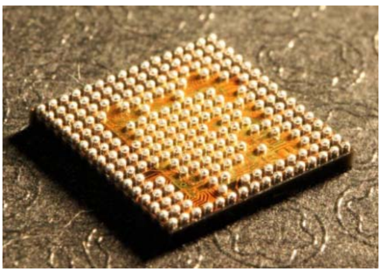
WLCSP - Fan Out

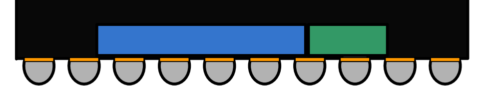
- Multiple approaches to Fanout WLCSP

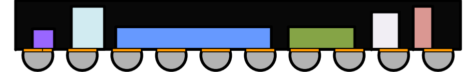


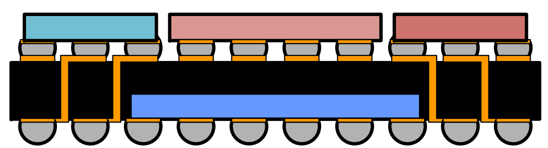
- Infineon's eWLB is first in high volume production: Millions per month

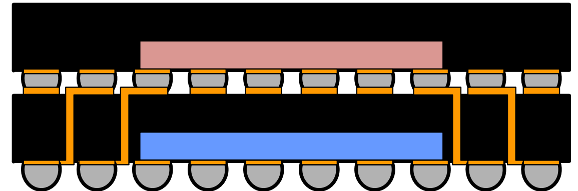


- Next Steps
  - Multi die & large size
  - 3D with thru vias - stacked POP
  - Panel Process
  - Thin package









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M&M & MtM Architecture in the Package

One of the most important trends in packaging is the incorporation of system level integration through System in Package (SiP)

- **This technology enables equivalent scaling through functional diversification**

This added complexity requires change in architecture, materials and processes and equipments

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Representative SIP types

Horizontal Placement		Wire Bonding Type	Flip Chip Type	
Stacked	Interposer Type	Wire Bonding Type	Wire Bonding + Flip Chip Type	PoP, e.g Flip Chip Type
		Terminal Through Via Type		
Embedded Structure		Chip(WLP) Embedded + Chip on Surface Type	3D Chip Embedded Type	
		WLP Embedded + Chip on Surface Type		

May include Wafer Level Packaged Components

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The 3D Packaging
A major Paradigm Change

Based upon tool boxes of technologies & infrastructure from Flip Chip and Wafer Level Packaging and Test

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Speed and Power Advantages of 3D-TSV

- 3D interconnect decreases path lengths.

Power reductions in electrical signaling as 3D, new materials (dielectrics and conductors), wider channels, etc. will move the length of E-O-E distance that is justified by cost and energy savings.

–Reduced power consumption

It is a moving target!

- Standby power reduced by 75% compared to PoP and MCP packages

–Smaller physical size

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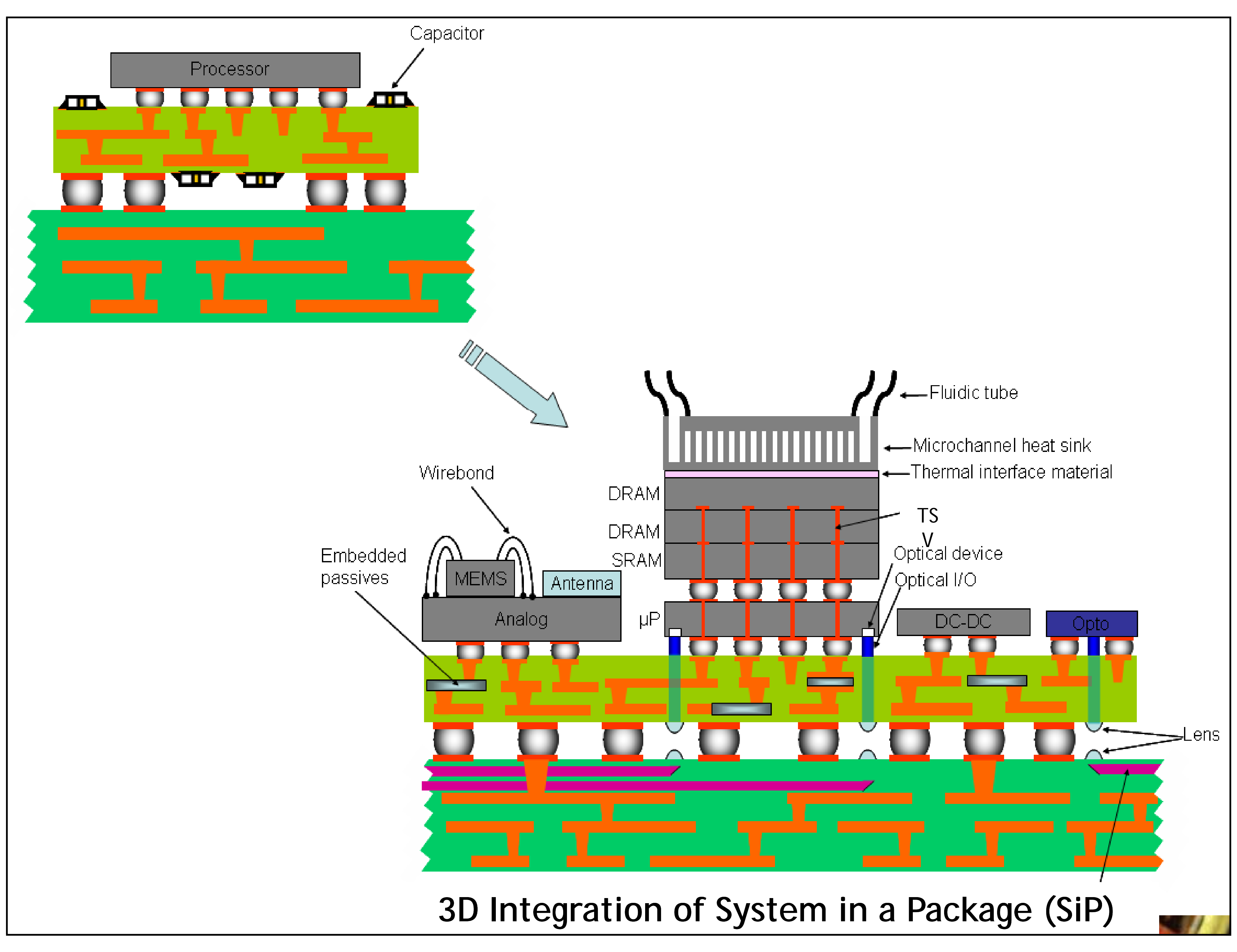
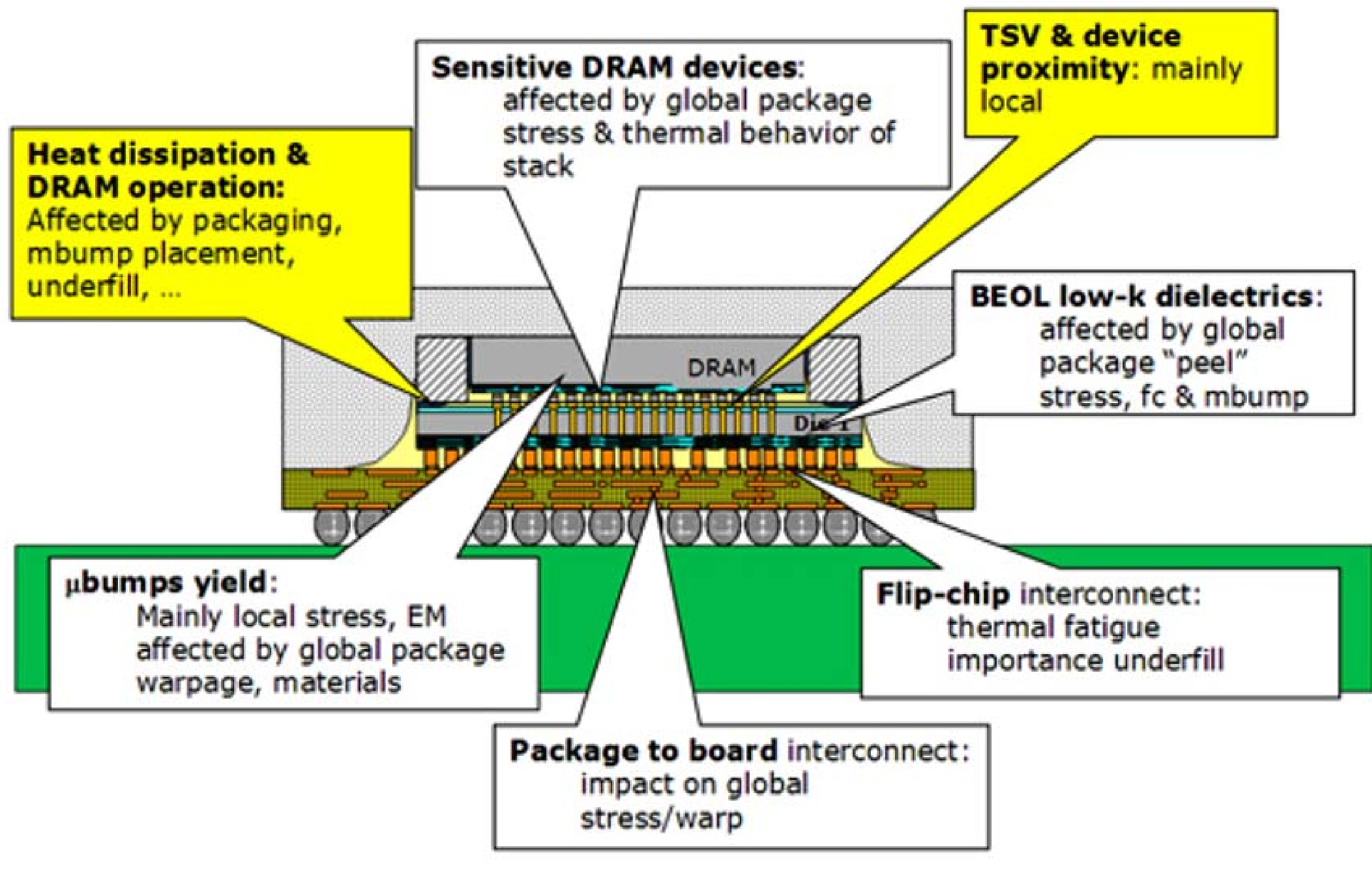


3D Integration of System in a Package (SiP)

Packaging Issues impacting Yield and Reliability for Deep Submicron



Source: Future Fab International Issue 34

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Some Examples

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Some are in Production today
Stacked 3D Camera Module

Source: Fraunhofer IZM

Cross section of the 3D camera stack with 3D stacking, functional diversification using TSV interconnect

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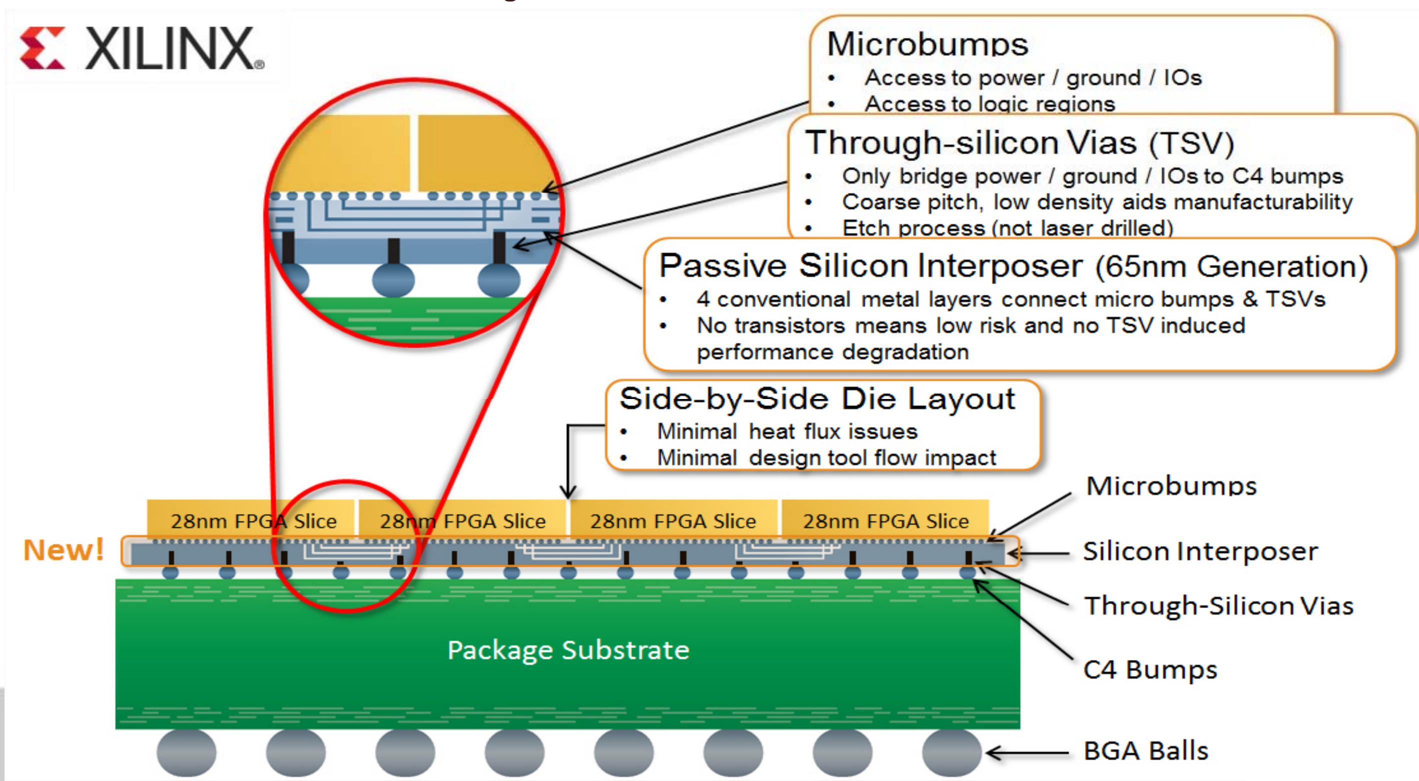
Xilinx Stacked Si Interposer FPGA

- Interposer substrate has more than 10,000 routing connections
- Compared with standard I/O connections it provides:
  - > 100X die-to-die bandwidth per watt
  - one-fifth the latency



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Tera-scale Computing by 2015

TSV die to die connection

Silicon Interposer with:

-Integrated thermal management

-Integrated Passive networks

200GB; 800GB/s memory

(16 sectors at 50GB/s)

Memory cube

1Tbyte; 800GB/s

(16 sectors at 50GB/s

Memory
Memory
Memory
Interposer
Memory
Memory
Memory
Interposer
Memory
Memory
Memory
Memory

Memory
Memory
Interposer
Processor
Processor
Interposer
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Processor
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Interposer
Processor
Processor

Optical channel

System in Package Substrate

With CNT based heat spreader

2TB/s optical transceiver for:

- Off package communication

- On package routing

Processor with 1000 cores/10 layers

Core transistor speed 1GHz

25um thick wafer (~400mV power)

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The Best Thing Since Sliced Bread

- Everyone says 3D is the "best thing since sliced bread"
  - We must close the distance between the bread maker, the deli counter, and the sandwich served on the dining table.
  - Whether it is BLT, Roast beef, or peanut butter & jelly, we must deliver our best sandwich to the customer.

- When TSV wafers roll out from the foundries in the not too distant future, the back end of the supply chain must be ready to assembly and test them cost effectively with good yield and cycle time.

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Special Applications

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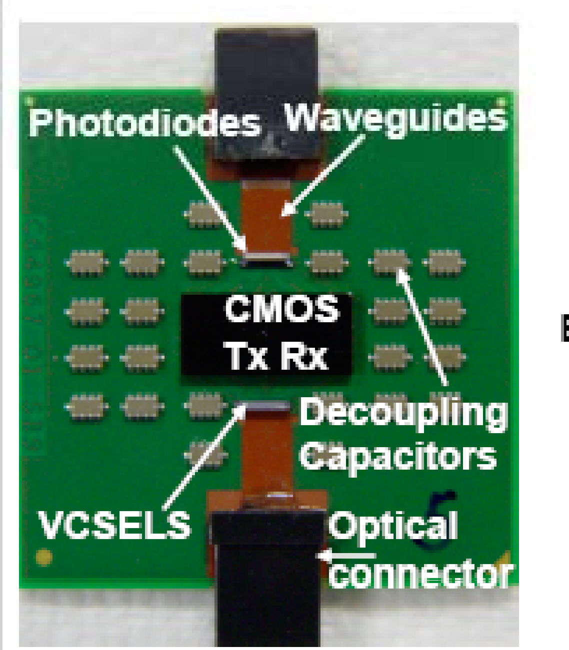
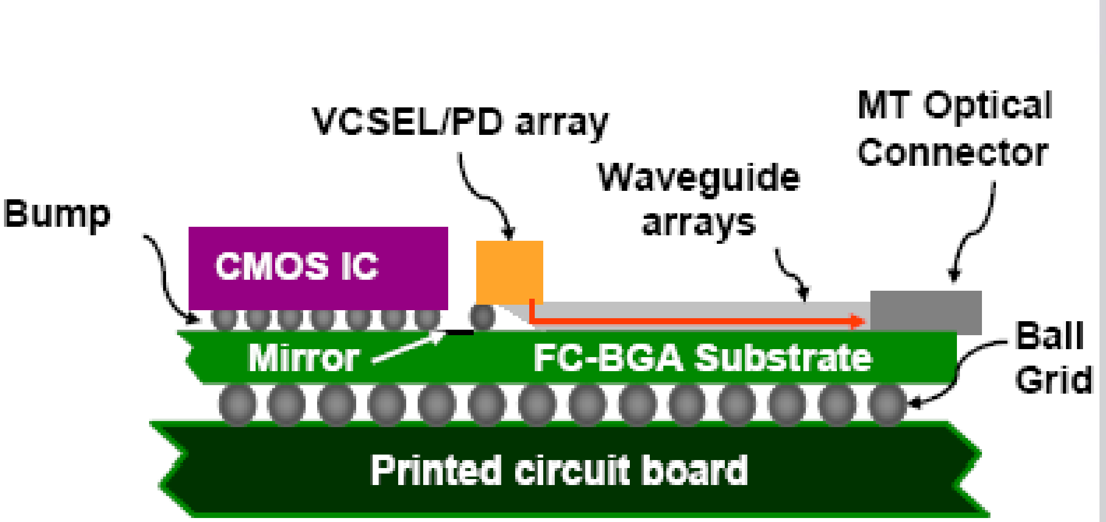
Photonic Signaling is Coming





Optical I/O Technology for Tera-Scale Computing; ISSCC 2009
Ian Young, Edris Mohammed, Jason Liao, Alexandra Kern, et al
Intel, Hillsboro, Oregon

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Expanded Coverage of Emerging Requirements for 2011:

Medical Electronics

- Medical electronics Categories to be addressed:
  - Portable/wearable medical electronics
  - Implantable medical electronics (Parkinson's disease symptom control)
- Selected technical Issues for Medical electronics
  - Power requirements: energy scavenging; wireless radiated power; batteries
  - Safety issues (voltage, biocompatibility, power delivery)
  - FDA certification
  - Reliability requirements
  - Environmental issues
  - Connectivity (wireless)
  - Optical components (cameras)
  - Microfluidics
  - Implantable micro-robotics
  - Sensors
  - MEMS

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Business Models & Infrastructure

Value-Add

Packaging
Test
Material

Semiconductor
Manufacturing

Chip
Architecture
Design

IDM
Fabless
Hybrid

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Food for Thought

- In our industry the backend is coming to the forefront of the technology supply chain
- Let us not forget that Market is still the deciding factor in what technologies will become mainstream.
- Technology, infrastructure, and business model and profit must come together for the industry and profession to prosper.

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Thank you for your kind attention

Any Questions

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Aknowledgments

I would like to thank my colleagues and friends for their generous advice and help in this presentation. I am especially indebted to Patricia Macleod for her excellent editing and support.

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