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A Hot Topic: Current Carrying Capacity, Tip Melting and Arcing

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Agenda

- **Motivation**
- **Current carrying and tip burning**
  - What is the difference?
- **Tip burning / melting / arcing**
- **Current carrying**
  - Different test methods and results
  - Modeling results
- **Current limiting circuits on probe cards**
- **Summary**

- **Coauthors**
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Motivation

- **Current in wafer test for DRAM is increasing**
  - Maximum current can reach 400 mA or more even under normal test conditions
  - Further increase with higher test frequency and use of DFT circuits for parallel test and test time reduction
- **Risk of current related probe damage is increasing**
  - With the use of power sharing methods higher currents are possible on a failing DUT
- **Increasing interest from our customers to understand and compare current carrying capability of different probe technologies**

Current Carrying Capacity and Tip Burning

- Current carrying capacity and tip burning/melting are related but separate topics
- Tip burning/melting is localized at the probe tip and occurs when the probe tip is getting too hot and the tip material is melting
- Current exceeding the maximum current carrying capacity affects the whole probe and results in the probe loosing its mechanical strength

Tip Burning/Melting

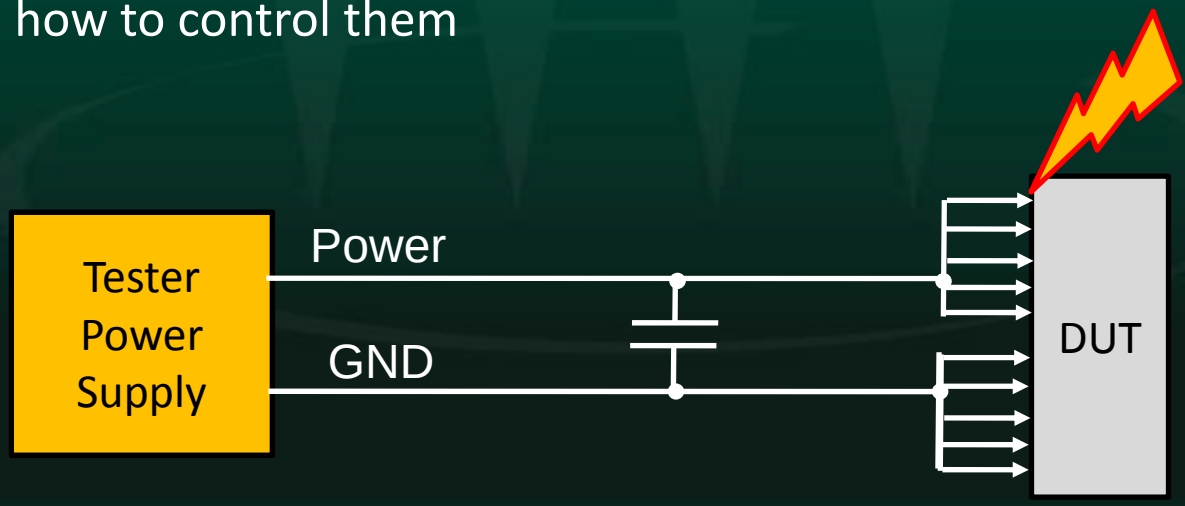
- Primary damage happens to the probe tip
- Caused by excessive power dissipation:

$$P = I^2 \times Cres$$

- Increase in contact resistance is caused by:
  - Insufficient cleaning
  - Tip melting caused by arcing
- Probe tips which have been affected by lower level of melting can be recovered by abrasive or chemical cleaning
- Very bad tip melting can impact the whole probe as a consequence

Tip Arcing

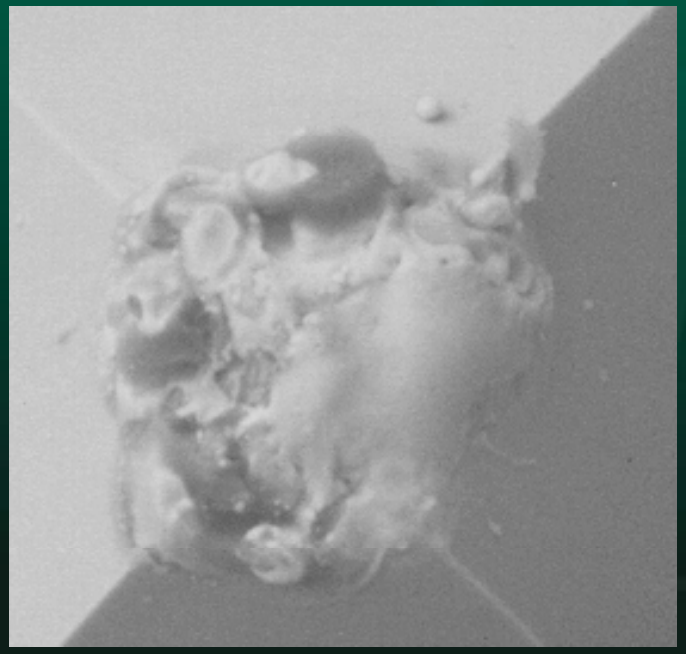
- **Arcing events are caused by touchdowns with not completely discharged capacitors or with the power supplies turned ON (hot stepping)**
- **Problem can be avoided by correct test programming:**
  - Clean power-down sequences
  - Sufficient time for capacitor discharge
  - Make sure you know all the relays in your wafer motherboard and how to control them



Tip Arcing – SEM Pictures

- **Arcing can be identified by SEM pictures**
  - Very distinct signature of melted tip material / splatters

Strong arcing event



“Micro” arcing

Current Carrying Capacity

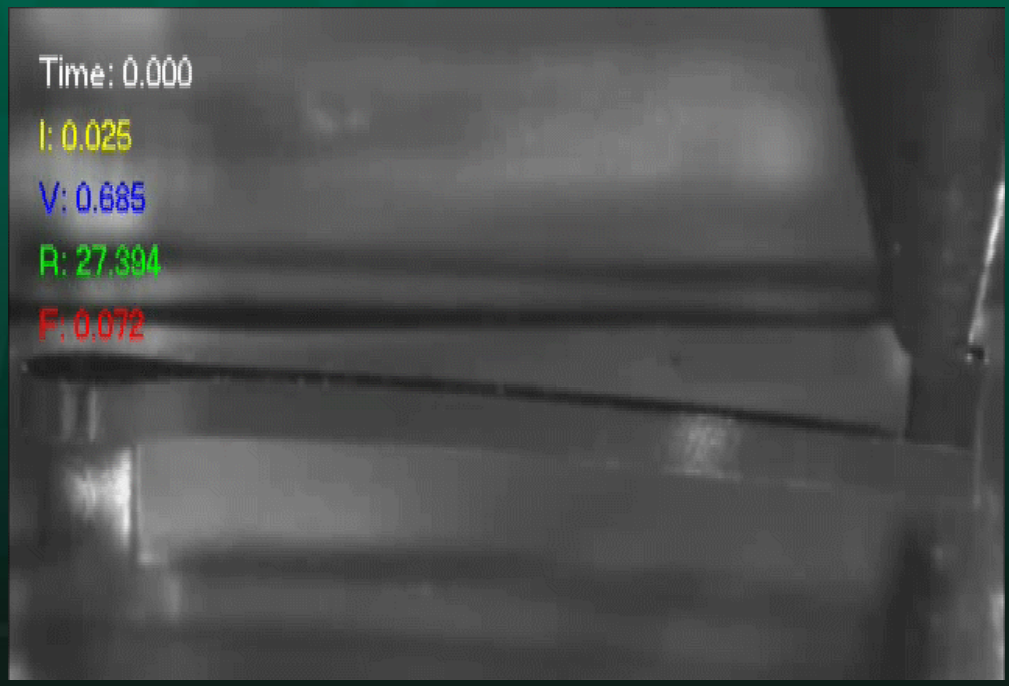
- **Max current is a function of spring design and environment**
  - Spring cross section area, length and material (= path resistance)
  - Thermal coupling of spring to the probe head (= heat sink)
  - Chuck temperature
  - Current/temperature and distance to neighboring springs
- **Max current capability will be degraded by:**
  - Contact resistance (additional heating from the tip)
  - Overtravel – impacting Cres and mechanical stress
  - Pad material
  - Cleaning recipe and effectiveness

Current Carrying Capacity

- **Different test methods used for CCC**
  - Current to failure test
  - Long term stress test
  - 20% force reduction test (ISMI standard)
- **What does that mean in the application?**
  - Standards are good to compare different technologies but will not tell the safe operating point of the probe
  - New probes with low Cres are used for the testing
  - Need to consider degradation in order to set a meaningful specification for max current in the application
  - Safe operating point should be set further away from the fail condition

Current Carrying Capacity
Current to Failure (FFI "standard")

- **Test Procedure: Ramp up current until fail**
  - Data Collected:
    (Thermal Runaway)
    - Current (I)
    - Voltage (V)
    - Cres (R)
    - Force (F)

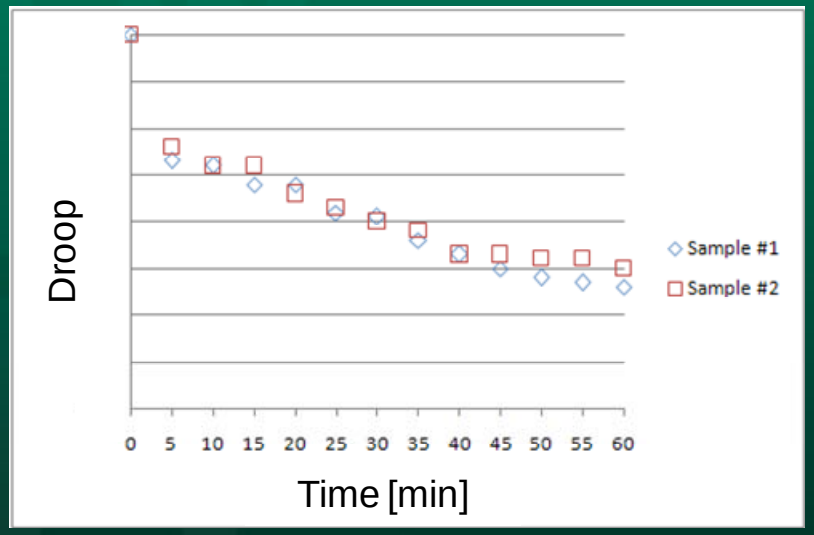


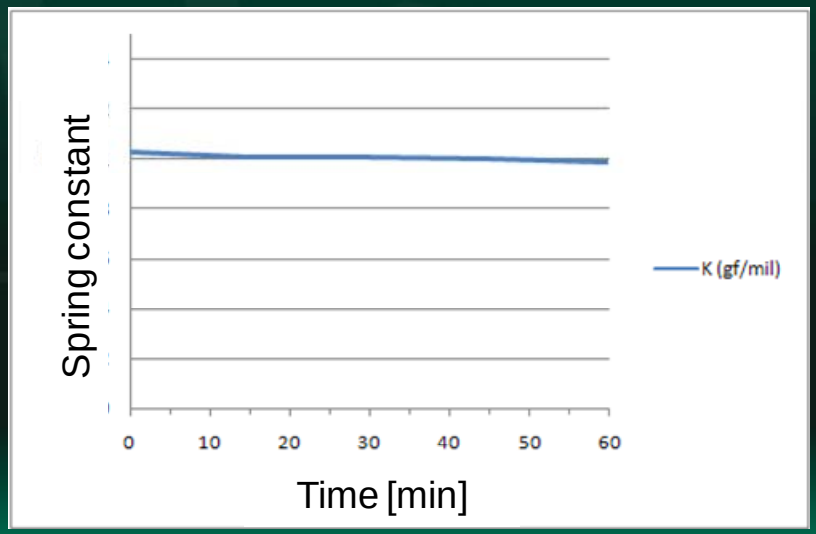
- **Results**
  - FFI MicroSprings™ typically support current >1.5A in this test

Current Carrying Capacity

Long Term Stress

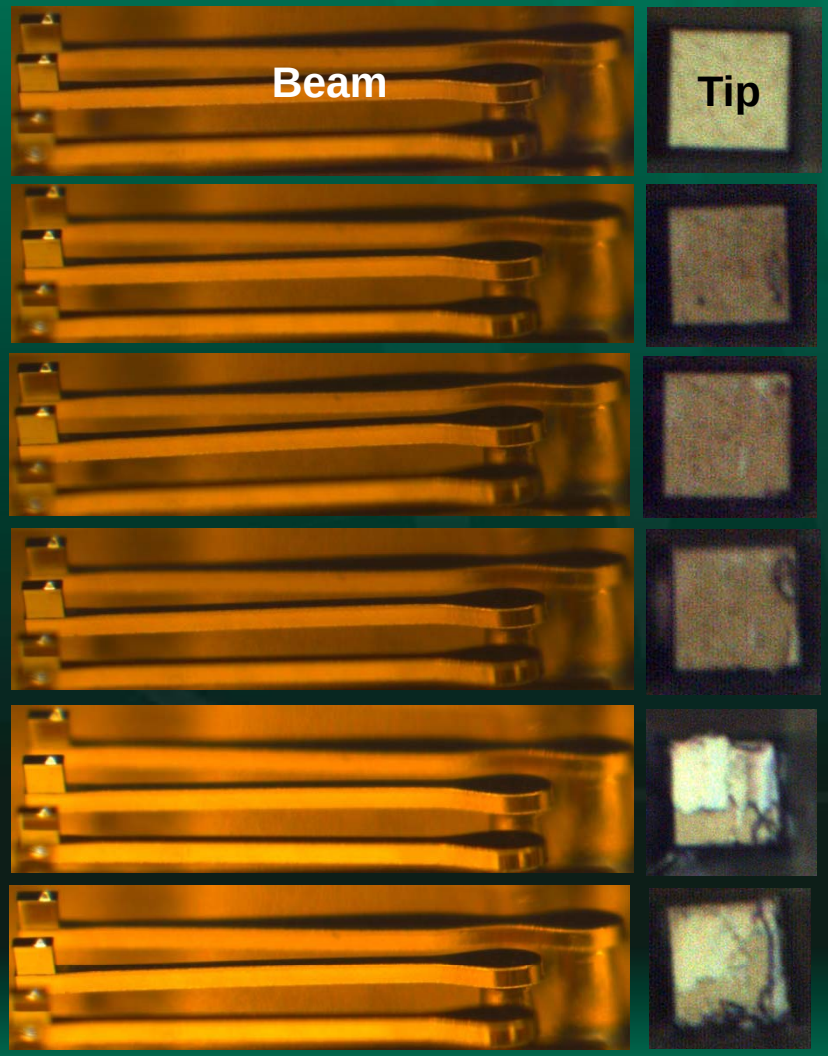
- **Test Procedure:**
  - 1A steady state current
  - @ OT = reset every 5min (Touchdown)
  - Test Temp. = 90°C
  - Test Time = 60 min
  - Data Collected:
    - Spring constant (K)
    - Droop
    - Visual inspection for damage
- **Results:**
  - Acceptable droop
  - No sign of discoloration
  - Δk = ±2%





Current Carrying Capacity

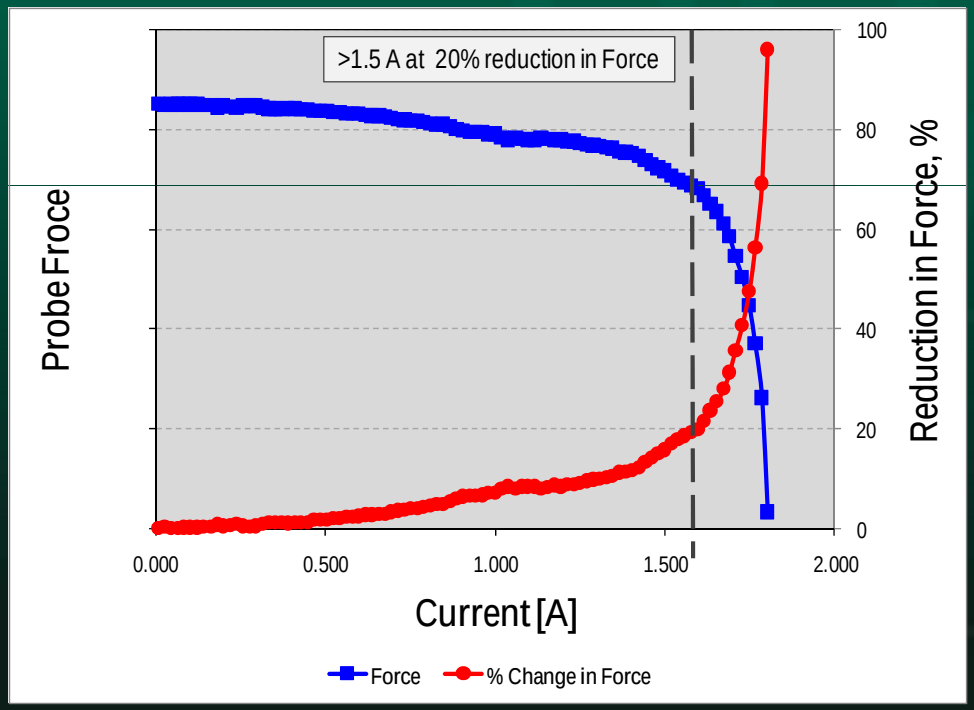
Long Term Stress



- No evidence of beam discoloration
- Residual Aluminum evident on tips at 90°C after extended times
- No significant change in K

ISMI Guideline for Current Carrying Capacity

- **Maximum allowable loss of contact force due to current passing through a probe is 20% - test done @ RT**

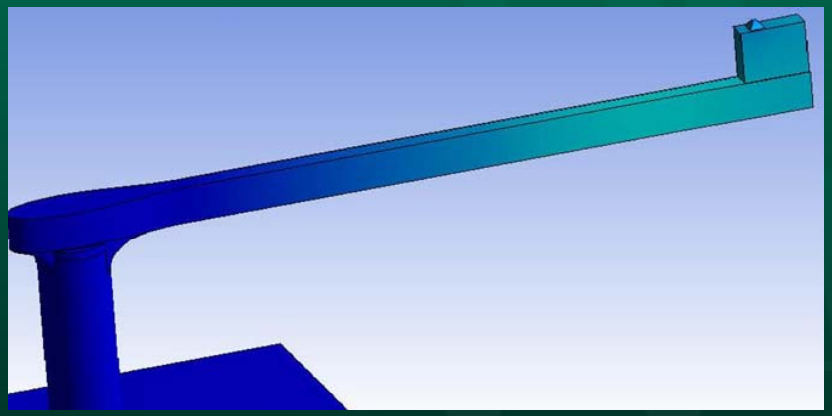


- **Data shown are from FFI current to failure test**
- **Not 100% aligned to ISMI guideline yet:**
  - Force is measured with current applied
  - Duration is different (continuous ramp)

- **Use condition should not be set to the 80% value**

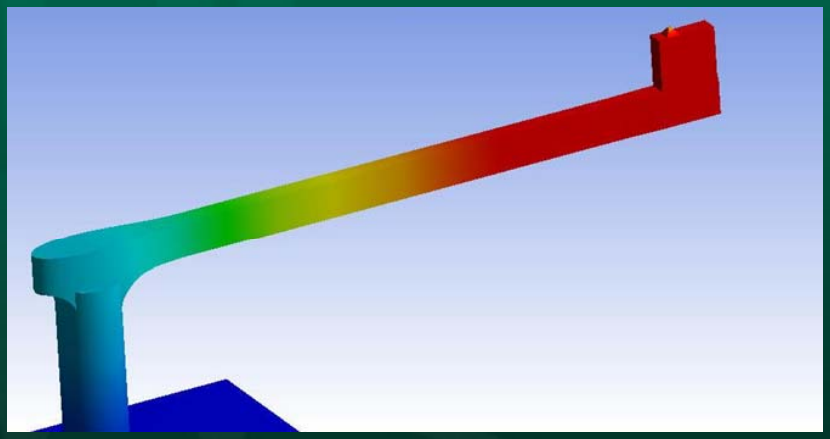
Current Carrying Capacity
Modeling results

Probe Temperature at 600 mA



- Temperature far below a critical value

Max. Current at Thermal Runaway

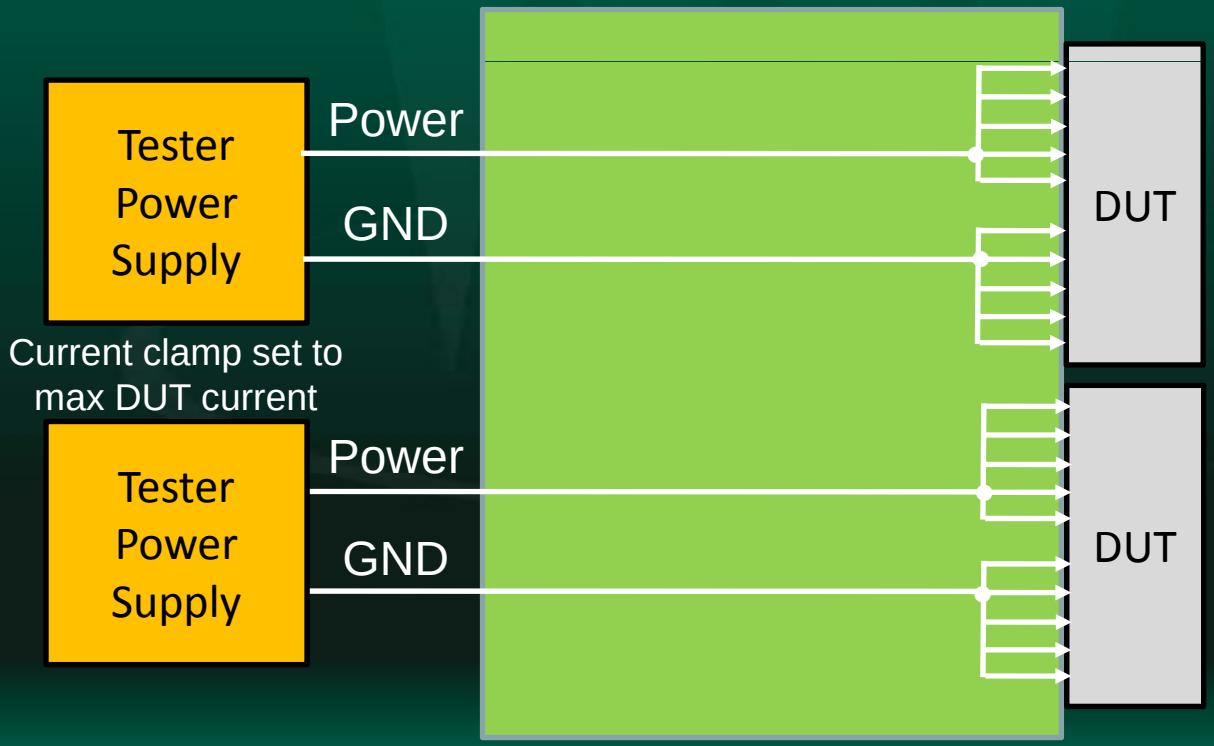


- Critical temperature is reached with 1.7 A of current

- Modeling matches very well with experimental results
- 3D MEMS process allows increase in cross section area leading to high current capability

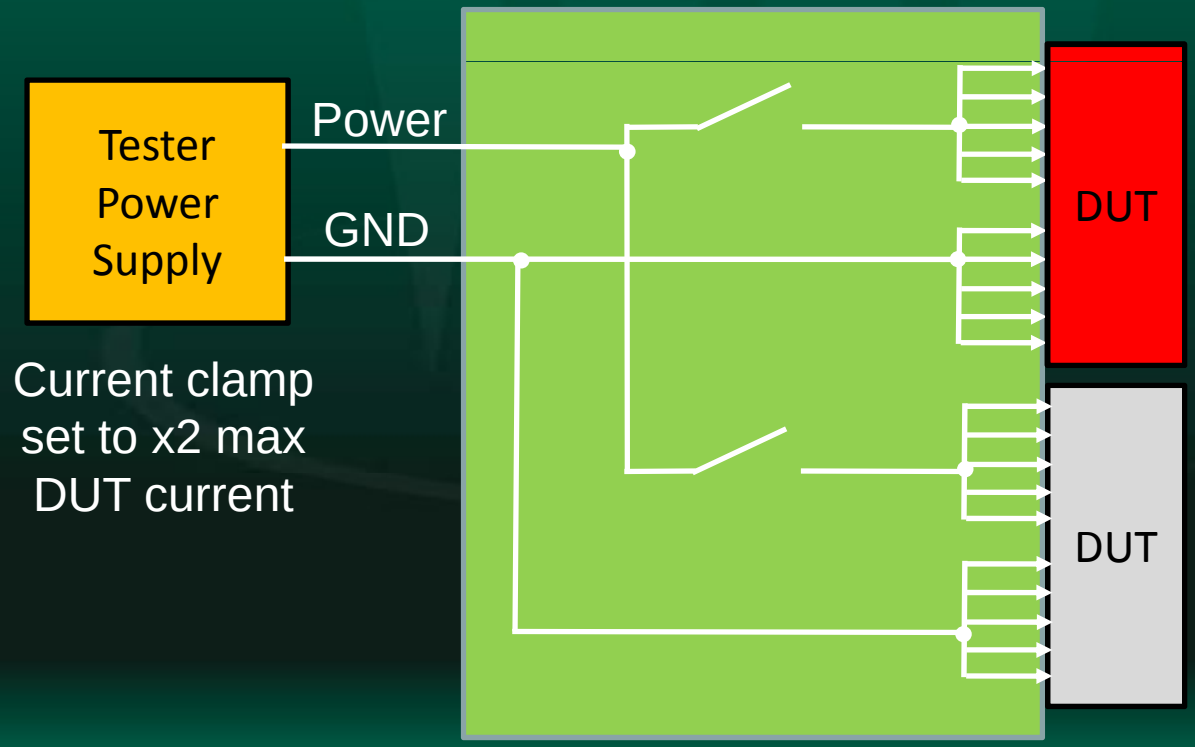
Current Limiting Circuits

- With one tester power supply per DUT the current limiting function can be used to control the max current
- If used correctly and probes support the required current, no over-current related damage should occur



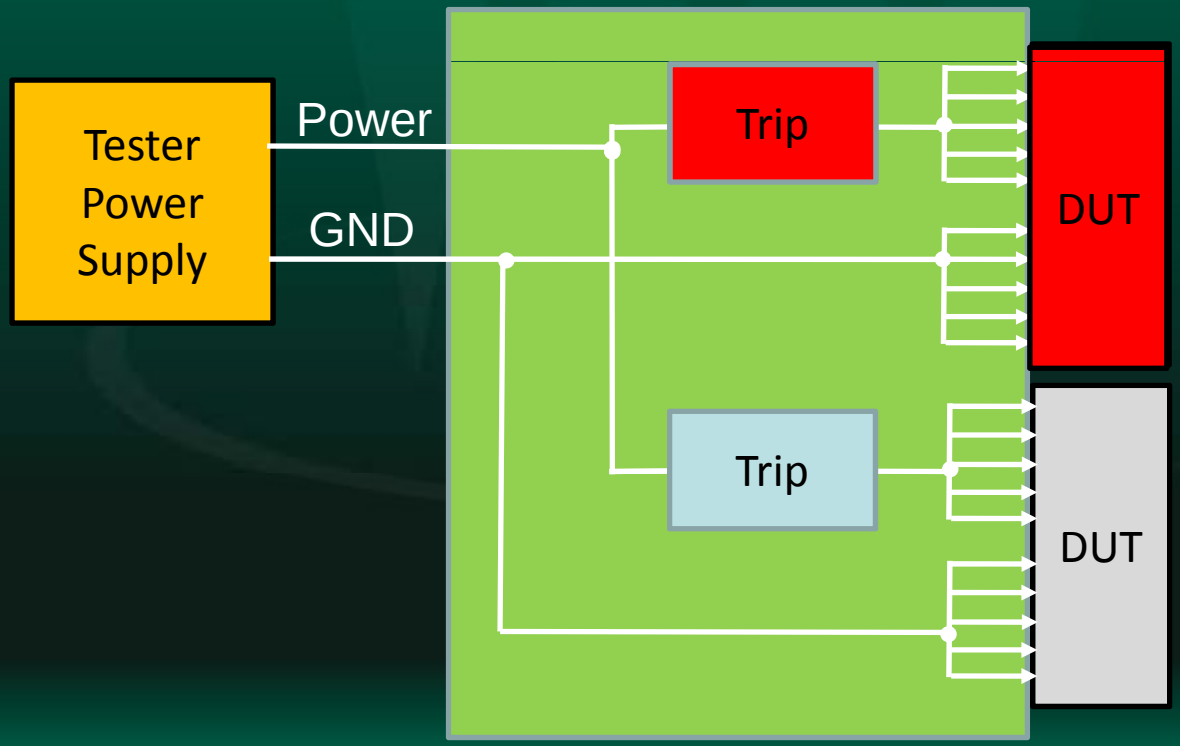
Current Limiting Circuits

- With power supply sharing the current clamp cannot be set to the max current of one DUT but to overall current
- A failing DUT can cause an over current condition
- Power sharing increases the risk of current related damage, no DUT specific current clamp



Current Limiting Circuits on Probecards

- **SORT-Boost™ FFI's latest Advanced TRE™ chip includes a programmable current trip function**
- **DUTs with excessive current consumption will be automatically disconnected from the power supply**



Increase Number of Probes

- **Increasing the number of probes is another way to reduce the current per probe to avoid over current related problems**
- **But the current may not be spread out equally over all probes**
  - Pads located close to current demanding circuits will have more current
  - Example: DRAM design where 2 out of 12 probes used for VDD/VDDQ had to carry 80% of the overall current
- **Increase probe count of power and ground does also improve the impedance of the power delivery system**
  - Adding probes drives impedance peaks to higher frequencies
  - SWTW 2007, Huebner et al. “26k Probes – A new Dimension in Probe Count”

Summary

- **Current carrying capacity and tip burning/melting are related but separated topics**
- **Tip burning / arcing can be minimized by regular cleaning and good test programming**
- **Use condition is impacting current carrying capability**
  - CCC tests like the ISMI standard can be used to compare probe technologies but should not be used to determine allowed the current in a use condition
- **Over current related damage can be avoided by use of current limiting circuits**

Acknowledgements

- **My coauthors**
- **Whole FFI probe development and reliability team**
- **Gaetan Mathieu, Garry Grube**

References

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- Matthew C Zeeman, ”A New Method for Assessing the Current Carrying Capability of Probes used at SORT”, SWTW 2010