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Multi-tip Probe (MtP) Contacts for Flip Chip Wafer Level Probing

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- **Approach**
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  - Production Qualification
- **Effect of OT on CRes**
- **Effect of Cleaning Frequency**
- **Actual Over Travel**
- **Comparative Analyses**
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- **Conclusion**
- **Acknowledgements**

Introduction

- Multi-site probing of Flip Chip devices with pin-counts approaching 12000 pins will physically strain the current mechanical test cell infrastructure capability and with increased electrical performance also required.
- Currently, CVPC- conventional vertical probe cards are used to probe Flip-Chip devices (~170um pitch, 100um dia. solder bumps) w/~7000 pins.
- The cost of probe cards are also expected to increase, primarily due to the need for custom interconnections. Typically, MLC-multi-layered substrates, are used to interconnect to the PCB.
- Moreover, if these tips can leverage a similar MLC inherent to current FFI-Formfactor probe card construction, then a cost effective approach would also be facilitated.

Approach

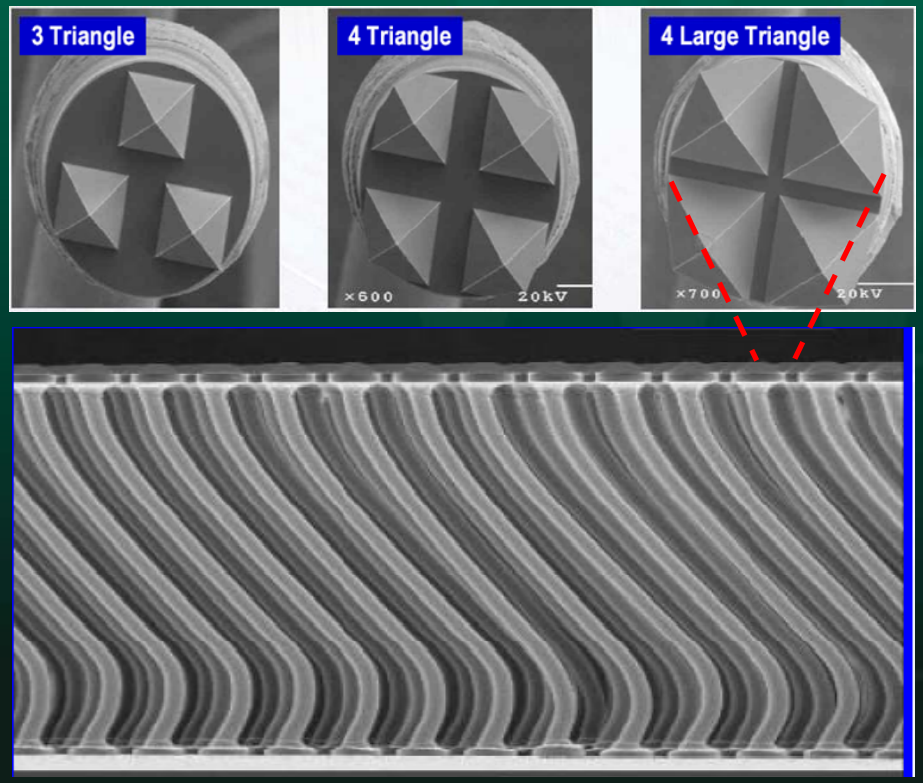
- A TI / FFI strategic probe development effort was initiated to MEMs fabricate probe tips on existing FFI MicroSpring® technology to validate the multi-tip “probe physics” on solder bumped features.

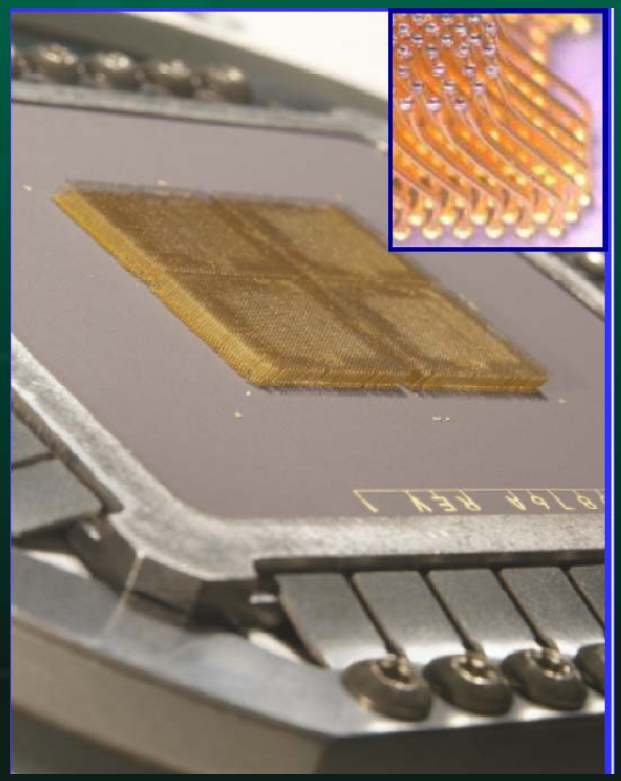
- A comparative analysis was then performed to determine if a better probe solution, in terms of electrical and physical performance would result vs. current C-VPC technology based on a test vehicle with ~4,000 spherical solder bumps at ~170um pitch.

- Probe qualification and integration based on a 2-step process;
  - **1-Technology Qualification: to validate technology**
  - **2-Production Qualification: to determine production worthiness.**

MtP / FFI-Micro-spring Probe Card Technology

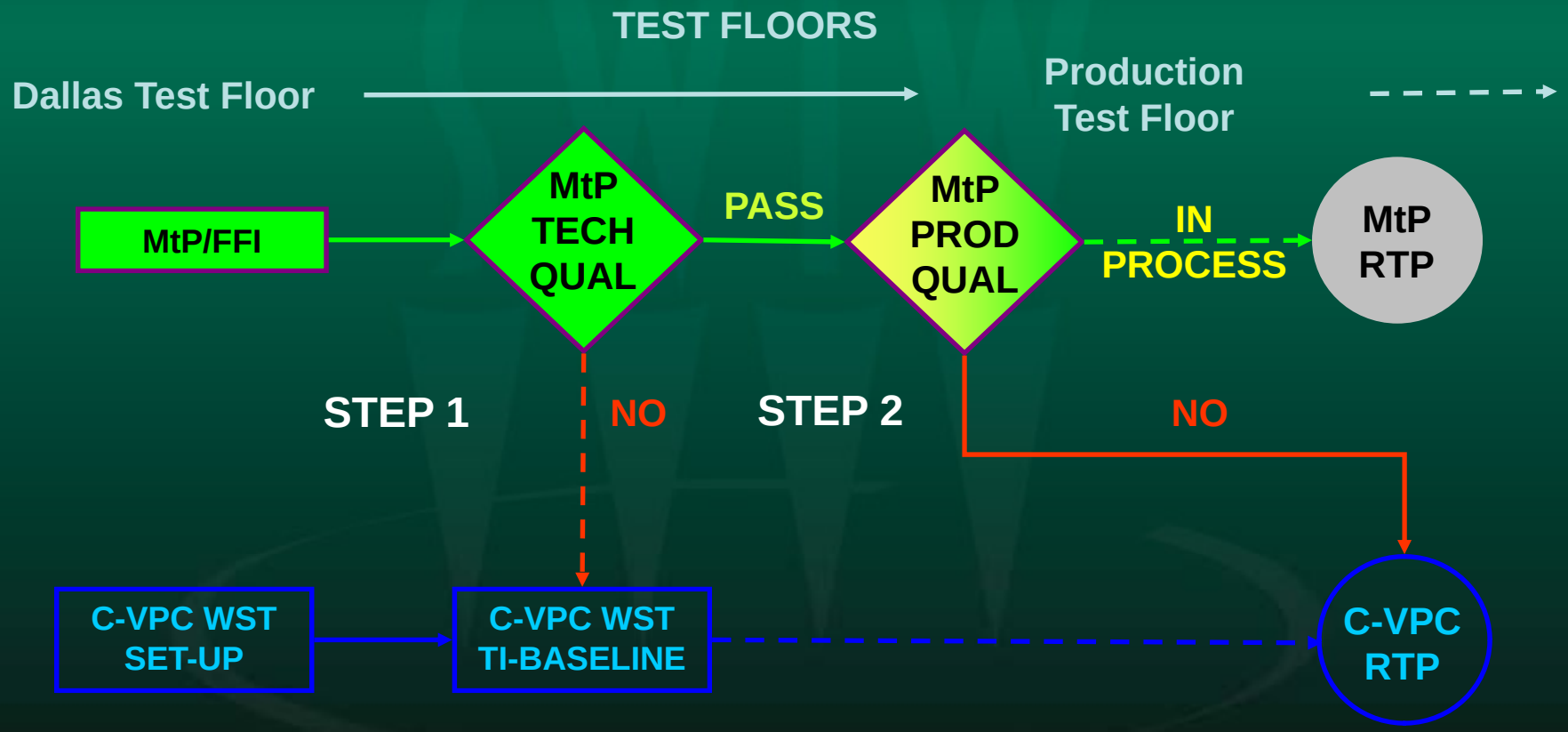
Micro Springs w/ MEMS used to form “Crown” tips, similar to WSP pogo-pin crown-tips, may offer a better COO when scaling from x1 to x4 multi-site applications, since the MLC-multi-layered ceramic is inherent in both.





Various crown tips or features can be custom fabricated on the micro-spring to optimize probing with the micro-springs fabricated on an MLC for multi-site.

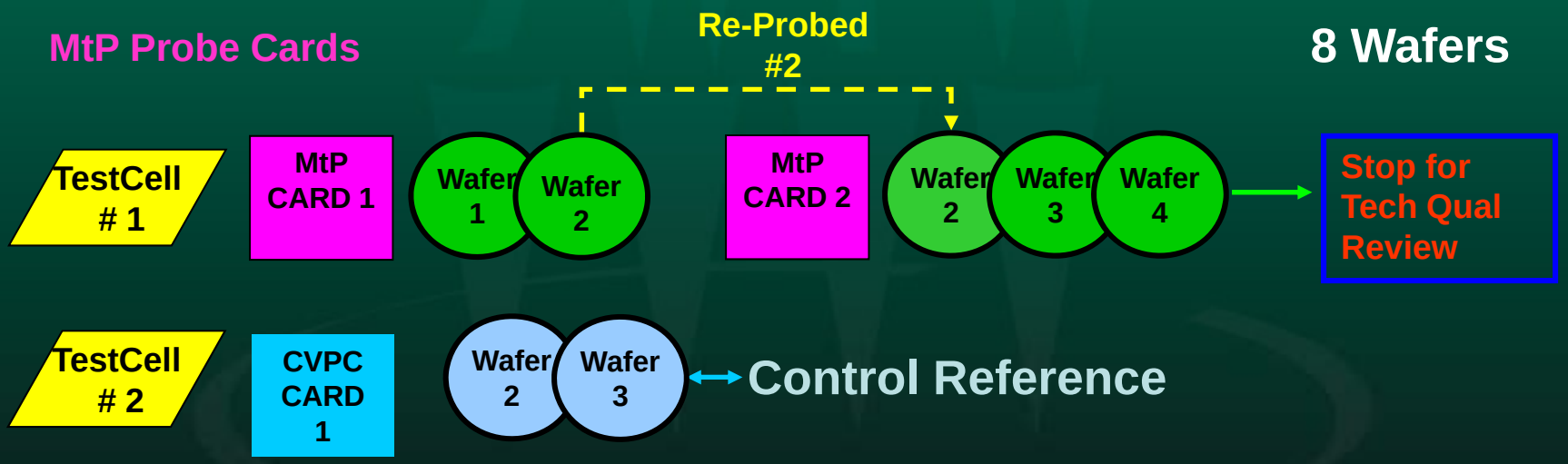
QUALIFICATION TEST FLOW: MtP vs. C-VPC



Comparative probe card analysis performed in parallel to CVPC to minimize risk to production delivery, if MtP did not work.

1-Technology Qualification Test Flow

Objective: Define a stable probe / cleaning process and HW set-up before volume production qualification phase.



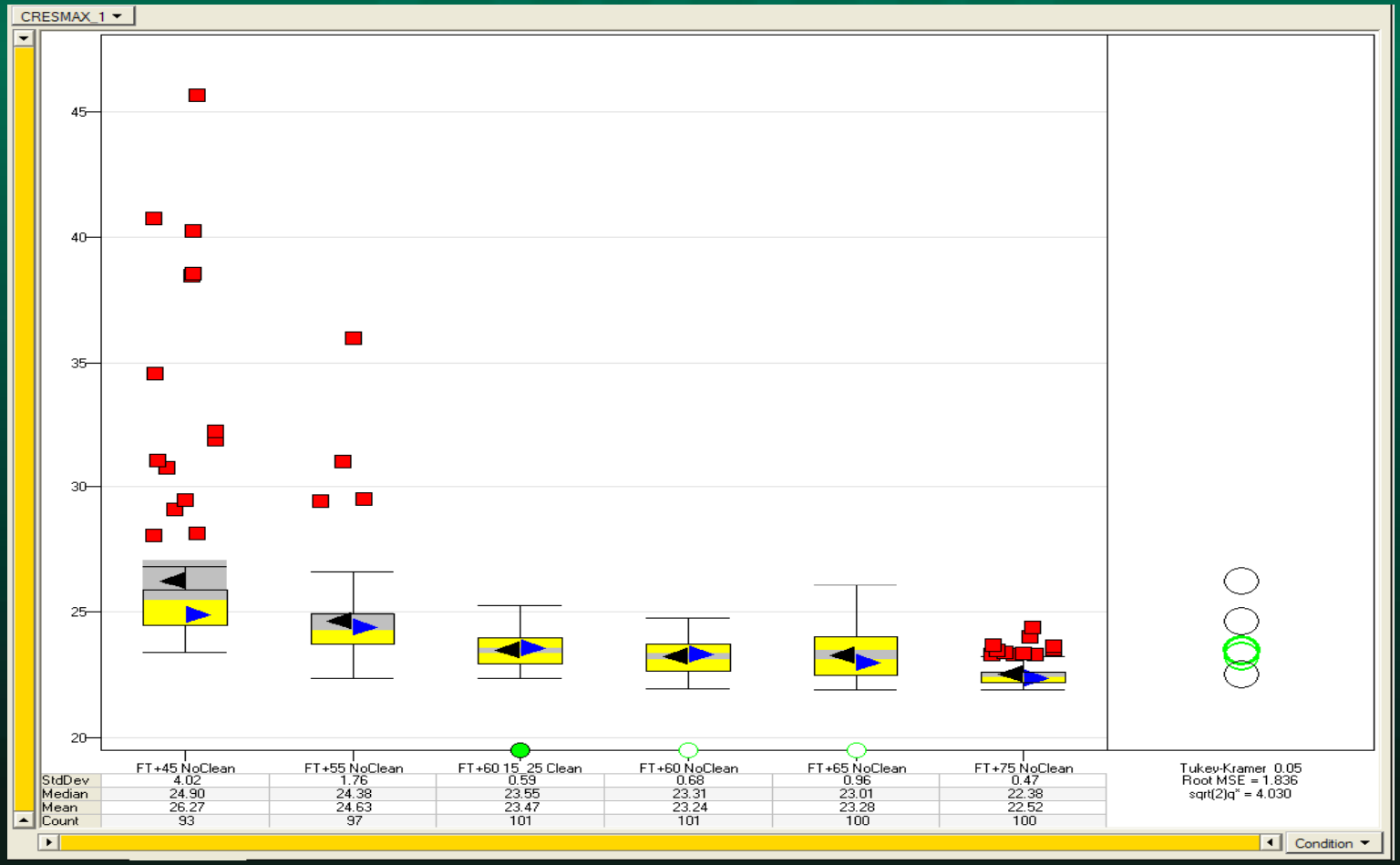
Input Variables:

- Probe Card to Probe Card
- Wafer to Wafer (Re-probe)

Output Variables:

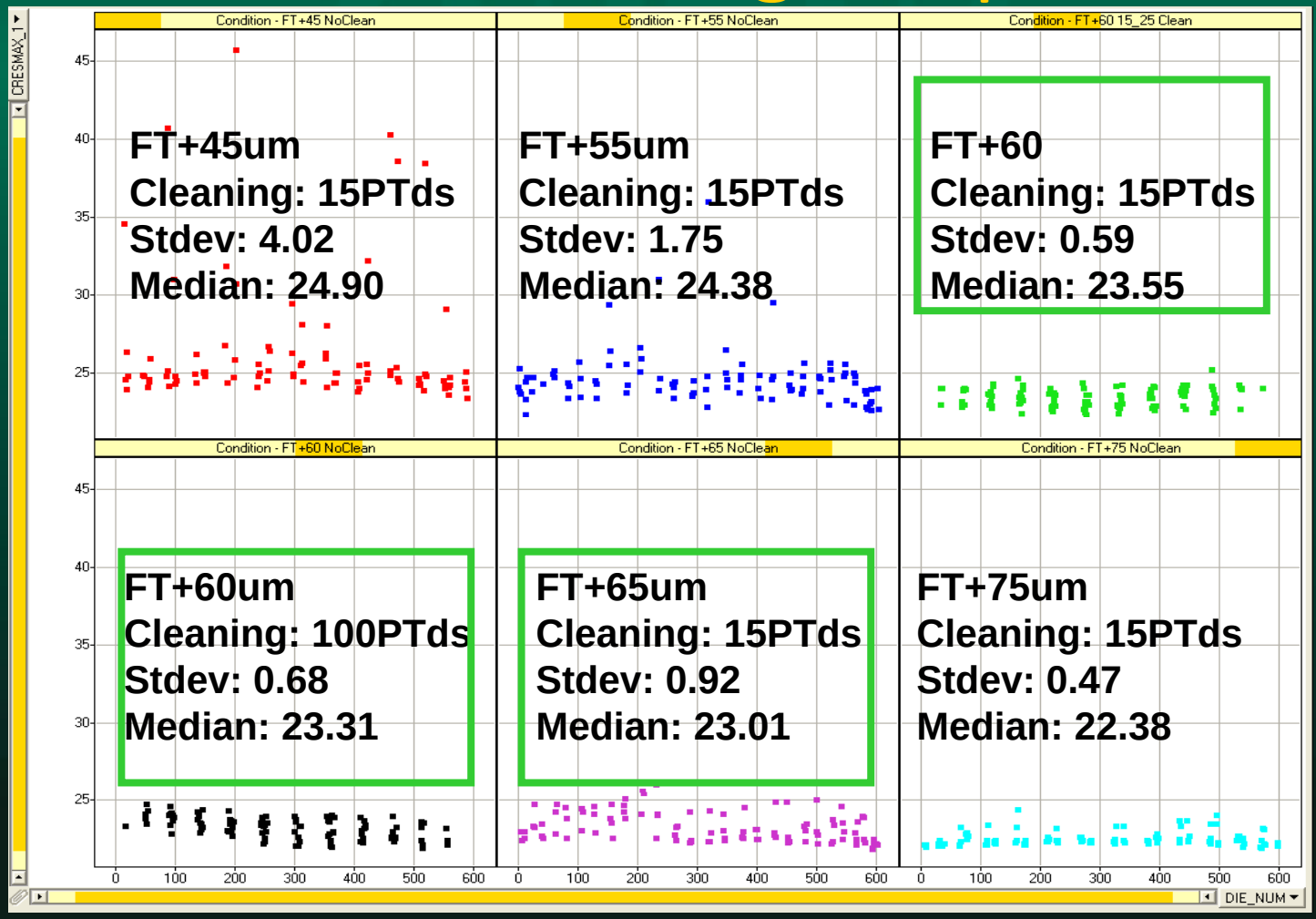
- CRes
- Yield
- Re-Probe Rate
- Throughput
- Bump Scrub Damage
- Planarity/Alignment

TQ: Effect of Over-travel on CRes



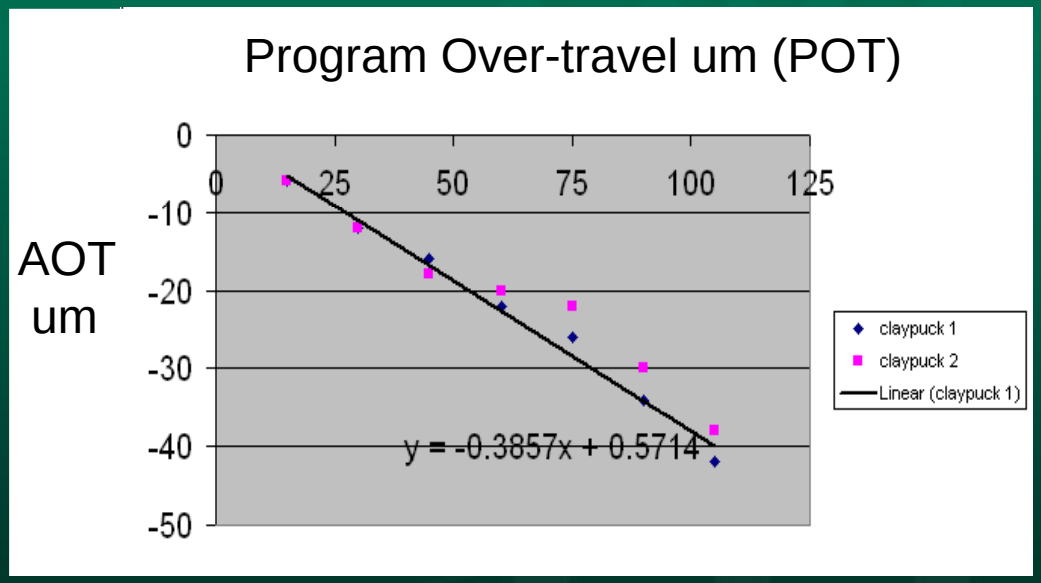
Better contact performance (low CRes) is observed as OT-over-travel increases, but minimum of 60um is needed to achieve a good stable contact.

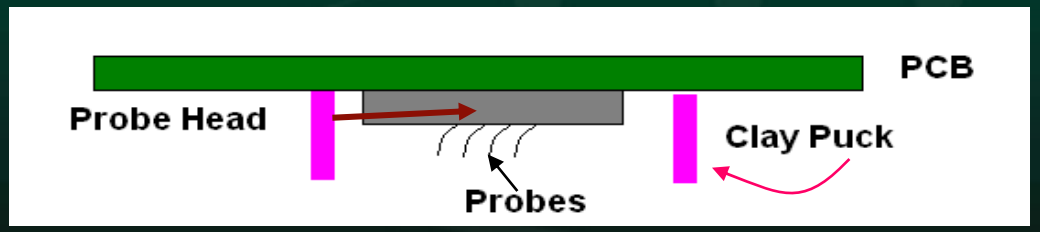
TQ: Effect of Cleaning Freq. on CRes



No statistical difference was observed between 60 and 65 um over-travel or between 15 and 100 PTds cleaning intervals, with the potential of further increasing this interval to further improves lifetime and test time.

TQ: Actual MtP Deflection in Test Cell





Dummy Wafer

Prober Chuck

- **Programmed Over-Travel (POT): The Z-movement of the prober chuck in the z-axis in the test cell.**
- **Actual Over-travel (AOT): The actual Z-movement / compression of the Multi Point Tip's micro-spring in the test cell.**

Actual MtP Deflection in Test Cell

- **Based on the in-situ "Clay Puck" tests, the actual over-travel (AOT) in the test cell was measured to be 40um with a POT of FT+100um.**
- **In other words, a programmed over-travel (POT) set at FT+100um is equivalent to 40um of actual over-travel (AOT).**
- **As a result, the current and stable programmed over-travel (POT) recipe was defined based on this characterization to within the capabilities of the MtP micro-spring deflection range and with an effective lower force required than if 100um was the AOT.**

TQ: MtP vs. CVPC Electrical Correlation

C-VPC

Wafer #1

MtP #1

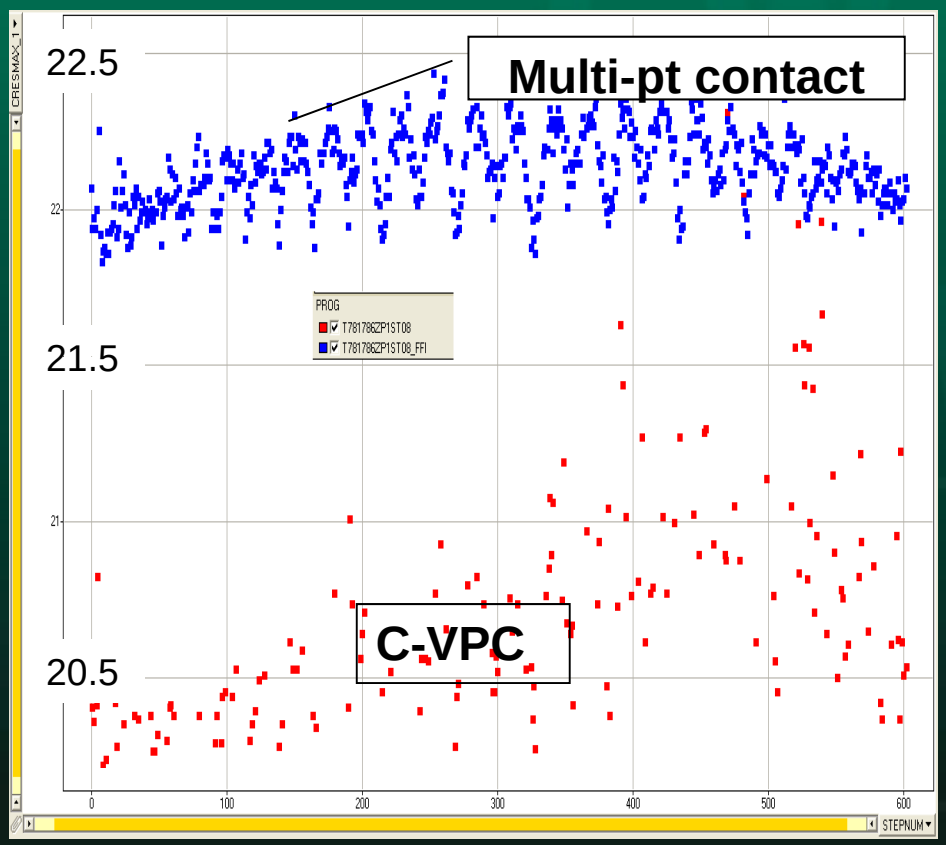
Wafer #1

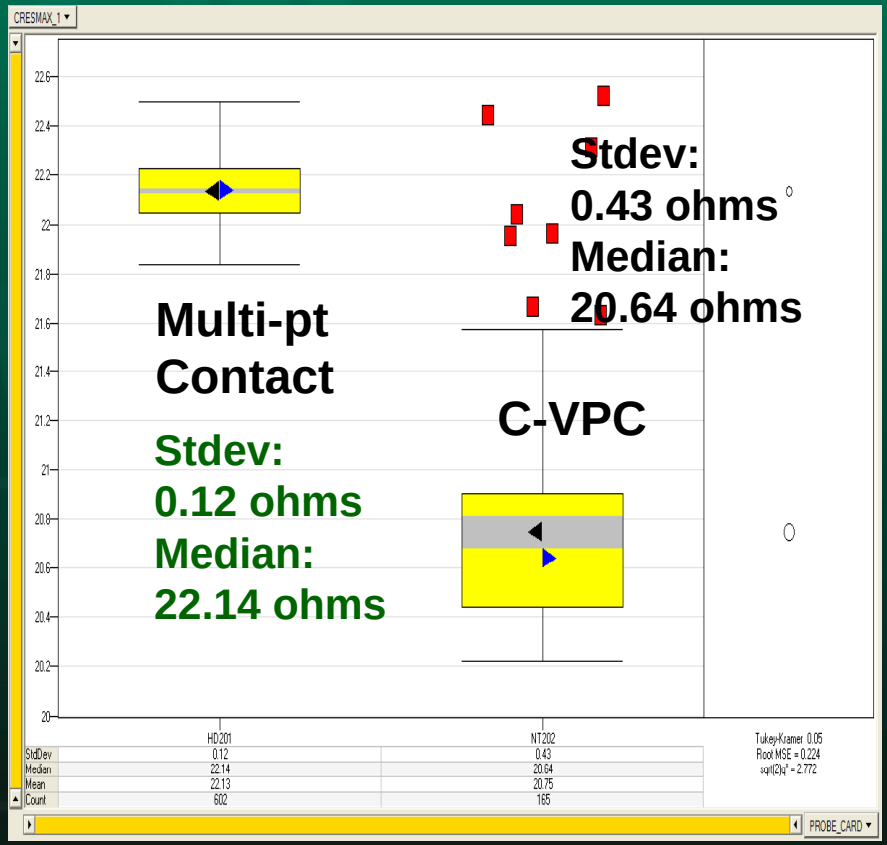
MtP#2

Wafer #1

Same wafer was probed with C-VPC and both HD2's cards
MtP-1 600/603 (99.5%) Bin to Bin correlation to C-VPC
MtP-2 597/603 (99.2%) Bin to Bin correlation to C-VPC

TQ: MtP vs. CVPC CRes Characterization

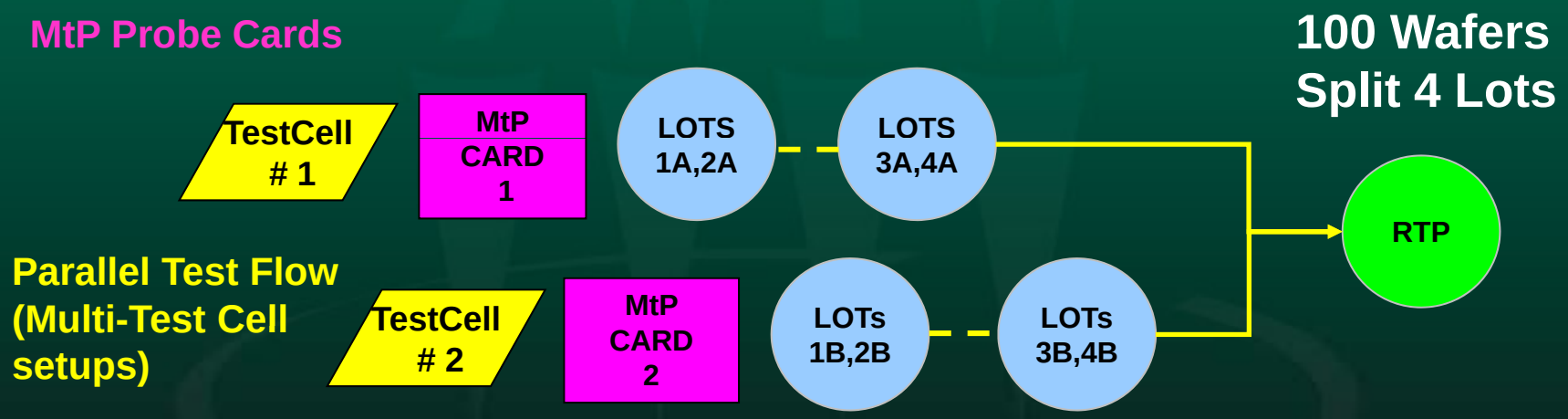




Although the CVPC shows a lower CRes median, the CRes stability or STD is much tighter than the CVPC. The higher MtP value is attributed to the way CRes is measured, which is defined by the total path resistance of the MLC/PCB/HW.

2-Production Qualification Test Flow

Objective: To validate long term stability of probe card / set-up and probe process reliability (Production Worthiness)



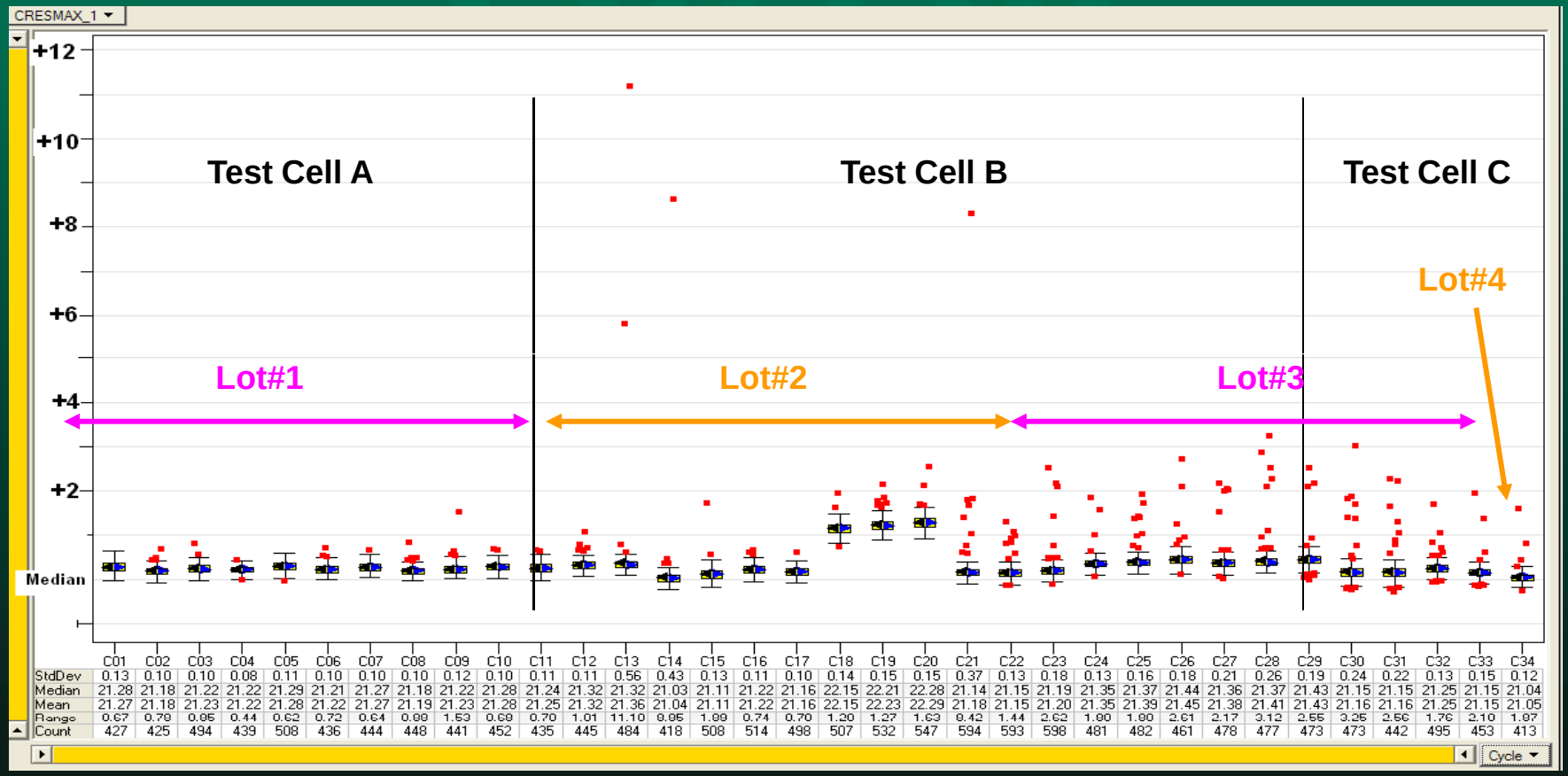
Input Variables:

- Probe Card to Probe Card
- Wafer to Wafer (Re-probe)
- Lot to Lot

Output Variables:

- CRes
- Yield
- Re-Probe Rate
- TPT
- Bump Scrub Damage
- Planarity/Alignment
- Lifetime/Reliability

PQ: MtP Production CRes Stability



	C01	C02	C03	C04	C05	C06	C07	C08	C09	C10	C11	C12	C13	C14	C15	C16	C17	C18	C19	C20	C21	C22	C23	C24	C25	C26	C27	C28	C29	C30	C31	C32	C33	C34
StdDev	0.13	0.10	0.10	0.08	0.11	0.10	0.10	0.10	0.12	0.10	0.11	0.11	0.56	0.43	0.13	0.11	0.10	0.14	0.15	0.15	0.37	0.13	0.18	0.13	0.16	0.18	0.21	0.26	0.19	0.24	0.22	0.13	0.15	0.12
Median	21.28	21.18	21.22	21.22	21.29	21.21	21.27	21.18	21.22	21.28	21.24	21.32	21.32	21.03	21.11	21.22	21.16	22.15	22.21	22.28	21.14	21.15	21.19	21.35	21.37	21.44	21.36	21.37	21.43	21.15	21.15	21.25	21.15	21.04
Mean	21.27	21.18	21.23	21.22	21.28	21.22	21.27	21.19	21.23	21.28	21.25	21.32	21.36	21.04	21.11	21.22	21.16	22.15	22.23	22.29	21.18	21.15	21.20	21.35	21.39	21.45	21.38	21.41	21.43	21.16	21.16	21.25	21.15	21.05
Range	0.67	0.79	0.95	0.44	0.62	0.72	0.64	0.89	1.53	0.69	0.70	1.01	11.10	9.95	1.99	0.74	0.70	1.20	1.27	1.63	9.42	1.44	2.62	1.90	1.90	2.61	2.17	3.12	2.55	3.25	2.56	1.76	2.10	1.97
Count	427	425	494	439	508	436	444	448	441	452	435	445	484	418	508	514	498	507	532	547	594	593	598	481	482	461	478	477	473	473	442	495	453	413

Continuous production lots ran during production qualification checkout demonstrated contact stability over many consecutive wafers probed. This validated the process recipe stability and margin for production fan out.

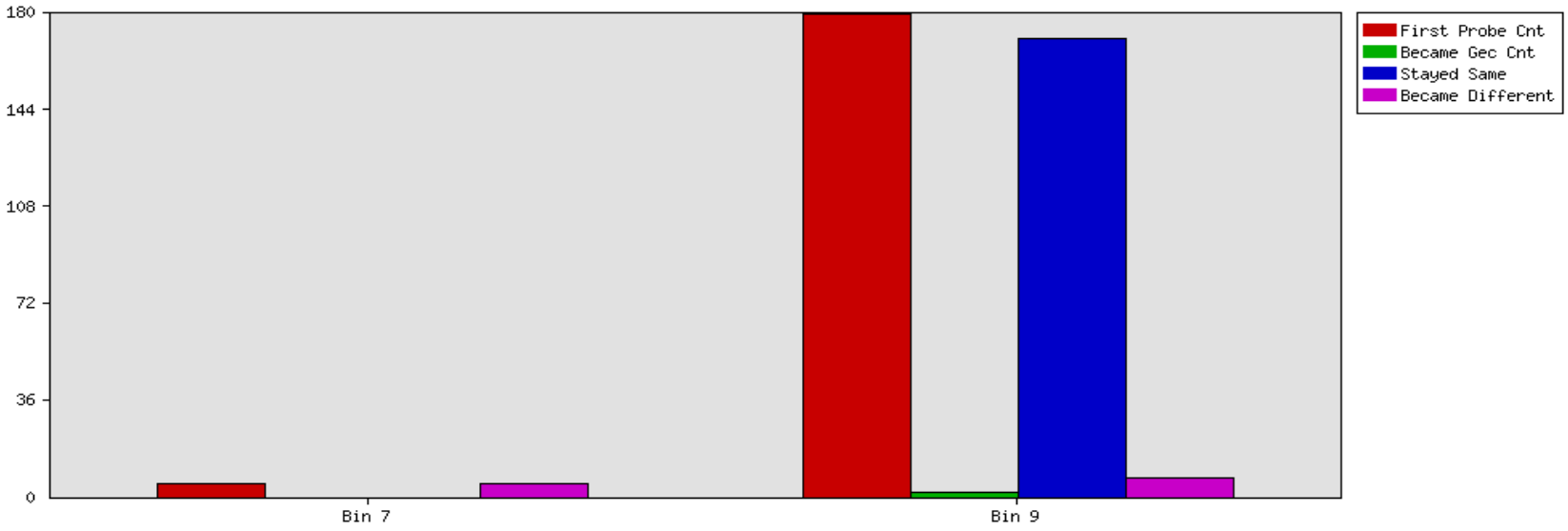
PQ: MtP Electrical Test Reliability

Reprobe Data for MULTIPROBE T781786AFFI15 10501

Reprobe Rules:

- BIN | 7 | TOTAL > 5 | INCLUSIVE | High IO Open
- BIN | 65 | PERCENT > 5 | INCLUSIVE | High CRES
- BIN | 9 | PERCENT > 1 | INCLUSIVE | High VDD Shorts
- BIN | 6 | TOTAL > 5 | INCLUSIVE | High VDD Open
- BIN | 8 | PERCENT > 1 | INCLUSIVE | High IO Shorts

	Total Die	to Gec	% to GEC	same Bin	% same Bin	diff Bin	% diff Bin
Bin 7	5	0	0.00	0	0.00	5	100.00
Bin 9	179	2	1.12	170	94.97	7	3.91
Total	**184**	**2**	**1.09**	**170**	**92.39**	**12**	**6.52**

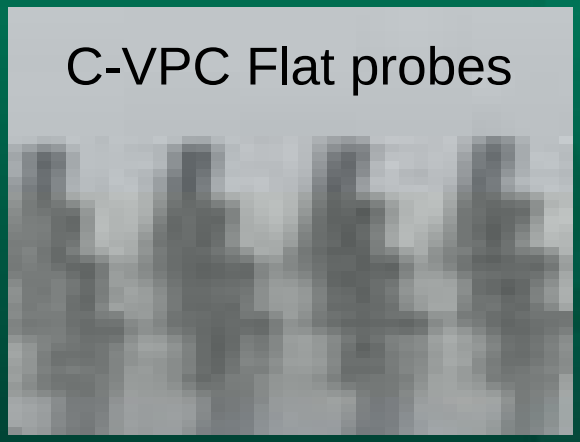


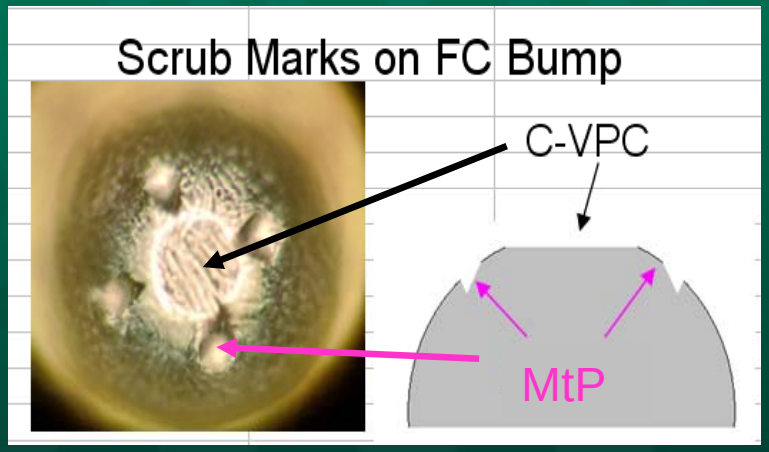
-Re-probe rate is very low w/ an average of 0.12% out of 40K die probed.

-Yield recovery from re-probe related to contact was extremely low.

-Implies: mis-contact is negligible and 1st Pass Yield is maximized

C-VPC vs. MtP: Effect on Bump





CVPC Flat probes compress or impact the apex of the bump. Bump height damage ≥ 1/3 of the bump is not desirable. Also, CRes not as stable thus, more frequent cleaning to remove compacted debris is required.

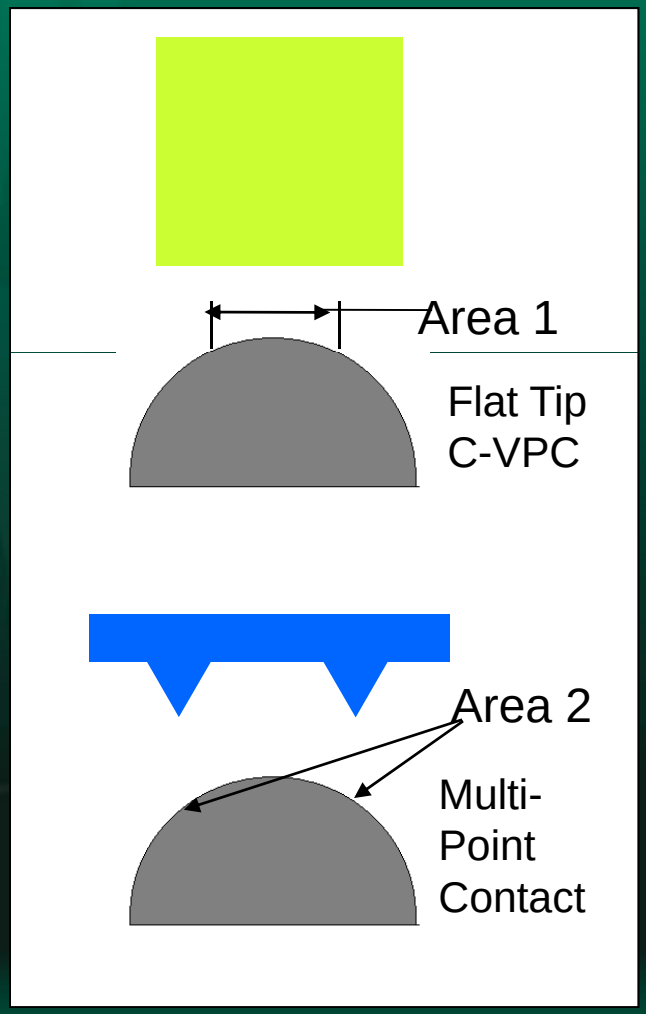
Multi-tip contacts create small dimple marks away from the apex of bump; not affecting bump height. The pointed tips better penetrate the bump's oxide layer, resulting in stable CRes using much lower probe force.

Key Learning: “Probe Physics”

- The pressure between any two (2) surfaces in contact with each other is a function of force and contact area.

Force = Pressure x Contact Area

- Multi-Point tip enables a lower force per probe creating adequate pressure to break into the surface of the bump to make a reliable electrical contact.
- To achieve the same effect, the corresponding flat tip of a C-VPC approach would requires a larger force to collapse the surface oxide of the bump apex
- The electrical contact surface area; however is comparable where the sides of the pyramid provide sufficient surface area for electrical conduction.



Summary of MTP Attributes

- Self alignment of tips to bump. Well centered
- No reflow of bump after probe is required
- CRes < C-VPC
- Force/Pin < C-VPC
- Cleaning ≤ C-VPC
- Planarization not required
- Cost Of Ownership < C-VPC (Multi-Site)

Metric	C-VPC	Multi-Point Contact
Clean Freq.	50 PTds	50 PTds or Higher
Alignment (um)	18	30um (Self-Aligns)
Cres STD Ω	0.43	0.12
Force/pin @OT (gm)	12 (Typical)	9 (Worst Case)
Repairability	Single Pin Repairable	Depends on damage
Bump Damage	Flattens apex	4 small dimples on side
CCC (A)	~1A	~1A
Min. Pitch (um)	135	170
Max OT	203	100
Planarization	Required	Not Required
COO	Single Site	MultiSite

Conclusion

- Multi-tip Probe contacts with the “piercing” action, demonstrated a stable and production worthy contact mechanism for Flip Chip bump probing using a lower force solution than the C-VPC

- The lower force exhibited by the MtP probe enables a path for a viable high pin-count / multi-site configurations probe solution with a lower Cost Of Ownership (COO)

- When this technology successfully completes the Production Qualification phase and if meets TI COO targets, then it will be deployed to test floors as production volumes warrant.

Acknowledgements

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