IEEE SW Test Workshop
Semiconductor Wafer Test Workshop

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San Diego, CA

Challenges of CIS high parallelism test

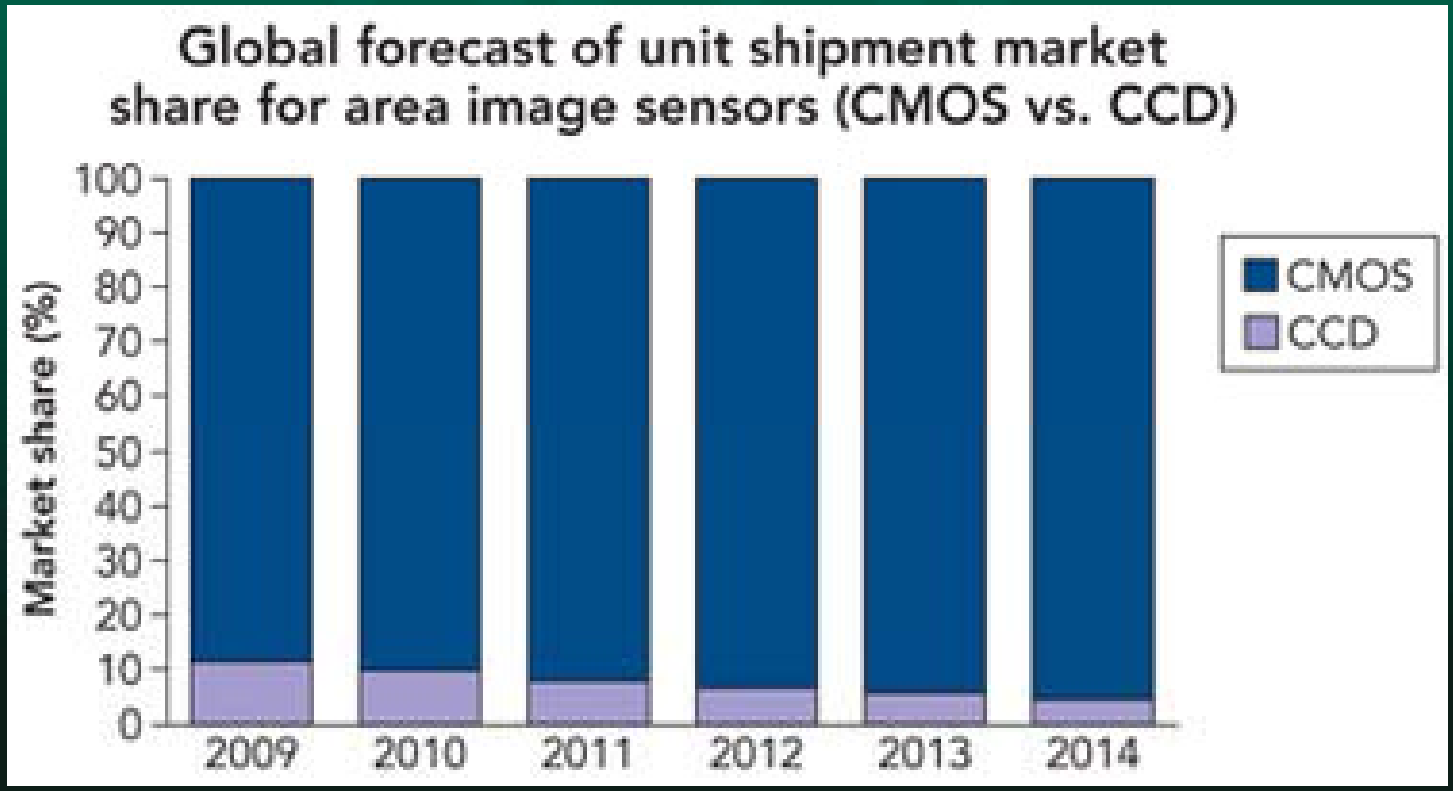
Larry Levy

FormFactor Inc.

Agenda

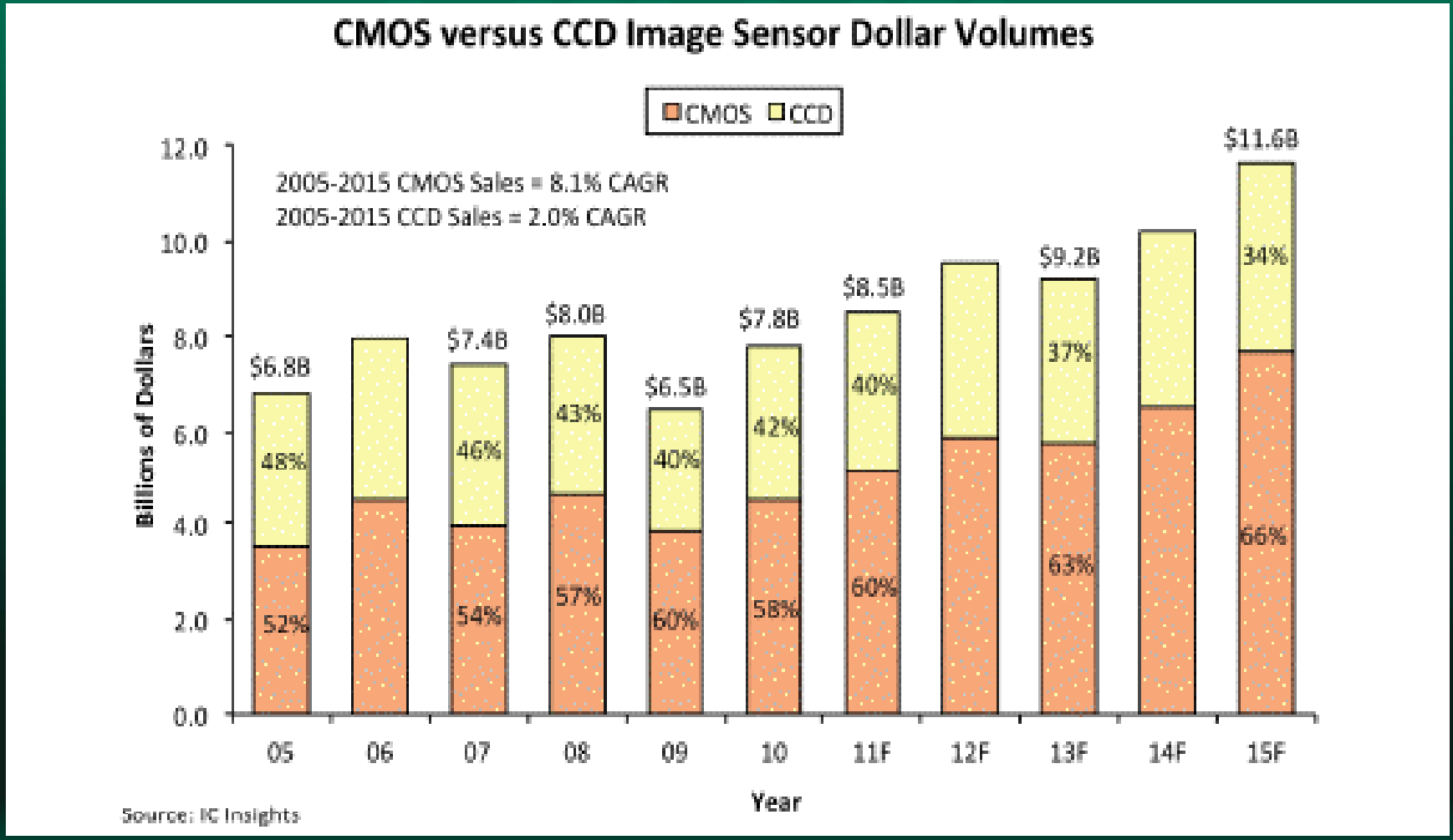
- CIS Market
- High parallelism
- CIS sort test challenges
- Summary

CIS vs CCD Units

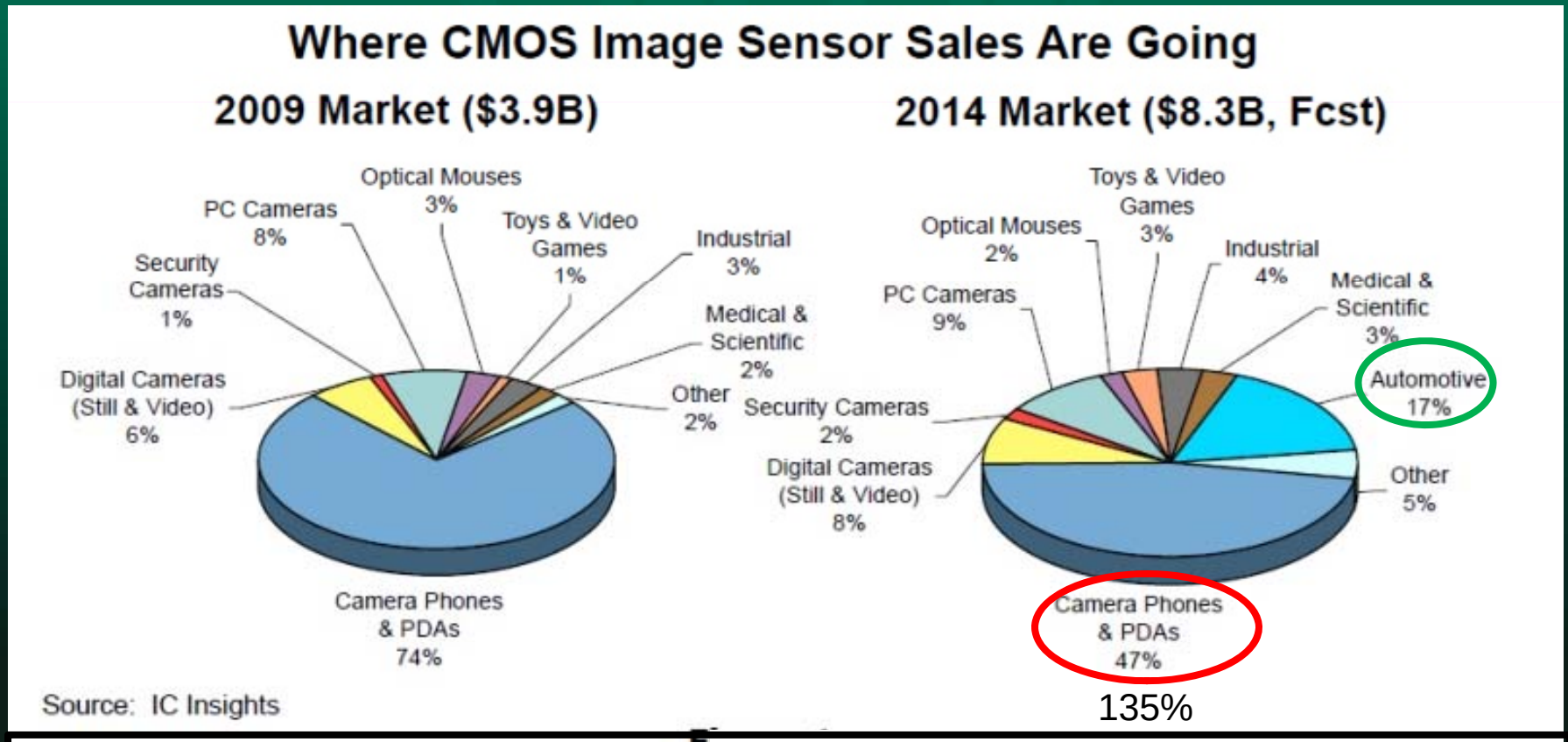


. Source: iSuppli, October 2010

CIS vs CCD Revenue



Growing CMOS Image Sensor Market



135%

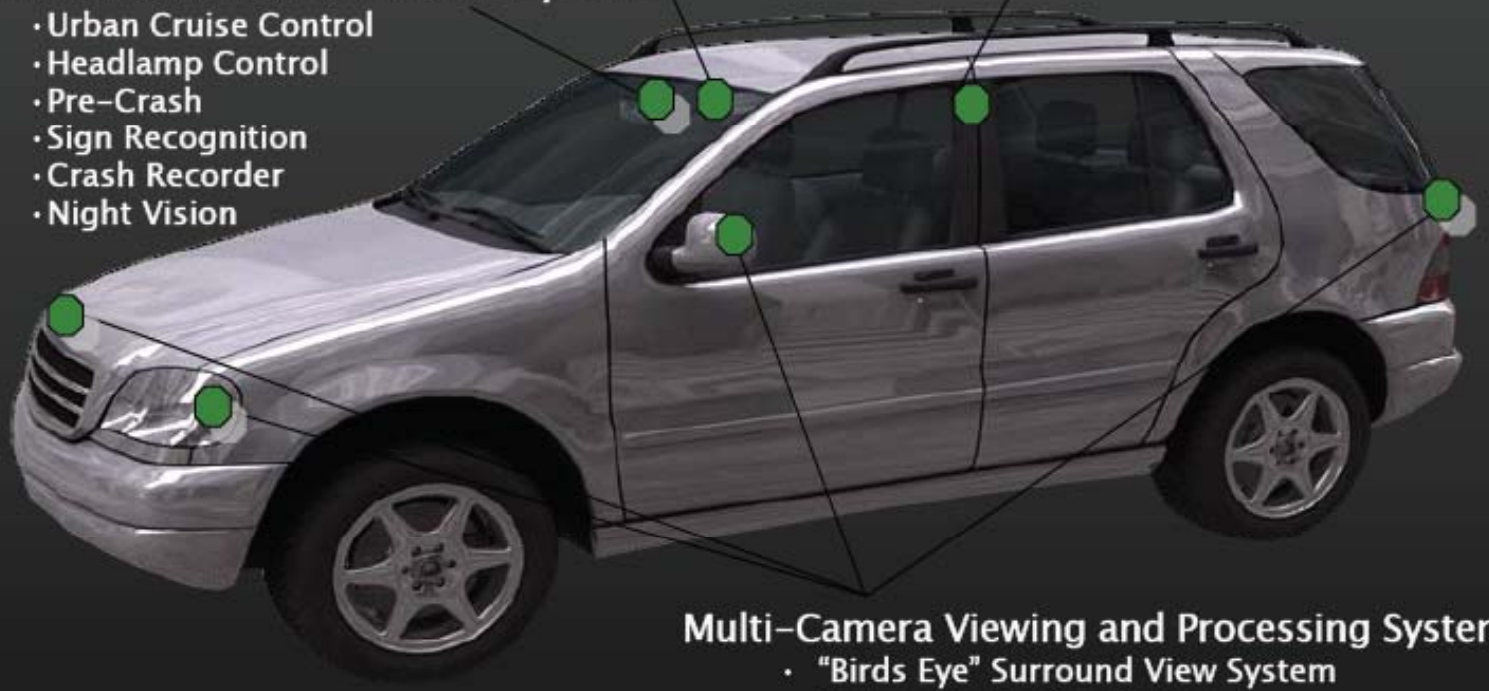
CMOS image sensor sales will grow 13 percent to a record high $5.1 billion in 2011, as more CMOS sensors are used in camera phones, digital cameras, automotive systems, and embedded webcams in laptops and tablet computers, according to researcher IC Insights

Automotive applications

Multi-Function Interior Camera System
- Occupant Classification
- Driver Recognition
- Drowsy Driver
- Crash Recorder

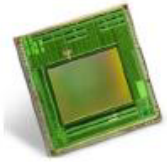
Multi-Function Rear Seat Camera
- Passenger Viewing
- Occupant Classification

Multi-Function Forward Camera System
- Urban Cruise Control
- Headlamp Control
- Pre-Crash
- Sign Recognition
- Crash Recorder
- Night Vision



Multi-Camera Viewing and Processing System
- "Birds Eye" Surround View System
- Automatic Parking System
- Lane Change Assist

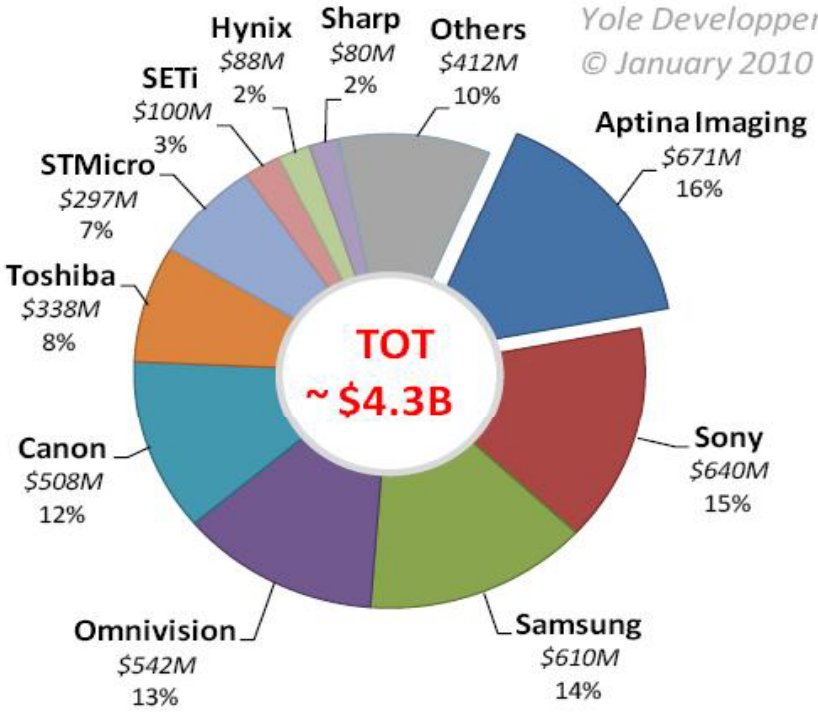
Source: Micron Automotive Segment Marketing



CMOS image sensors Revenues

- 2009 Market Shares -

(Based on estimated business value of 'first-level-packaged' CIS sensors)



Yole Developpement
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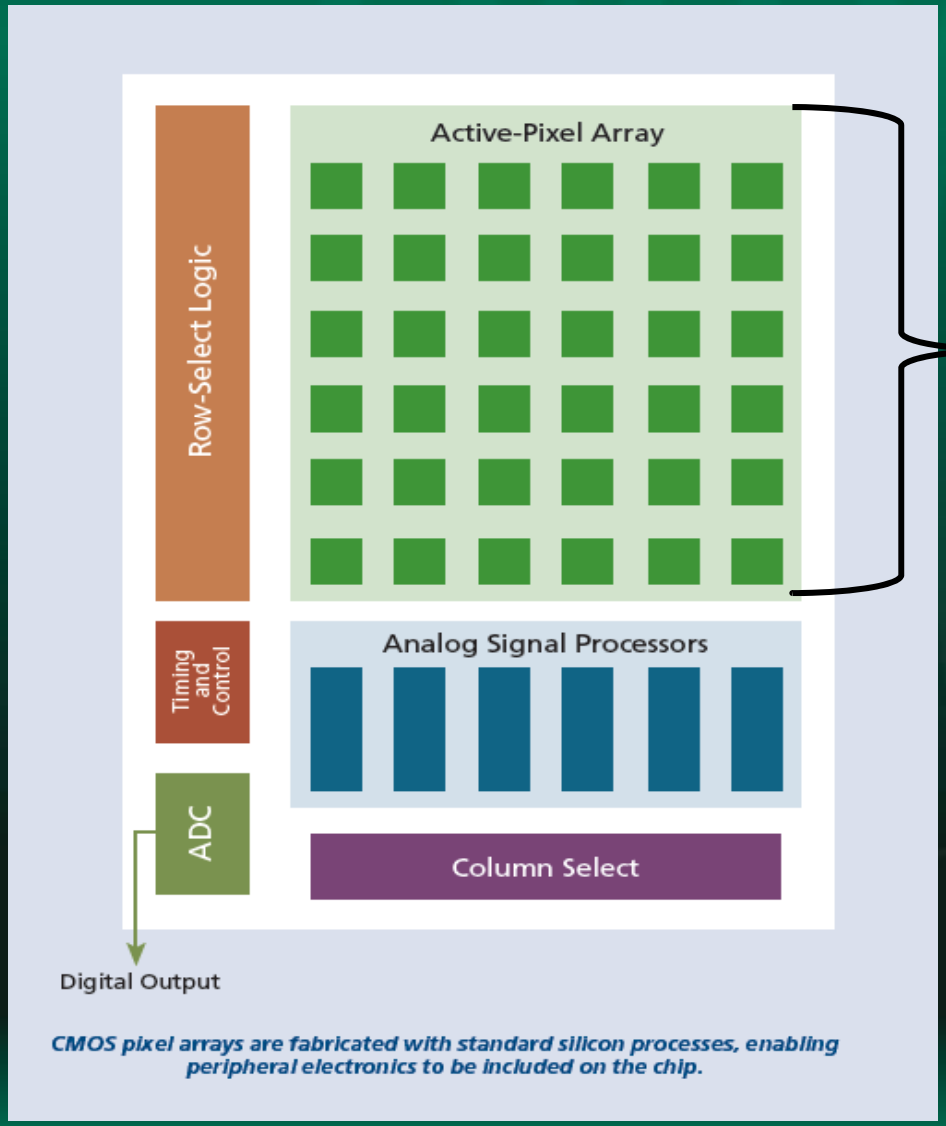
CMOS Image Sensors Revenues:
2009 Market Shares ($M)

	Company	2009	share
1	Aptina Imaging	$671	16%
2	Sony	$640	15%
3	Samsung	$610	14%
4	Omnivision	$542	13%
5	Canon	$508	12%
6	Toshiba	$338	8%
7	STMicro	$297	7%
8	SETi	$100	2%
9	Hynix	$88	2%
10	Sharp	$80	2%
	Others	$412	10%
	TOT	$4 287	

* Others include Cypress, Kodak, Pixart, SiliconFile, PixelPlus, GalaxyCore, Melexis, Himax Imaging, Panasonic, NIT, CMOSIS, Forza Silicon, e2v, Awaiba, SuperPix, Canesta, ViTi, Foveon, KunShan RuiXin Micro, Crysview, Anafocus, Altasens, Novatek, Pixim and Daisa

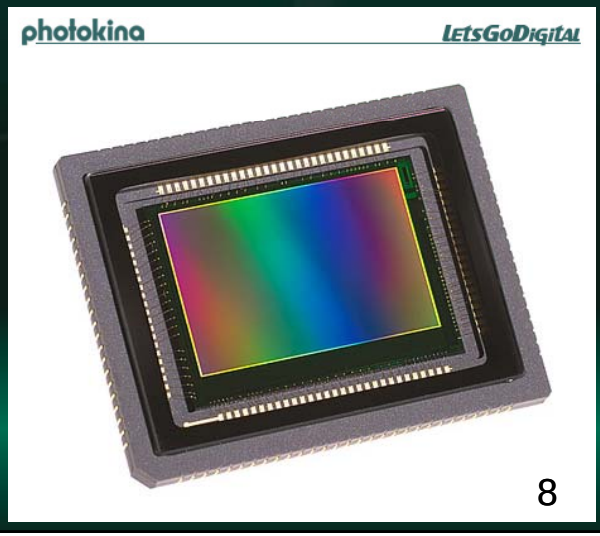
- Sony has grown fast, mainly thanks to the success of the introduction of its BSI CMOS sensor in the **camcorders and DSC / SLR camera's space along** with its high-end mobile camera module activity
- Samsung is also growing, both in the low-end and high-end CMOS image sensor space
- Canon pioneered in the introduction of CMOS sensor technology in its high-end DSC / SLR and video camcorder cameras product line

Common CIS Device Layout



Light Sensitive Area

Can have 3 sort steps
- Light test
- Dark test
- Logic test



Common CIS Testers

Magnum IPC

Yokogawa

Advantest T2000

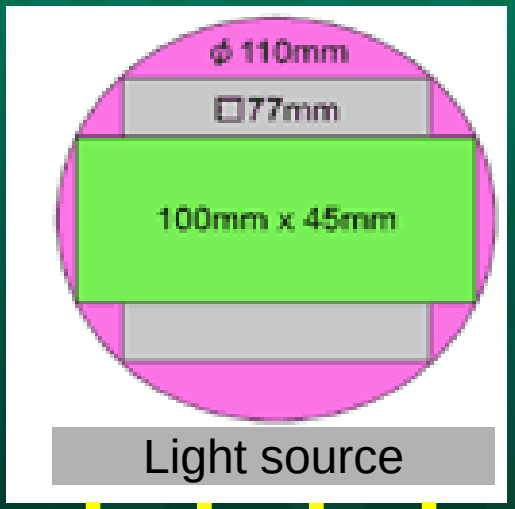
CIS Attributes

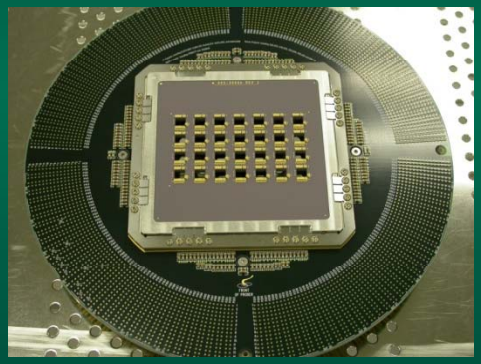
	DRAM	Flash	SOC	CIS
Test time increasing with density	Yes	Yes	?	Yes Pixels
Move to higher //	2 to 6 TD	1TD	slowly	>30TD
Majority market suppliers	4	5	Many	7
High speed	Yes	No	Some	Yes
Power supply levels	Few	Few	Many	Many*
Major products	Computing	Consumer	Consumer	Consumer
Average pixel count	N/A	N/A	N/A	Increasing
Average pixel size	N/A	N/A	N/A	Decreasing

*CIS devices seem to be more noise sensitive

X-Sectional Image of FormFactor CIS Probe Card

160mm x 150mm light source now available





Why is CIS Moving to Higher Parallelism?

	# of testers	# of probe cards	Cost/good die	Capital reduction*
x8	66	69	$0.0393	Base
x16	43	45	$0.0320	$9M
x16 Matrix Array	31	32	$0.0257	$23M
x32 Matrix array	13	14	$0.0154	$37M

Sematech model

x32 > 50% reduction in cost of test

Cost of Ownership Model Assumptions

30K 200mm wafers/Month

1,000 DPW

1% Yield increase due to MEMs probe card fidelity

30% test time reduction for x32 tester

* Capital is calculated as if adding all new testers and probers

Parallelism vs Touch Downs

	# of testers	# of probe cards	Cost/good die	Capital reduction*
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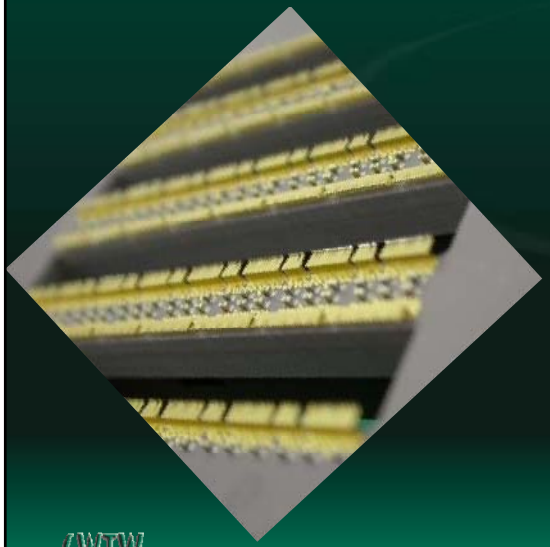
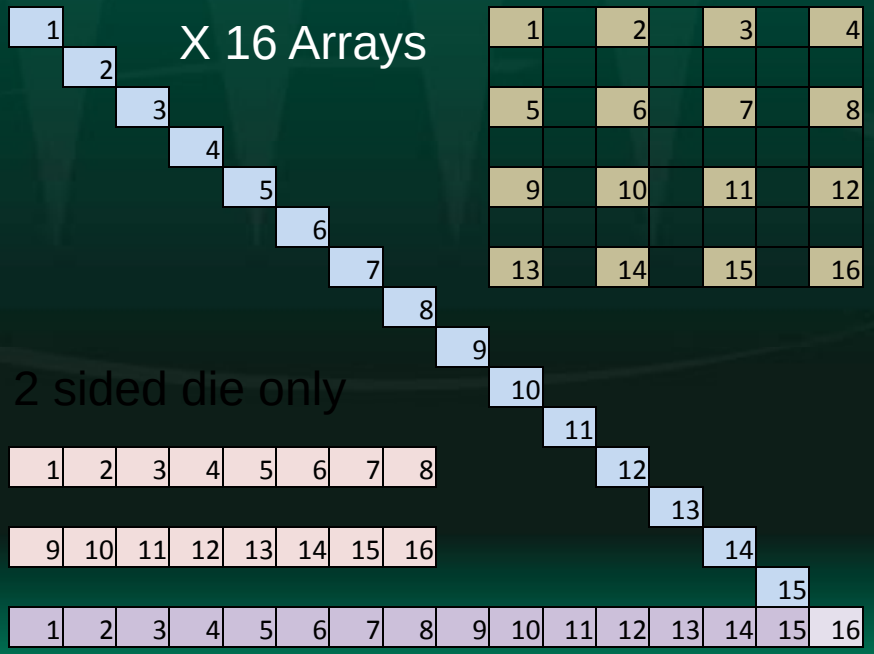


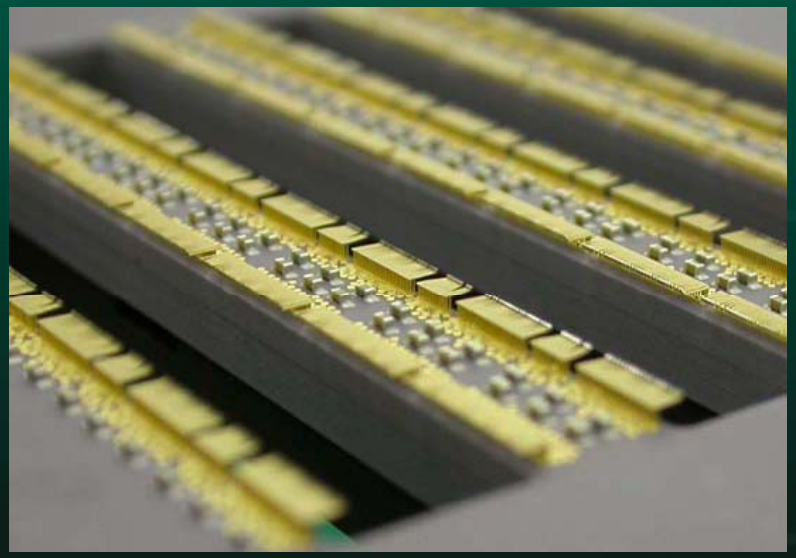


Touch Down Efficiency- 5 to 6mm Square Die

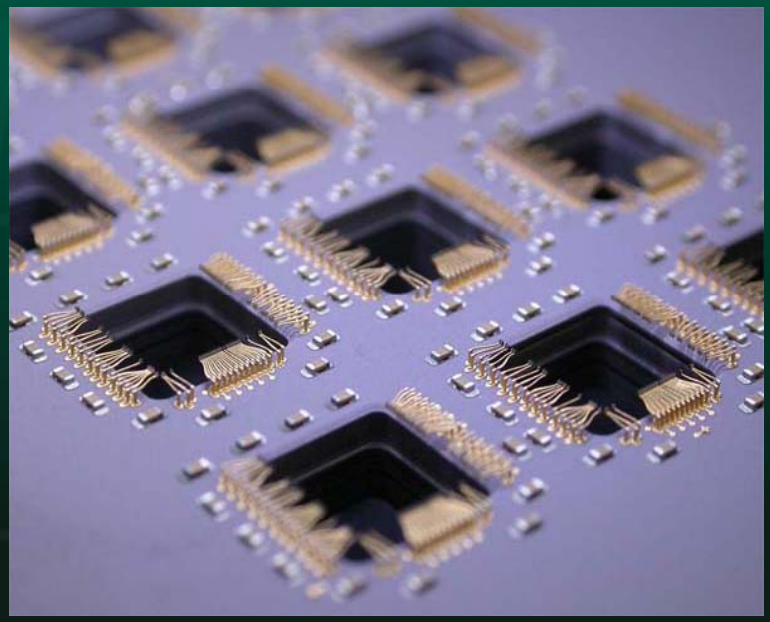
//	Array (Skip R & C)	TD	TD reduction %
32	8x4	32	70%
32	4x8	32	70%
30	6x5	35	67%
30	5x6	36	66%
25	5x5	36	66%
28	4x7	38	64%
28	7x4	38	64%
24	4x6	40	63%
24	6x4	42	61%
16	4x4	56	48%
8	4x2	105	2%
8	2x4	106	1%
8	8x1	107	Base
8	8x1 Solid Diagonal	107	Base

CIS Sort Testing Trend

Springs on 2 sides
Skip row

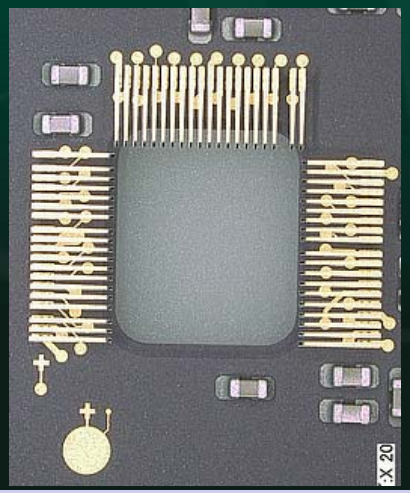


Springs on 3 sides
Skip row and column



CIS Sort Test Challenges

- **Three sided devices have unbalanced force**
  - X 16 1.6Kg unopposed force (with **low force** 5 grams/spring x 20 springs/DUT)
  - X 32 3.2Kg unopposed force
    - Impacts scrub mark

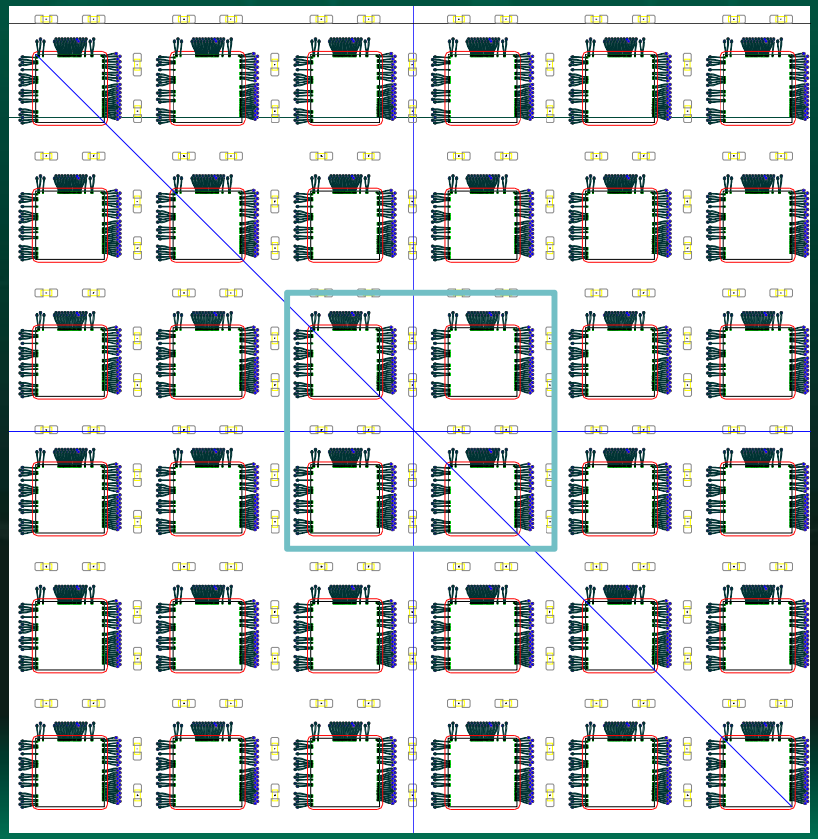


Many customers increase OT to try to get larger scrub marks

CIS Sort Test Challenges

- **Complex design from inner DUTs**

X 32 Matrix array



CIS Sort Test Challenges

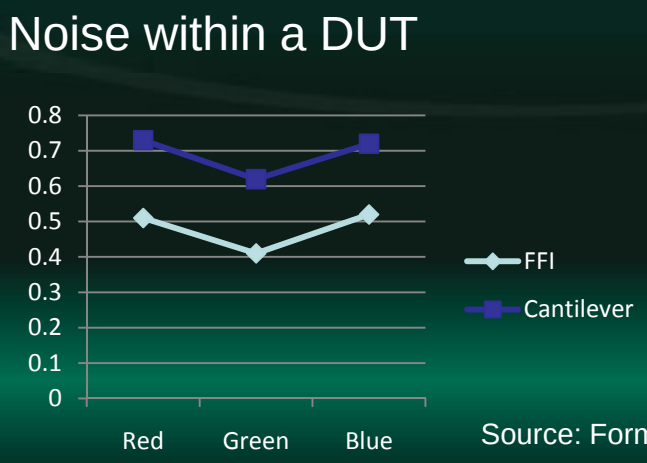
Light Fixed-Pattern Noise (PRNU)

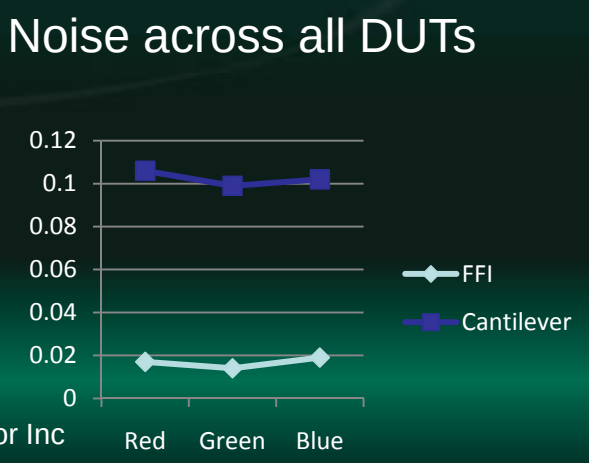
Origin : non-uniformities on pixel response, threshold variations, gain and off-set differences.

Countermeasure :
- look-up tables
- technology dependent
- lay-out/design dependent
- off-set cancellation

CIS Sort Test Challenges

- **Light fixed pattern noise sensitivity**
  - Many power supply levels
  - Noise both within a DUT and across DUTs can cause longer test times and require more frame captures
  - Customer data shows MEMs cards reduce noise by ~ 40% within a DUT and >5 time lower across all DUTs





Source: FormFactor Inc

CIS Sort Test Challenges

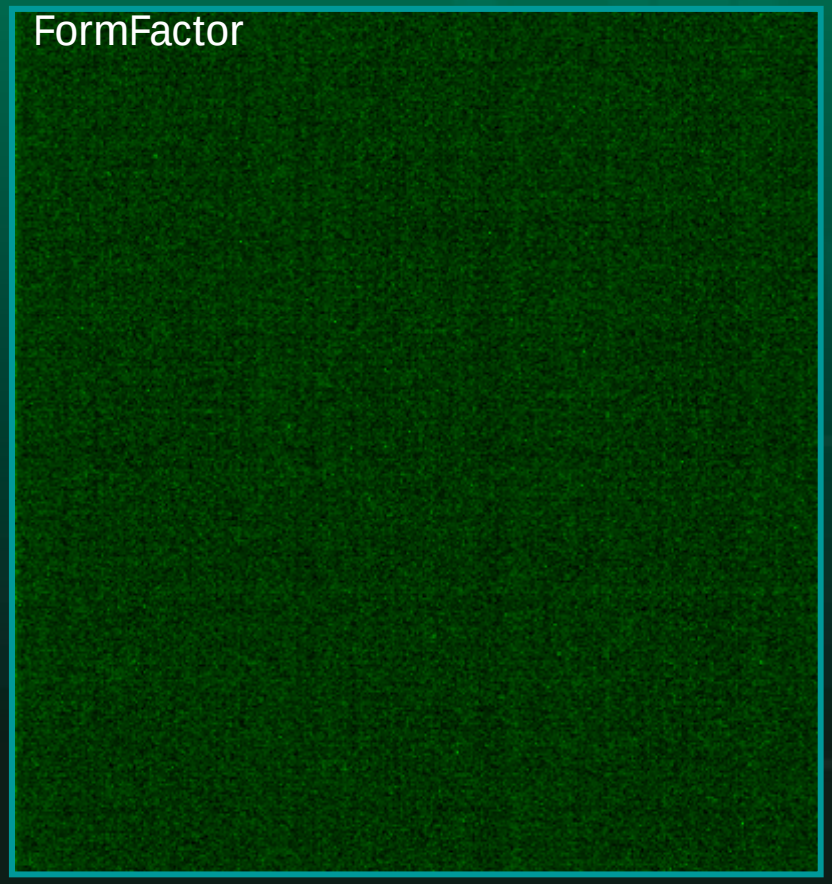
Dark Fixed-Pattern Noise

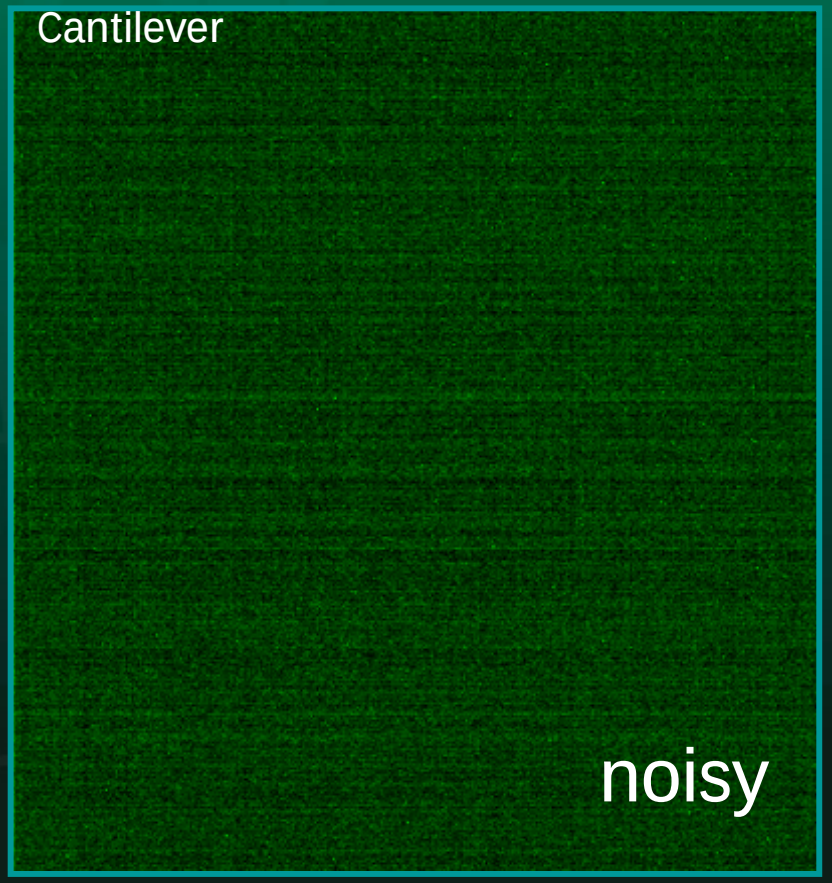
Origin : non-uniformities on dark current generation, threshold variations, gain and off-set differences.

Countermeasure :
- low temperature
- technology dependent
- lay-out/design dependent
- off-set cancellation

Albert Theuwissen ISE 2011

CIS Sort Test Challenges





* Capture Image (1frame capture, Dark 7lsb)

Source: FormFactor Inc

CIS Sort Challenges

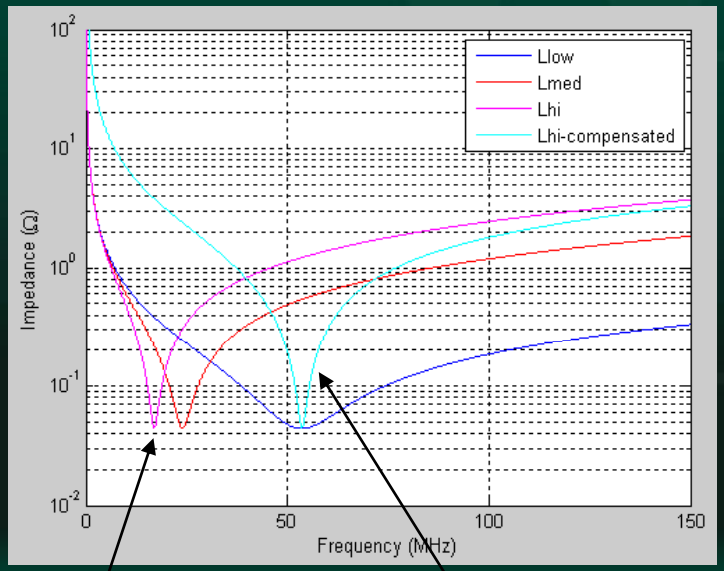
- **Noise sensitivity**
- **Decoupling capacitors provide low Power Delivery System impedance over range of frequencies**
  - Smaller capacitors used for high frequency (high F_{res})

This part shows 19 caps/
DUT on the ceramic

Decoupling Capacitors Near the DUT

- **Capacitors mounted on boards add loop inductance to Equivalent Series Inductance (ESL)**
  - Greater distance from DUT increases loop inductance
  - Decreases effective Fres of capacitor
  - Causes resonant peak to be sharper, reducing effectiveness of capacitor to reduce PDS impedance
- **Reducing capacitance to move back Fres to offset effect of loop inductance is less effective because of the increase in sharpness of resonant peak**

Always best to keep loop inductance low!

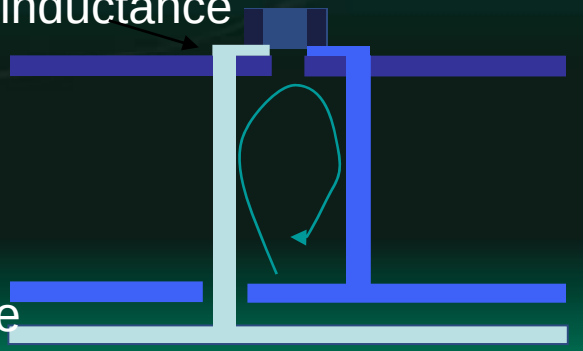


Higher loop inductance

Compensating high loop inductance with smaller capacitance

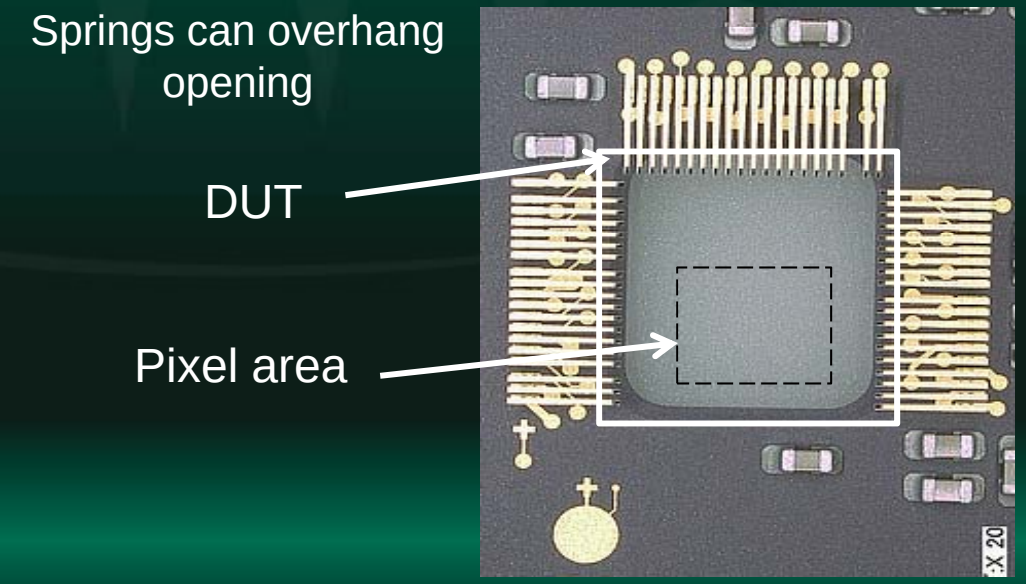
Low loop inductance

High loop inductance

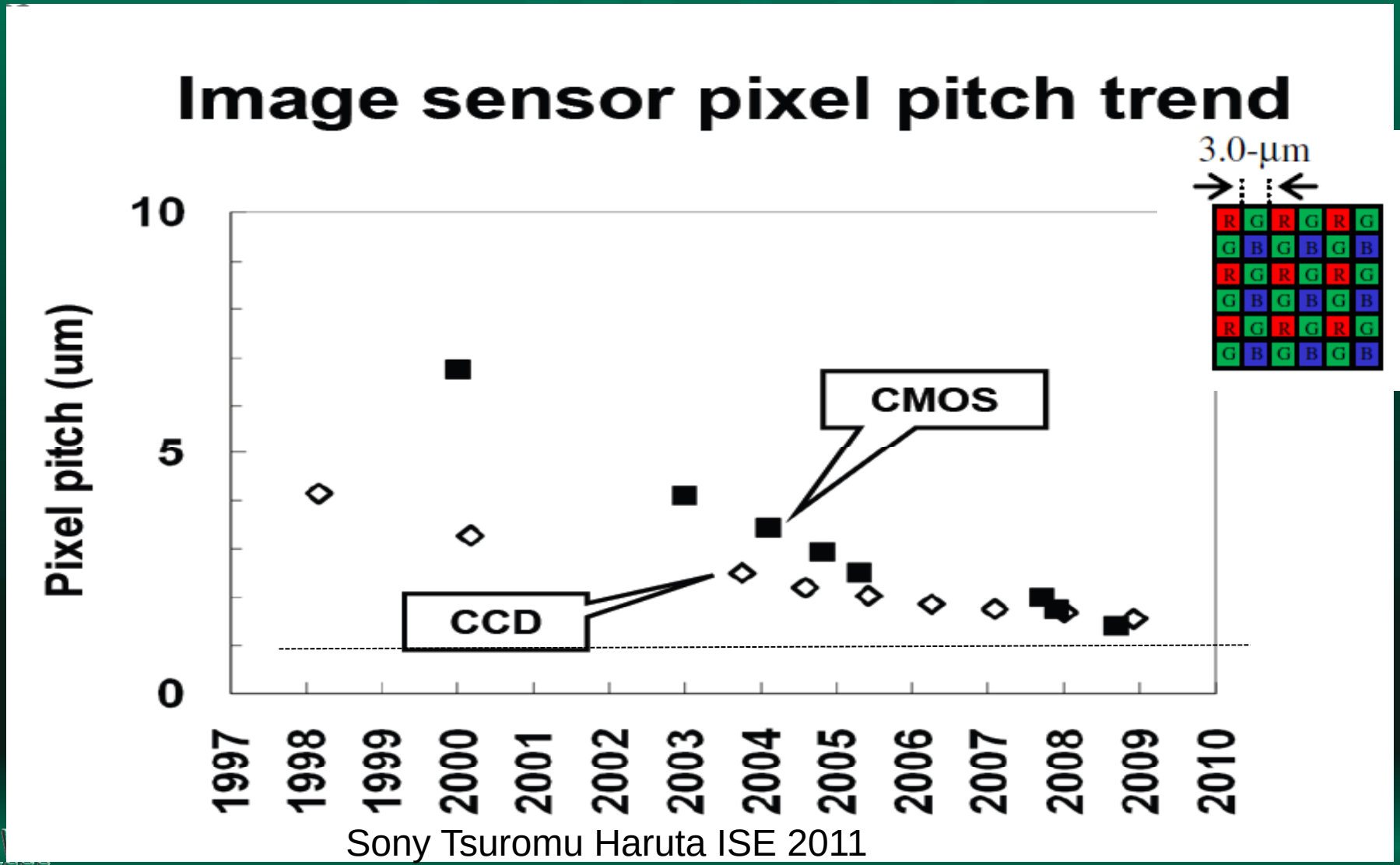


CIS Sort Test Challenges

- **Uniform light intensity**
  - Design for largest possible window opening
    - Avoid reflection from side walls
  - All hardware must be non reflective



Higher Pixel Counts Drive Smaller Pixel Sizes

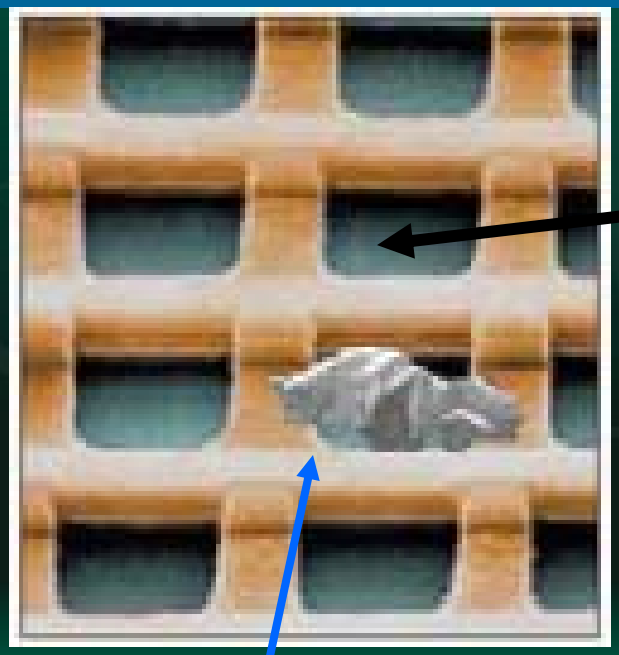


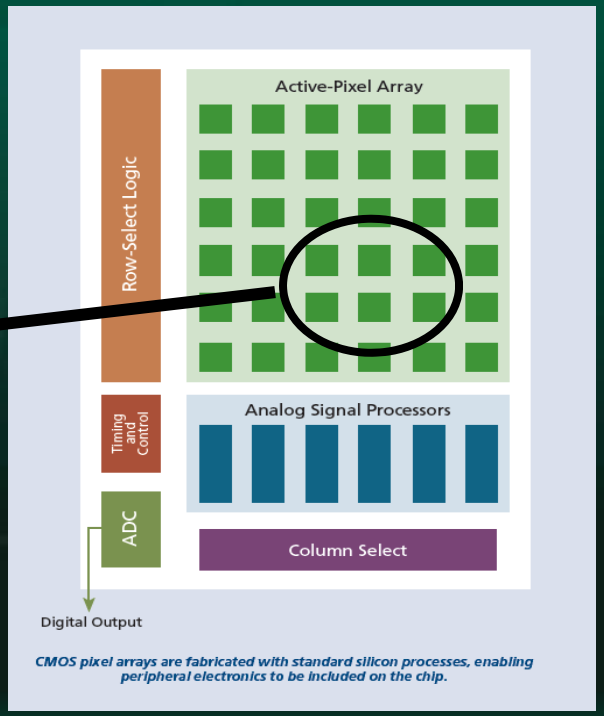
Sony Tsuromu Haruta ISE 2011

CIS Sort Test Challenges

- **Particle sensitivity**
  - Smaller Pixels are more prone to particle defects
  - Requires low particle generation sort solution

Greatly enlarged pixels on an image sensor.





Shadows caused by particles cause pixels to fail

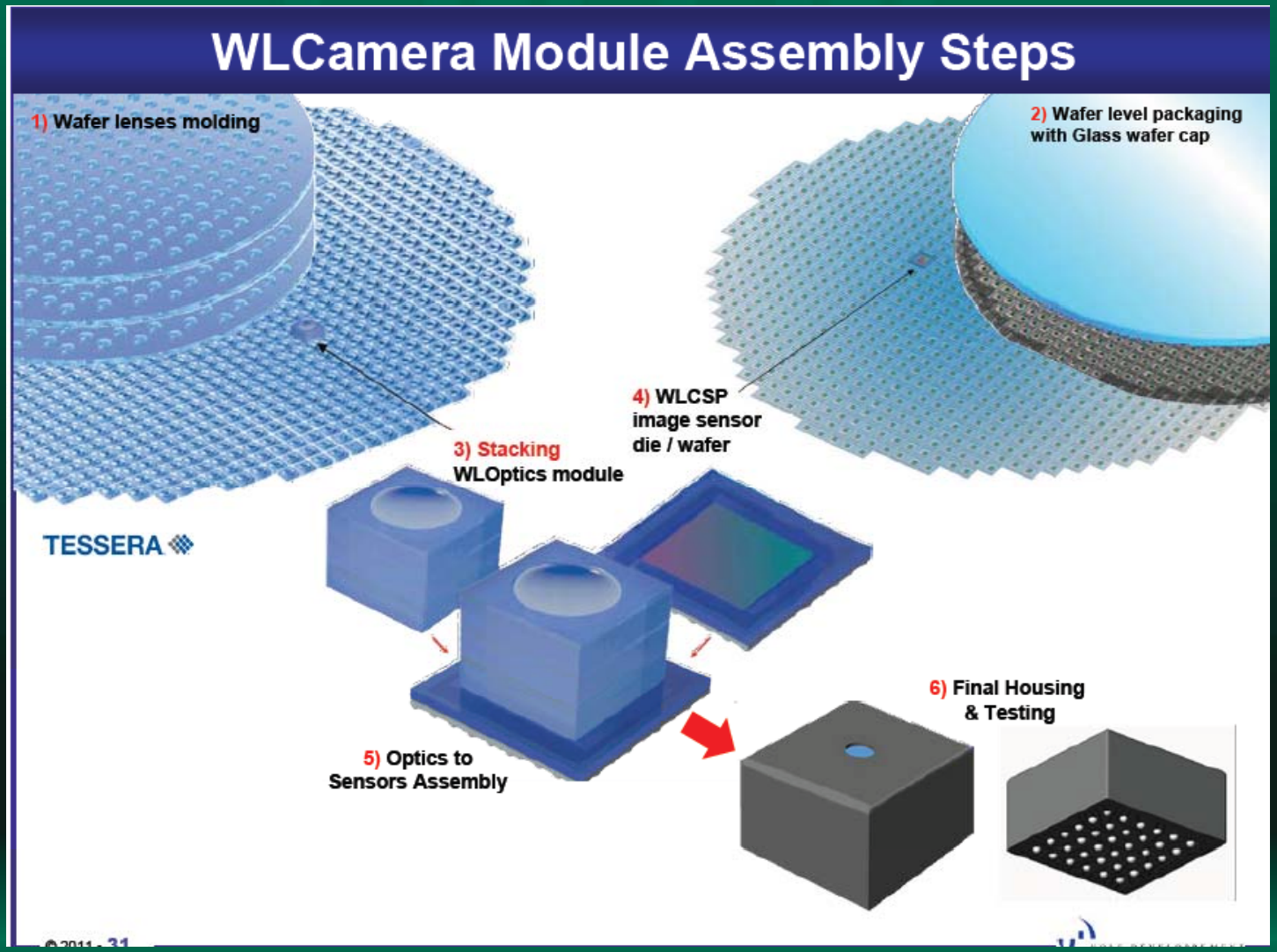
CIS Sort Test Challenges

In-Stat, has projected that by 2016, up to 70 percent of image sensor interfaces in the electronics industry would use the high-speed camera serial interface (CSI) developed by the Mobile Industry Processor Interface (MIPI) Alliance

- **MIPI requirements**
  - Currently running at >800 mbps
  - Clock and 2 lines (serial interface)
- **Projections for the number of LVDS per DUT increasing over time**
  - Number of pads to be probed remains fairly constant
- **Industry roadmap extends beyond 1.2 gbps need**
  - Device rise time can limit frequency

CIS Sort Test Challenges

Wafer sales and WLCSP are driving more test at sort



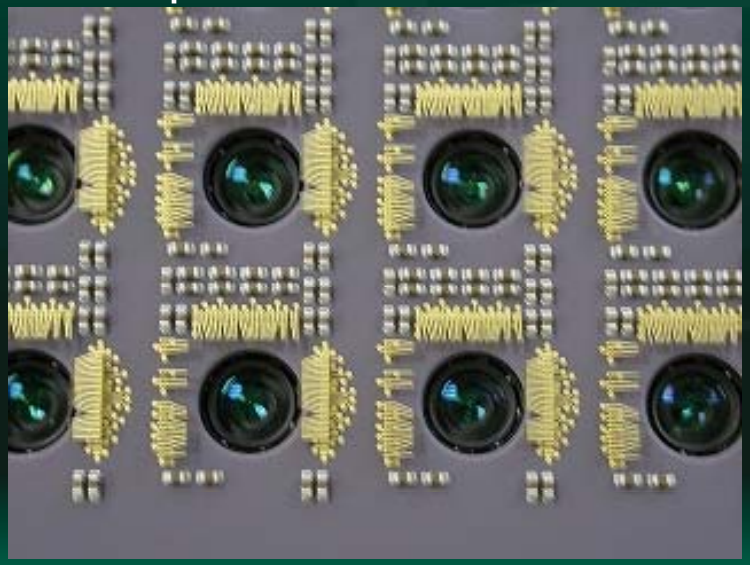
CIS Sort Test Challenges

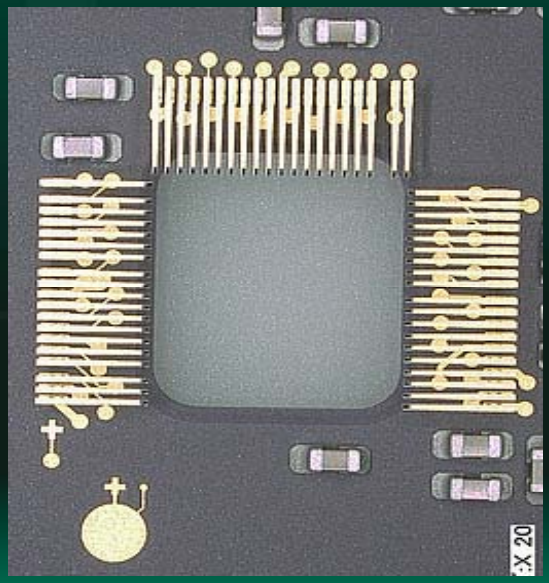
Wafer sales and WLCSP are driving more test at sort

Lens Module and Diffuser options becoming more common

Installation of lens or diffuser must be at prescribed distance to the device

Lens must fit inside of where probes are attached

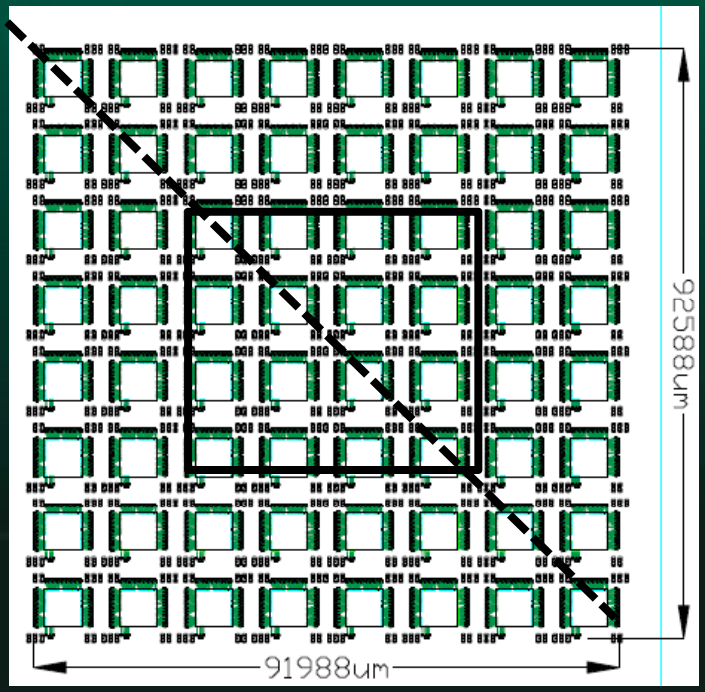




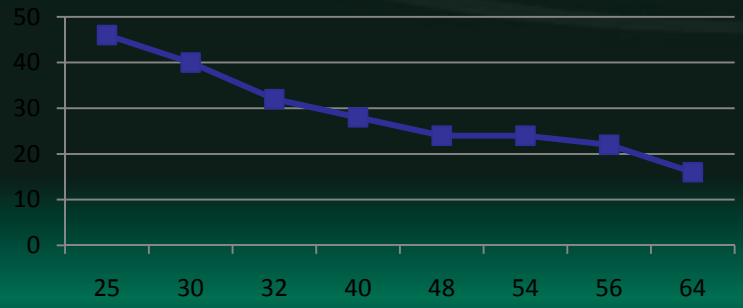
CIS Sort Test Challenges

- **X 64 development**
  - TD's reduced by half from x32
  - Requires larger light source
  - Increased design difficulty
    - In ceramic and PCB
  - MIPI targeted at 1.2 gbps

~130mm Dia



Touchdown study for development device



Summary

- **CIS sort test has some unique requirements**
- **Increased parallelism offers lower cost of test**
- **Choice of probe card/ spring type technology can make a difference**
- **Road blocks exist to increased parallelism**
  - Light source area may be a limitation in the future
  - Probe card design is more difficult due to openings in the card
    - Will likely limit frequency
- **Future innovation will be required to extend parallelism capability for CIS**

Thank You