IEEE Semiconductor Wafer Test Workshop

June 10 to 13, 2012 at Rancho Bernardo Inn, San Diego, CA

Submitted by …

Jerry Broz, Ph.D., General Chair of IEEE SW Test and IEEE Senior Member
Ira Feldman, IEEE Member and Executive Committee of IEEE SFBA Nanotechnology Council

San Diego, CA: Wafer level test and probe technologists met in San Diego, CA, from June 10 to 13, 2012 for the 22nd Annual IEEE Semiconductor Wafer Test Workshop (SW Test) at the Rancho Bernardo Inn. This annual IEEE / CPMT sponsored workshop brings together technologists, engineers, and managers as well as sales and marketing professionals involved with all aspects of probe technology and wafer level testing. This year, SW Test had a total of 357 attendees from 15 countries with 28% of the attendees from outside the US for a global gathering of leading technologists and related suppliers. The 2012 Workshop drew a great mix of end-users (~31%) and suppliers / vendors (~69%) for the technical program and exhibition during the three day event. This unique workshop promotes a friendly networking environment between colleagues, new attendees, salesman / marketers, and students. The grassroots agenda provides for plenty of time to have informal interaction and discussions.

The SW Test Program began with a Sunday tutorial from Doug Sottaway of Intel Corporation on the basics of Process Control Systems with applicability to wafer level sort. Mr. Sottaway discussed the strength of decision making based on process feedback for wafer sort improvements. This tutorial was a valuable follow-on to the Statistics Tutorial that was made by Lance Milner, also of Intel, at SW Test 2011.

On Sunday night, Matt Nowak, Senior Director, Advanced Technology, Qualcomm CDMA Technologies, provided an informative keynote presentation entitled "*Emerging High Density 3D Through Silicon Stacking (TSS) – What's Next?*" Mr. Nowak began with examples of Thru Silicon Vias (TSVs) technology that have been in high volume production for image sensors for several years now; but at a significantly lower density than for 3D packaging. The great interest in 3D packaging is driven by the "mega-economic" trend for the electronics industry, that predicts ~29% per year cost reductions and pushes new lower cost solutions, especially when wafer fabrication processes become more expensive. As demands for mobile devices continue to dominate the market, critical issues of improved performance, greater power efficiency, continued miniaturization, and cost reduction must be addressed.

Mr. Nowak expanded on the three key reasons behind 3D TSV packaging – power, form factor, and economics. Power management is not just the concern over battery life of a mobile device. As mobile devices continue to gain more functionality, there is an upper limit on how fast they can operate and how many processor cores can be active at a time. As an example, mobile phones can dissipate about 3 Watts of power before the device becomes "too hot handle", i.e., handheld case temperature exceed 40 C. In many applications, especially mobile devices which everyone wants to be smaller or which require a larger battery to operate longer, there is a concern over the 3D volume of semiconductor package not just the planar 2D size. From the economics side, the consumer wants lower cost devices with better performance; regardless of the manufacturing costs. 3D packaging helps to address all of these challenges and, as such, Qualcomm has been building 3D parts with up to five stacked die.

Today the limit to stacking is economics based upon yield, cost of test, and ability to repair defects once stacked. To control costs, Qualcomm has examined using two die from older process nodes in a 3D package versus building a single die in the latest process node. This approach can accelerate time to market (when a newer process node is not yet ready) or where the die is extremely large (resulting in very low initial yields at the newer process node).

The industry has developed a long list of concerns in regards to implementing 3D packaging using TSVs which include reliability testing, processing, design for memory die on logic die, product concerns, and TSV technical challenges. Mr. Nowak highlighted a few areas that still remain the most problematic: (1) Testability – test methods and needed infrastructure are still being developed and no solutions exist for repair after assembly, e.g., how to correct for an assembly process defect or a defect in each die discovered after the stack is assembled; (2) Yield & High Volume – many yield issues, including process sensitivities, only become apparent once products are ramped to high volume; and (3) Design Challenges – device and chip set interactions that may impact product reliability must be considered for 3D package design. For example, it is undesirable to have the hot spots (areas that tend to heat up faster) on each die aligned in the stack; or, there may be similar localized mechanical stresses on each die that interact once stacked resulting in device failure or reliability problems.

Mr. Nowak concluded by saying that the semiconductor "game" is changing; it is no longer about architecture and differentiation in the future will come from packaging. It is really the system software and chipset architecture that will drive the product. In fact, over two-thirds of the engineers at Qualcomm are software engineers and the 3D packaging of stacked chips provides a "new bag of tricks" for chipset architects. Momentum is building in the development of TSV technology and associated infrastructure to make 3D packaging; however, the biggest challenge currently is the high prices from suppliers.

In terms of product development, Mr. Nowak expects to see memory stacking (especially for higher value data center applications and to replace the package-on-package stacks of memory on microprocessors) followed by 2.5D interposer applications, then logic-on-logic applications and finally 3D stacks side-by-side on interposers. These developments will present plenty of challenges in stacking silicon and opportunities to keep the industry quite busy. Matt Nowak's keynote entire presentation is available for download on the SW Test website (http://www.swtest.org).

On Monday morning, Dr. Jerry Broz, SW Test General Chair, welcomed the attendees to the 22st Annual SW Test Workshop. Dr. Broz reviewed a number of SIA and WSTS statistics; however, since Intel and AMD withdrew from WSTS and SICAS was discontinued after Nanya Technology, Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) and United Microelectronics Corporation (UMC) withdrew, the semiconductor industry lost definitive sources of capacity and utilization data, a key component in determining current and near term industry conditions.

The VLSI Research probe card market overview (released in May, 2012) showed that the total probe card revenue was up slightly in 2011, a gain of ~17% (from ~$999M in 2010 to ~$1170M in 2011). The top three revenue generating probe card suppliers saw a change for the first time in almost 10 years – (1) Micronics Japan (MJC); (2), FormFactor, Inc. (FFI); and (3) Japan

Electronic Materials (JEM). Of the top five probe card suppliers, MicroProbe reported the greatest percentage growth while FormFactor experienced the largest decrease in revenue from 2010.

Dr. Broz announced that the IEEE William R. Mann Student Travel Grant was awarded to Mr. Soheil Khavandi from the University of Nevada, Reno. This grant supports undergraduate or graduate student participation at IEEE ITC or IEEE SW Test (one grant per conference per year). After the Chairman's Welcome to Attendees, the technical program kicked-off and the excellent podium presentations covered various facets of the wafer test process from *Process Improvements for HVM* to *New Probe and Contactor Technologies* to *Fine Pitch Probing Challenges*. The next three days were filled with a broad technical program; with 5-hours of supplier exhibits (which did not compete with the technical sessions), and a Hawaiian Luau Social Event to promote friendly networking amongst the international attendees.

Individual highlights from the technical program included a discussion by Doron Avidar (Micron – Israel) for process improvements using "ghosting" for touchdown reduction for alternate site sharing. Understanding key issues of overtravel control with advanced probe cards was discussed by Tommie Berry (FFI) in a collaborative effort with Freescale Semiconductor. Bernd Bischoff (Texas Instruments – Germany) discussed pad aluminum thickness effects for process control, cleaning optimization, and probe card lifetime extension. Stevan Hunter (ON Semiconductor) presented continuing investigations into bond pad cracking under harsh probing with three different probe card technologies. Kong Meng Hui (ISS-NUS – Singapore) discussed using of artificial intelligence concepts for interpreting wafer maps. Ira Feldman (Feldman Engineering Corp.) discussed the test challenges and possible solutions for the transition to 450 mm. Dr. Raffaele Vallauri (TechnoProbe – Italy) introduced a new vertical MEMS solution for high current, low pitch applications. Gert Hohenwarter, Ph.D., (Gatewave Northern) outlined fine pitch high performance needle probe concept using novel micro-plating technique. Jose Horas (Intel Mobile Communications - Germany) presented a study focused on 28nm mobile SoC copper pillar probing study. Test and measurement challenges for 3D IC development were presented by Raphael Robertazzi, Ph.D. (IBM Research). Senthil Theppakuttai, Ph.D. (SV Probe) and Todd Tsao (ASE Global - Taiwan) covered the challenges of advanced Cu-pillar applications at 50µm for enabling fine pitch probing. John Strom (Rudolph Technologies) proposed innovative approaches and concepts for reducing the cost of probe card test. Developments with a novel carbonaceous film with high electrical conductivity and ultra high hardness for test probes were presented by Dr. Teruyuki Kitagawa (Nomura Plating, Co., Ltd. - Japan). Detailed summaries from all of the technical sessions (including the questions & answers) from of all of the technical sessions can be found at Ira Feldman's Blog at http://hightechbizdev.com/.

Overall, the technical program had 29 podium presentations with 59% from suppliers, 15% from semiconductor manufacturers, and 26% collaborative presentations from both manufacturers and suppliers. All the presentations from SW Test 2012 as well as previous workshops (1993 to 2012) are available at the SW Test website (http://www.swtest.org).

The committee recognized the best podium presentations and Rey Rincon (Technical Program Chair) awarded the authors …

- **Best Presentation:**

Full Wafer Contact Breakthrough with Ultra-High Pin Count
Daisuke Takano and Takashi Naito (Advantest - Japan)
Tsutomu Shoji (Japan Electronic Materials, Corp. - Japan)

- **Best Data Presented *(awarded jointly)***

  (1) Wafer Probe Challenges for the Automotive Market
  Luc Van Cauwenberghe, Frank De Ruyck, and Wim Dobbelaere (ON Semiconductor - Belgium)
  Riccardo Liberini, Marco Di Egidio, and Riccardo Vettori (Technoprobe SPA - Italy)

  (2) Case Study: Integrating a 300mm Probing Solution with a Diagnostic Emission Microscopy
  Richard Portune and Kevin Eseltine (DCG Systems, Inc.)

- **Most "Inspirational" Presentation**

  An Analysis of Probing CRES in Gold Bumping Pad using Automatic Test Equipment
  Chang Hyun (Samsung Semiconductor Institute of Technology)
  Hyun-Ho Park and Sik-Sang Hahm (Samsung - Korea)

- **Best Presentation, Tutorial in Nature**

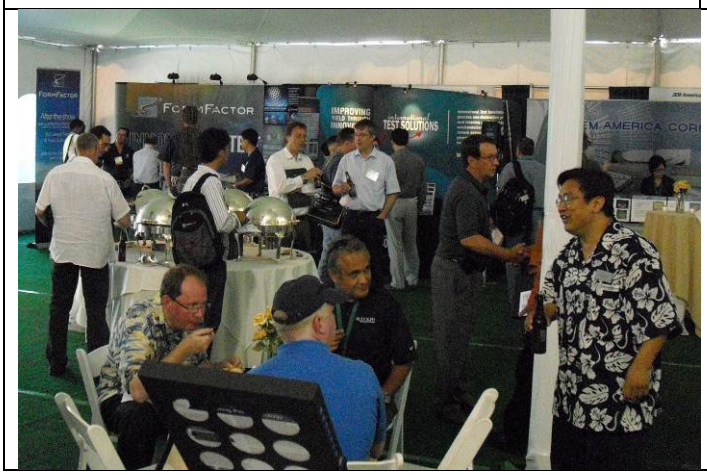
  Crossover in TD efficiency - When the Brick Wall is Not the Best.
  Keith Breinlinger, Ph.D. (FormFactor, Inc.)

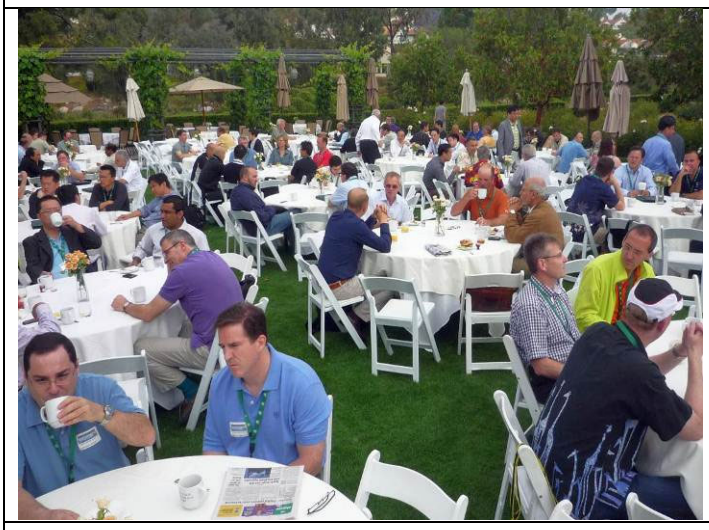
During the SW Test Tech EXPO, 37 full size exhibits showcased products from the wafer sort industry and the associated critical infrastructure. The international exhibitors from the US, Europe, and Asia represented key probe card vendors, major prober equipment manufacturers, probe card analyzer and probe process metrology companies, companies specializing in probe card cleaning, micro-pogo spring pin suppliers, and a variety of other probe related service providers.

SW Test 2012 also had four Platinum Supporters - International Test Solutions, FormFactor, Inc. (FFI), JEM America, Micronics Japan (MJC); four Gold Supporters – MultiTest, Teradyne, Rudolph Technologies, T.I.P.S. Messtechnik; and one Silver Supporter – Advanced Probing Systems, Inc. All corporate supporters participated in the 1st Annual SW Test Golf Scramble and for SW Test 2013, the 2nd Annual Scramble will be open to both supporters and exhibitors.

Plans are already underway for the 23rd Annual IEEE SW Test Workshop and Tech EXPO which will be held on *June 9-12, 2013* at the Rancho Bernardo Inn, San Diego, CA (http://www.ranchobernardoinn.com). Abstract submission for the technical program and exhibitor registration for the Tech EXPO are already open!

SW Test Technical Program 2012 in Session	
	

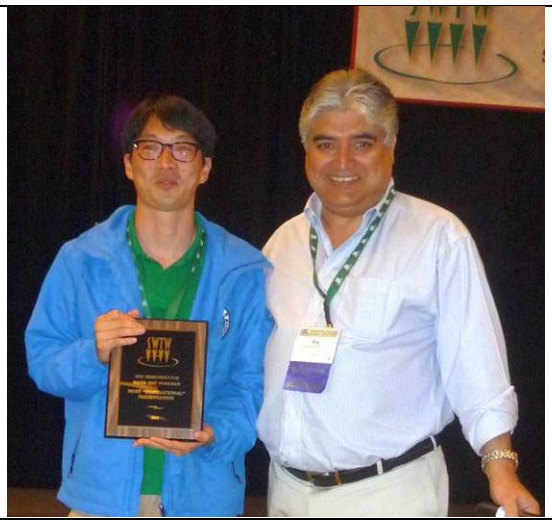
SW Test Technology EXPO 2012 Pavilion	
	

Networking at Rancho Bernardo Lawn	***Conference Social / Networking Event***
	
International networking on the lawn during one of the breaks between technical sessions.	SW Test 2012 Hawaiian Luau themed social and networking event.

IEEE SW Test Committee 2012

Front (L): Tatsuo Inoue, John Caldwell, Jerry Broz, Ph.D. (General Chair), Patrick Mui, Mark Ojeda, Amy Leong, Fred Taber, Darren James.
Back (L): Matt Zeman, Ph.D., Jan Martens, Rey Rincon (Program Chair), Michael Huebner, Ph.D., Gunther Boehm.
Not pictured: Boyd Daniels

Rey Rincon (Technical Program Chair) awards the ***"Best Overall Presentation"***	***"Best Data Presented"*** ***(awarded jointly)***
	
Daisuke Takano (Advantest) Tsutomu Shoji (Japan Electronic Materials)	Left: Luc Van Cauwenberghe (ON Semiconductor) Right: Richard Portune (DCG Systems, Inc.)

"Best Presentation, Tutorial in Nature"	***"Most Inspirational Presentation"***
	
Keith Breinlinger, Ph.D. (FormFactor, Inc.)	Chang Hyun (Samsung Semiconductor Institute of Technology)