Keynote Speaker

“Emerging High Density 3D Through Silicon Stacking (TSS) – What’s Next?”

Matt Nowak

Senior Director
Advanced Technology
Qualcomm CDMA Technologies

QUALCOMM® CDMA Technologies

Emerging High Density 3D Through Silicon Stacking

-*What's Next?*

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Emerging High Density 3D Through Silicon Stacking
What's Next ?

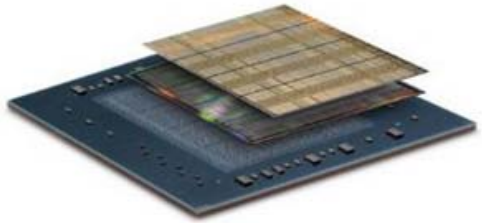
Outline

- Applications and Motivations
- Technology Status & Progress
- Key Challenges
- Conclusions

2.5D / 3D TSV Stacking : Everybody is Doing It

Sector	Company
Memory	Samsung
	Elpida
	Hynix
	Micron
Foundry	tsmc
	Global
	UMC
OSAT	Amkor
	ASE
CPU / GPU	Intel
	AMD
	IBM
	nVidia
FPGA	Xilinx
	Altera
Mobile	STM / STE
	TI
	Intel
	Samsung

Have All Talked about Activities in 2.5D and/or 3D Domains During 2011- 2012



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> ADVANCED PACKAGING: 3D IC, WLP & TSV — Jun 8th, 2010
TSMC reveals plan for 3DIC designs based on Silicon interposers & TSV

> ADVANCED PACKAGING: 3D IC, WLP & TSV — Jun 23rd, 2010
Elpida, PTI & UMC to partner for 3DIC commercialization of Logic+DRAM stacks by 2011

> ADVANCED PACKAGING: 3D IC, WLP & TSV — Oct 27th, 2010
Xilinx brings 3D TSV interconnects to commercialization phase in digital FPGA world

> ADVANCED PACKAGING: 3D IC, WLP & TSV — Sep 17th, 2010
3DIC memory with wide I/O interface is coming by 2013 says NOKIA

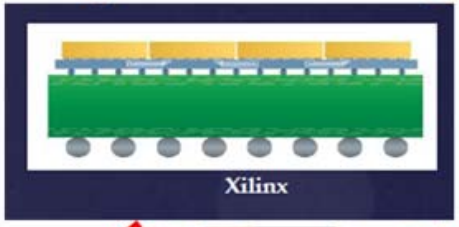
> ADVANCED PACKAGING: 3D IC, WLP & TSV — Feb 18th, 2011
Micron reveals "Hyper Memory Cube" 3DIC Technology

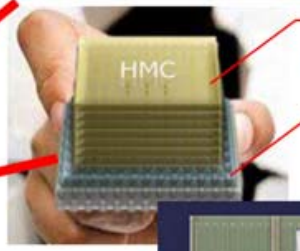
> ADVANCED PACKAGING: 3D IC, WLP & TSV — Feb 28th, 2011
Samsung Wide IO Memory for Mobile Products - A Deeper Look

> ADVANCED PACKAGING: 3D IC, WLP & TSV — Jun 28th, 2011
Elpida begins sample shipments of DDR3 SDRAM (x32) based on TSV stacking technology

> ADVANCED PACKAGING: 3D IC, WLP & TSV — Dec 7th, 2011
STMicroelectronics' TSV middle for advanced 28nm SoC unveiled

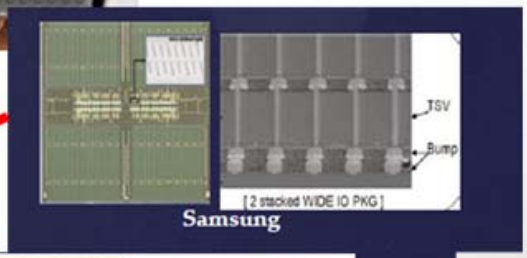
JEDEC Publishes Breakthrough Standard for Wide I/O Mobile DRAM

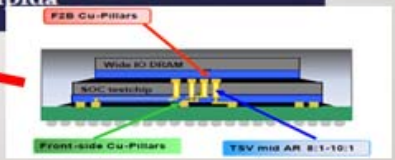




Memory Cube (Micron)

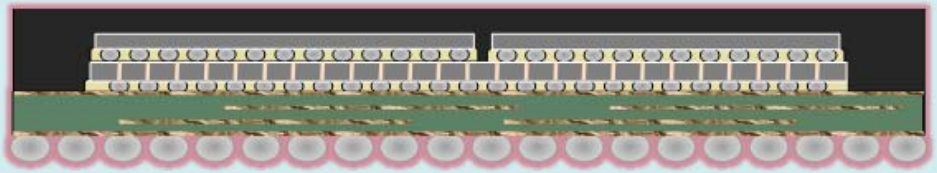
Logic Controller chip (IBM)



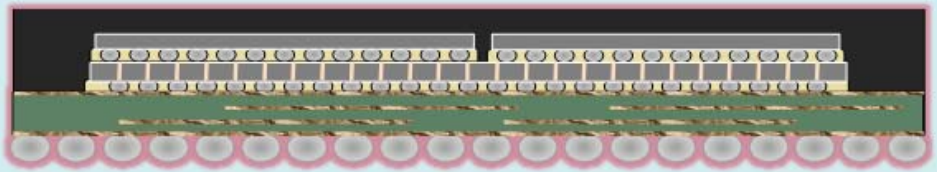
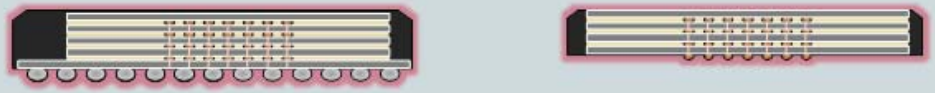
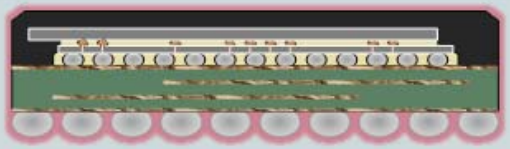
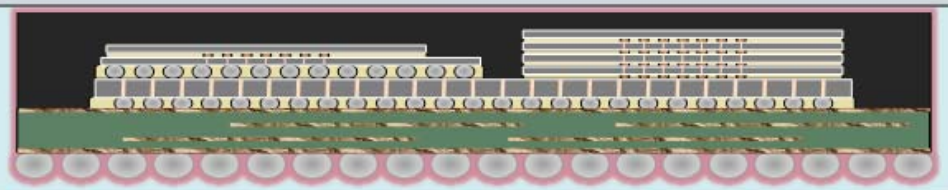


Some of the Current Hi Density 2.5D/3D Applications

High Density = 5-10um dia vias, ~10:1 AR, 1K-10K's TSVs and ubumps, 10's um pitch ubumps

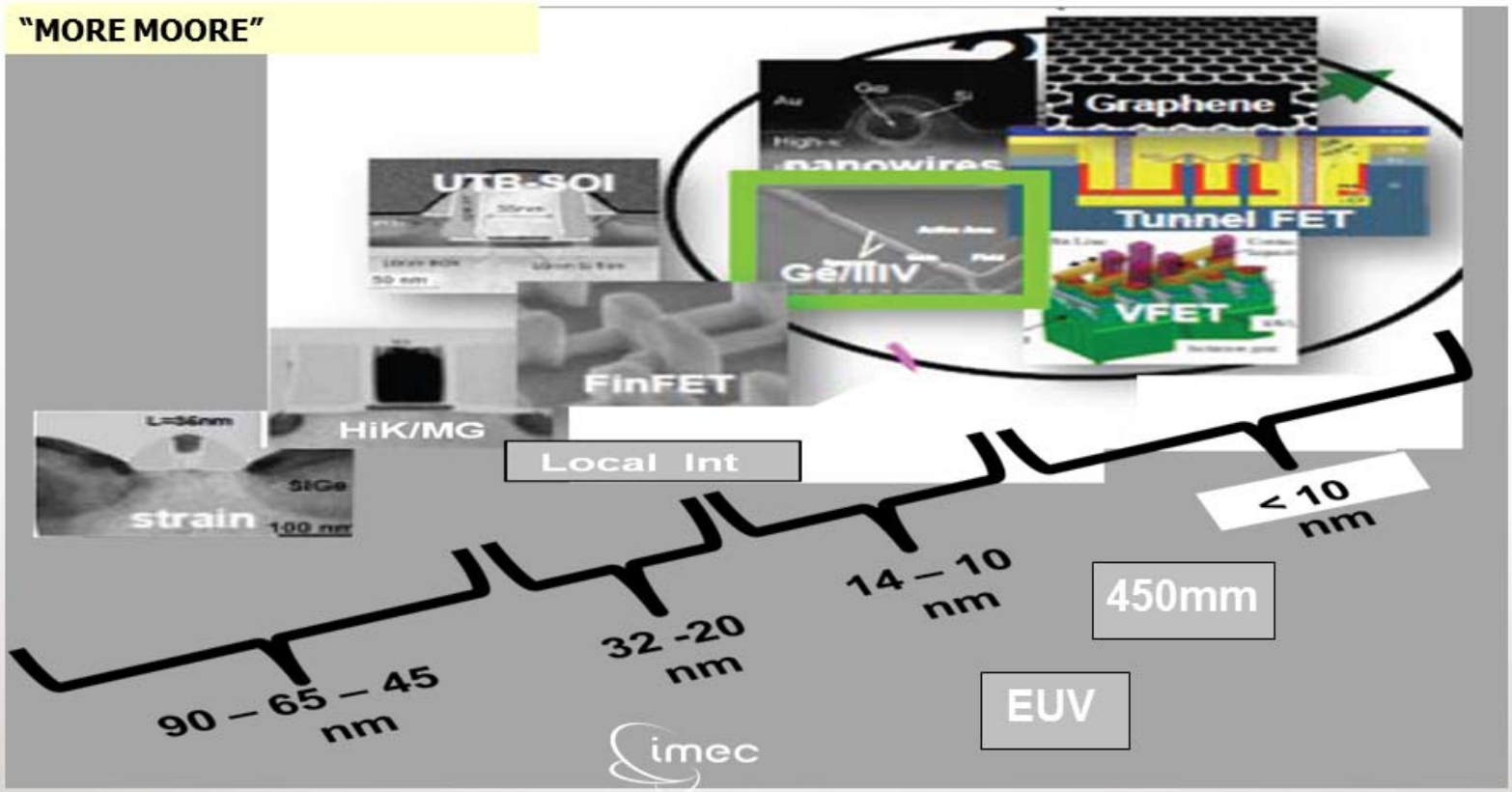
2.5D	Side by side die stacked on a passive interposer that includes TSVs	
3D Memory	Multiple DRAM die stacked standalone or on an active interposer	
3D Memory on Logic	One or More DRAM die stacked directly on logic die (M-0-L) (or L-O-M for high power processors)	

What's Next?

2.5D	Side by side die stacked on a passive interposer that includes TSVs	
3D Memory	Multiple DRAM die stacked standalone or on an active interposer	
3D Memory on Logic	One or More DRAM die stacked directly on logic die (M-0-L) (or L-O-M for high power processors)	
3D Logic on Logic	Multiple logic die stacked on top of each other (L-o-L)	
3D + Interposer	Mix of side by side and stacked schemes with a passive or active interposer	

High Density Through Silicon Vias: Motivation

- **Semiconductor future will be a series of disruptive technology changes**
  - end of conventional CMOS scaling but continue Moore's law with new devices



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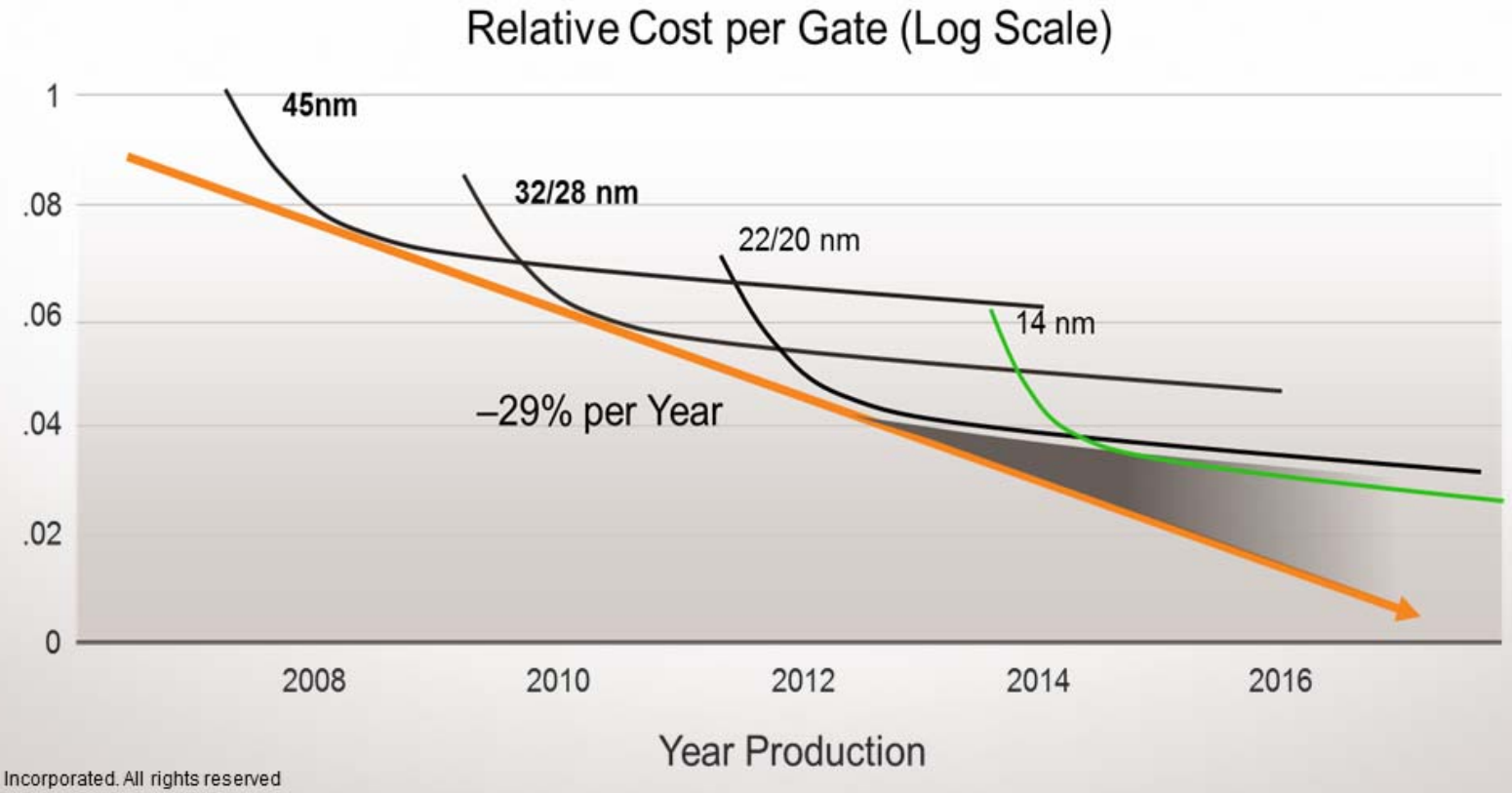

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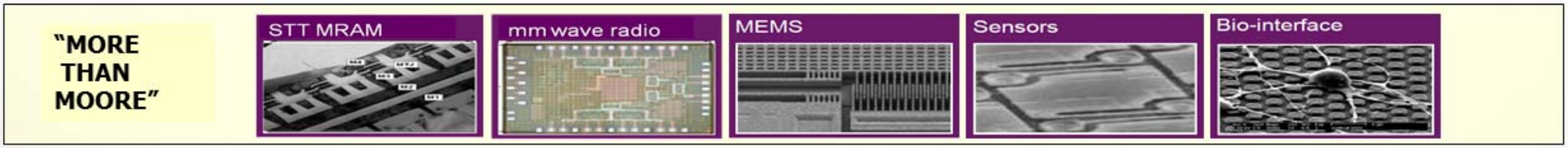
- **Semiconductor future will be a series of disruptive technology changes**
  - end of conventional CMOS scaling but continue Moore's law with new devices
  - diminishing of the traditional 29% per year cost reduction megatrend
  - increasing impact of "More than Moore" functionality

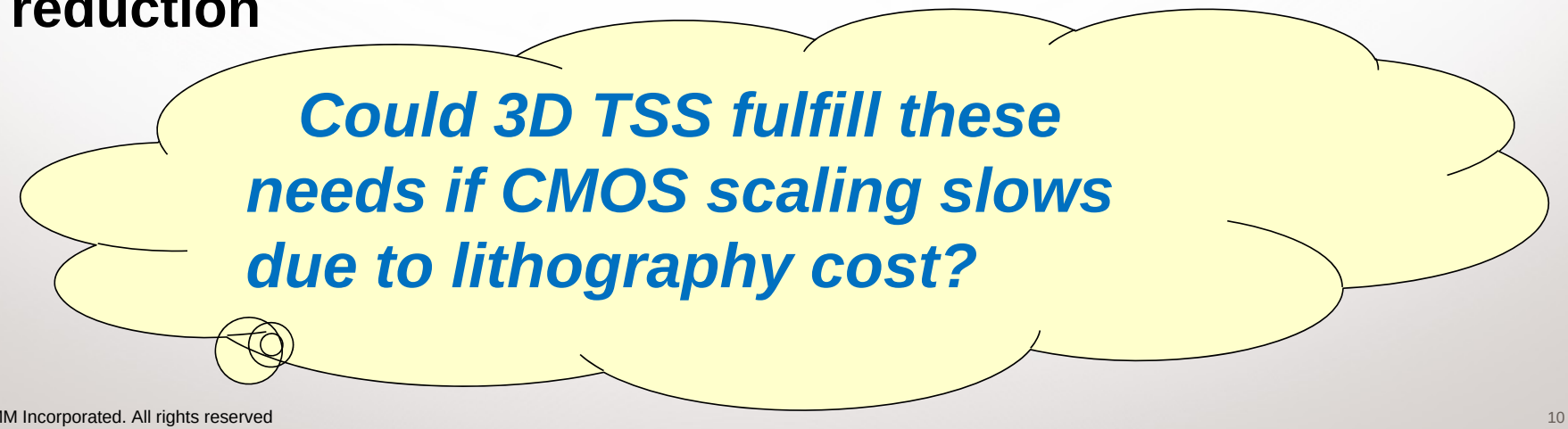


The game is changing……

High Density 3D TSS provides a platform to navigate these disruptive changes

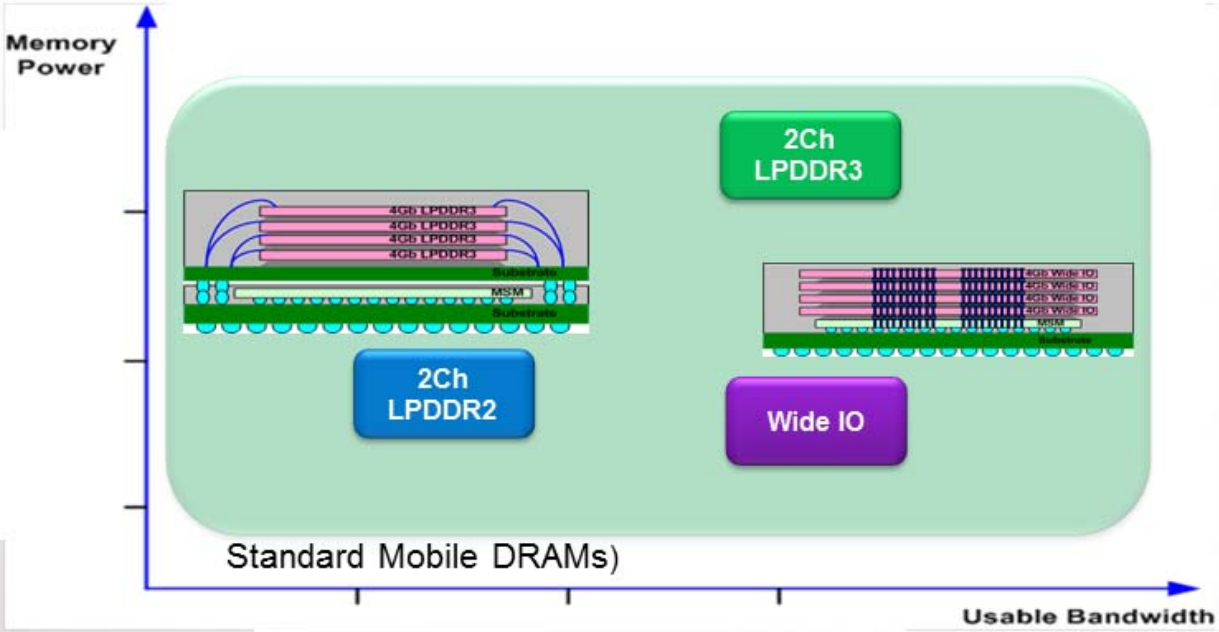
High Density Through Silicon Stacking (TSS)
Motivations common with CMOS scaling

- **Performance enhancement**
- **Improved power efficiency**
- **Form factor miniaturization**
- **Cost reduction**



Value Proposition : Power – Performance

- For Example : Wide IO Memory



	LPDDR3	Wide IO
Max BW	12.8GByte/s	12.8GByte/s
Max Density (2013)	4Gbit die 2GByte POP	4Gbit die 2GByte Cube
Power @ Usable BW	~800 mW	~400 mW

- Wide IO Memory Inherently Superior Power Efficiency
  - Increasing advantage with increasing Bandwidth demand

Value Proposition : Power – Performance

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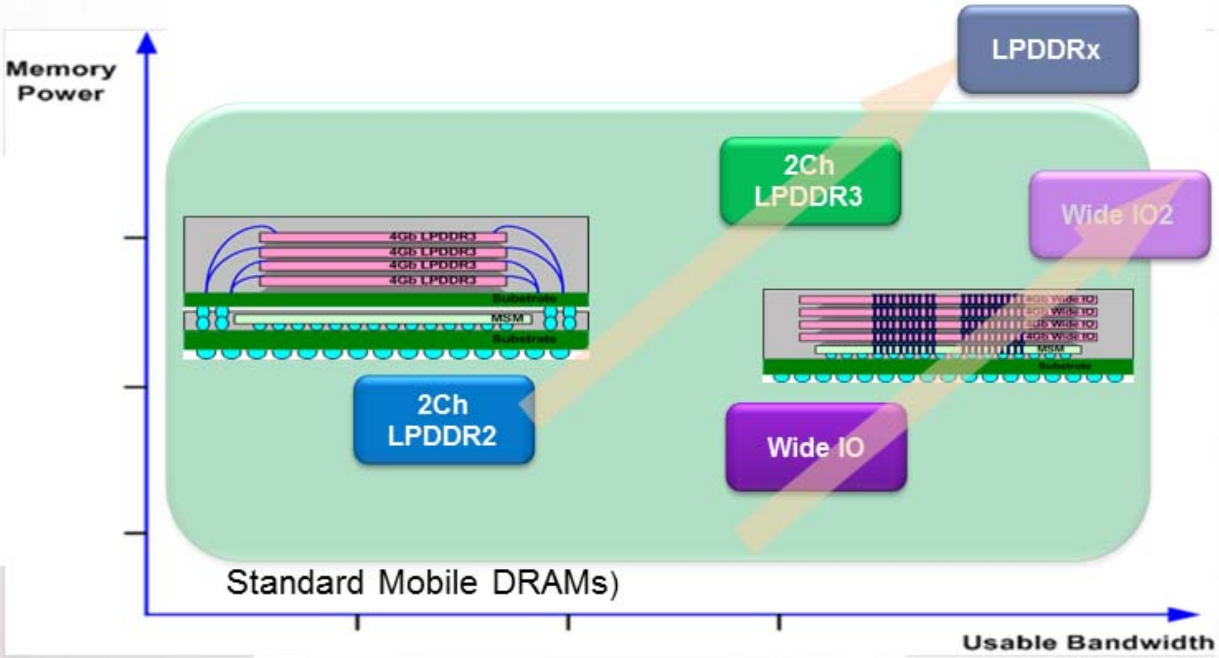

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- Wide IO Memory Inherently More Scalable to Higher Bandwidths
  - Wide IO : SDR @ 200MHz => SDR @ 266MHz => DDR => overclocked DDR…
  - DDRx : LPDDR @ 800 MHz => 1000 MHz + and/or Low Voltage Swing

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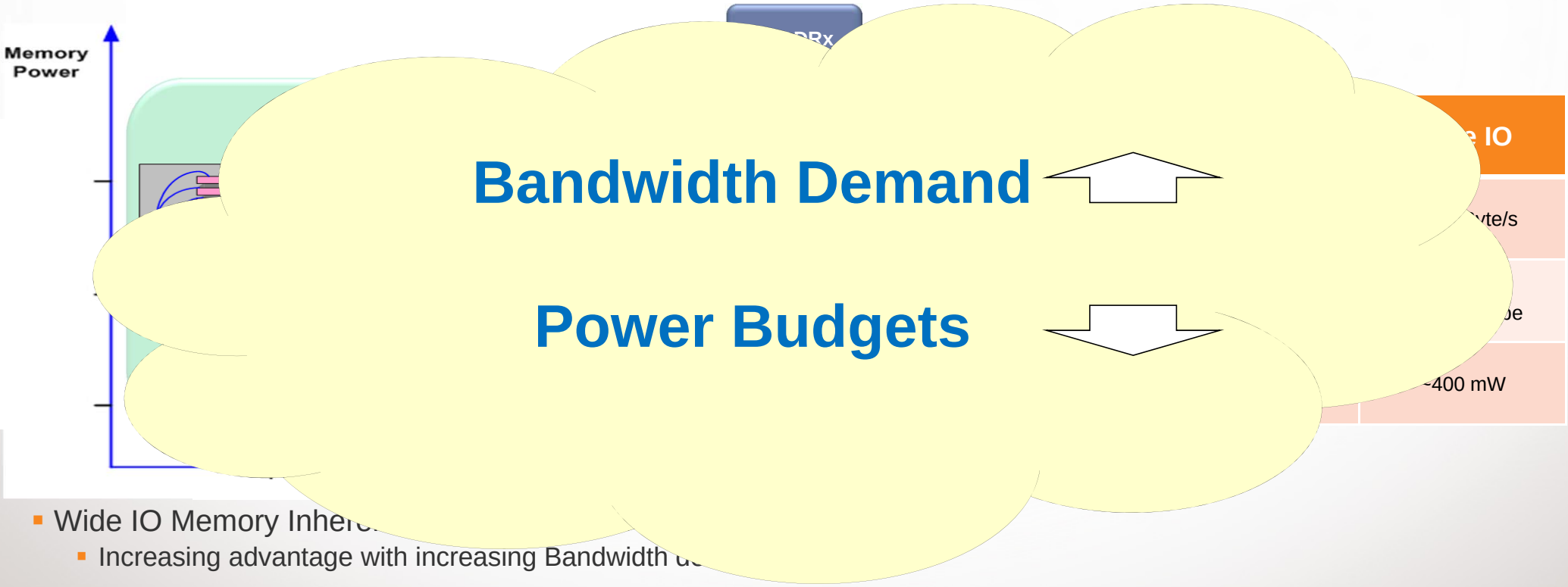

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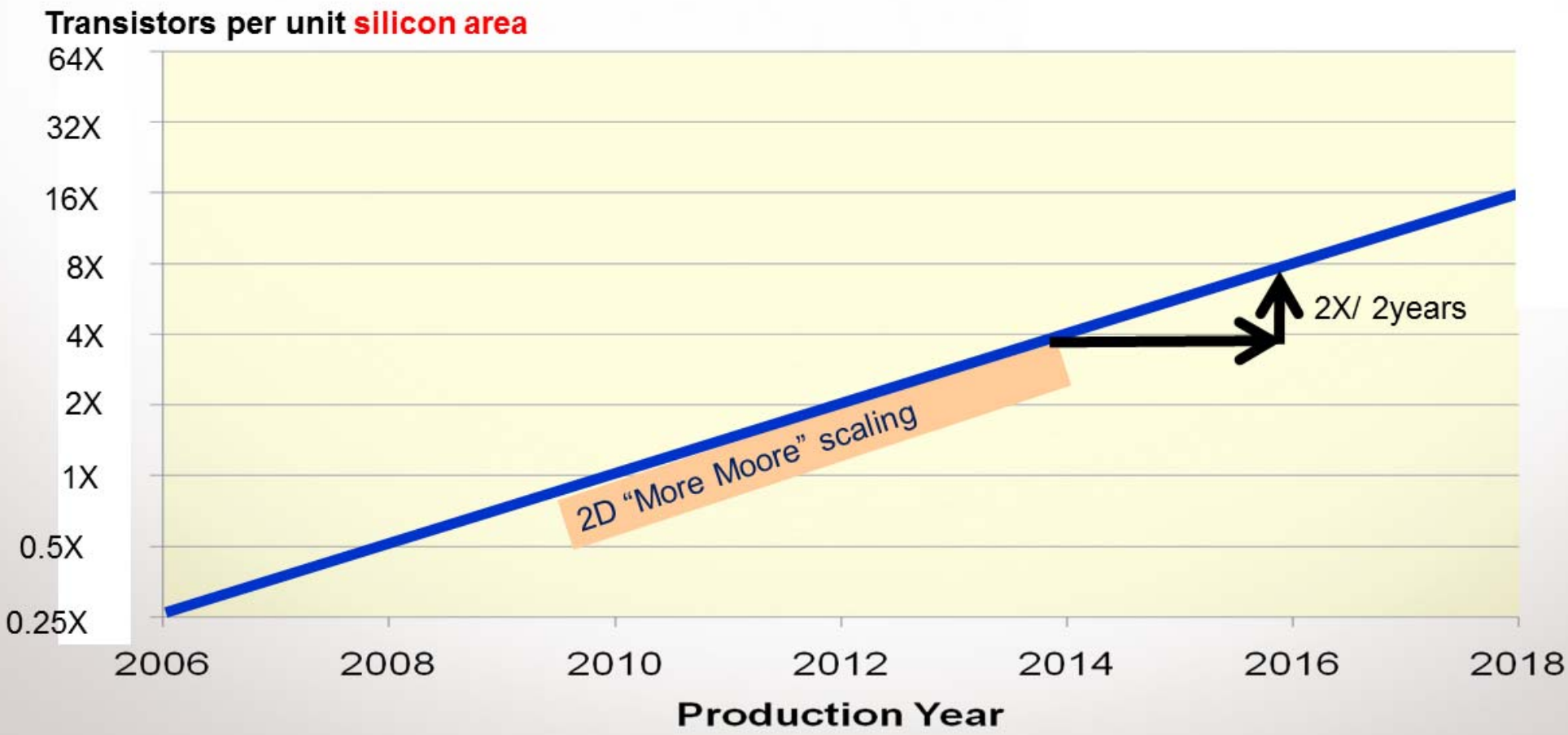
Value Proposition : Form Factor

- 3D vs. 2D Scaling



Value Proposition : Form Factor

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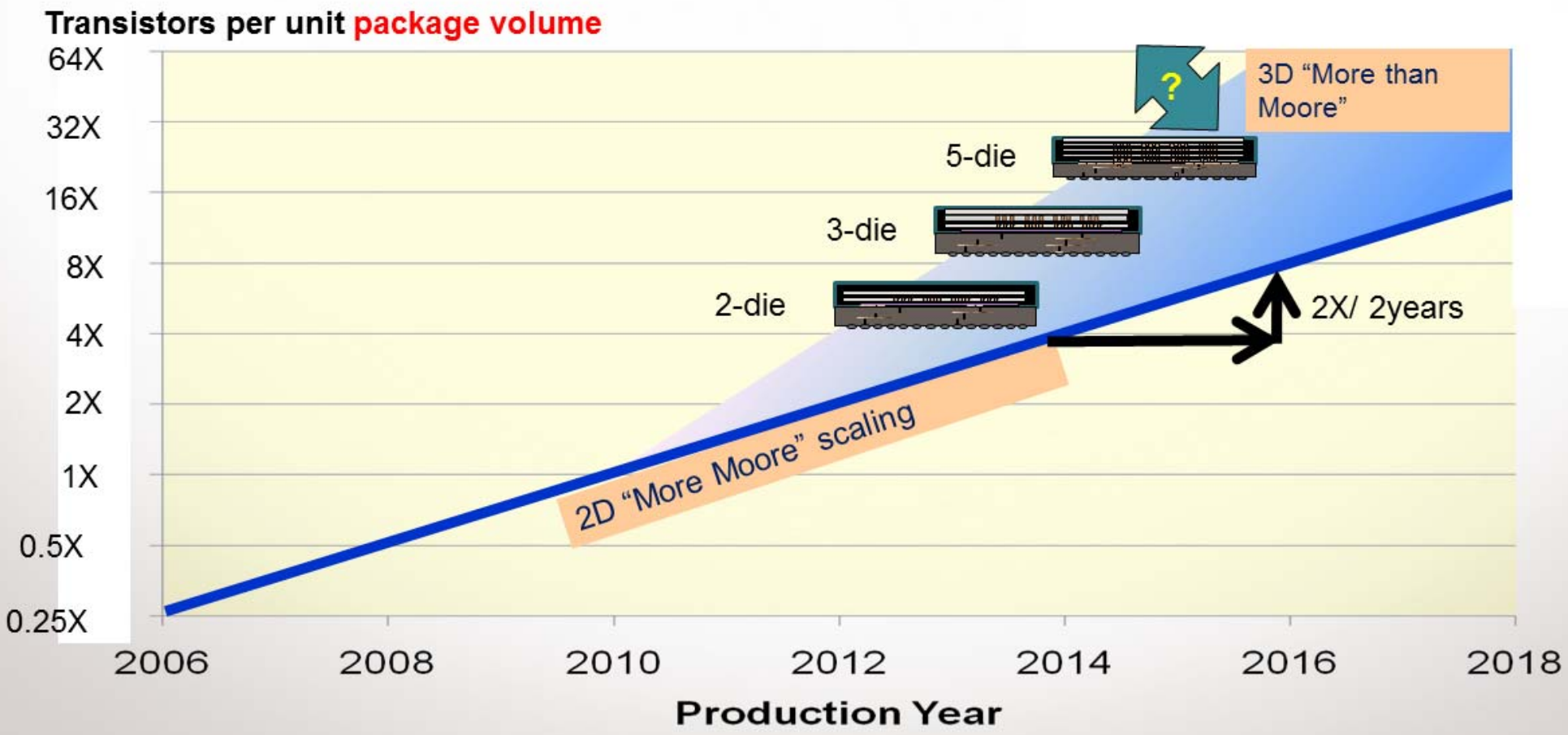
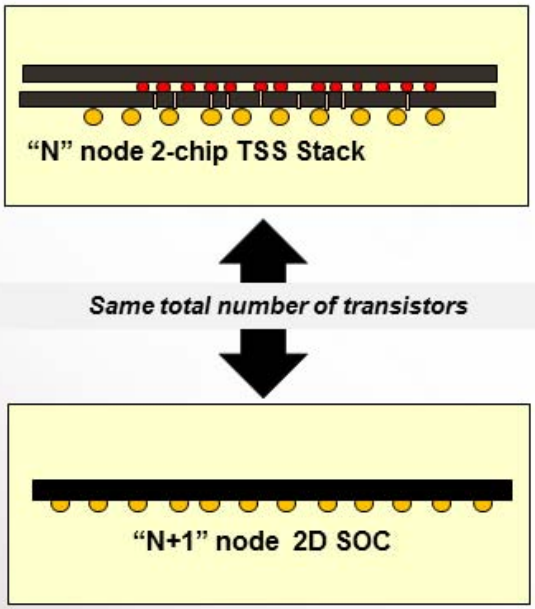
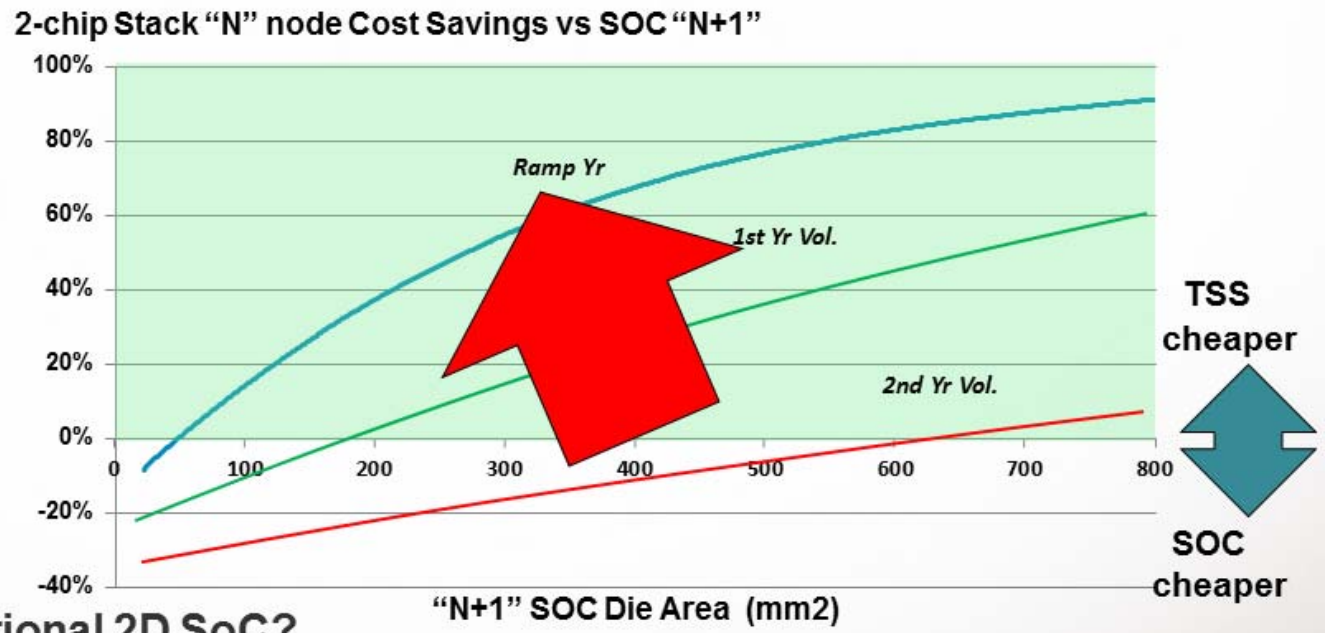


Value Proposition : Cost



Assuming ***less than*** *29% per year cost reduction megatrend*



- **Is TSS Cheaper than Conventional 2D SoC?**
  - Yes – early in N+1 node availability and for larger die sizes
- **More Savings Possible if :**
  - Consider lower cost reduction from 2D scaling
  - Split large 2D SOC at N+1 node into multiple smaller N+1 die
  - Or if mix 'n match technology nodes with 2-chip TSS stack

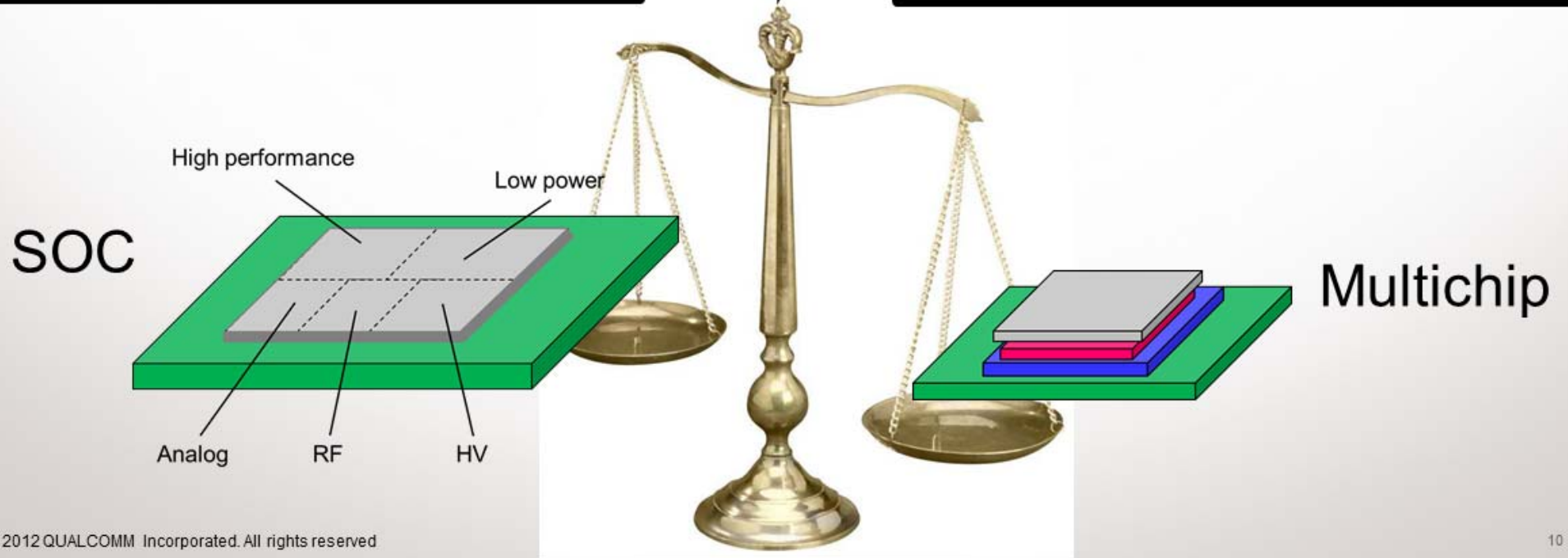
The Game is Changing

Diminishing Cost Reduction

+ "More than Moore"

+ High Density TSV

Shift SOC vs. Multichip balance in favor of TSS Multichip to create new chipset architectures



Emerging High Density 3D Through Silicon Stacking
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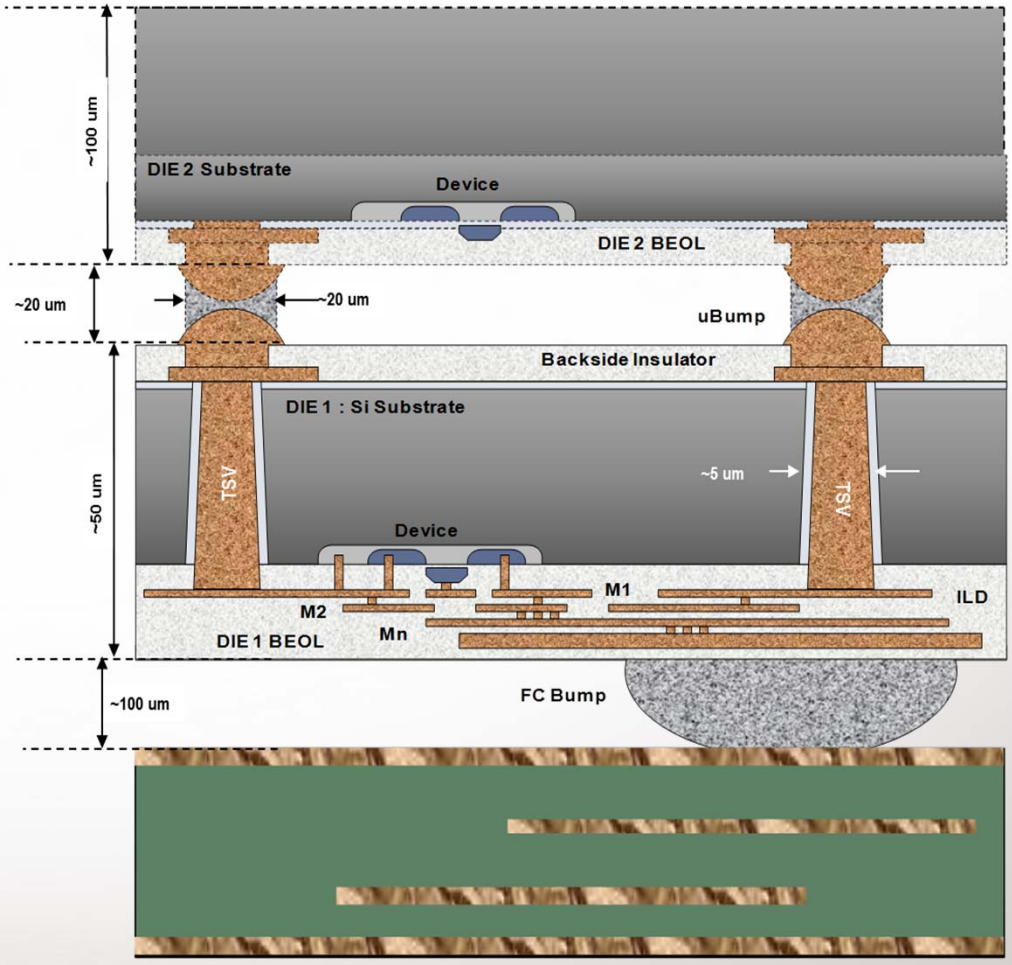
3D TSS: Three Major Process Modules



TSV Formation (via middle)

Post Contact CMP

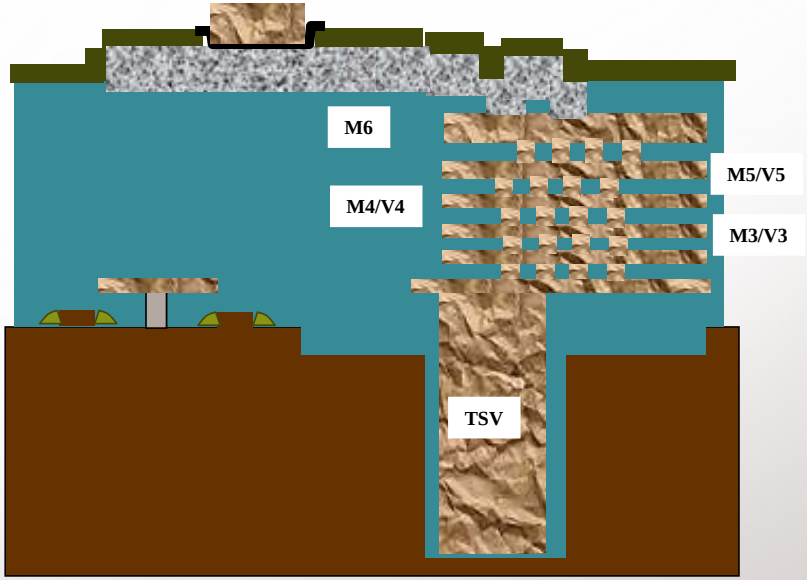
Step1: TSV mask and etch blind via

Step 2: TSV isolation

Step3: TSV barrier/ seed/plate

Step 4: TSV CMP

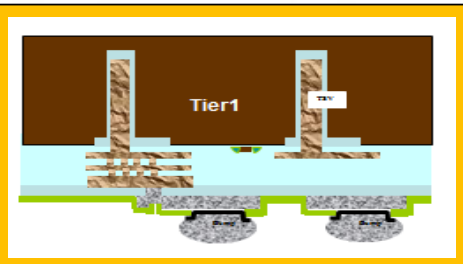
Continue BEOL

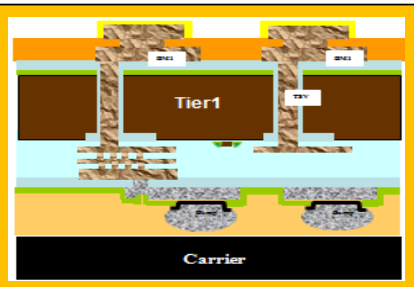


Backside Processing and Chip Stacking

Die to Substrate Flow

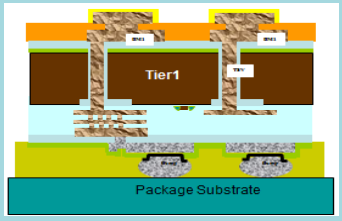
Tier 1 wafer



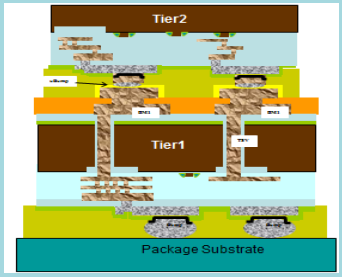


Temp carrier, thin/reveal, B-RDL, ubump

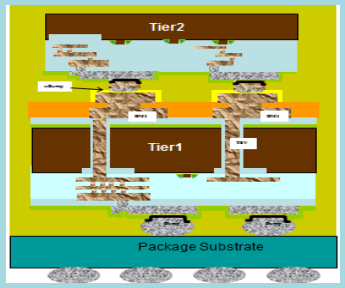
Demount to tape



Dicing, bond to pkg substrate, Tier 1 to Substrate Underfill

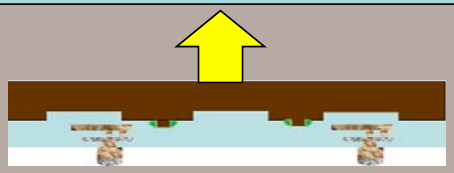


Thermal compressive bonding Tier 2 to tier 1



UF, Molding, ball attach, pkg singulation

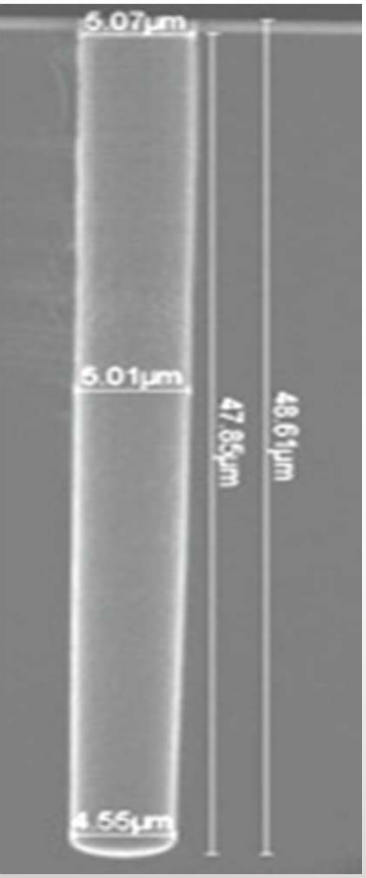
Tier 2 wafer



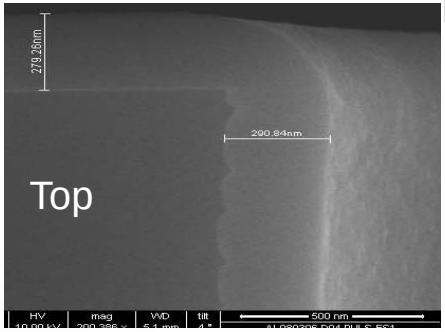
KGD with ubump

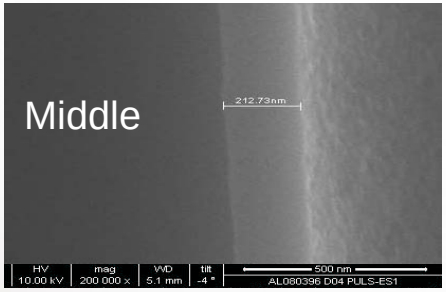
High Density TSV Processes Demo'd

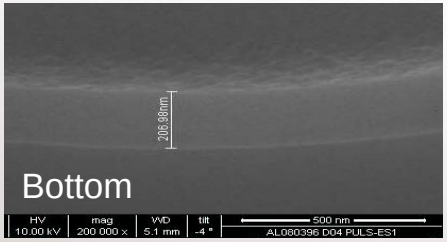
Via etch



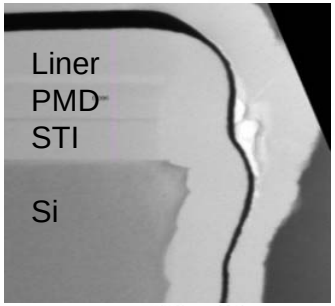
oxide Liner

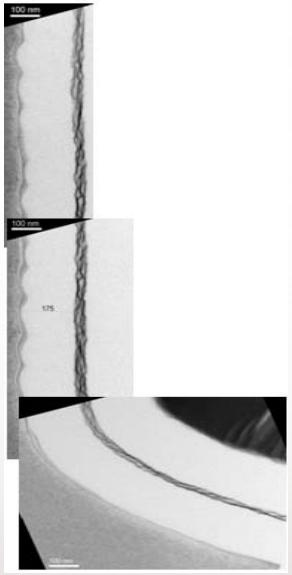




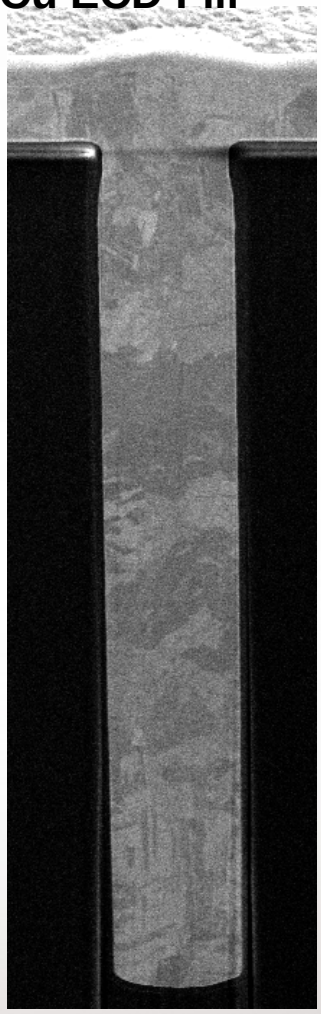


PVD Ta/ Cu barrier seed

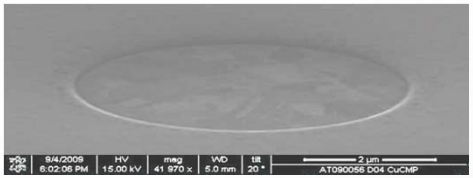




Cu ECD Fill



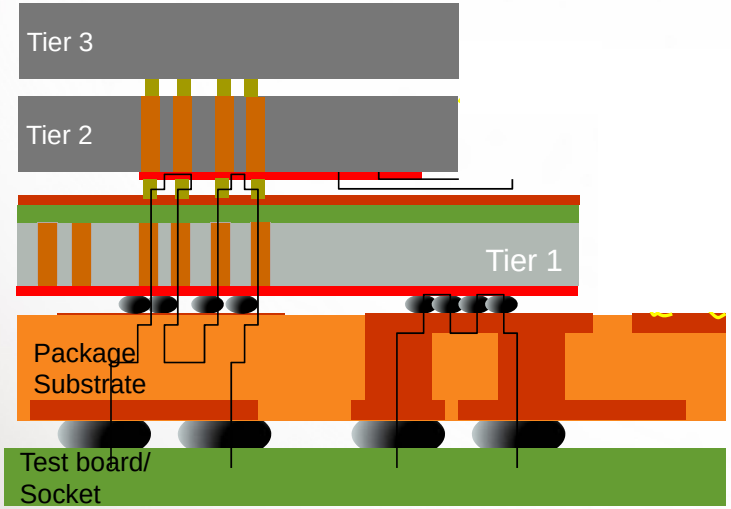
TSV anneal & CMP

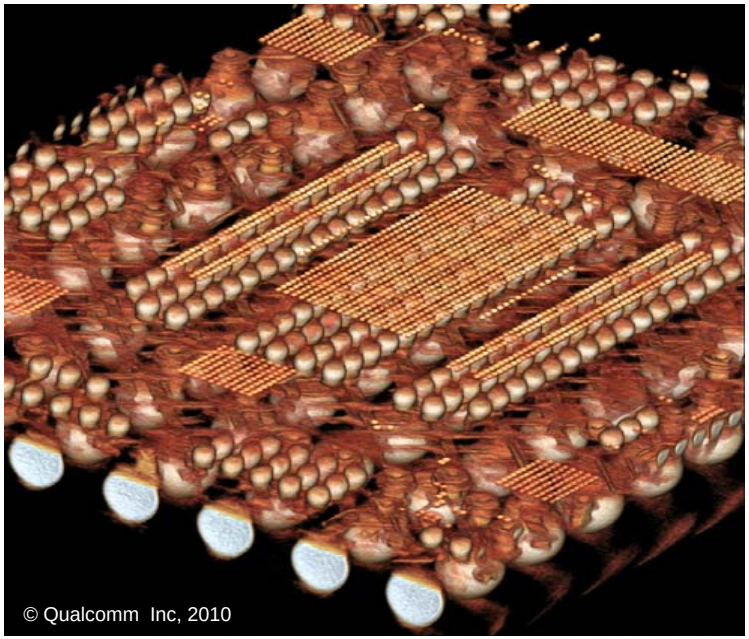


5µm

Source by permission: IMEC/ERIC BEYNE

Qualcomm TSS Integrated Demonstrators



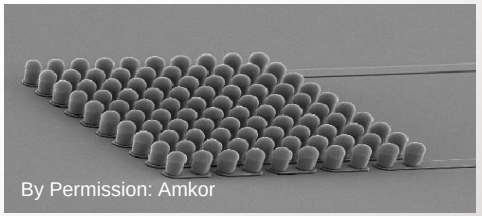


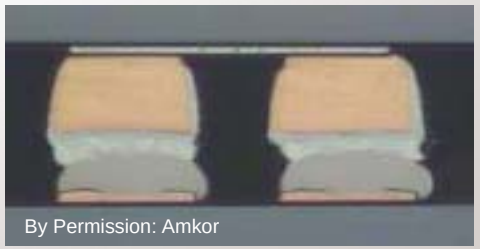
NEW MODULES

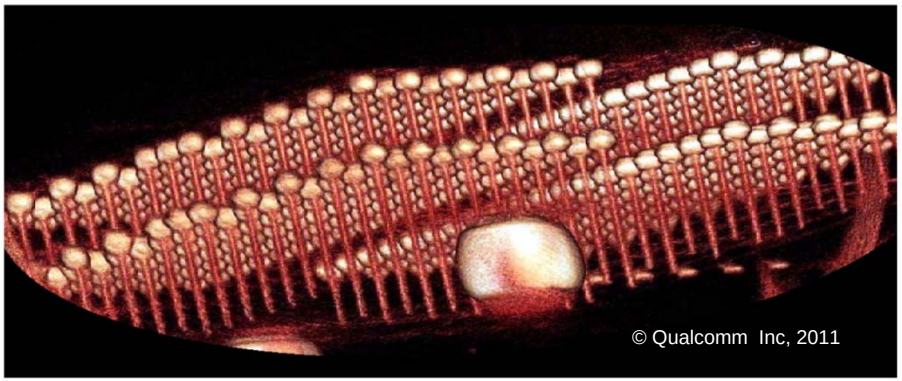
- TSVs
- Backside wf processing
- Microbumps

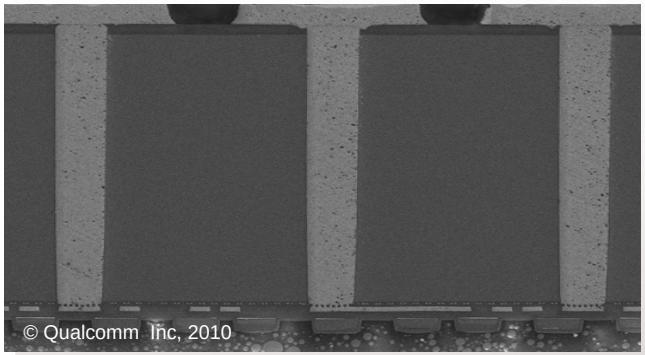
INTEGRATION

- Via-middle
- 28nm, HiK/MG
- FinFET (w. IMEC)
- Wide IO memory
- N>2 chip stacking

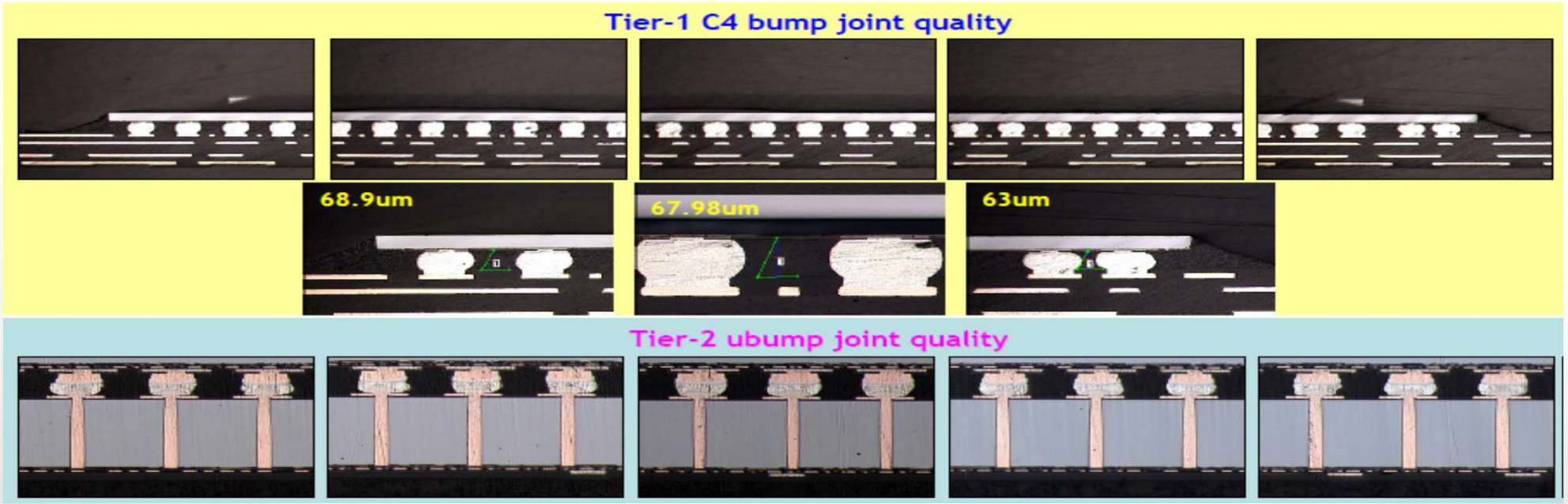








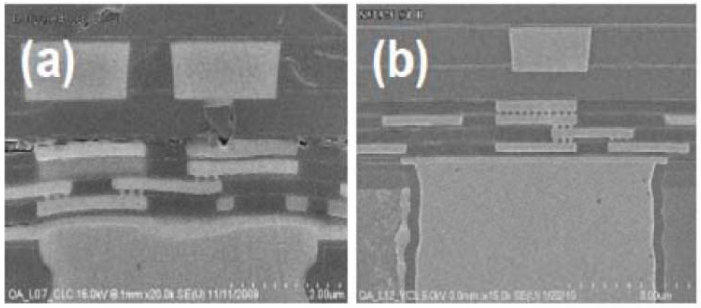
Fine Pitch Microbump Assembly



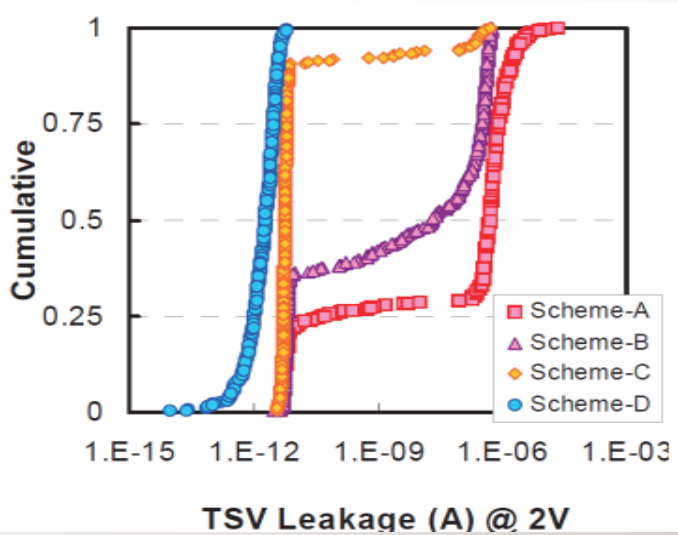
3D TSV Reliability Progress

Intrinsic Reliability Data Collected

- TSV: Cu pumping mitigation solutions
- TSV leakage reduced
- Microbump: EM no worse than C4
- Package: HAST/TC/HTS passed JEDEC spec



J.C. Lin et al 2010 IEDM



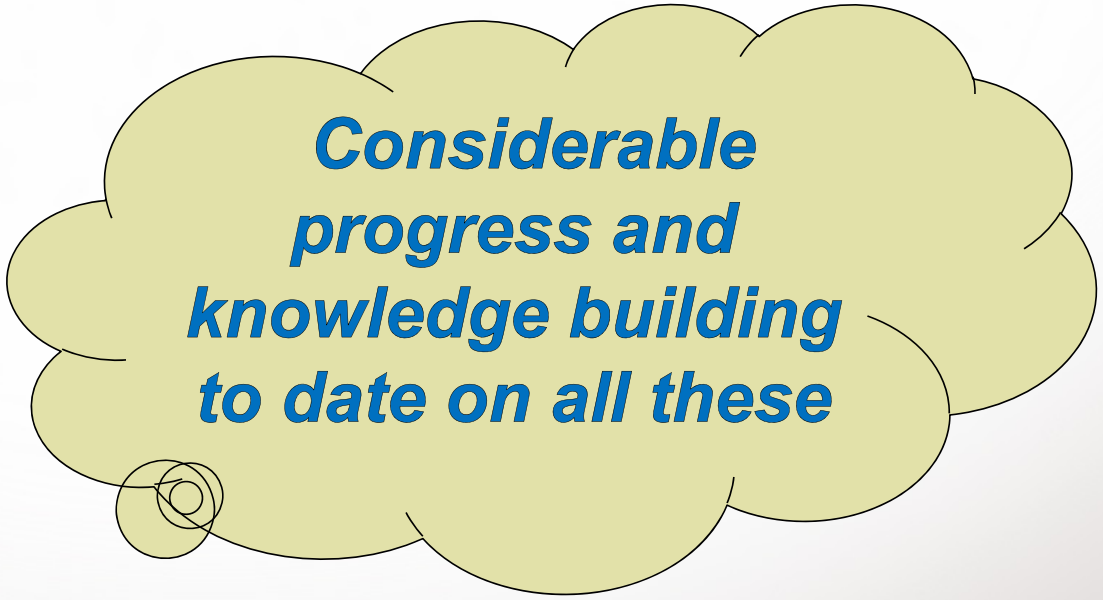
C.L. Yu et al, 2011 VLSI

Snapshot of Intrinsic Technology Status

	Was (common concern a few years ago)	Is (our take)
Process	High aspect ratio (10:1) 5/50 TSV process	✓
	Thinning & Backside wafer processing	✓
	Microbump and Joining	✓
	Integration & Stacking	✓
	Intrinsic Reliability Assessment	☛ in flight
	Standards (JEDEC, SEMI, Sematech, 3D EC, …)	☛ in flight
Design (M-o-L)	Design Enablement (for "2D-like" Memory-on-Logic design)	✓
	Variability (Corner for "2D-like" Memory-on-Logic design)	✓
	EDA tools (for "2D-like" Memory-on-Logic design)	☛ mostly
	Testability (for "2D-like" Memory-on-Logic design)	☛ in flight
Product	Stress Modeling & Design for Stress	☛ in flight
	Thermal Modeling & Design for Thermal	☛ in flight
	Cost Structure & Business Models	TBD
	Yield and Yield Learning	TBD
	Volume Manufacturing Ramp	TBD

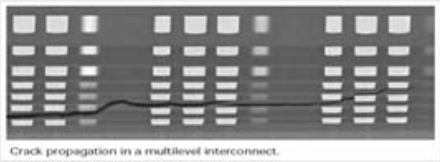
TSS Technical Challenges

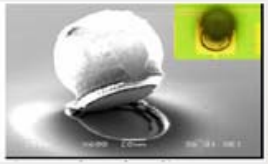
- **Most often mentioned**
  - Reliability
  - Thermal
  - Design tools and flows
  - Thin wafer handling
  - Mechanical stress effects
  - Test/DFT
  - Inspection & metrology



Mechanical Stress: Avoiding the "Perfect Storm"

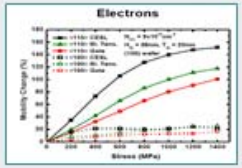
- Chip-Package Interactions (CPI)
  - Package-Si CTE Mismatch
    - Weak ELK + Hard Cu
    - Hard Pb-Free Balls
    - Harder Cu-Pillars

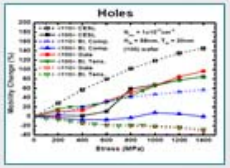




- Material Integrity Issues

- On Chip Strain Sources
  - BEOL-FEOL CTE Mismatch
    - Liners (CESL / memorization)
    - SEG Strained Si (eSiGe, eSiC)
    - Metal Gates & Contacts / STI …





  - Device Electrical Integrity Issues

- 3D TSS Technology Interactions
  - TSV : interaction of Cu TSV and surrounding devices
  - μ-Bump: stress points in both Tier 1 and Tier 2 die
  - Thin Si : Enhanced CTE Mismatches: BEOL-FEOL + Si-Package
  - B-RDL : new CTE Mismatch challenges
  - Die Corners and Edges : stress concentration among stacked die

Yield

Reliability

Performance

Variability

Mechanical Stress: Avoiding the "Perfect Storm"

- Chip-Package Interactions (CPI)
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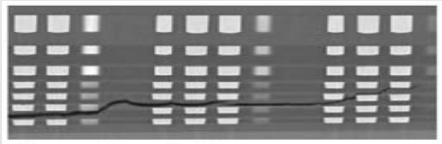
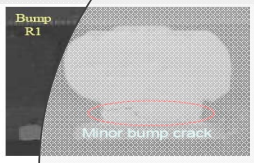

Crack propagation in a multilevel interconnect.



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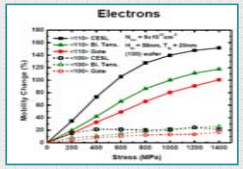

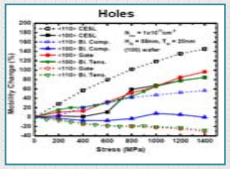

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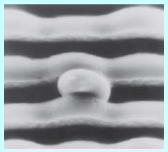
→ Yield
→ Reliability
→ Performance
→ Variability

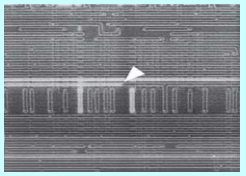
Fault Classes

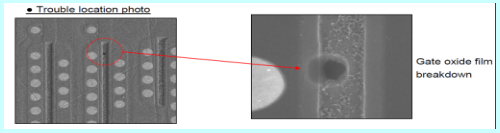
High Fault Coverage

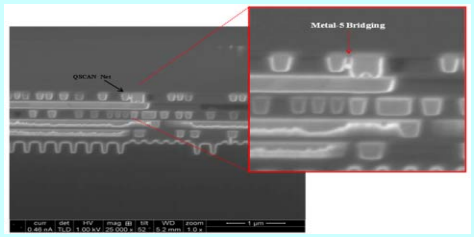
Random Process Defects

Particles
Contaminants
Oxide Pinholes
Etc.





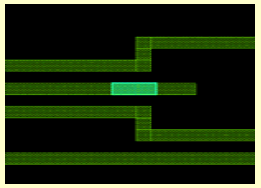


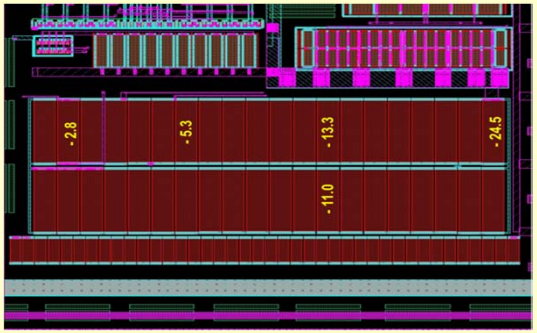


Good Characterization

Systematic Defects

Litho/Printability
Etch Loading
CMP Loading
On Chip Stress
Etc.

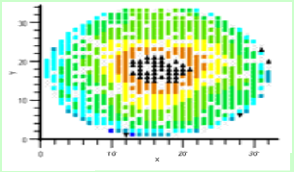


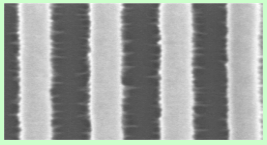


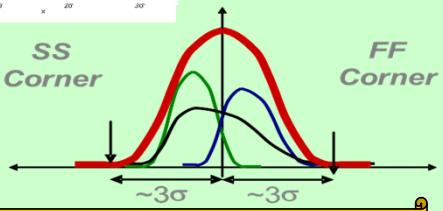
Process Variability

Global Variability
X-Wafer, X-Chip
Local Variability

Tox, implant dose
CD, LER, RDF
Etc.

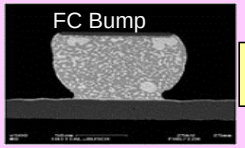


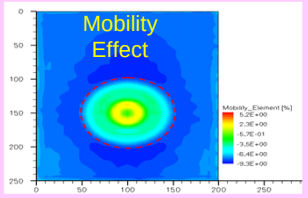


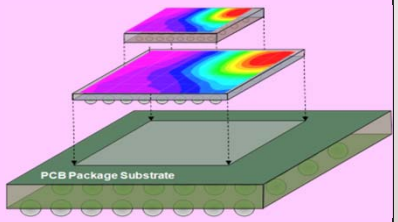


Systematic Interaction Faults

Thermal Hot Spots
Electric/Magnetic coupling
Mechanical Stress – CPI
Etc.



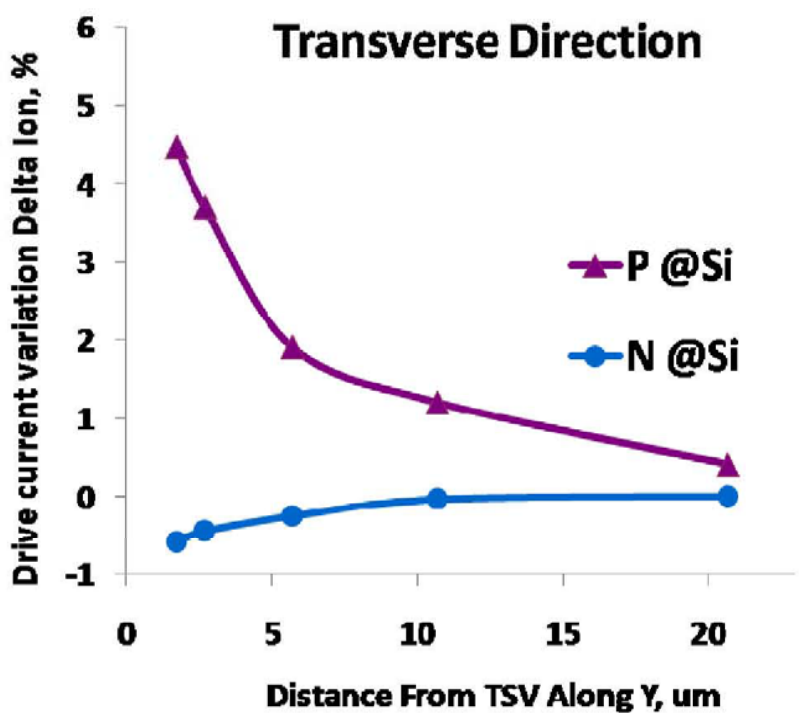


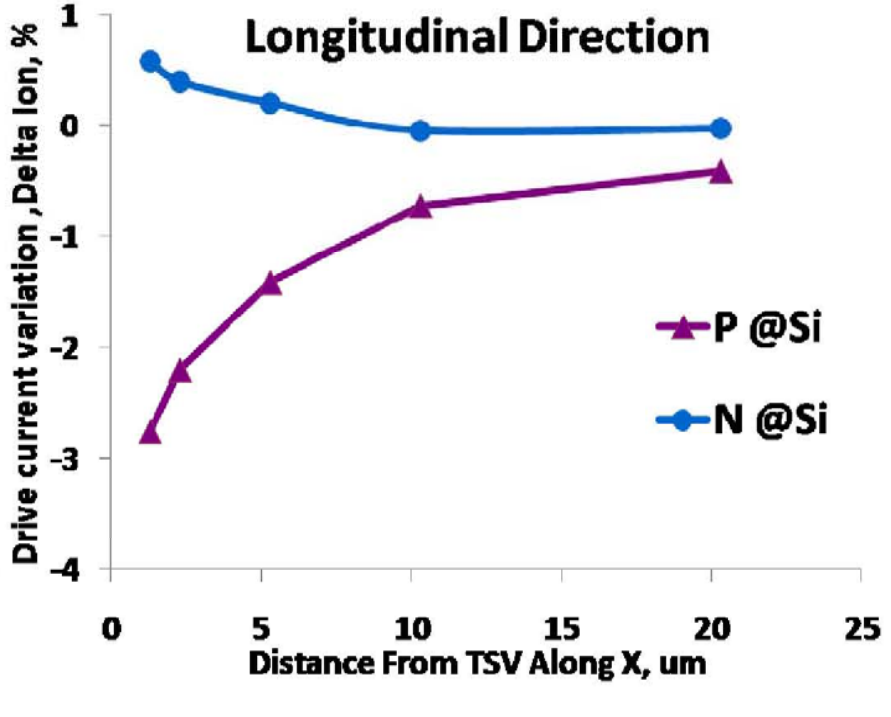


AC + Leak, High Fault Coverage

Characterization + ?

Impact of TSV Stress on Neighboring Transistors

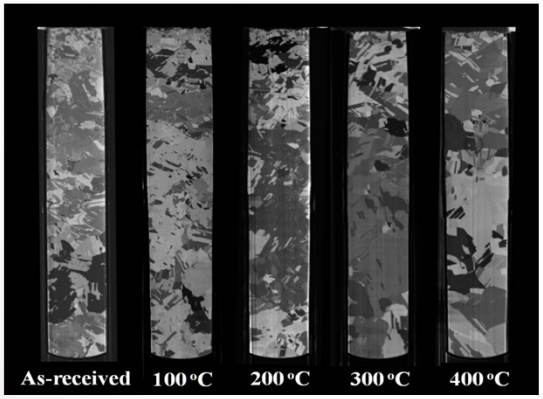




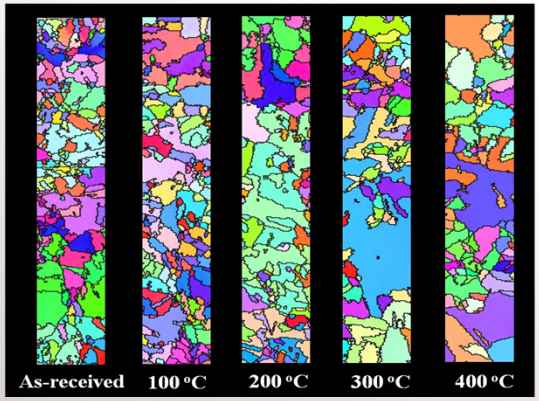
Manage Cu Grain Growth to Mitigate Cu Pumping

Electron Backscatter Diffraction Images showing TSV grain texture change with anneal temp

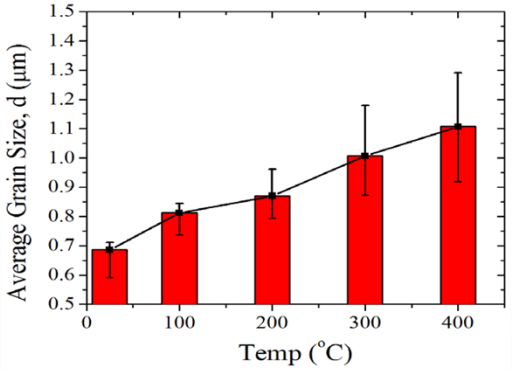
FIB

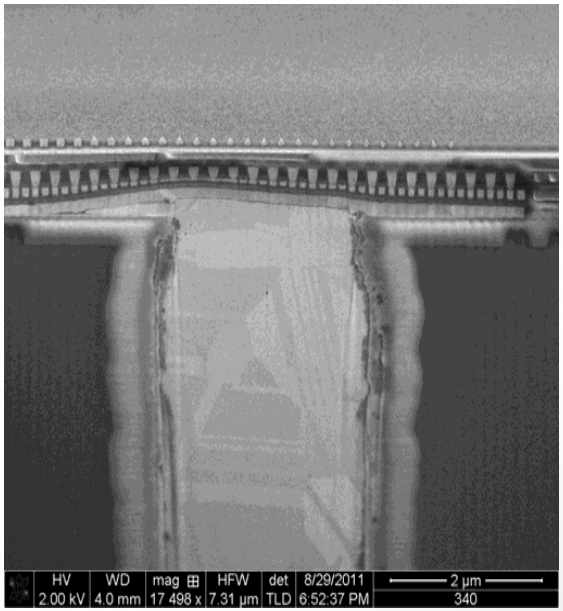


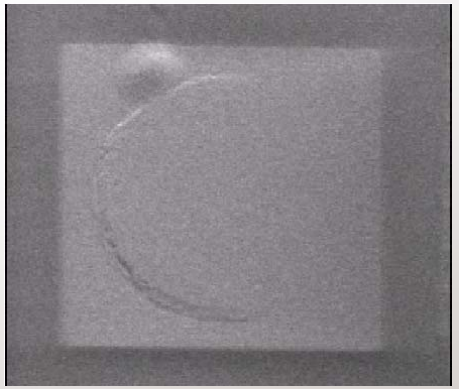
EBSD



Grain Growth with Temperature:







P. Ho et al , U Texas 2012 Austin 3D Workshop

New Fault Mechanisms – TSV Formation

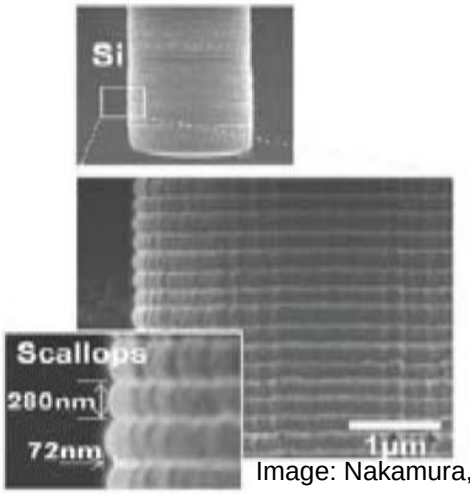
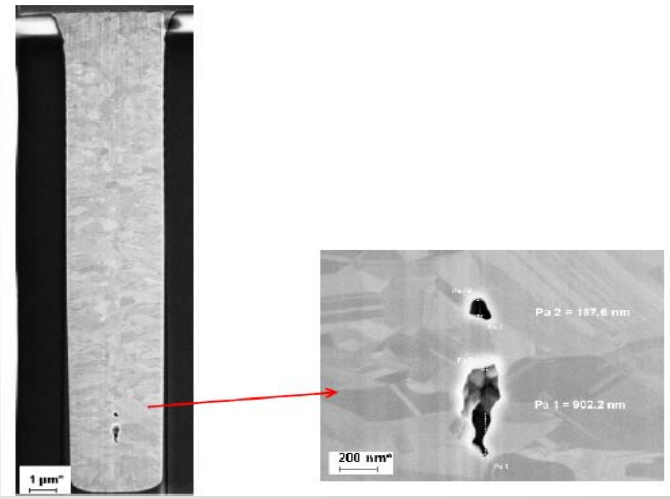


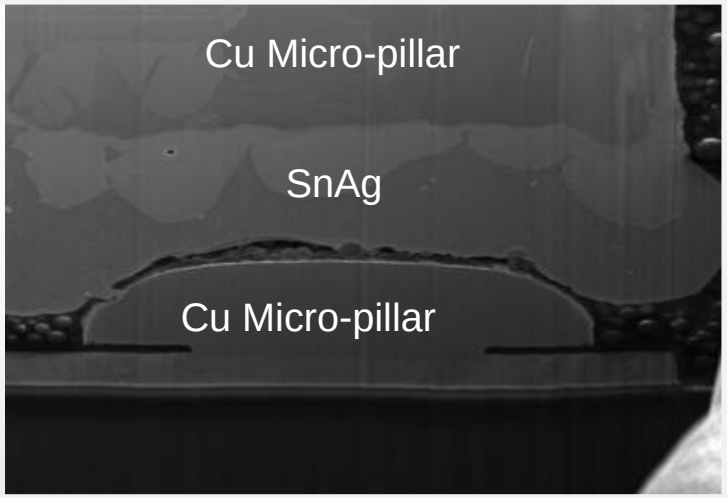
Image: Nakamura, 3DIC2011

- Poor TSV etch profile
- Poor liner/barrier/seed sidewall coverage of scallop underside & TSV bottom
  - ➢ Results in liner leakage, Cu diffusion into silicon, poor Cu fill, liner cracking

- Submicron Cu voids

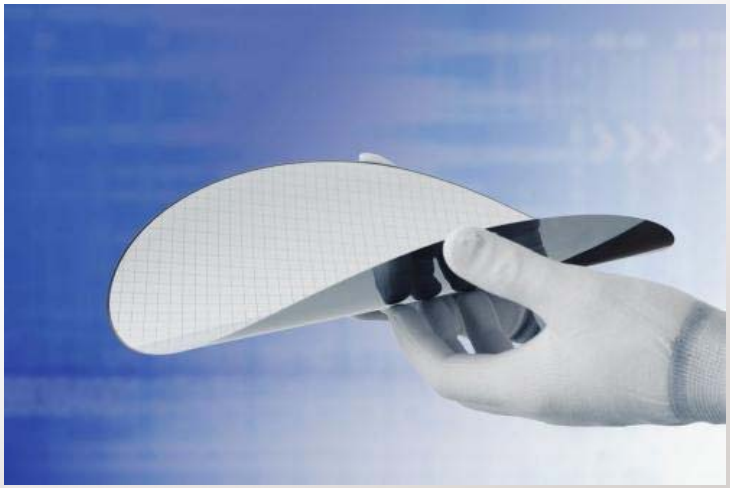


New Fault Mechanisms - Stacking



- No-flow underfill (NUF) trapped in microbump joint

- Thin wafer and die subsurface micro-cracks



Concerns in Managing 3D TSS Mechanical Stress with Test/DFT

- **The impact is parametric thus the tests required are AC**
  - AC Tests can be expensive
- **CPI Stress is a systematic mechanism and thus not random**
  - Location dependent on package design and component placement
  - Circuit sensitivity plays an important role
- **Increasing AC Fault Coverage in Production Test is Inefficient**
  - For a given device/design problem areas are not random and will not change

Managing Mechanical Stress at Test/DFT – What Can We Do? A Few Ideas

- **Utilize Stress Models/Checks to predict stress hot spots and note which IP/Blocks are nearby**
- **More extensive AC test suite for Device Characterization**
  - Target High Stress Areas and Sensitive IP/Blocks
  - Test at Cold Temps and possibly Hot (cold is usually WC for package stress)
- **If warranted select a small subset of AC tests to add to production test**
  - Tests that have shown a stress sensitivity in characterization
- **Look for possible interactions with other mechanisms**
  - Eg. Thermal Hot Spots could interact with Stress
- **Think Outside the Vector Box**
  - Opportunity for new test techniques

Conclusions: What's Next?

- **The semiconductor game is changing**
  - **rising cost of lithography-driven CMOS scaling**
  - **architectural differentiation from packaging**
- **3D chip stacking using TSVs offers a new bag of tricks for chipset architects**
- **Development of high density TSV technology and associated industry infrastructure has considerable momentum**
- **Memory stacking and 2.5D interposers, then LOL and 3.5D**
- **Many TSS challenges and opportunities to keep us busy**