

# Crossover in TD efficiency – When brick wall is not the best.



Keith Breinlinger Ph.D.

FormFactor, Inc.



**IEEE SW Test Workshop**  
**Semiconductor Wafer Test Workshop**

June 10 - 13, 2012 | San Diego, California

# Overview

- **Background**
- **Method of Analysis – FFI TDO Tool**
- **Analysis of thirteen 300mm wafers**
- **The Crossover Formula**
- **What about skip row or skip row & column?**
- **Summary**
- **Does it really work?**

# When does it make sense to use a Full Wafer Contactor??

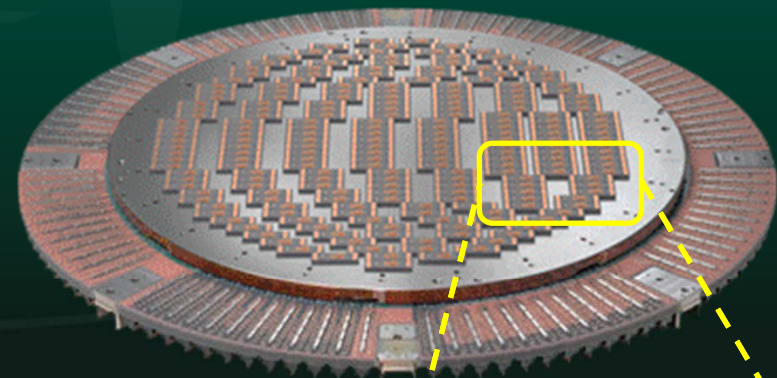
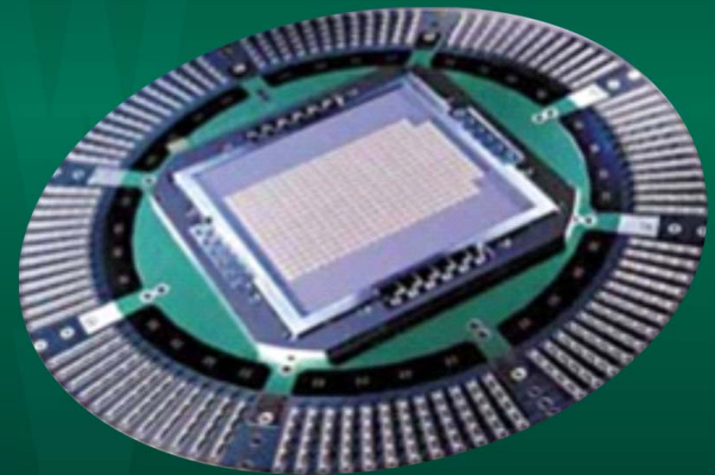
## Probe Head

- Multiple sizes from 50mm to 150mm.
- Depending on the die can do:
  - Brick wall (no gaps between tested die)
  - Skip R or C (a 1 die gap in one direction)
  - Skip R & C (a 1 die gap in both directions)

## Full Wafer Contactor (FWC)

- Touches the entire wafer at once (200mm or 300mm)
- DUTlet based system uses the same routing on all sites
- Initial cost is higher than PH, but ROI is worth it when parallelism is high enough.

***But when is the parallelism high enough??***



“DUTLETs”

June 10 - 13, 2012



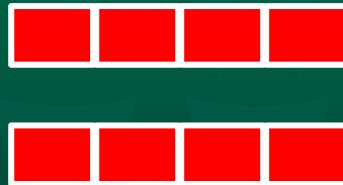
IEEE Workshop

# Terminology & Method of Analysis

- **Brickwall**



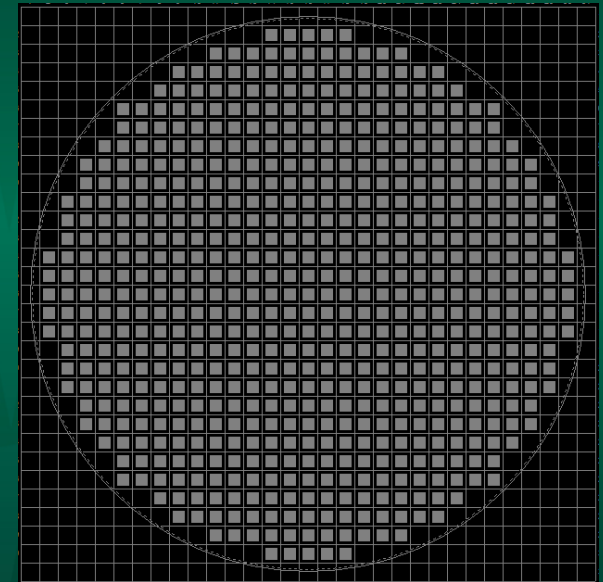
- **Skip Row**



- **Skip Column**



- **Skip R & C**



*300mm wafer,  
2mm edge exclusion.*

*For each die size from:  
4mm x 4mm to 12mm x 12mm:  
Run 4 analyses*

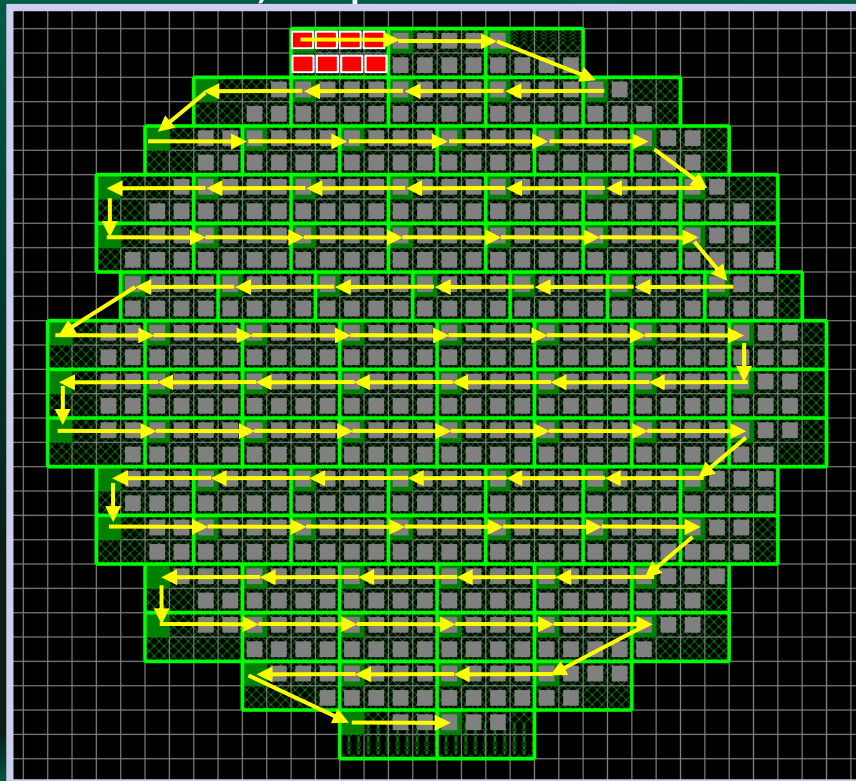
- 1) PH Brickwall,*
- 2) PH Skip R and PH Skip C*
- 3) PH Skip R & C*
- 4) Full Wafer Contactor*

# Analysis #1 – 8 DUTs in Parallel

300mm wafer, 10x10 die, 633 DPW

## Probe Head

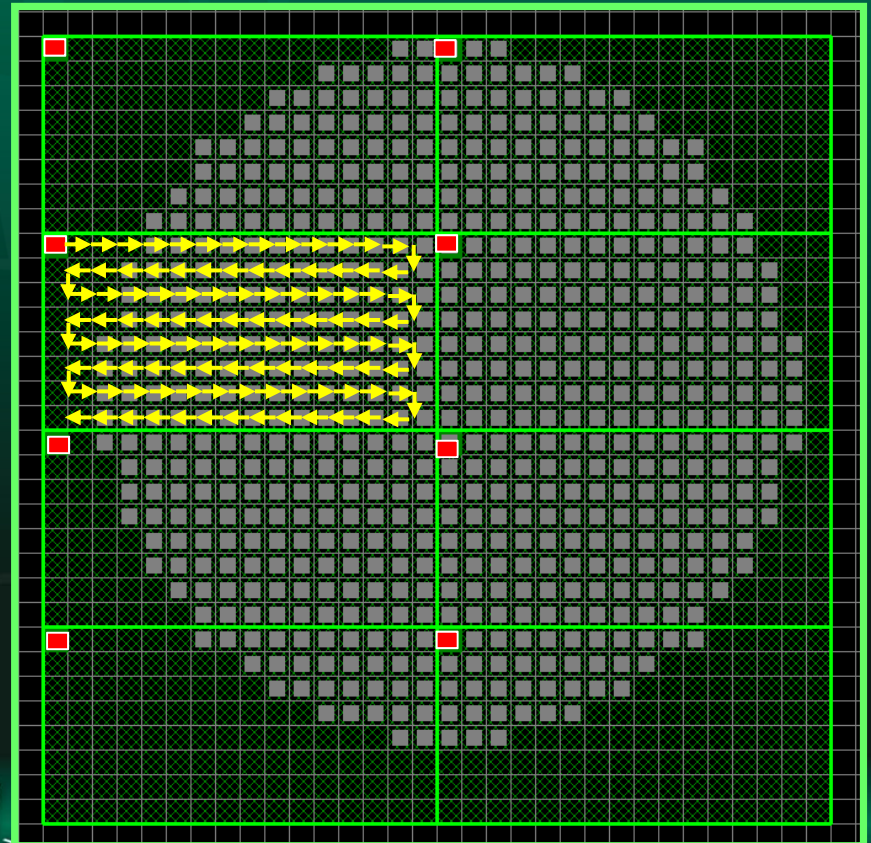
- 2x4, brickwall = 91 TDs
- 2x4, skip R = 93 TDs
- 2x4, skip R&C = 97 TDs



June 10 - 13, 2012

## Full Wafer Contactor

- 7 skip R x 14 skip C  
= 120 TDs

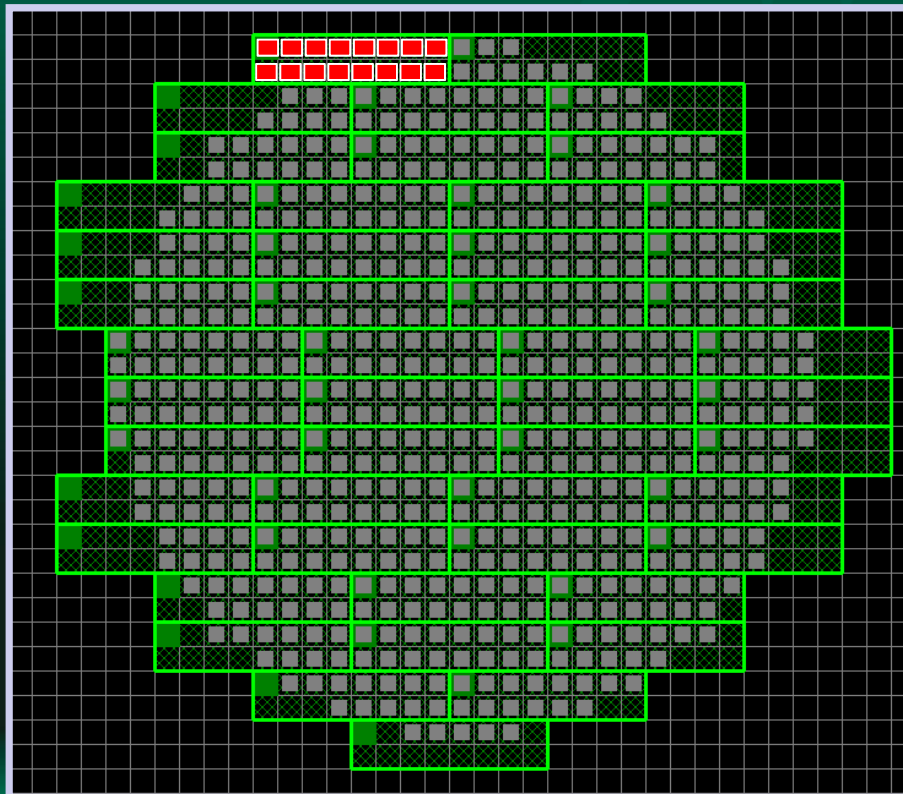


# Analysis #1 – 16 DUTs in Parallel

300mm wafer, 10x10 die, 633 DPW

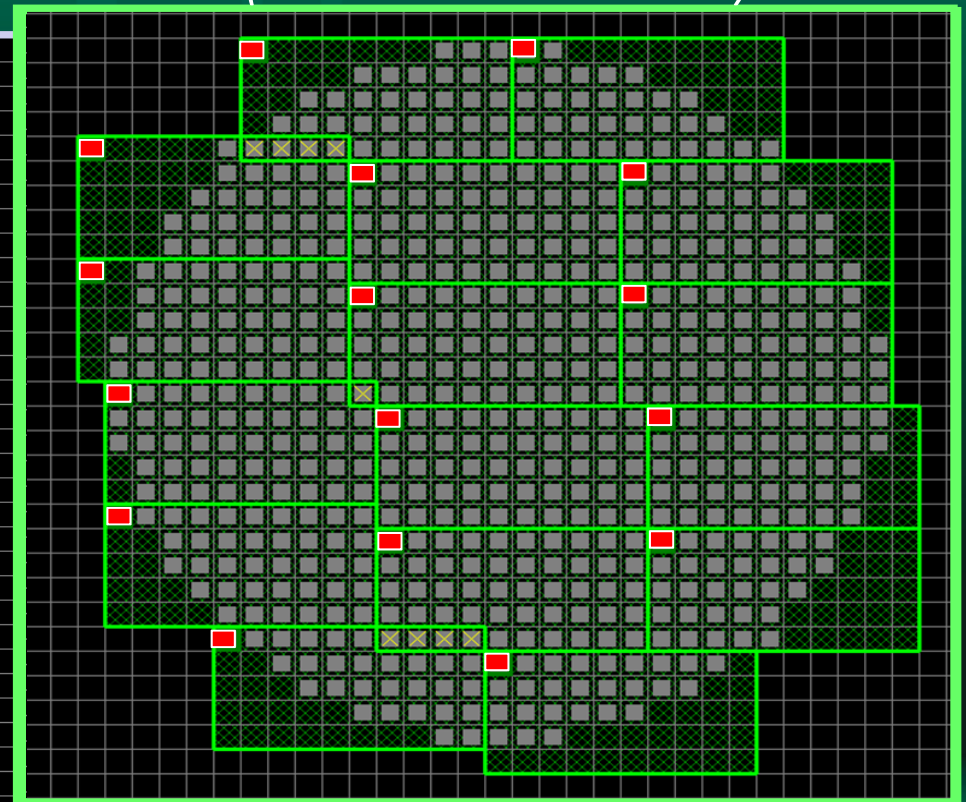
## Probe Head

- 2x8, brickwall = 49 TDs
- 2x8, skip R = 51 TDs
- 2x8, skip R&C = 54 TDs



## Full Wafer Contactor

- 4 skip R x 10 skip C = 55 TDs
- 4 skip R x 9 skip C = 50 TDs  
*(with 9 double touches)*



# Analysis #1 – 32 DUTs in Parallel

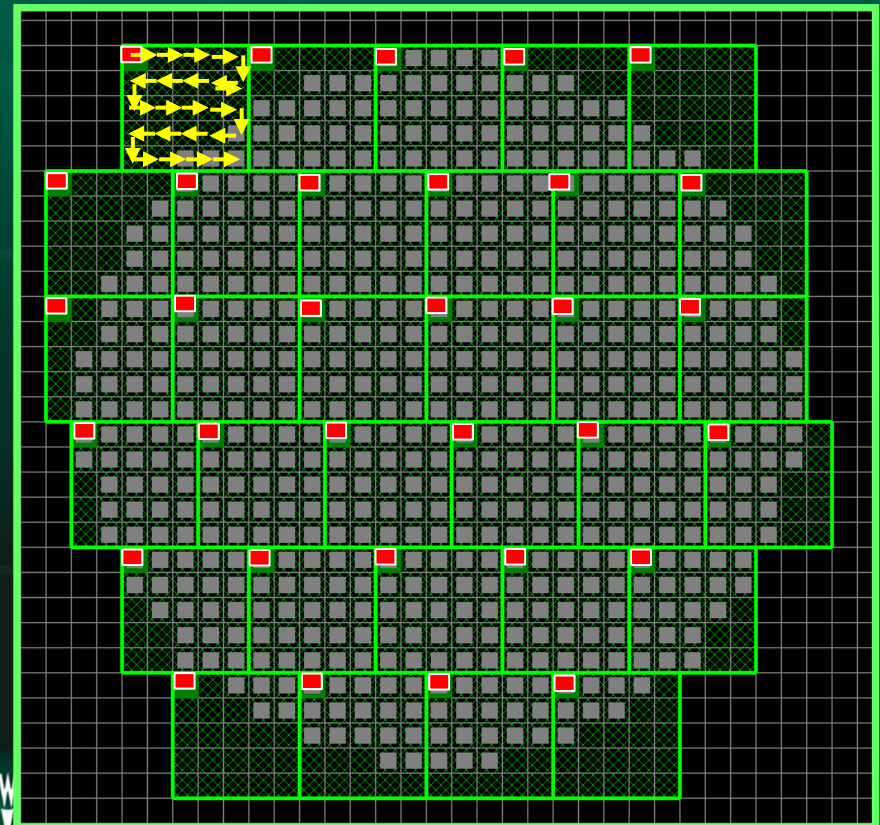
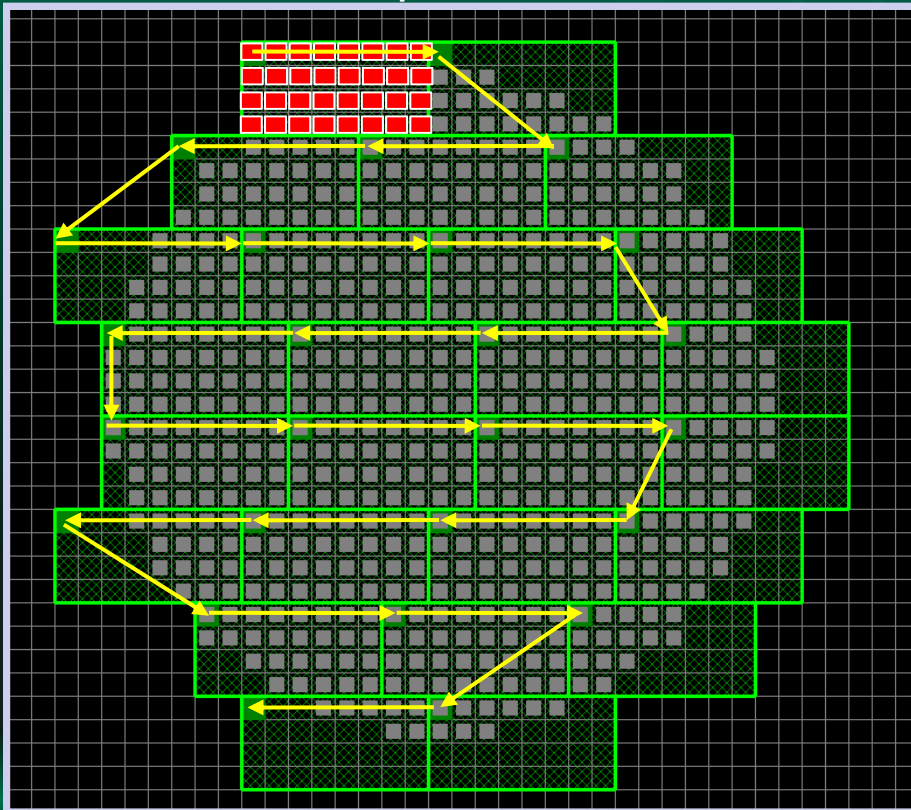
300mm wafer, 10x10 die, 633 DPW

## Probe Head

- 4x8, brickwall = 26 TDs
- 4x8, skip R = 28 TDs
- 4x8, skip R&C = 31 TDs

## Full Wafer Contactor

- 4 skip R x 4 skip C = 25 TDs



# Analysis #1 – 48 DUTs in Parallel

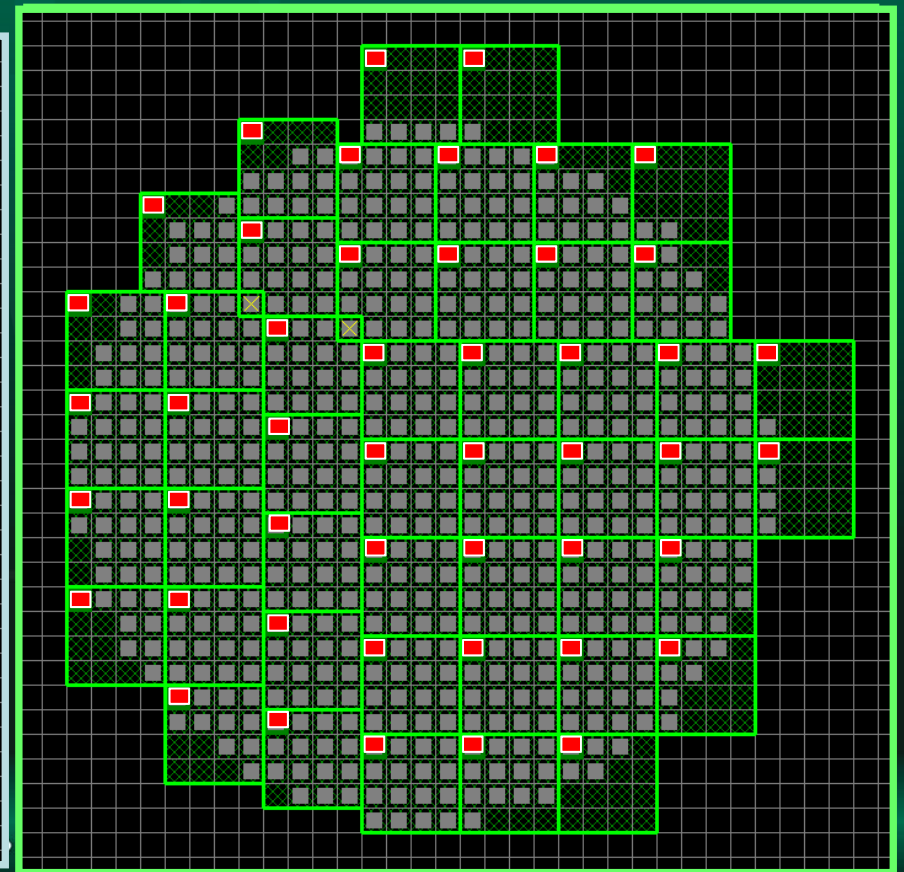
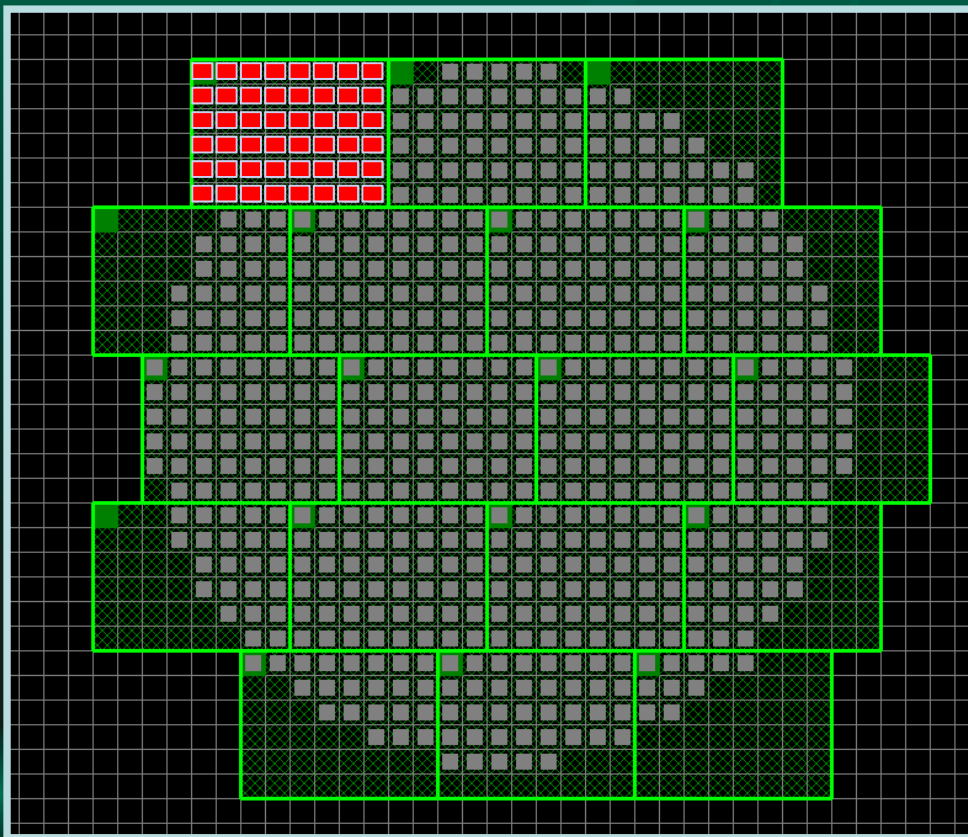
300mm wafer, 10x10 die, 633 DPW

## Probe Head

- 6x8, brickwall = 18 TDs
- 6x8, skip R = 20 TDs
- 6x8, skip R&C = 23 TDs

## Full Wafer Contactor

- 2 skip R x 5 skip C = 18 TDs  
*(and uses only 42 DUTs)*
- Or 16 TDs *(with 2 double touches)*



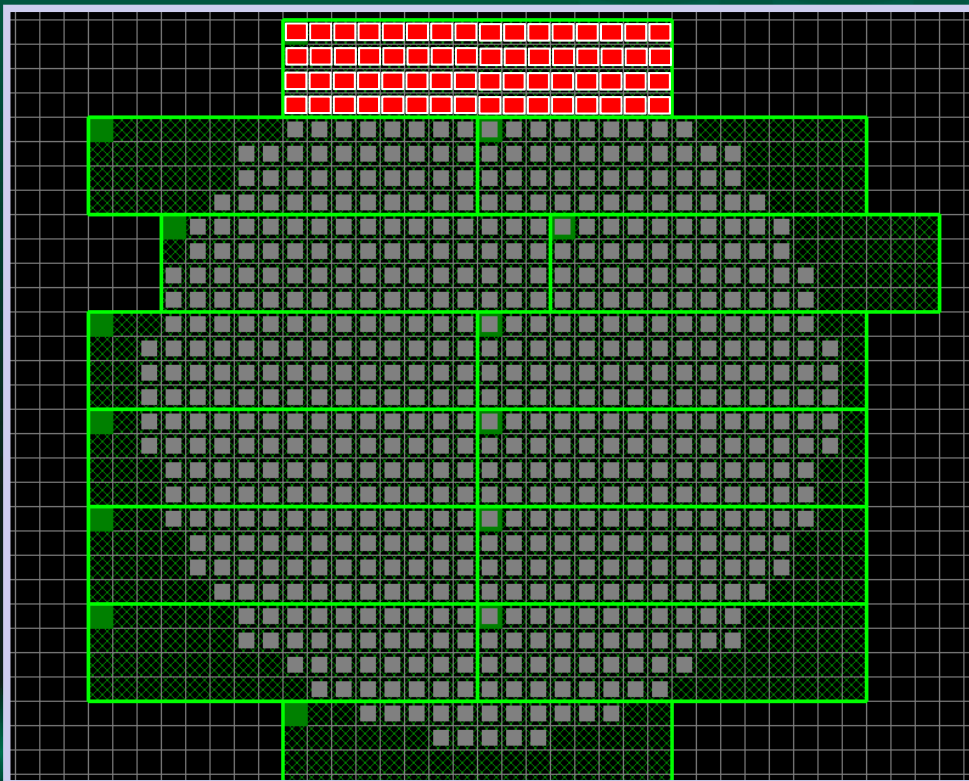


# Analysis #1 – 64 DUTs in Parallel

300mm wafer, 10x10 die, 633 DPW

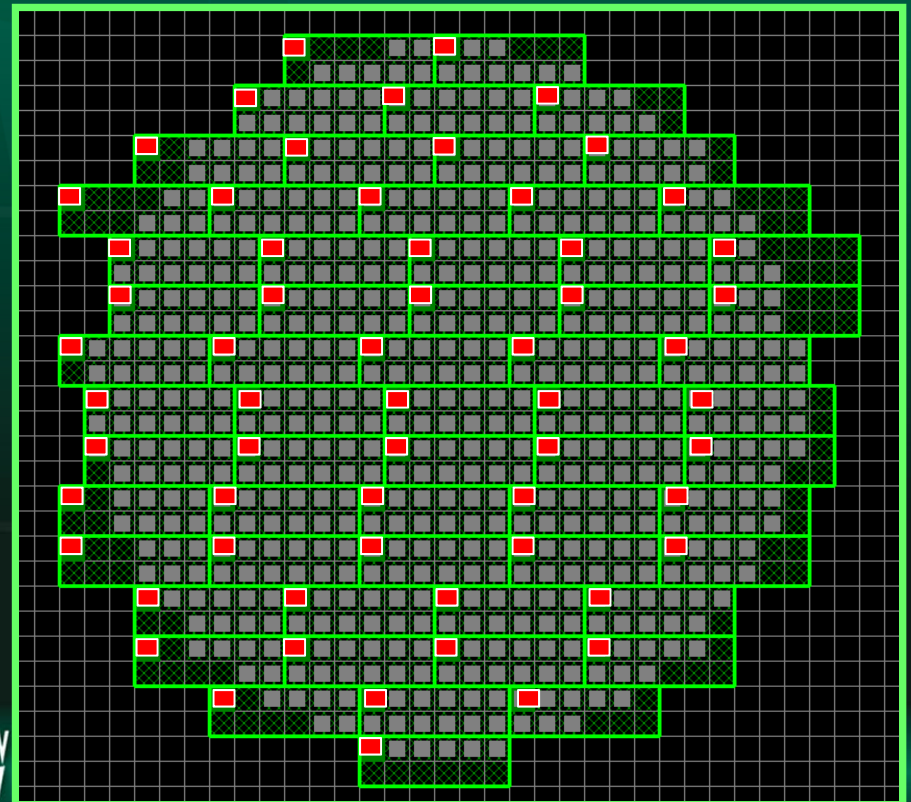
## Probe Head

- 4x16, brickwall = 14 TDs
- 4x16, skip R = 16 TDs
- 4x16, skip R&C = 16 TDs



## Full Wafer Contactor

- 1 skip R x 5 skip C  
= 12 TDs  
*(and only uses 61 DUTs)*



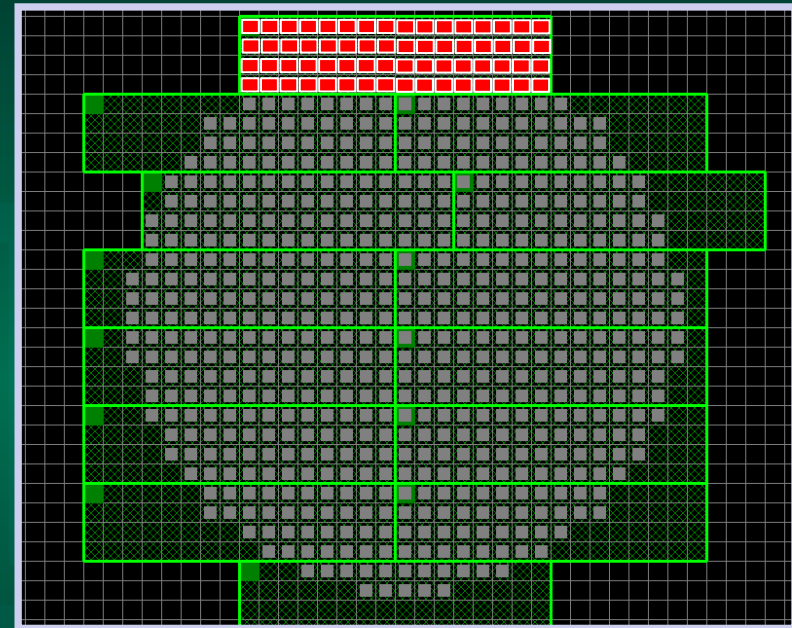
# Sidenote:

300mm wafer, 10x10 die, 633 DPW

- **64 DUTs in Parallel**

## Probe Head

– 4x16, brickwall = 14 TDs



- For each and every analysis – I run all possible rectangular combinations. For example – in this case – 15x4, 4x15, 9x7, 8x8, etc. – all yield a 14TD design. In all cases I try to minimize the TD count with the maximum resources allocated (64 in this case).

#	TD Count	Probe Card Array	Probe Card DUTs
1	14	15 x 4	60
2	14	4 x 15	60
3	14	9 x 7	63
4	14	7 x 9	63
7	14	8 x 8	64
5	14	16 x 4	64
6	14	4 x 16	64

# Analysis #1 – 96 DUTs in Parallel

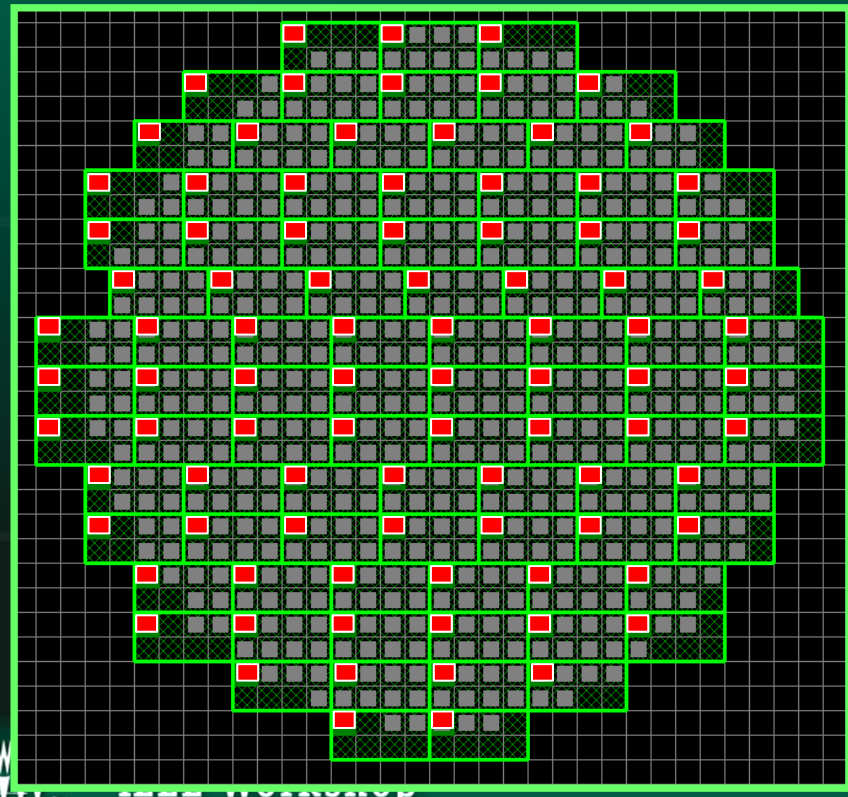
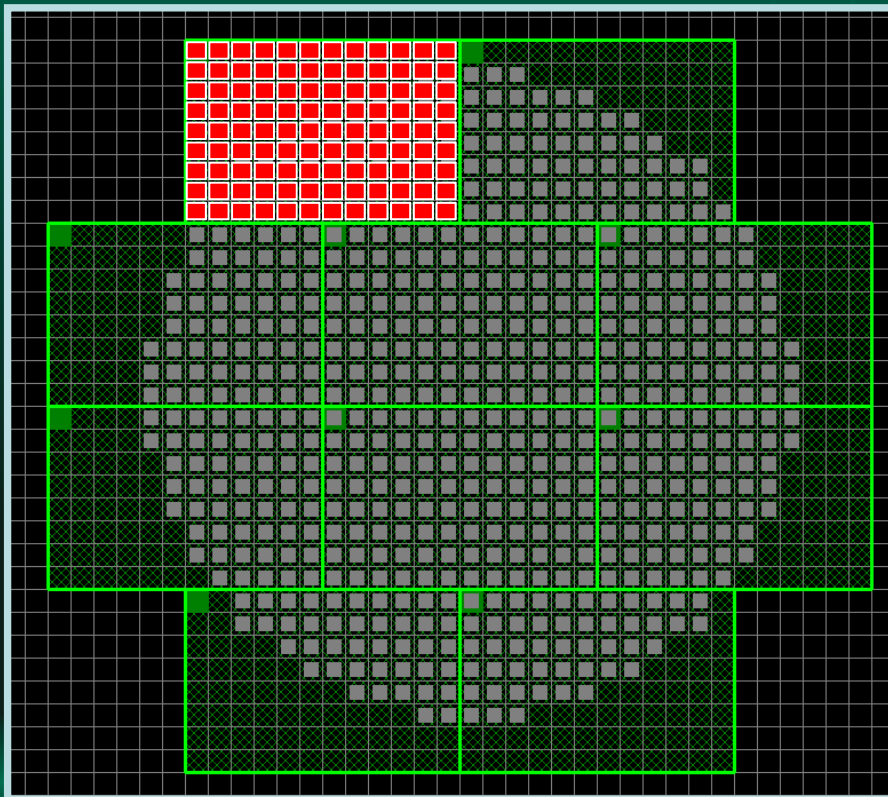
300mm wafer, 10x10 die, 633 DPW

## Probe Head

- 8x12, brickwall = 10 TDs
- 8x12, skip R = 10 TDs
- 8x12, skip R&C = 12 TDs

## Full Wafer Contactor

- 1 skip R x 5 skip C  
= 8 TDs  
(and only uses 91 DUTs)

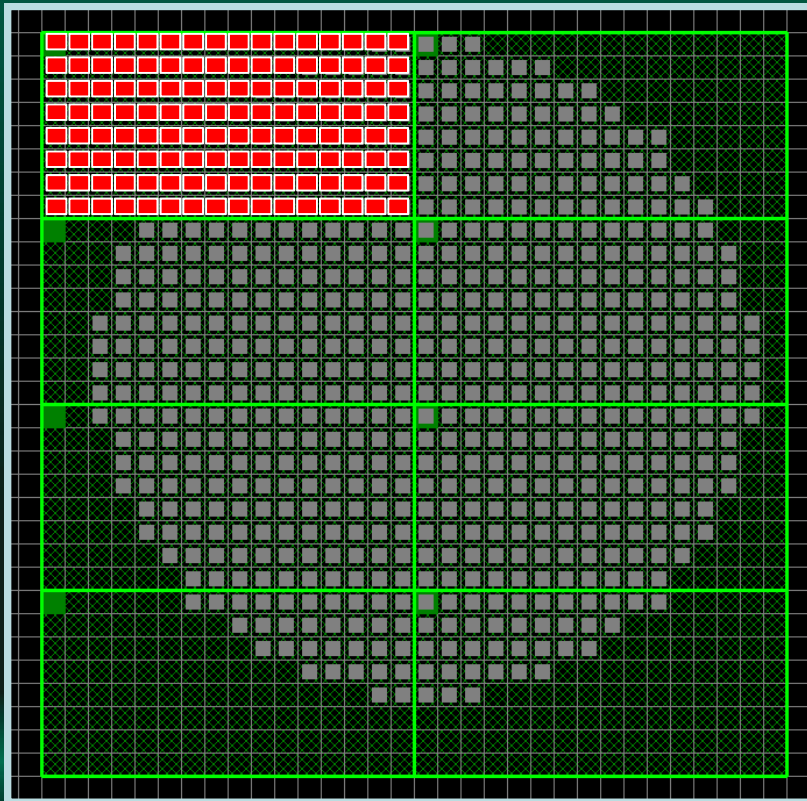


# Analysis #1 – 128 DUTs in Parallel

300mm wafer, 10x10 die, 633 DPW

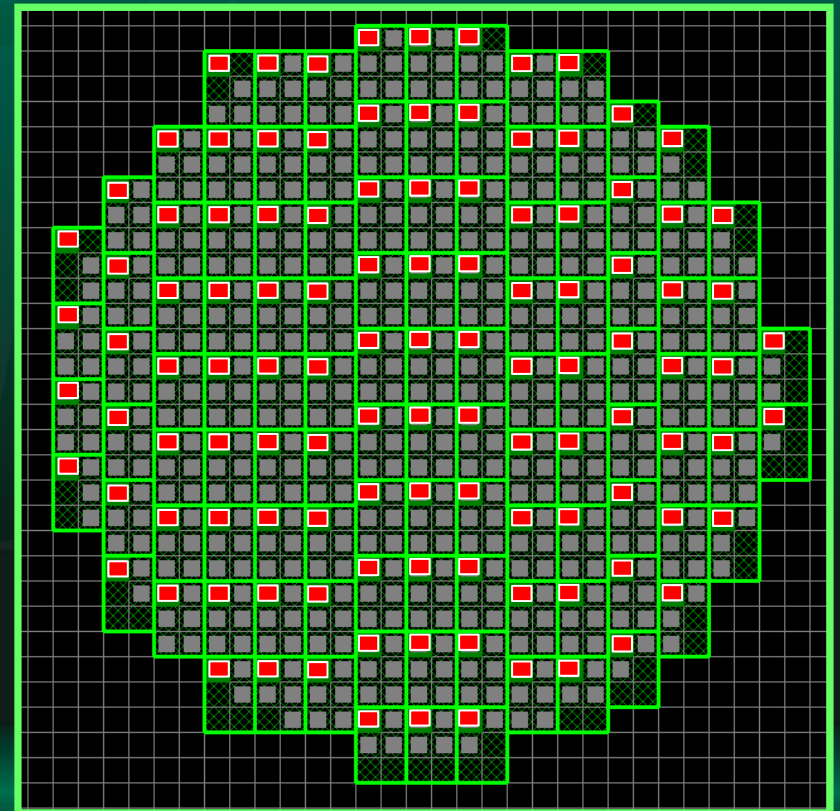
## Probe Head

- 8x16, brickwall = 8 TDs
- 8x16 skip R = 8 TDs
- 8x16 skip R&C = 8 TDs



## Full Wafer Contactor

- 1 skip R x 2 skip C  
= 6 TDs  
*(and only uses 114 DUTs)*



# Touchdown Efficiency

$$\frac{\# \text{ TDs}_{PH}}{\# \text{ of TDs}_{FWC}} = \text{TD Efficiency}$$

If TD Efficiency is < 100% PH is better

If TD Efficiency is > 100% FWC is better

Example 1:

$$\# \text{TDs}_{PH} = 20$$

$$\# \text{TDs}_{FWC} = 23$$

$$\text{TD efficiency} = 20/23 = 87\%$$

Example 2:

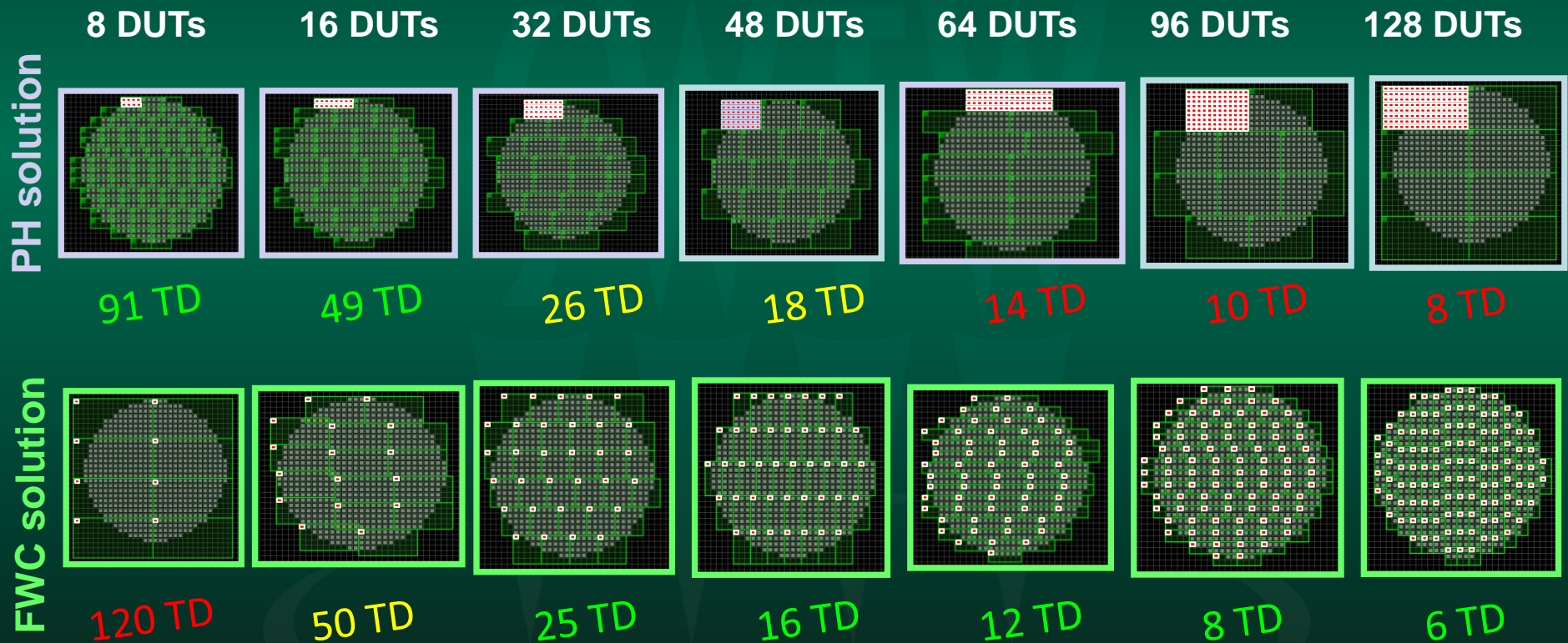
$$\# \text{TDs}_{PH} = 22$$

$$\# \text{TDs}_{FWC} = 18$$

$$\text{TD efficiency} = 22/18 = 122\%$$

# Analysis #1 *(same as the last 7 slides condensed to a single slide)*

300mm wafer, 10x10 die, 633 DPW



TD efficiency PH vs FWC

The crossover point



PH is better

FWC is better

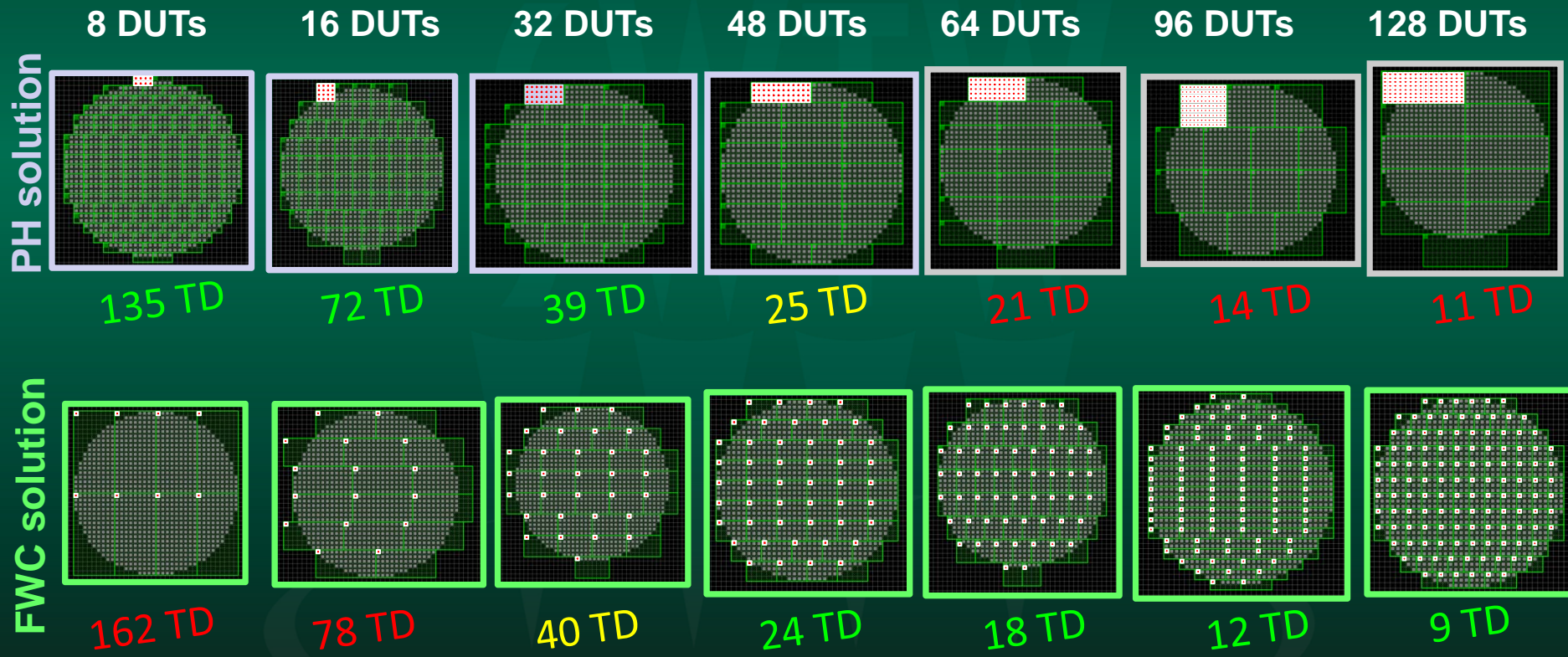
June 10 - 13, 2012



IEEE Workshop

# Analysis #2

300mm wafer, 8x8 die, 1020 DPW



TD efficiency PH vs FWC



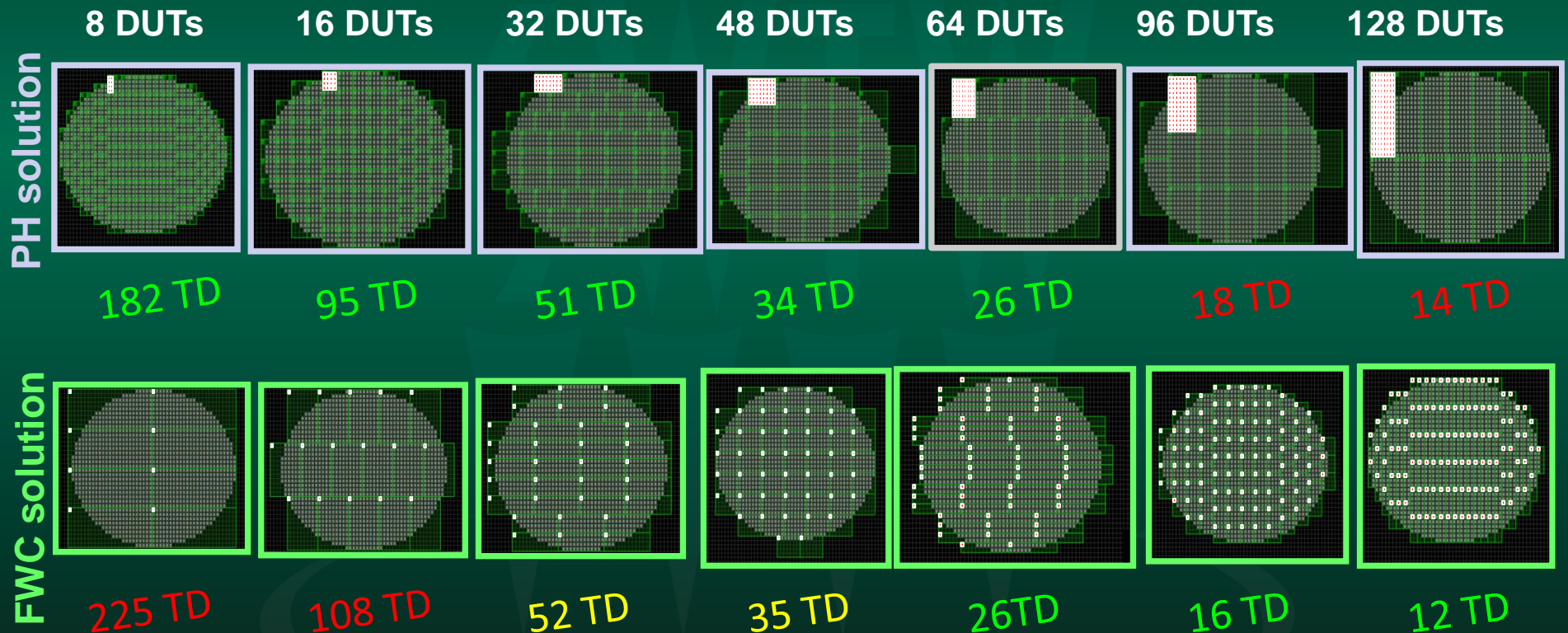
June 10 - 13, 2012



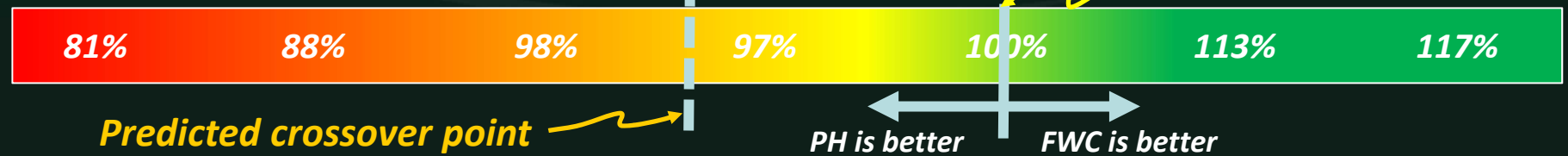
IEEE Workshop

# Analysis #3

300mm wafer, 6x8 die, 1372 DPW



TD efficiency PH vs FWC



June 10 - 13, 2012

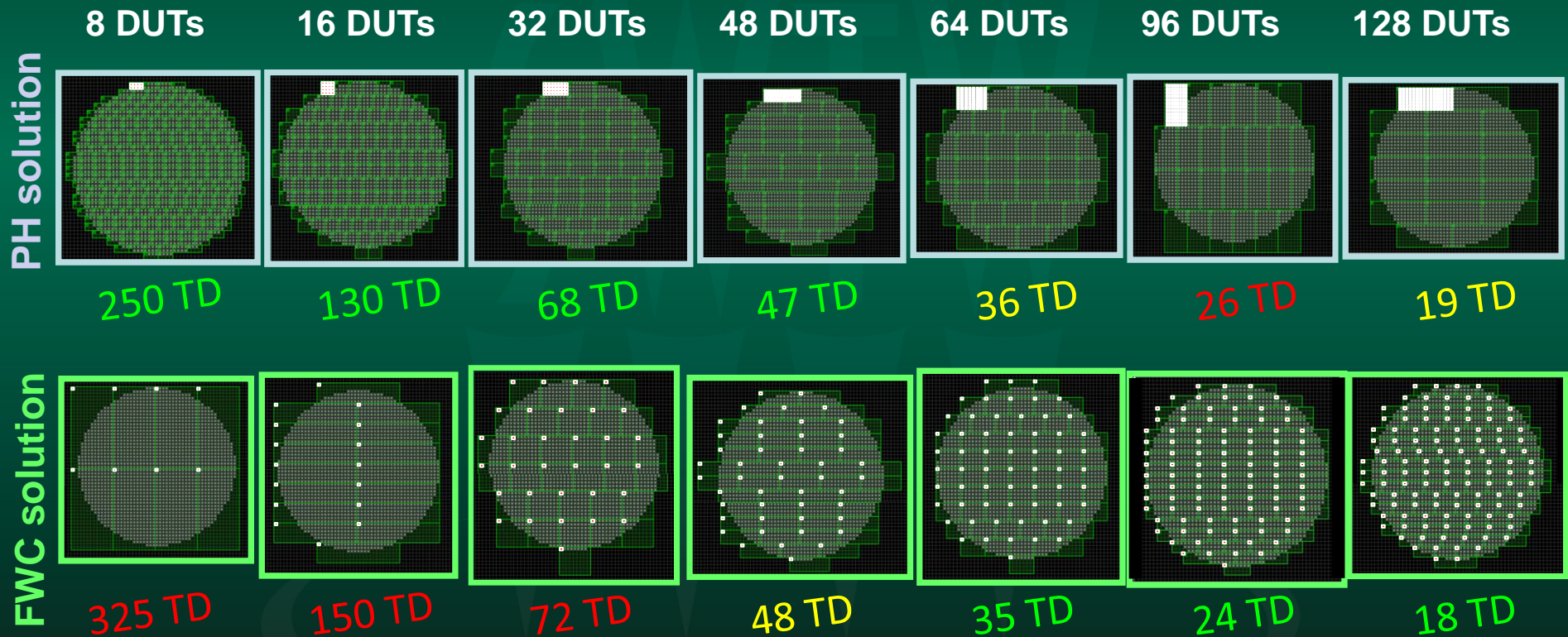


IEEE Workshop

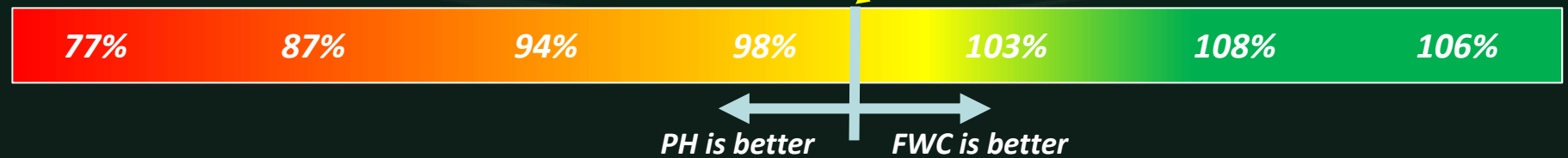


# Analysis #4

300mm wafer, 6x6 die, 1845 DPW



TD efficiency PH vs FWC



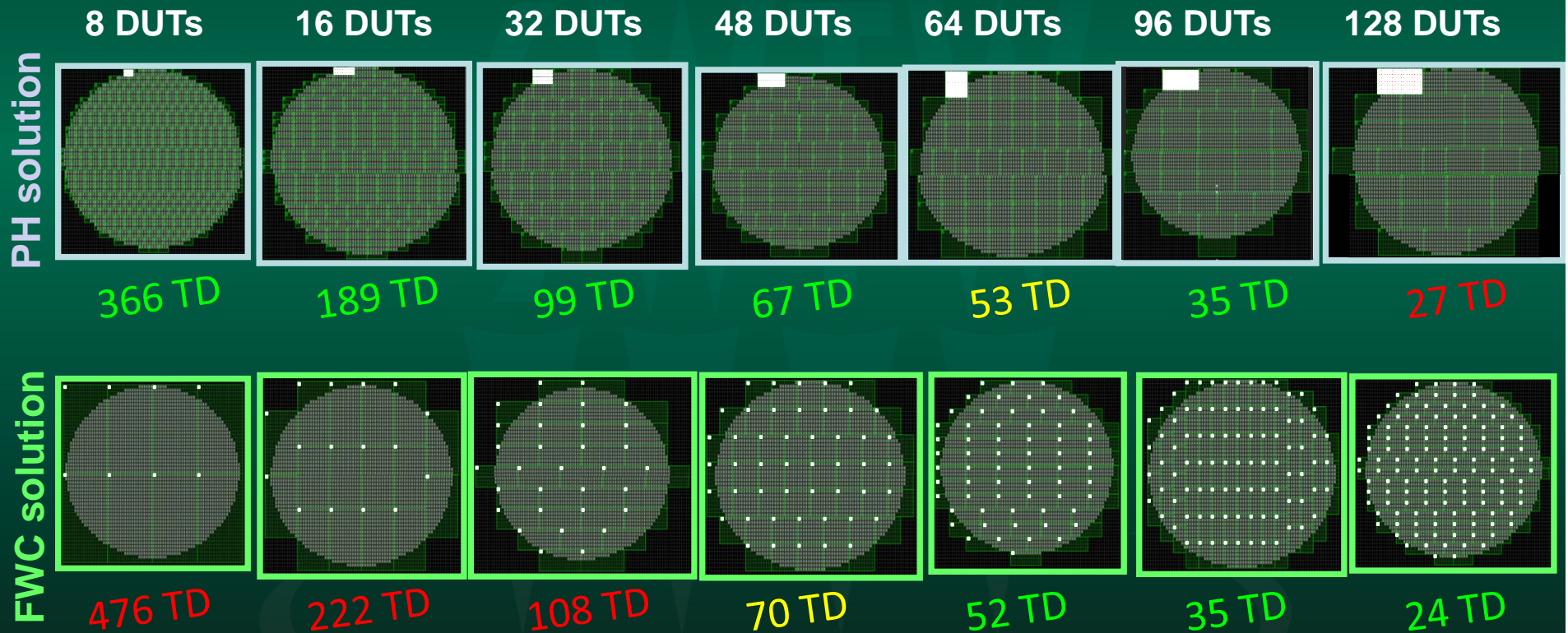
June 10 - 13, 2012



IEEE Workshop

# Analysis #5

300mm wafer, 4x6 die, 2798 DPW



TD efficiency PH vs FWC



June 10 - 13, 2012



IEEE Workshop

# The Crossover Ratio

$$\frac{\# \text{ DUTs}}{\# \text{ of TDs}_{PH}} = \text{Crossover Ratio}$$

Example 1:

$\#DUTs = 32$

$\#TDs_{PH} = 64$

**Crossover Ratio =  $32/64 = 0.5$**

Example 2:

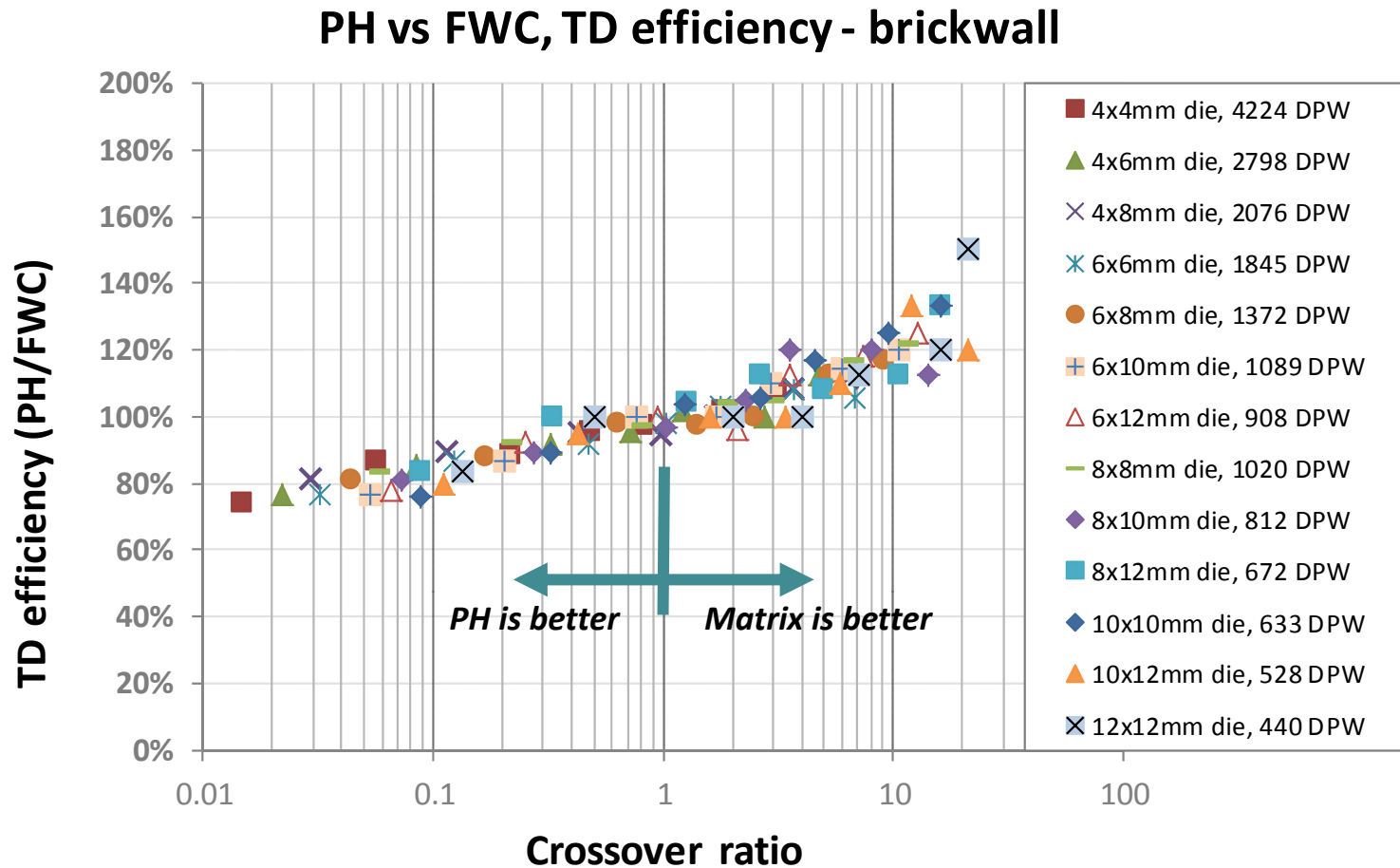
$\#DUTs = 32$

$\#TDs_{PH} = 16$

**Crossover Ratio =  $32/16 = 2$**

# Analysis #1-13 – Brickwall vs FWC

300mm wafer, 4x4 die – 12x12 in 2mm increments, 8 DUTs – 128 DUTs



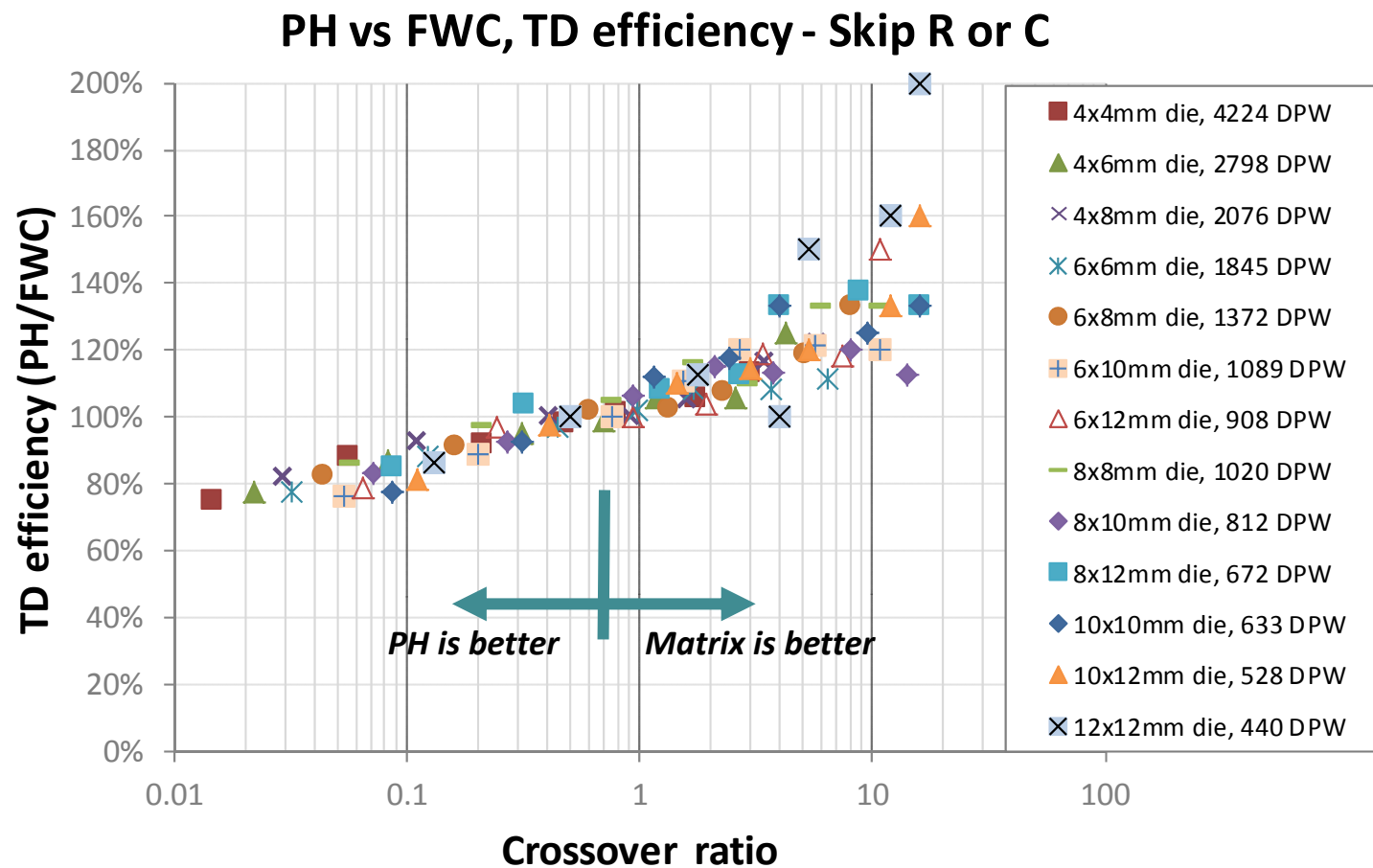
# The Crossover Formula

$$\frac{\text{\# DUTS}}{\text{\# of TDs}_{\text{brickwall}}} = \text{Crossover Ratio}$$

If Crossover ratio > 1, FWC is better  
If Crossover ratio < 1, PH is better

# Analysis #14-26 – Skip R or C vs FWC

300mm wafer, 4x4 die – 12x12 in 2mm increments, 8 DUTs – 128 DUTs



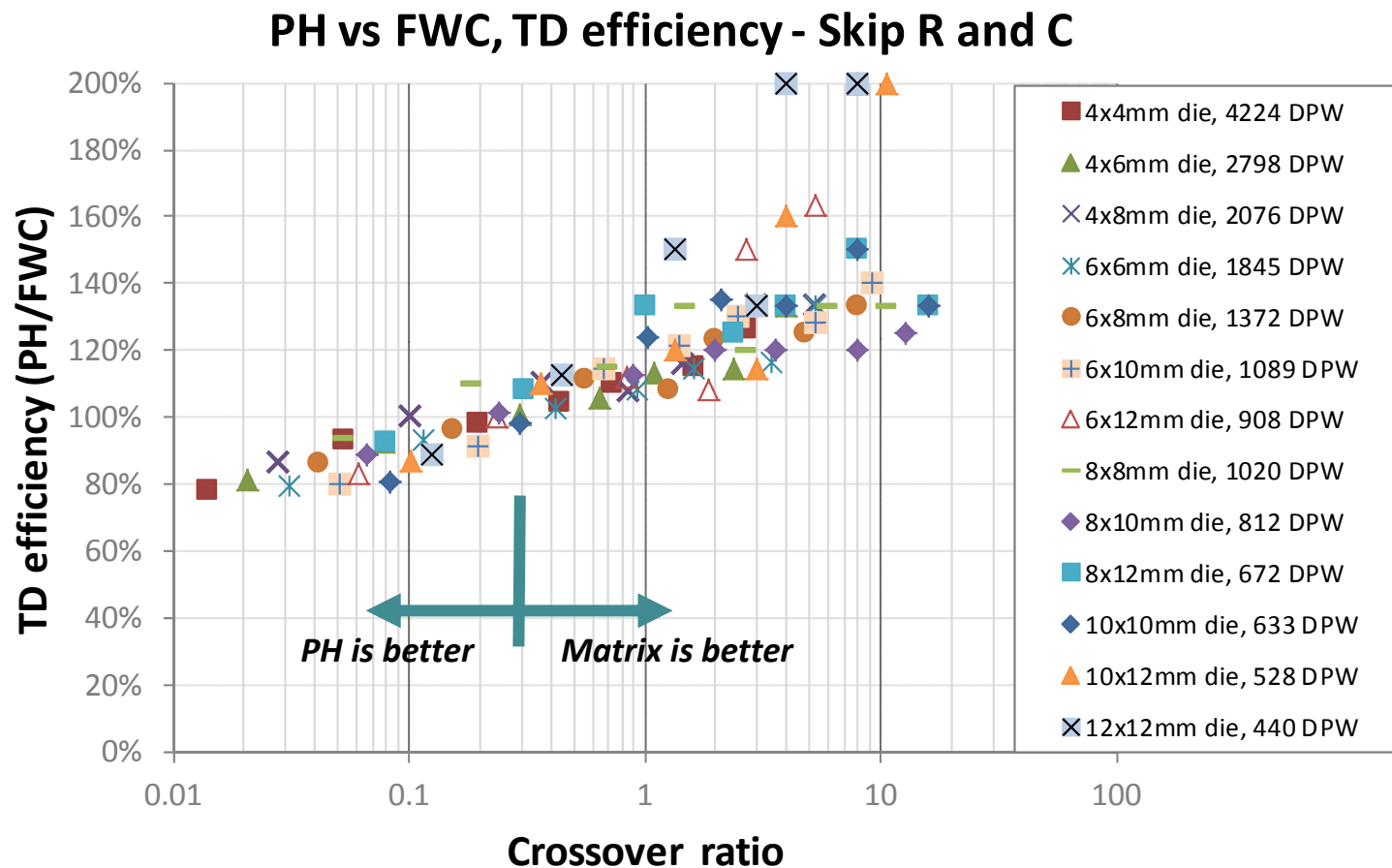
# The Crossover Formula (for skip Row or skip Column)

$$\frac{\text{\# DUTS}}{\text{\# of TDs}_{\text{skipRorC}}} = \text{Crossover Ratio}$$

If Crossover ratio > 0.7, FWC is better  
If Crossover ratio < 0.7, PH is better

# Analysis #27-39 – Skip R&C vs FWC

300mm wafer, 4x4 die – 12x12 in 2mm increments, 8 DUTs – 128 DUTs





# The Crossover Formula (for skip Row and skip Column)

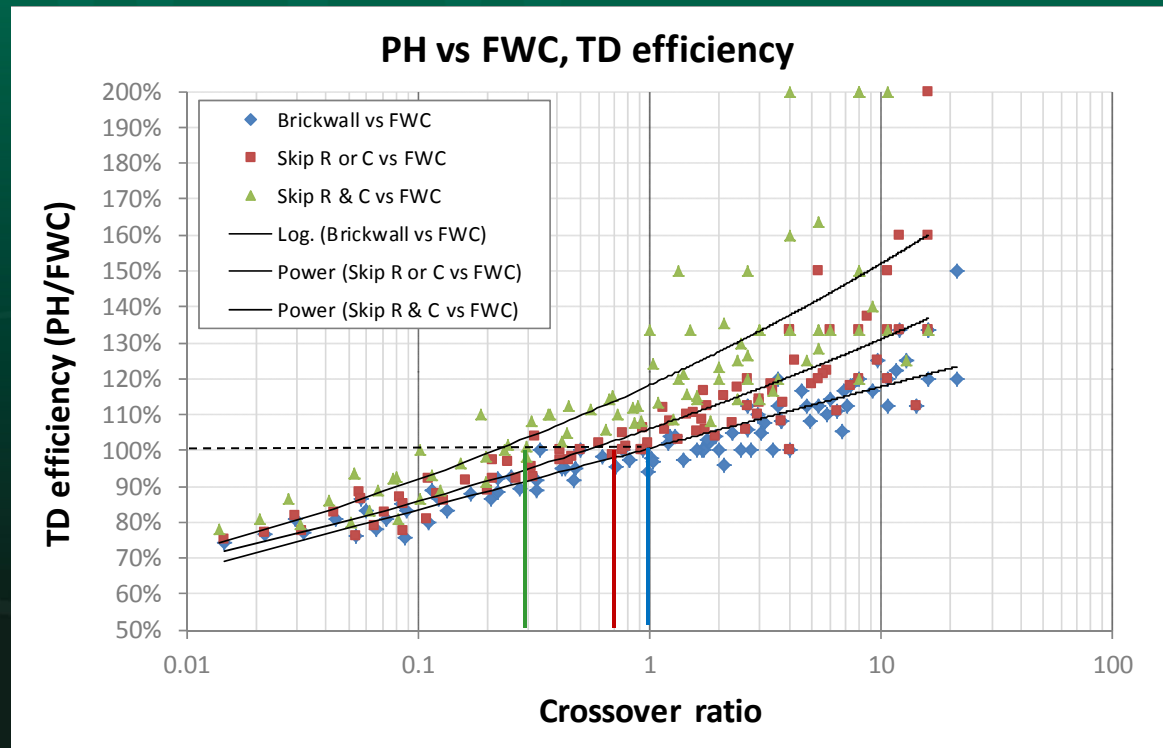
$$\frac{\text{\# DUTS}}{\text{\# of TDs}_{\text{skipR\&C}}} = \text{Crossover Ratio}$$

If Crossover ratio > 0.3, FWC is better  
If Crossover ratio < 0.3, PH is better

# Summary:

## *A Few Simple Rules of Thumb*

- When number of DUTs in parallel exceeds the number of touchdowns, a TrueScale Matrix product will give you better touchdown efficiency than a PH product.
- The larger the ratio of DUTs to TDs, the bigger the TD efficiency benefit.
- Use TrueScale Matrix when Crossover Ratio
  - $> 1.0$  for brick wall
  - $> 0.7$  for skip R or C
  - $> 0.3$  for skip R & C

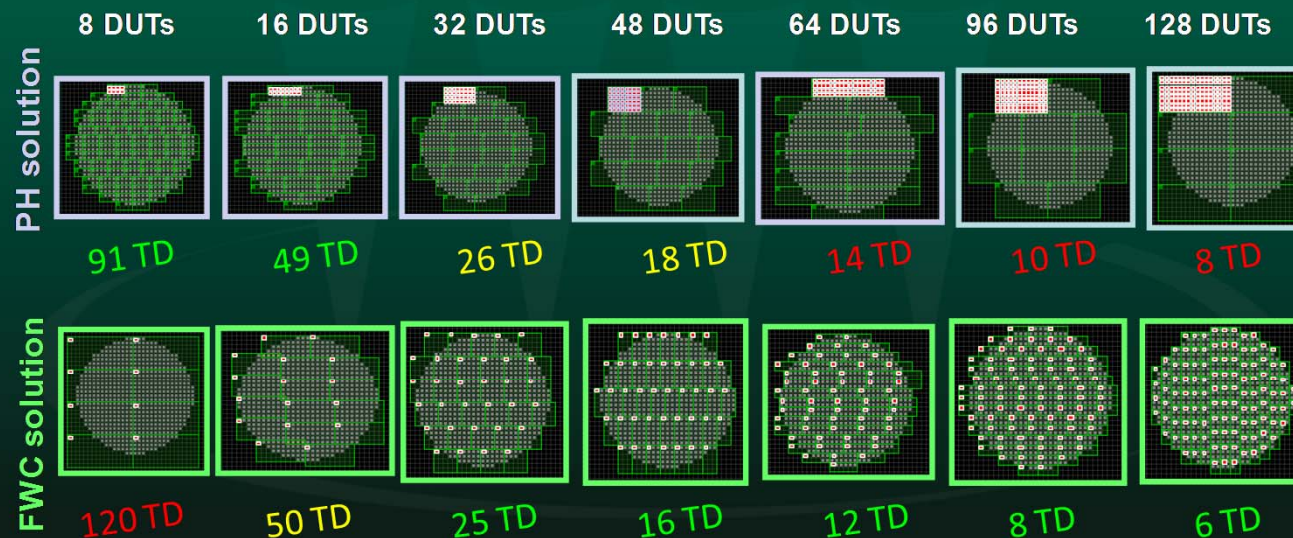


# Same Analysis on 200mm wafers

- Take any 300mm analysis and multiply die & wafer by 0.667
  - e.g. – 10mmx10mm die on 300mm wafer analysis is EXACTLY the same as 6.67mmx6.67mm on 200mm wafer - crossover occurs at same point
  - Formulas work on 200mm and 300mm wafers

## Analysis #40

200mm wafer, 6.67x6.67 die, 633 DPW



TD efficiency PH vs FWC



PH is better ← FWC is better →  
June 10 - 13, 2012

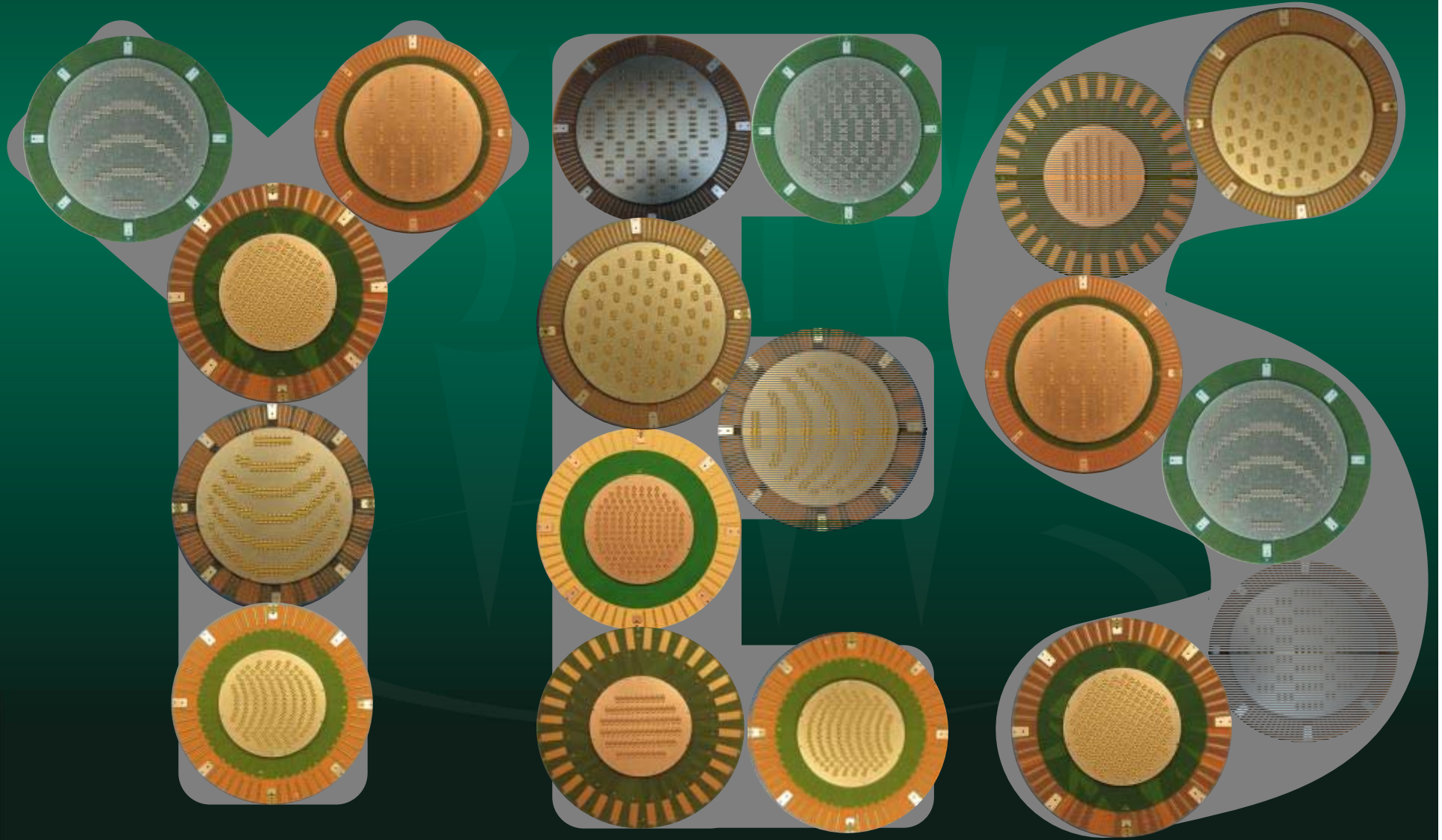


IEEE Workshop

# Additional Benefits of Matrix FWC

- **Electrical Performance**
  - Less crosstalk
  - Better noise isolation
  - More room for components
- **Force balance on chuck**
  - Some probers are quite sensitive to off-center loading
- **Thermal Soak & Stability Performance**
  - Card is nearly always over the chuck

# Does it really work?



June 10 - 13, 2012



IEEE Workshop

29

# One final formula:

*(with 3 different constants)*

$$DPW = \eta * \# DUTs * \# TDs$$

*When # DUTs = # TDs, crossover occurs.  
At the crossover point  $\eta \approx 85\%$ .*

**So:**  $\#DUTs_{\text{Brickwall Crossover}} \approx 1.1\sqrt{DPW}$

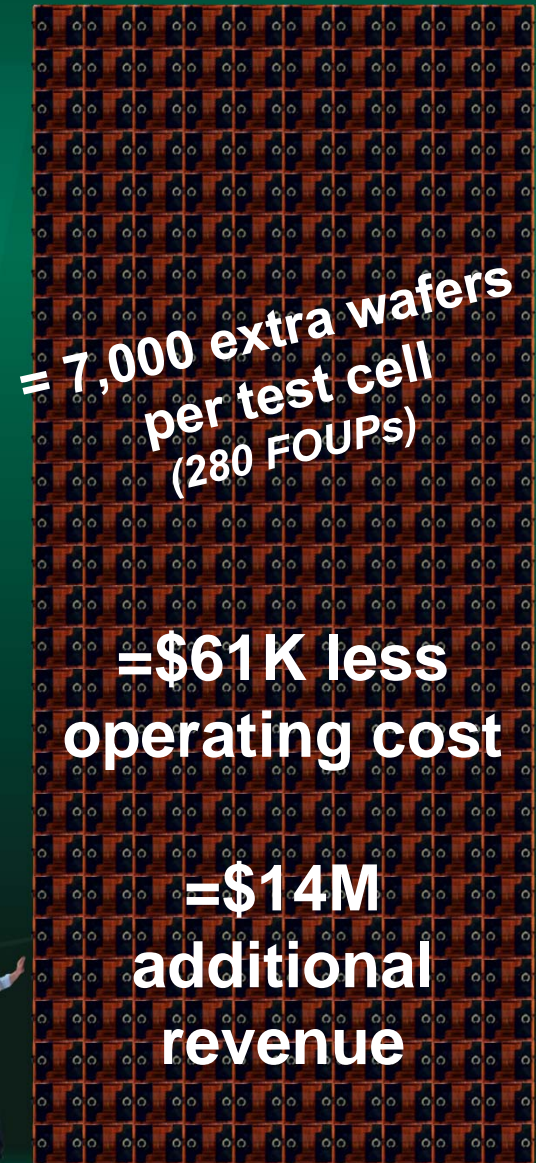
$$\#DUTs_{\text{Skip R or C Crossover}} \approx 0.9\sqrt{DPW}$$

$$\#DUTs_{\text{Skip R \& C Crossover}} \approx 0.6\sqrt{DPW}$$

# Return On Investment

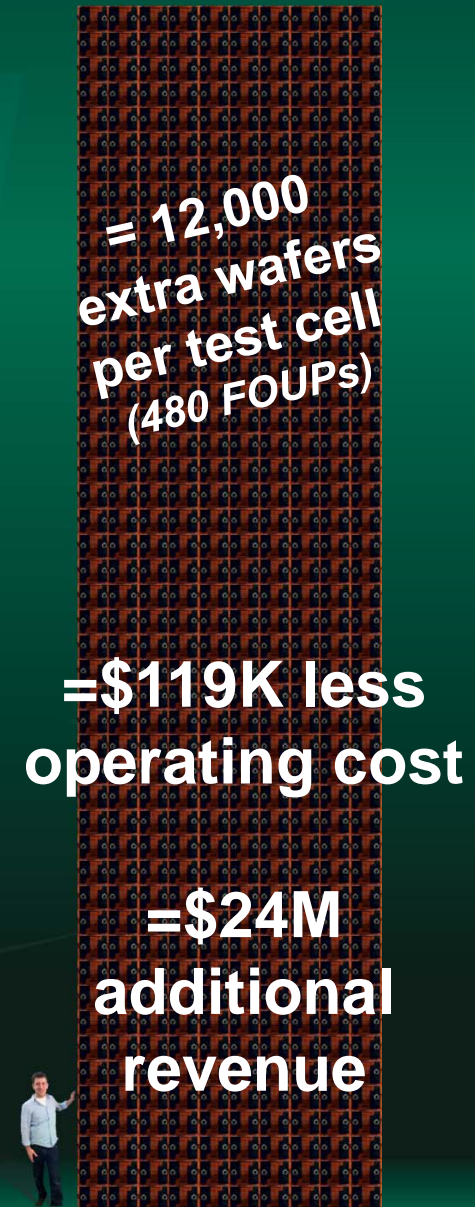
- **Using the 10x10, 64 site example:**
  - Assume 1 min test time
  - Running for 18 months
  - Assume Test Cell Depreciation + Operating cost = \$240K/year (J750 or equiv.)
  - Assume overall equipment effectiveness = 75%
  - Assume revenue per wafer = \$2000
  - Model is for 1 test cell

- **Compared to brickwall:  
efficiency was 17%  
higher = 42K vs 49K wafers**



# Return On Investment

- Using the 10x10, 64 site example:
  - Assume 1 min test time
  - Running for 18 months
  - Assume Test Cell Depreciation + Operating cost = \$240K/year (J750 or equiv.)
  - Assume overall equipment effectiveness = 75%
  - Assume revenue per wafer = \$2000
  - Model is for 1 test cell



- 
- Compared to skip R:  
efficiency was 33%  
higher = 37K vs 49K wafers
- 





# Thank you

Tim Henson

John Long

Shannon Collier

Michelle Griffing