Meeting the 1st Silicon:
An Alternate Approach for Reducing Probe Card Cycles

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Overview

- **Market Requirement - *to Meet 1st Silicon with Probing Solution***
  - WLCSP Applications Rely 100% on the Probe Hardware Cycle due to Combined Wafer & Final Package Test
  - More Tests Moving from Final Package to Probe for Improved Yield & Lower COO
  - Device Cycles are Reducing due to Improved Design Software Tools & Semi Fabs Reduced Silicon Cycles

Conventional Interconnects

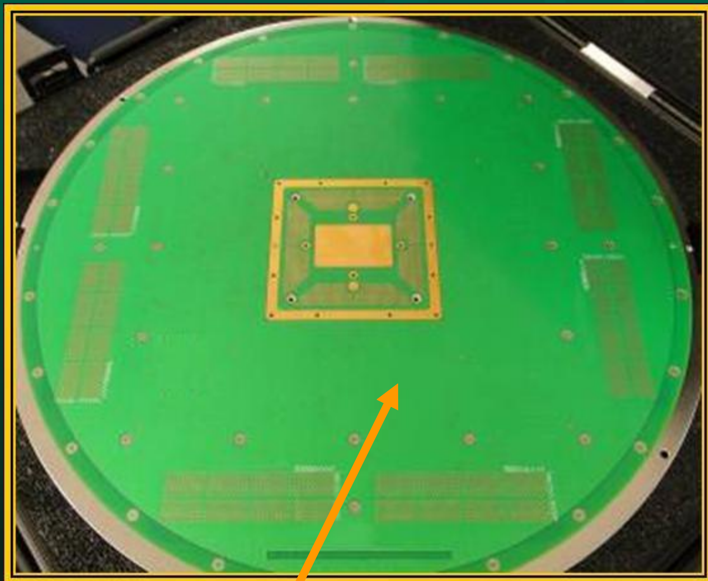
- **There are Several Drawbacks to Traditional Interconnects (MLC/MLO, Direct) –**
  - Long Cycle Time
  - Not Capable of Fine Pitch
  - PCBs Must be Custom
    - Cannot House Internal Components
    - Die Changes after PCB FAB Incur Costs, Lots Scrapped & Re-Design Required

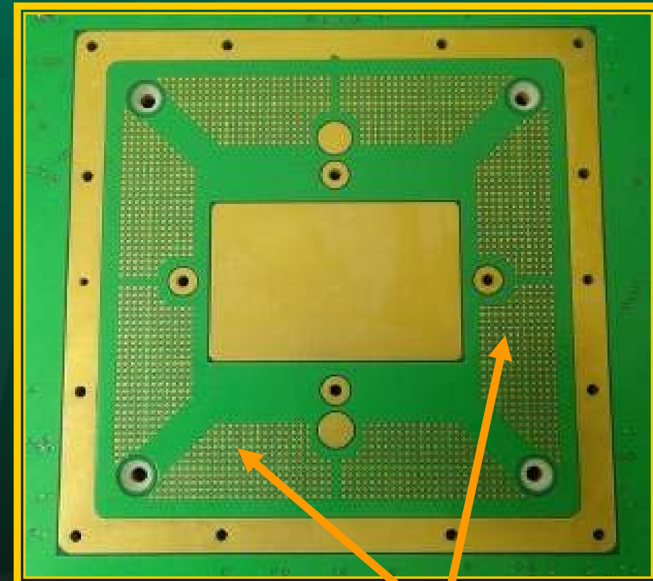
Modular Space Transformer™

- **New Probe Hardware Paradigm Required**
  - Shorter Cycle
  - Improved HVM to Meet Wafer Ramp
  - COO Sensitive
  - Reduced 1st Silicon Debug Capable
  - Ability to Make Resource Changes
  - Utilize for Common Components
- **Innovation Resulted in a New Type of Interconnect – the *Modular Space Transformer* or MST™**
  - Modular
  - Short Cycle
  - Ability to Change Connections
  - Low Path Resistance
  - RF Compatible
  - Supports a Common Board
- **The MST Fit this Scenario**

MST™- Common Board Approach

- Common Board Designed with Resources Required to Support Multiple Devices (similar to a PIB)
- Each New Device/MST then Selects the Appropriate Resource
- The Board Design/FAB is no longer the Gating Cycle Item and a Common Board also supports Device Pad/Bump Pitch Shrink

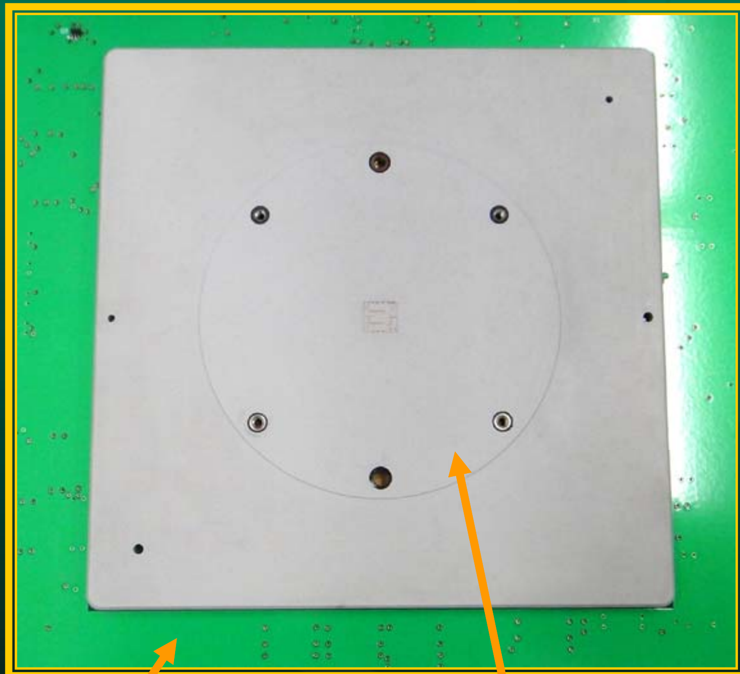




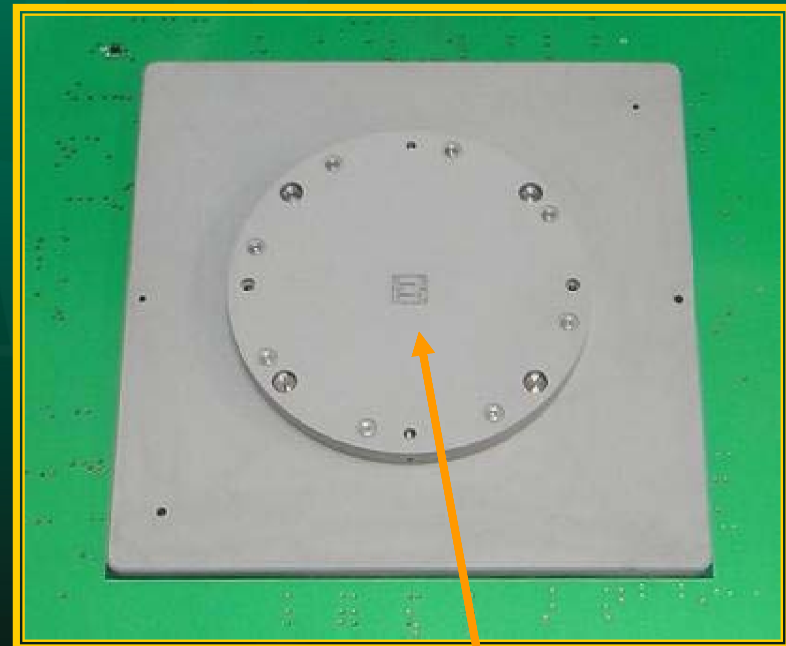
Common Board with Common Keep Out & 1,800 LGA Pattern

MST™ & Probe Head

MST Attached to Board



MST with WLCSP SpringTouch™ PH



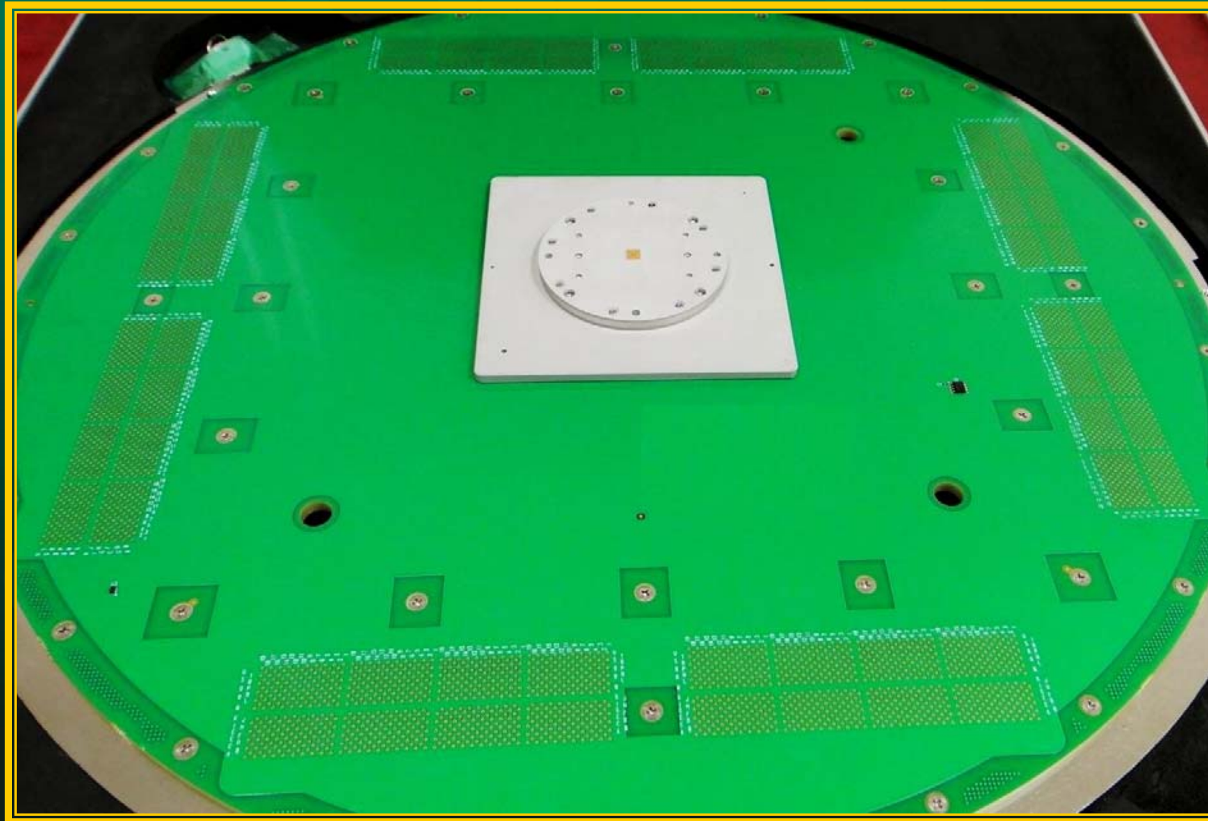
PCB

MST

Probe Head

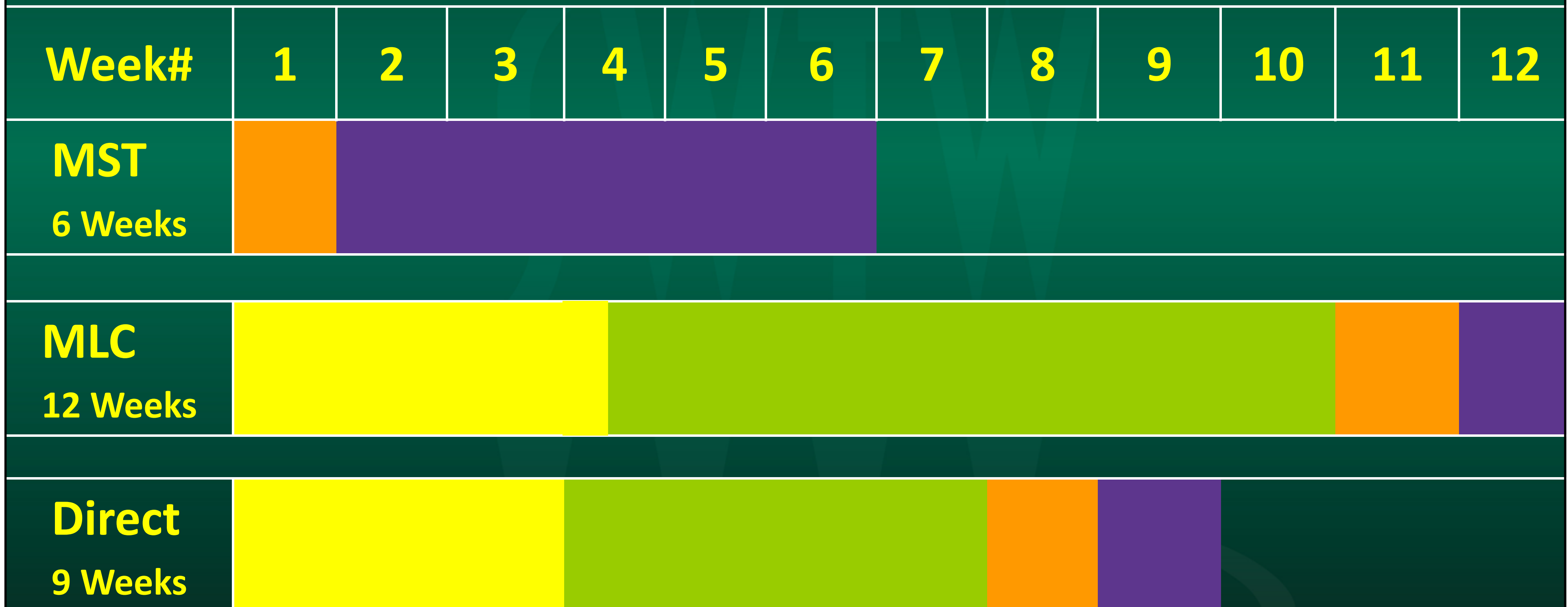
MST™ Fully Assembled Probe Card

- Simple Three Component Assembly Probe Card using Common Board



MST™ Approach
Value-added Advantages

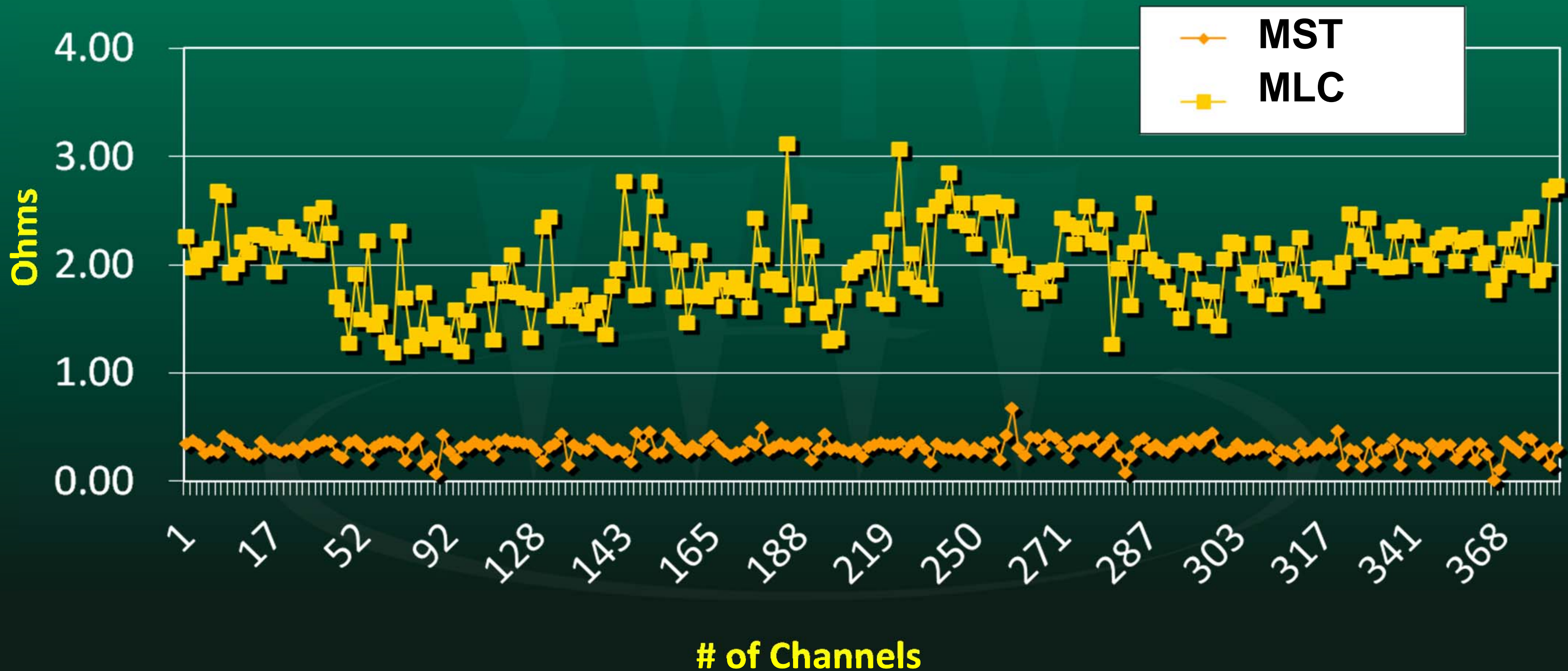
Cycle Time Advantage



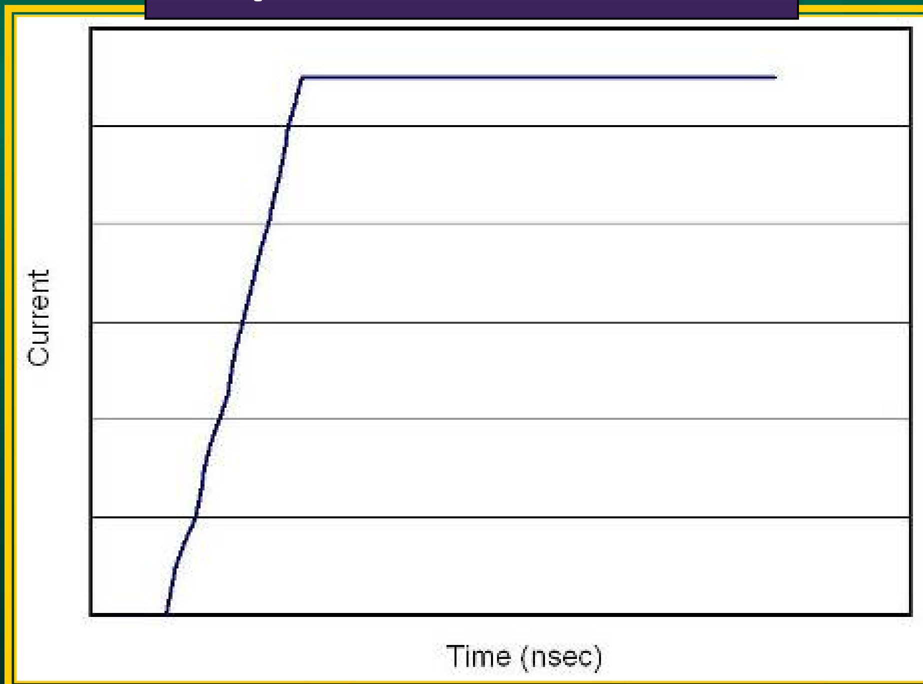
** Cycle Model based upon maximum of 500 probes using standard MST (no internal components) & common board in stock.*

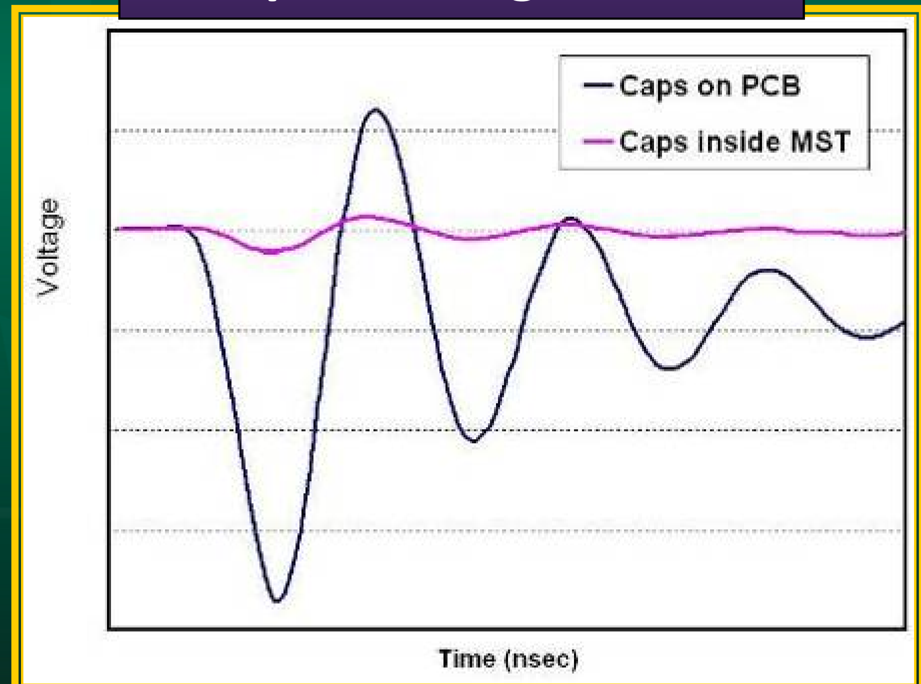
- Design (PCB & Interconnect)
- FAB (PCB & Interconnect – MLC)
- PCB BOM Assembly
- Probe Hardware AFB, Assembly, Test

Path Resistance Advantage



Internal Component Advantage

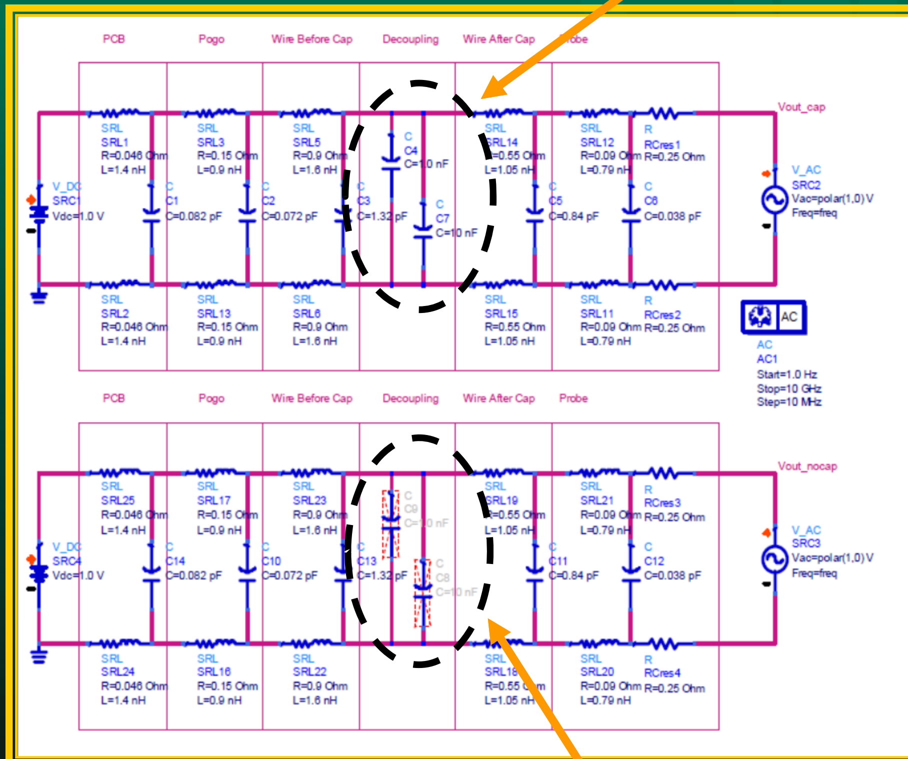


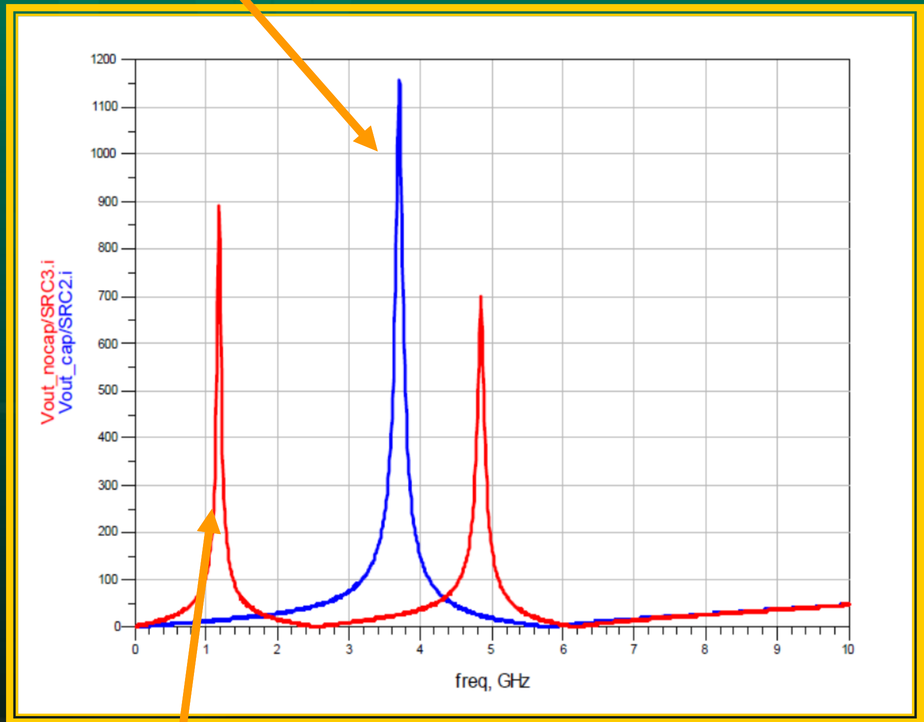


- **Housing Components within the Modular ST has Several Advantages:**
  - Minimal Voltage Drop & More Stable Supply Voltage
  - Less Noise Coupling to the Supply Lines
  - Voltage Output that is Clean & Stable (*Right*)
  - Resulting in a More Robust Testing & Lower Probe Card COO

Internal Component Advantage

With caps installed 500 mils from MST probe contact pad.

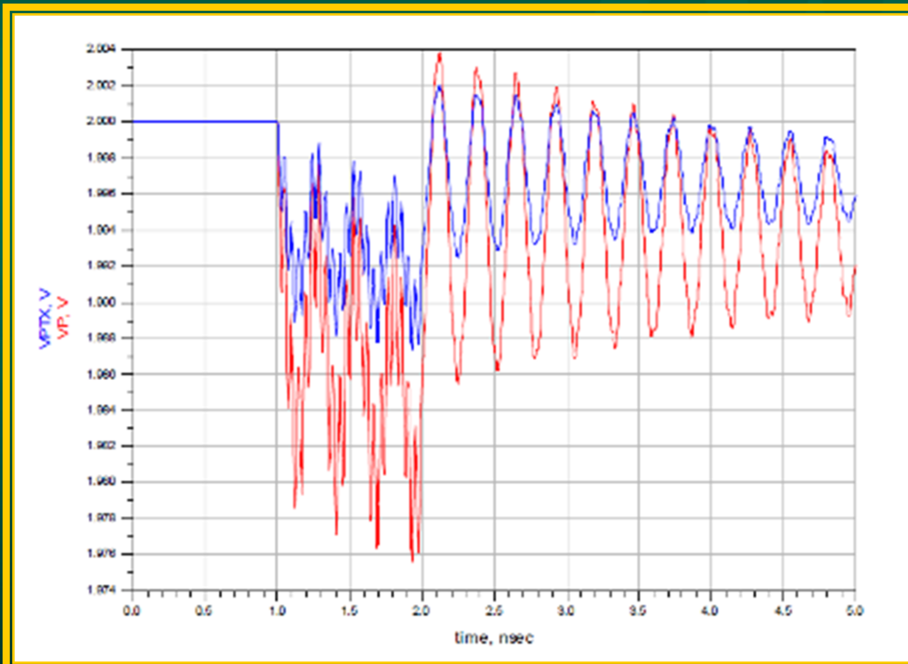




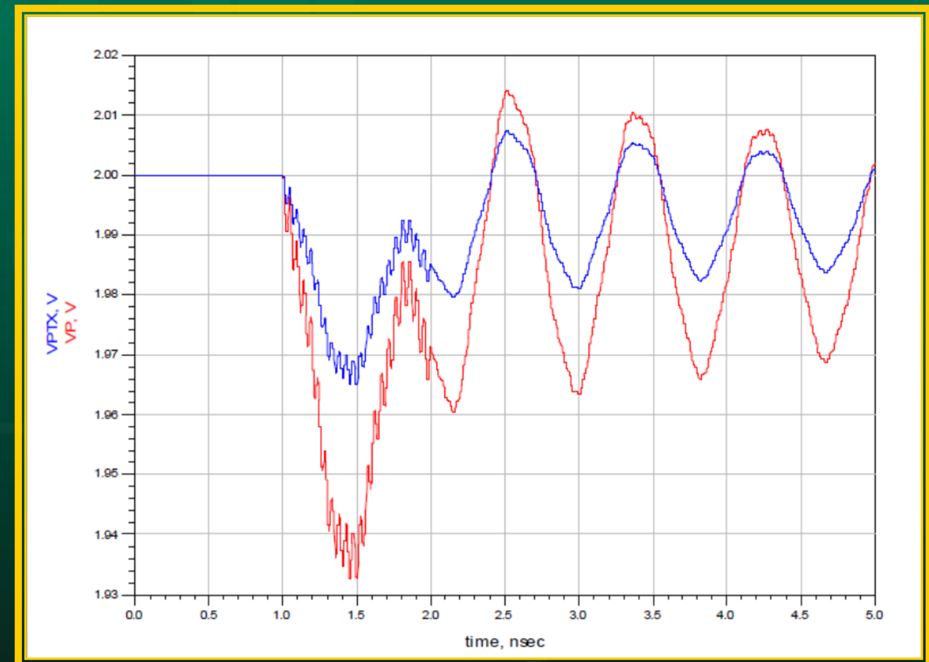
MST with caps only on PCB

In this example, being able to locate decoupling closer to DUT drives 1st resonant frequency from 1.2 GHz to 3.6 GHz.

Internal Component Advantage

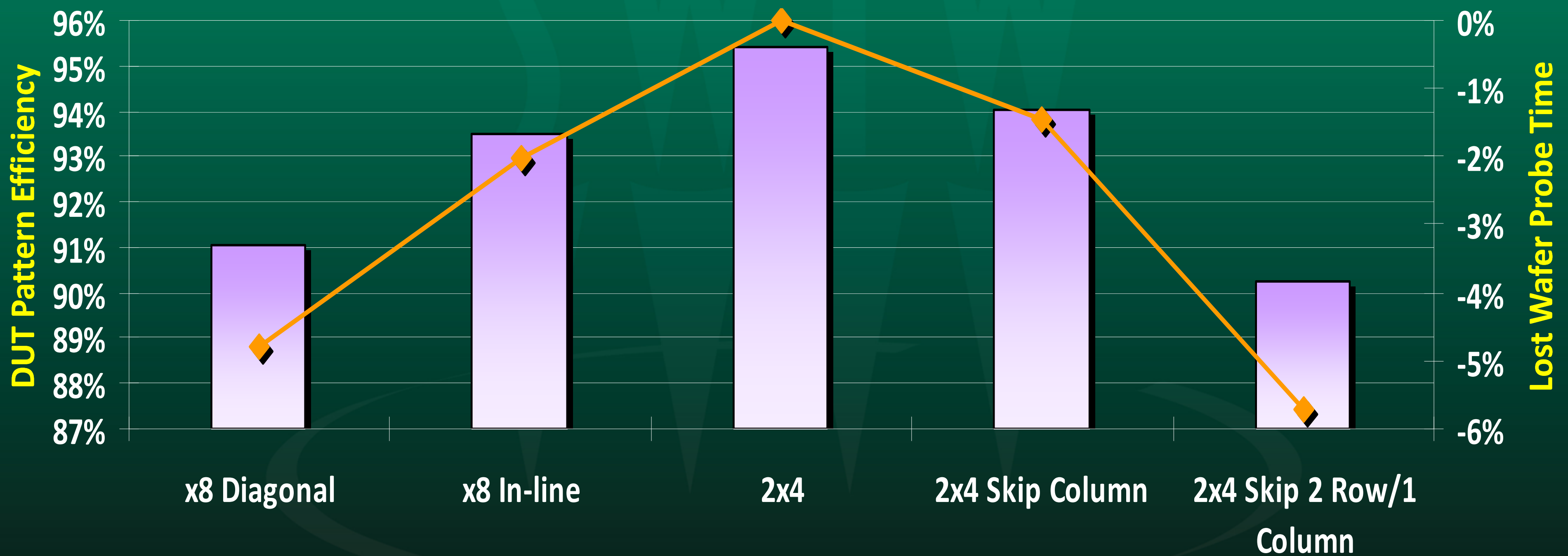


With Caps Inside MST



Caps on PCB Only

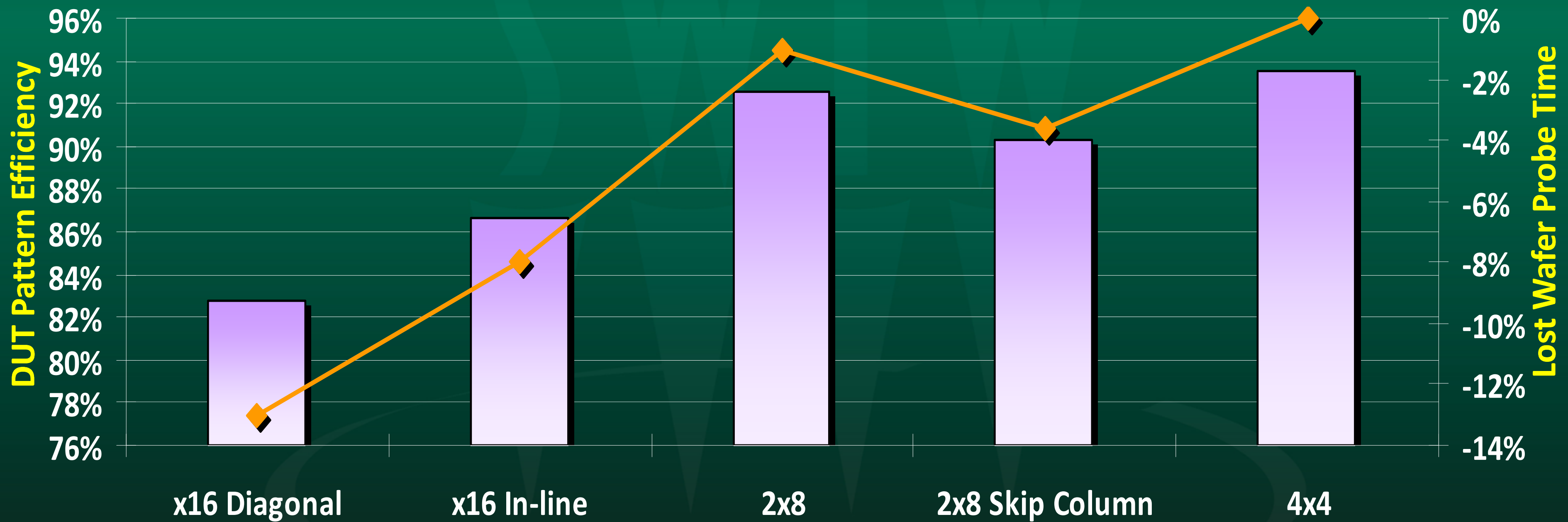
Step Efficiency Advantage



Test Details

- 200mm Wafer
- 778 Die/Wafer
- Die 6mm x 6mm

Step Efficiency Advantage



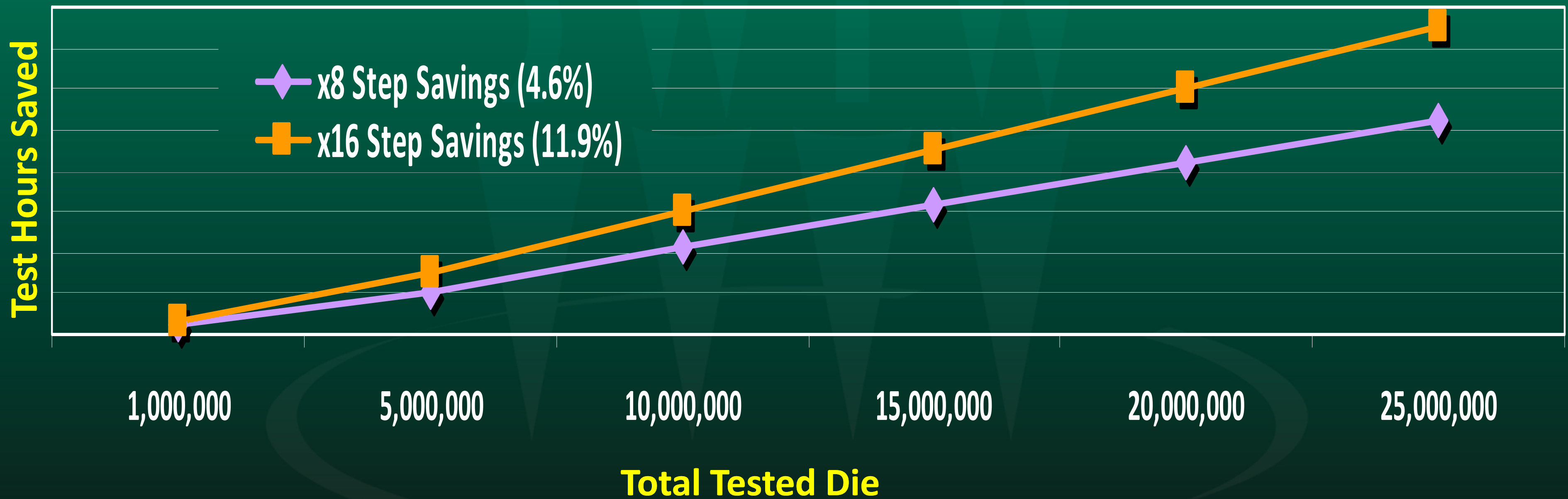
Test Details

- 200mm Wafer
- 778 Die/Wafer
- Die 6mm x 6mm

Step Efficiency Advantage

ATE Time Savings Using Increased Step Efficiency (Best minus Worst)

"Translates into Reduced COO"



Test Details

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MST™ Approach

"Electrical Tests"

Standard MST ™ Electrical

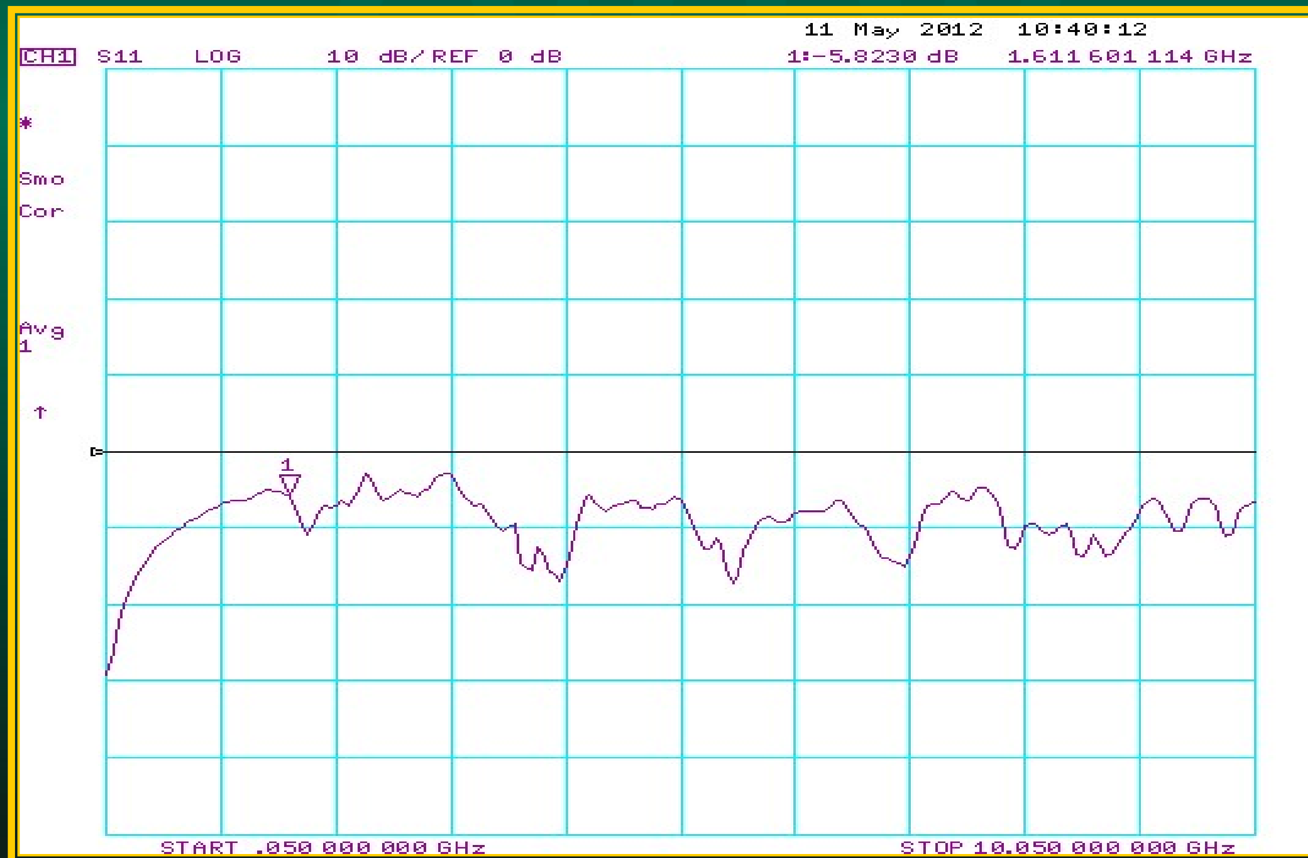
	Example of Basic* MST Interconnect (No Probe)
Impedance Max (Ω)	80
Risetime (ps)	220
-1 dB Bandwidth (GHz)	1.000
-3 dB Bandwidth (GHz)	1.850

**** Note: Optional enhanced MST includes internal components and/or routing improvements.***

Standard MST ™ Insertion Loss (S21)

- **Bandwidth: -3 dB at 1.85 GHz**

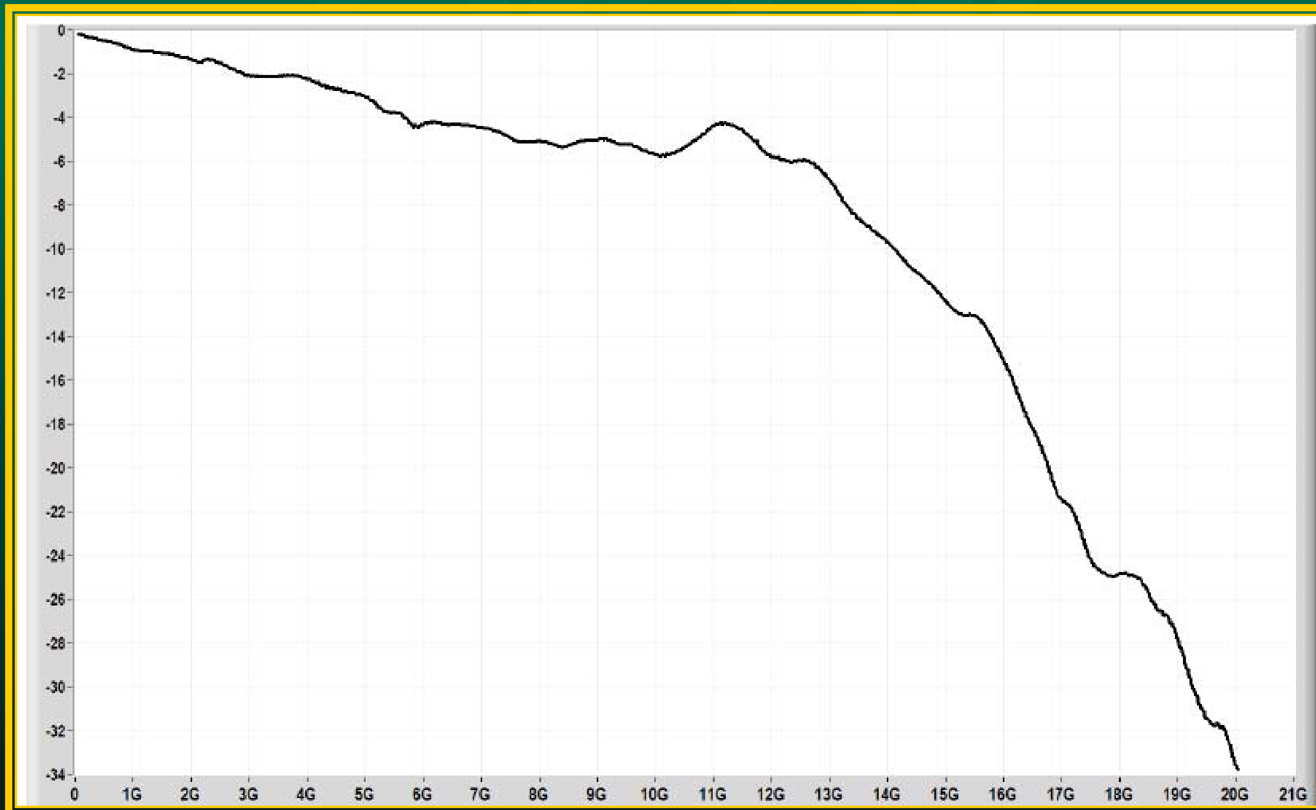
Standard MST ™ Return Loss (S11)



- **-5.8 dB loss at 1.611GHz**

Optional Enhanced MST ™ Electrical

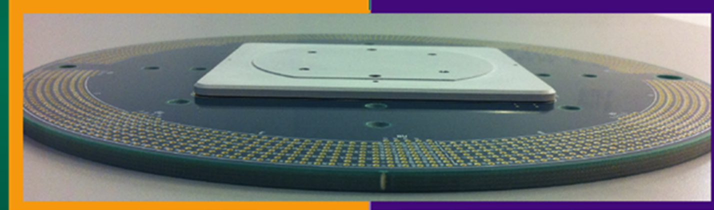
(Stand-alone, No Probe)

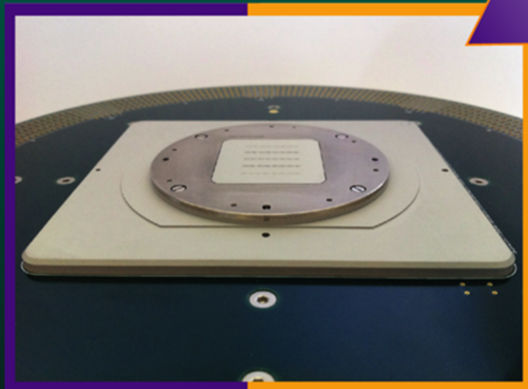


Measurement, S21: -1dB bandwidth is 1.39 GHz. -3dB bandwidth is 4.97 GHz

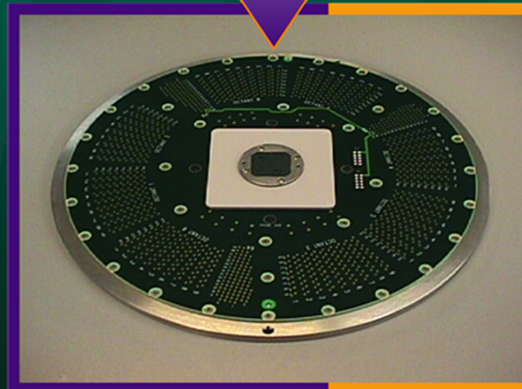
MST™ Probe Technology Range

MST™





Trio™ - Flip Chip



LogicTouch™
Fine Pitch 50μm

SpringTouch™
WLCSP

Summary

- ***By utilizing a flexible interconnect (MST) & common board, cycle times for first probe cards can be greatly reduced to meet 1st silicon.***
  - Direct attaching probe hardware to a board improves electrical test performance verses using interconnect, but most applications do not require a high level of performance.
  - Multi-DUT direct probe hardware also requires implementing a less efficient pattern (i.e. skipped row &/or column) to support board LGA fan-out, which in-turn reduces step efficiency & increases test time/cost per die.
  - Utilizing the MST interconnect is ideal for DC to mid-level RF applications, can support a common board for reduced cycle, allows for non-skipped DUT for improved step efficiency thereby reducing tester time & COO, which for HVM off-sets any added costs of the MST.

Summary

- **Future Work**
  - Completing x8 and x16 multi-DUT probe hardware for this same application *(note: x16 probe solution is already in production for other applications).*
  - Next generation MST enhancing RF performance & reduced cycle time.

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