High Frequency Performance of Modular Wafer Probecards – A Numerical Approach

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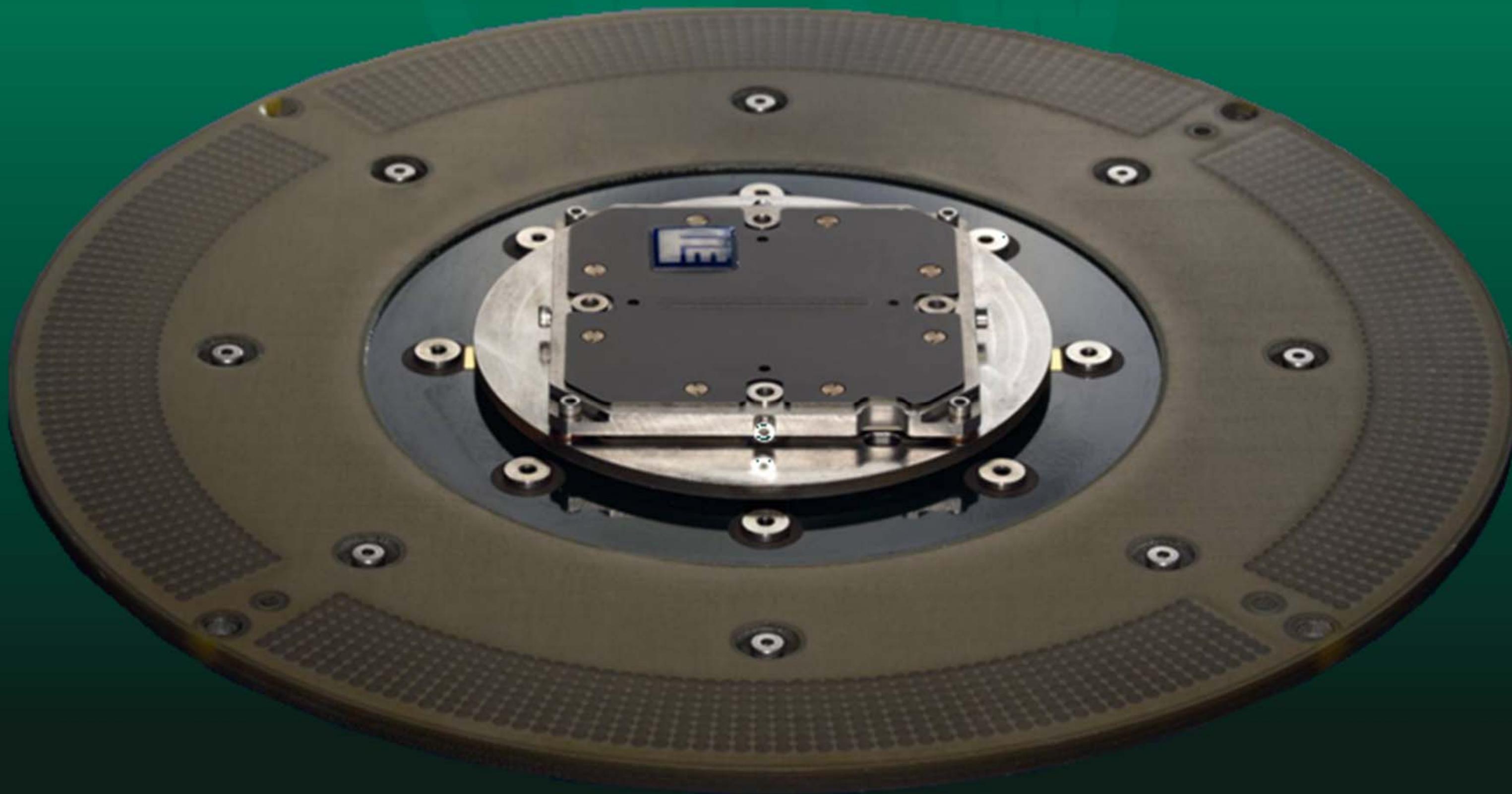
Overview

- Technology Overview
- Motivation for this Work
- Simulation Overview
- Performance & Optimization
- Conclusion

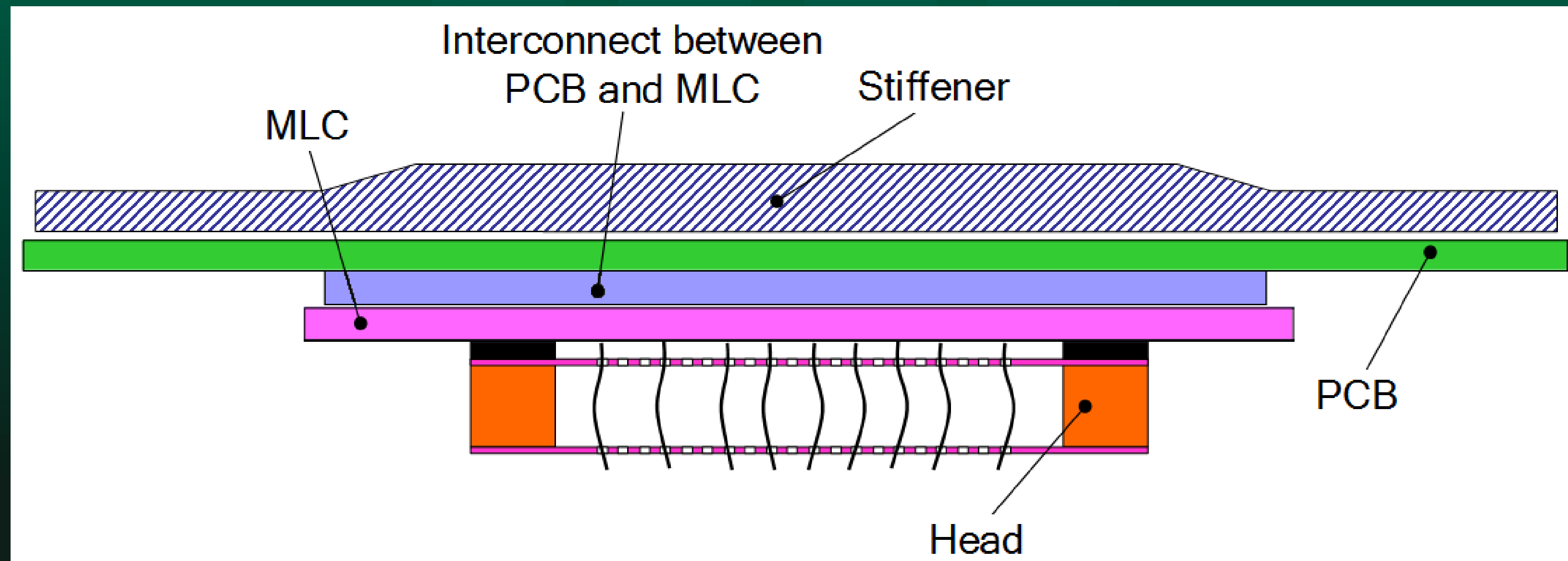
Technology Overview – S22

- Probe Card with MLC Space Transformer



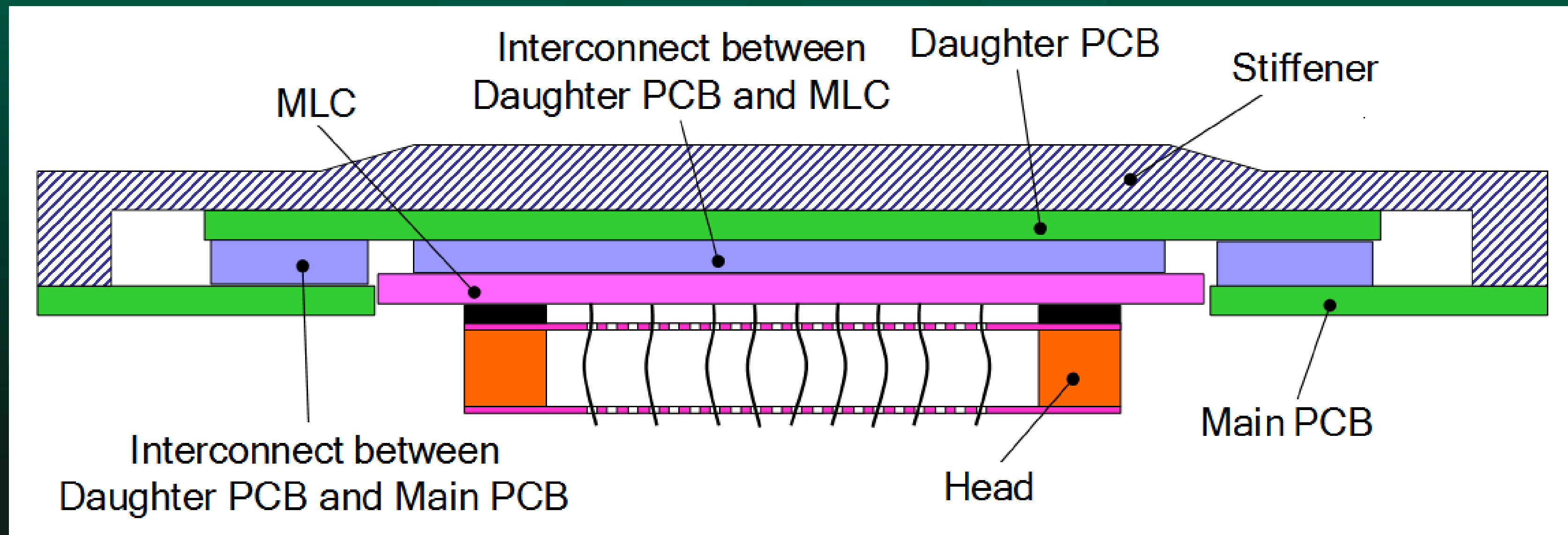
Technology Overview – S22

- **Principle Drawing**
  - Active area: 40mm x 40mm
  - Minimum pitch: 59µm
  - Maximum pin count: 5,000



Technology Overview – S23

- **Principle Drawing**
  - Same Head as S22: 59µm Pitch; 5,000 Pin Maximum
  - Adjustable Probe Tip Depth
  - Split in 2 PCBs – Main PCB and Daughter PCB



Technology Overview – S22 vs S23

- **Why S22?**
  - Standard Design – only 1 PCB necessary
  - Fewer Parts
  - Optimized Electrical Path

- **Why S23?**
  - Adjustable Probe Tip Depth
  - Modular Design Allows More Flexibility (i.e. Direct Docking)
  - Better Testability for Complex Circuits

Motivations for this Work

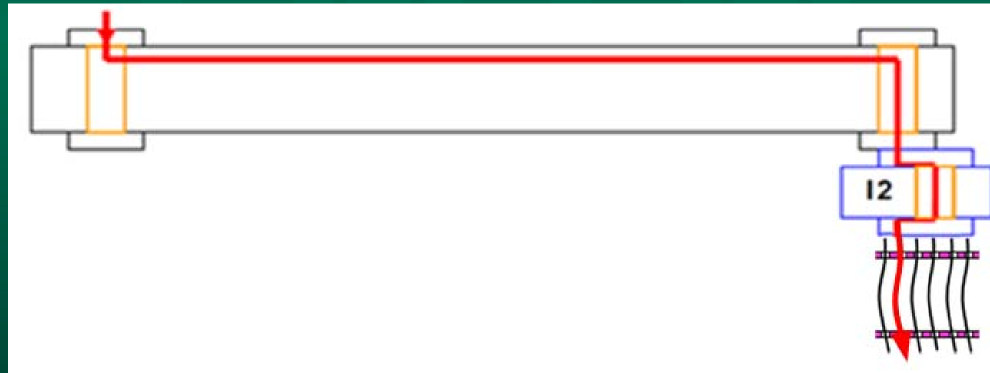
- Simulation is Required to Determine Electrical Performance for Both S22 and S23
- Simulation Confirms that S23 Performance is Suitable Despite the More Complex Electrical Path
- Performance Must be Suitable for the Following Applications:
  - Automotive e.g. MCU
  - SOC
  - …

Simulation Overview – Method

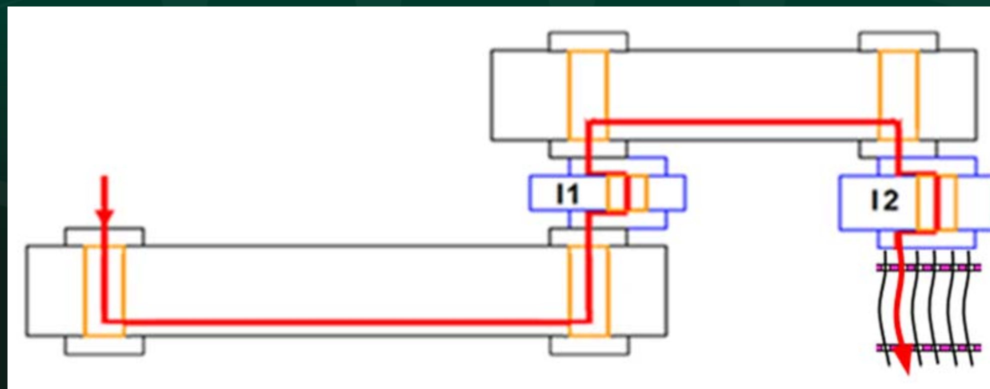
- **Simulate Entire Path from Tester to DUT**
  - Sixteen Different Signal Paths to Determine a Reasonable Range of Expected Performance
  - Complex Structures (Vias, Interconnects, Probe Head) to be Simulated with 3D Electromagnetic Solver (HFSS) to Maximize Simulation Accuracy
  - Determine Maximum Performance for Both Analog and Digital Signals
  - Compare Performance of S22 and S23

Simulation Overview – Path Description

- **S22: Tester-Main PCB-I2-Head**

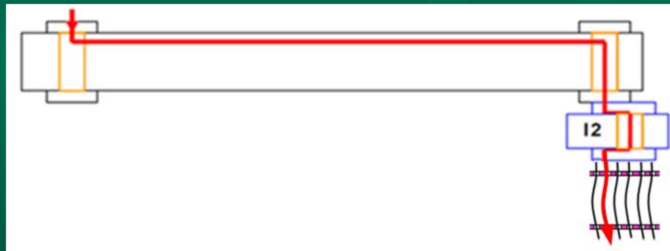


- **S23: Tester-Main PCB-I1-Daughter PCB-I2-Head**



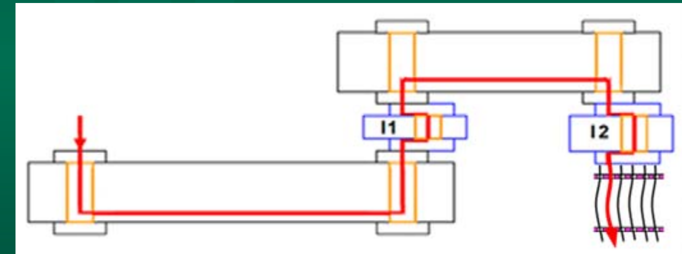
Simulation Overview – Path Description

S22



- Tester Via
- PCB Trace
- DUT Via
- I2 Interconnect
- Probe Head

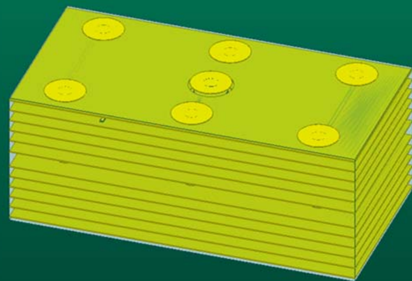
S23



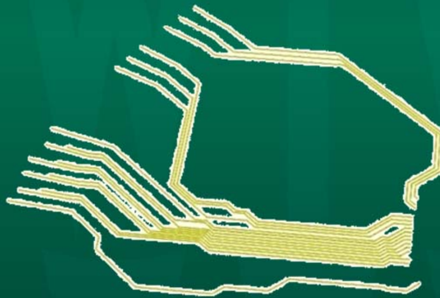
- Tester Via
- PCB Traces
- Intermediate Via #1
- I1 Interconnect
- Intermediate Via #2
- DUT Via
- I2 Interconnect
- Probe Head

Simulation Overview – Path Description

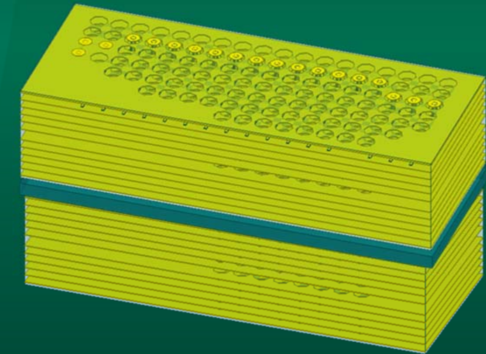
- **Simulation Models**



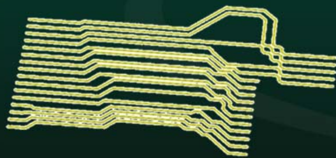
#1 Tester Via



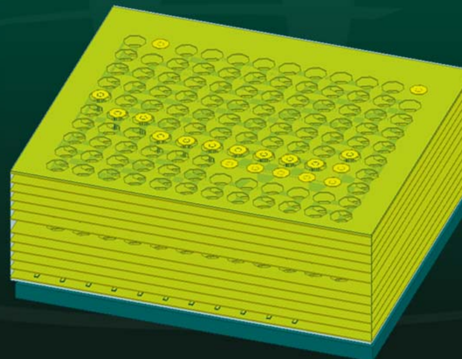
#2 Main PCB



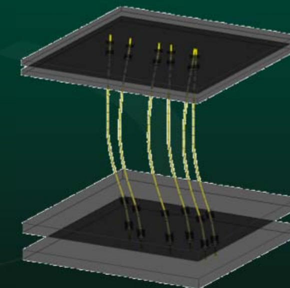
#3 Via – Interconnect – Via



#4 Daughter PCB



#5 Via – Interconnect

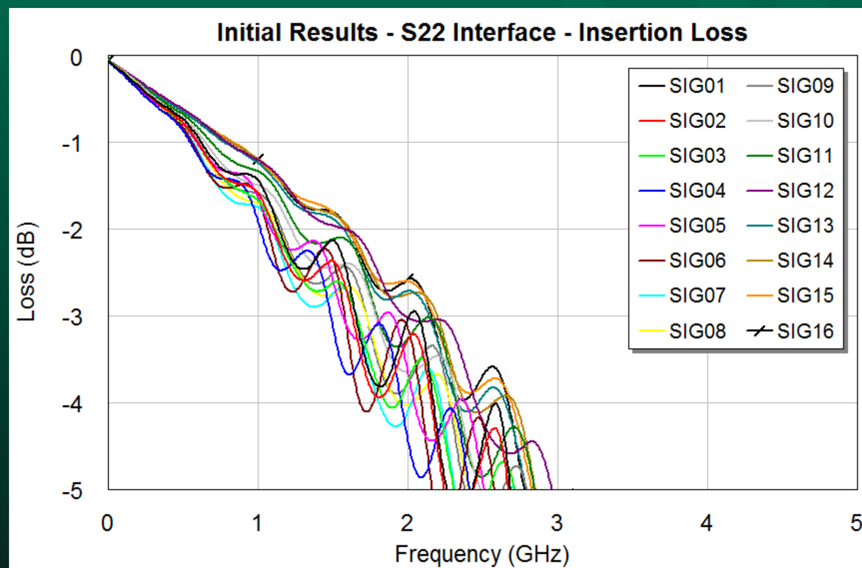


#6 Probe Head

Performance – Insertion Loss

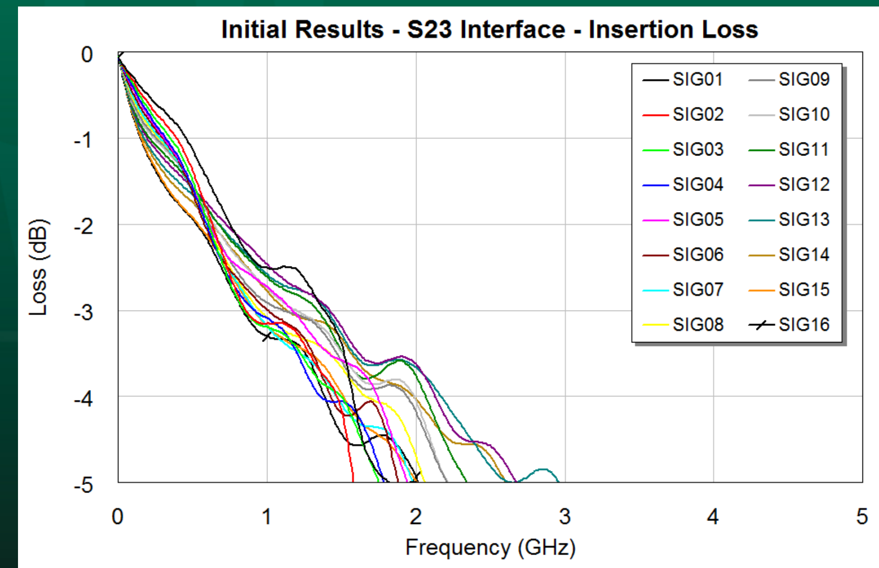
Interface without Probe Head – Initial Results

S22



	-3dB Bandwidth	
S22 Initial Performance	MIN	MAX
	1.5 GHz	2.2 GHz

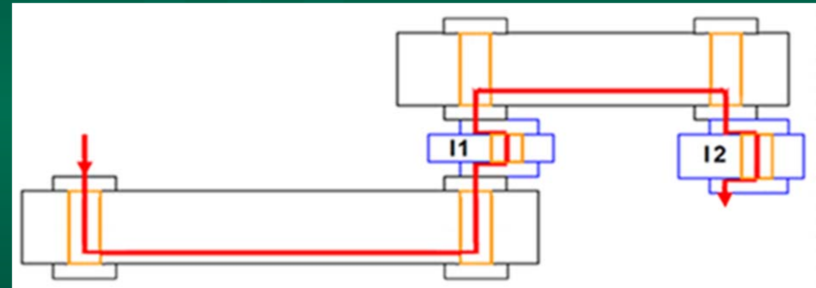
S23

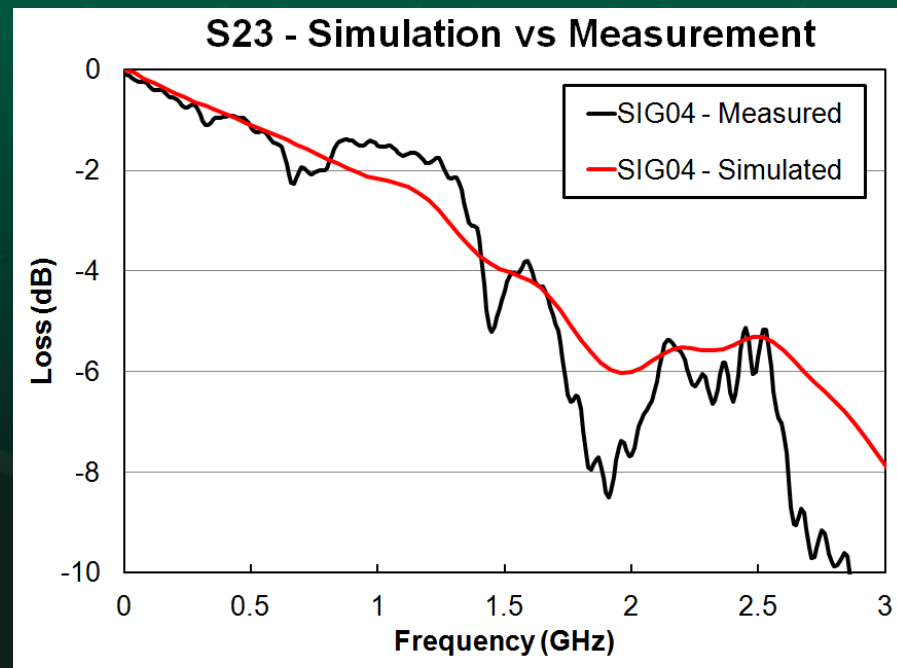


	-3dB Bandwidth	
S23 Initial Performance	MIN	MAX
	0.8 GHz	1.4 GHz

Measurement Correlation – S23

- **Path**
  - S23 Without Probe Head
  - No Stub Drill

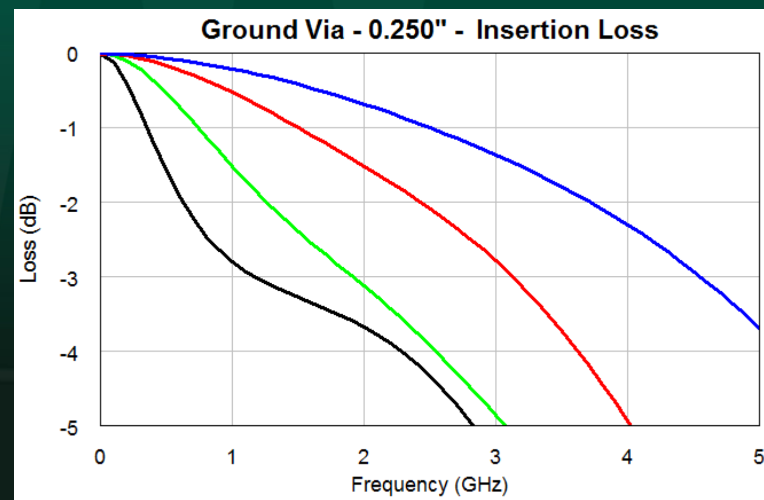




Performance – Ground Via Proximity

- The Variations in Bandwidth are Caused by the Distance of each Signal Via to the Nearest Ground Via
- Placing Ground Vias Close to each Critical Signal Via Significantly Improves Performance
- Critical for All Signals > 100 MHz
- Example:
  - 0.250” PCB
  - 0.187” Via Length

Via Distance = 1mm
Via Distance = 2mm
Via Distance = 4mm
Via Distance = 8mm



Performance – Optimization

- **Design is Optimized by Reviewing and Potentially Modifying the Following:**

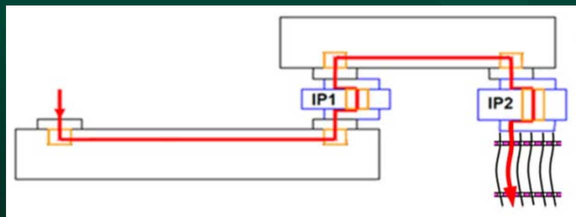
#1 – Signal Via Stubs

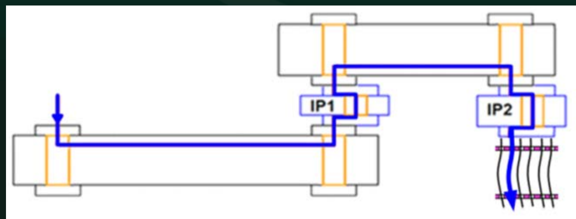
#2 – Signal Layer Locations

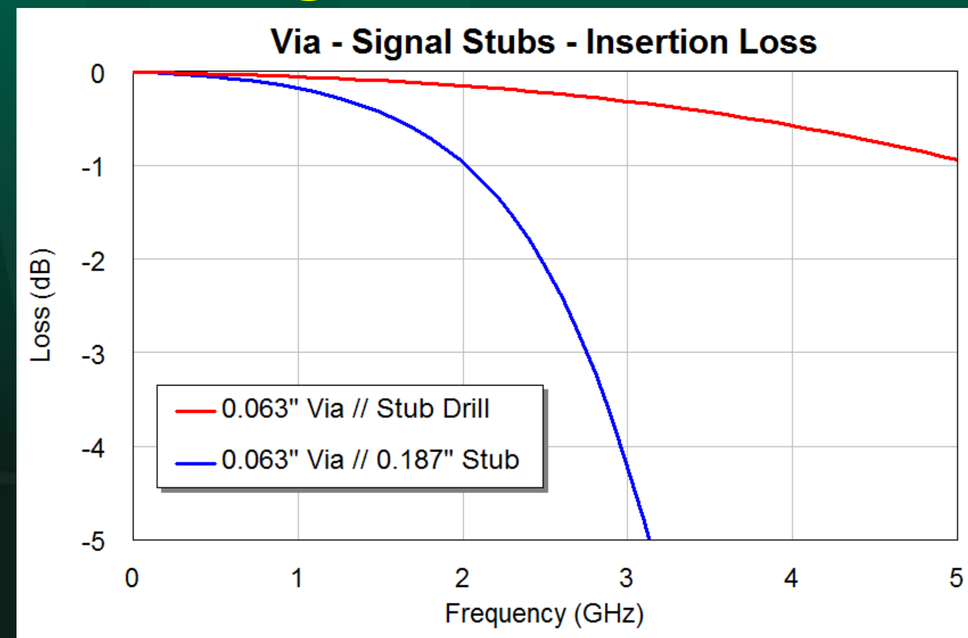
#3 – PCB Material

Optimization #1 – Signal Via Stubs

- The Stub is the Unnecessary Part of the Via Beyond the Trace and it Causes Reflections
- Drilling Removes the Stub
- Should be Considered for Signals > 1 GHz
- Ex: 0.250” PCB

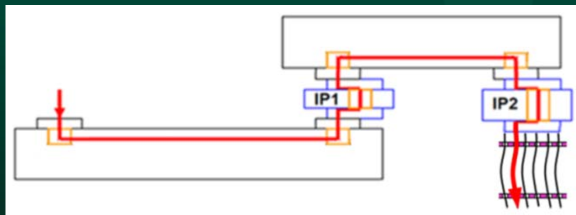


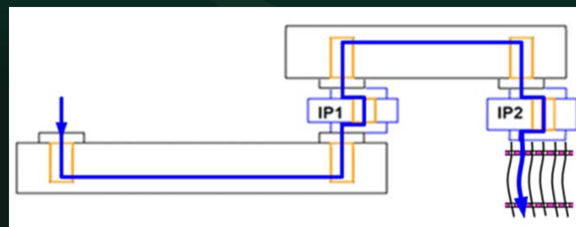


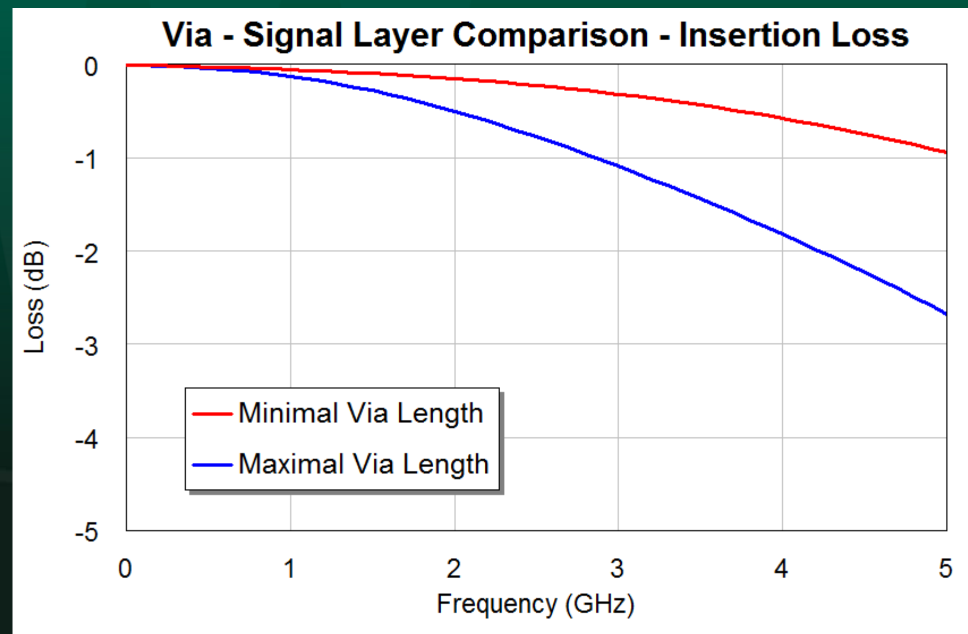


Optimization #2 – Signal Layer Locations

- Selecting Signal Layers that Minimize the Length of the Signal Via can Improve Performance
- Should be Considered for Signals > 1 GHz
- Ex: 0.250” PCB

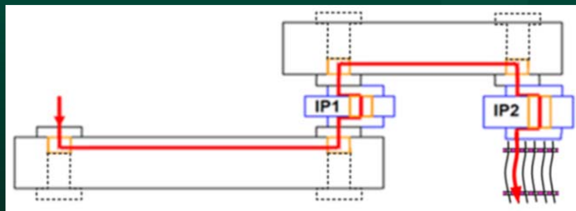


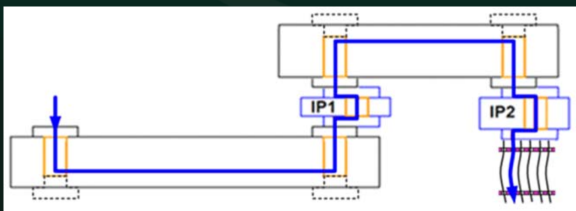


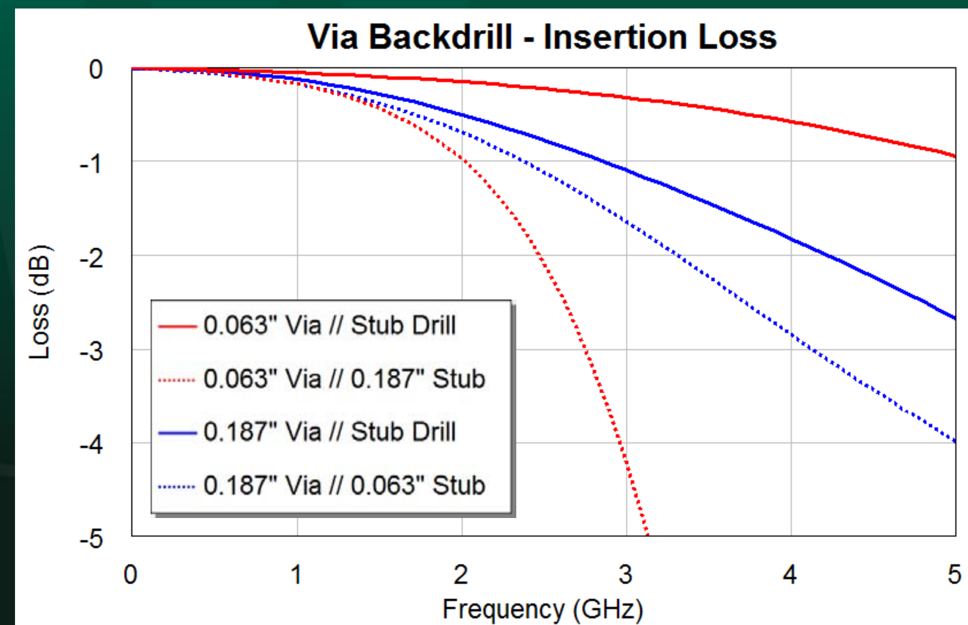


Optimization – Signal Layer and Via Stubs

- **Relationship between Signal Layer and Stub Length:**
  - Without Stub Drill, the Layer Furthest from Entry is Best
  - With Stub Drill, the Layer Closest to Entry is Best
- **Ex: 0.250" PCB**

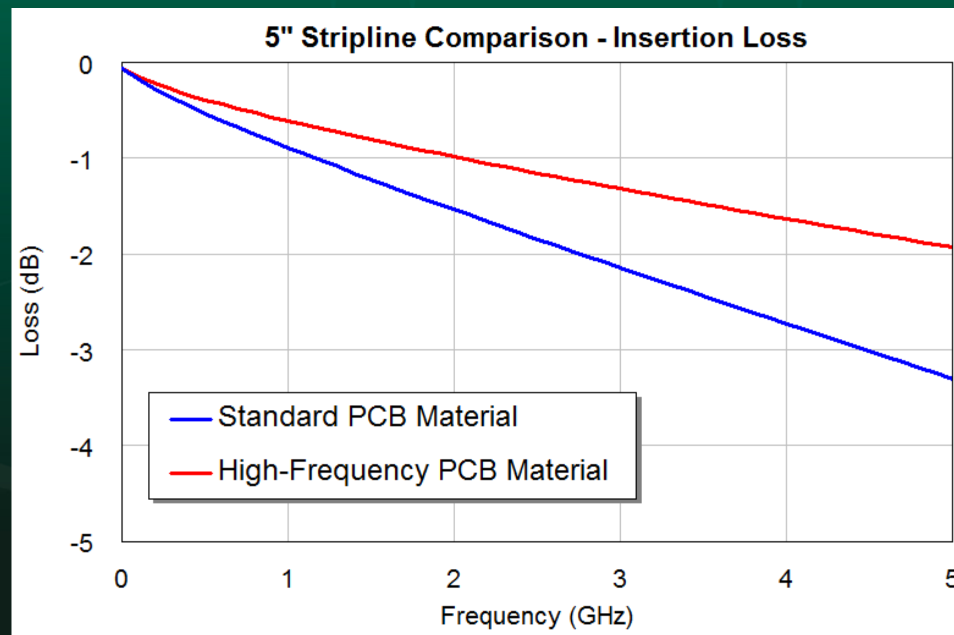






Optimization #3 – PCB Material

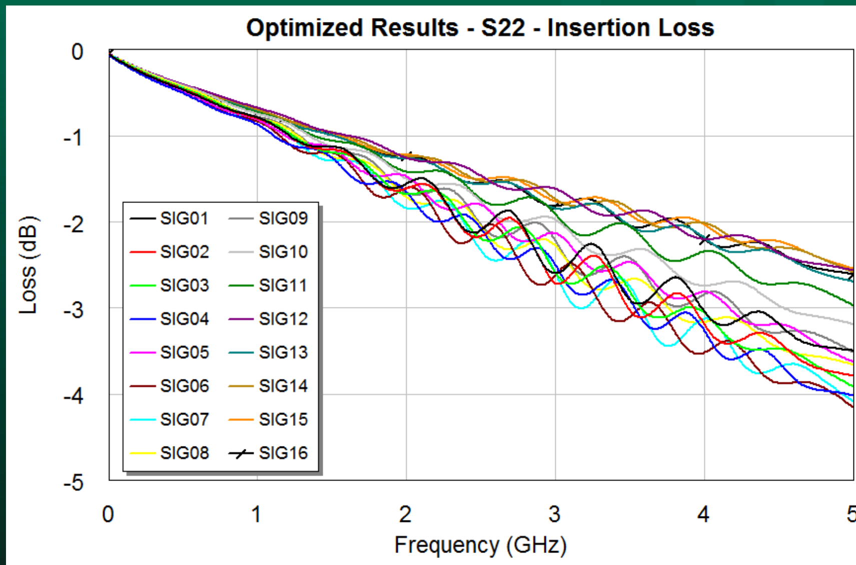
- Selecting a High-Frequency PCB Material can also Improve Performance
- Should be Considered for Signals > 1 GHz

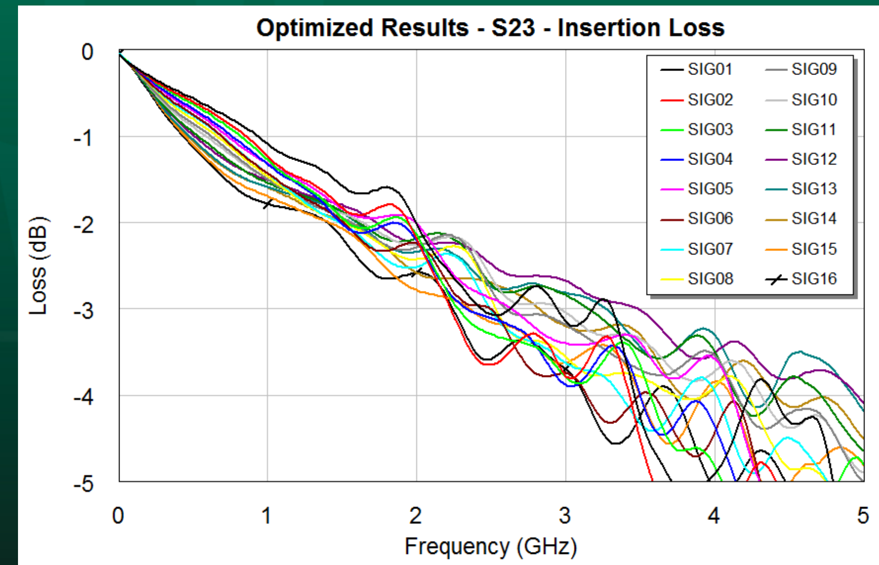


Performance – Optimization

Interface without Probe Head – Optimized Results

S22 **S23**



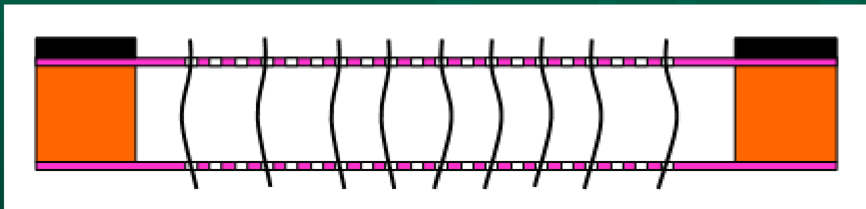


S22 Performance	-3dB Bandwidth	
	MIN	MAX
Initial	1.5 GHz	2.2 GHz
Optimized	**3.2 GHz**	**5.6 GHz**

S23 Performance	-3dB Bandwidth	
	MIN	MAX
Initial	0.8 GHz	1.4 GHz
Optimized	**2.2 GHz**	**3.5 GHz**

Performance – Adding Probe Head

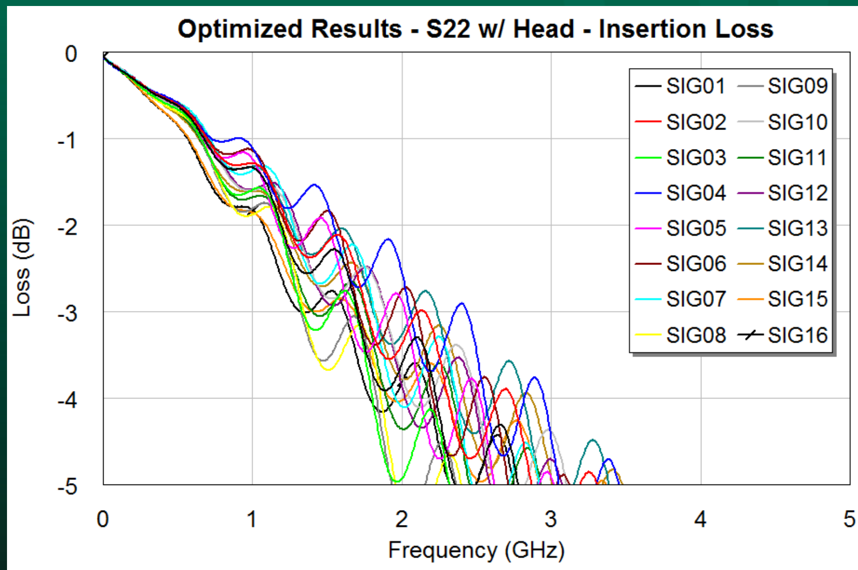
- Feinmetall Viprobe® Head
- Buckling Beam with Guiding Plates



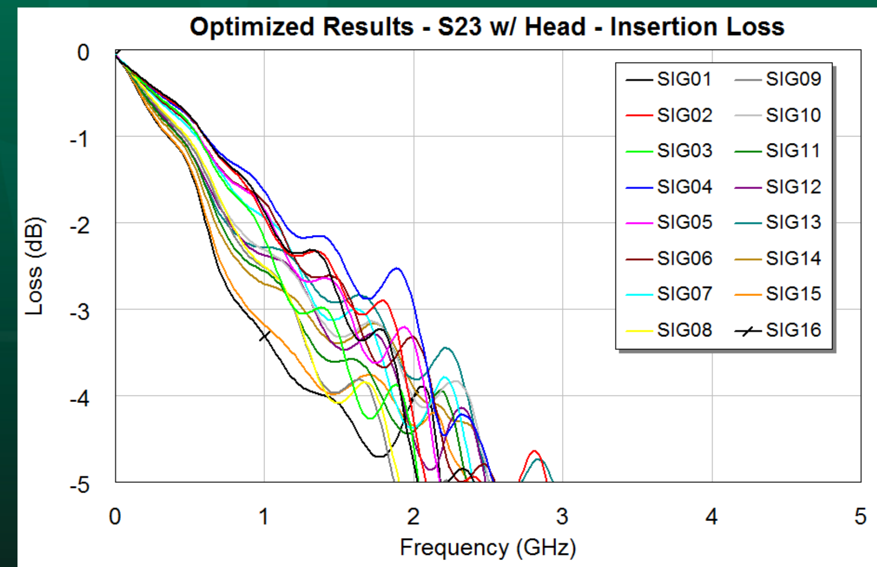
Performance – Adding Probe Head

Interface with Probe Head – Optimized Results

S22



S23



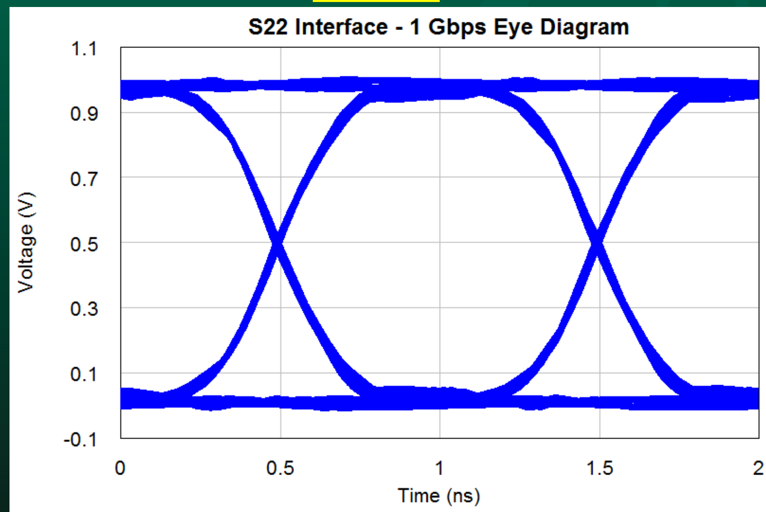
S22 Performance	-3dB Bandwidth	
	MIN	MAX
w/o Probe Head	3.2 GHz	5.6 GHz
w/ Probe Head	1.3 GHz	2.1 GHz

S23 Performance	-3dB Bandwidth	
	MIN	MAX
w/o Probe Head	2.2 GHz	3.5 GHz
w/ Probe Head	0.9 GHz	2.0 GHz

Performance – 1 Gbps Eye Diagram

- Optimized Interface with Probe Head
- Results Reflect Worst Case Signals

S22



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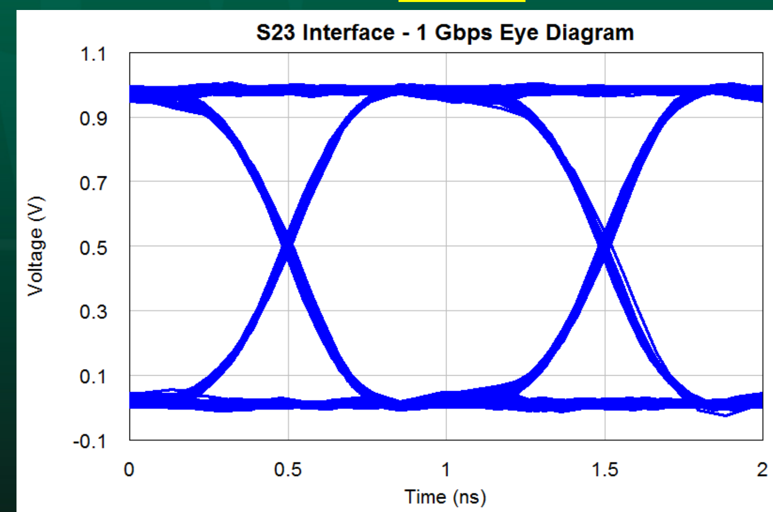
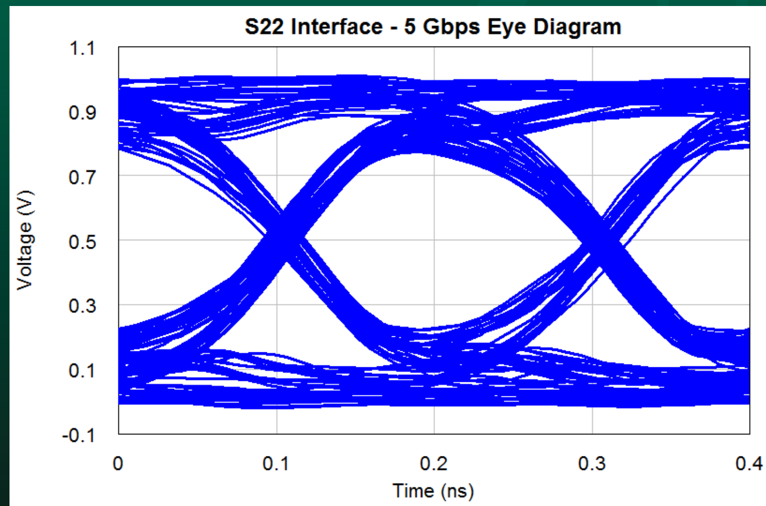


- Interface can Easily Pass 1 Gbps Signals

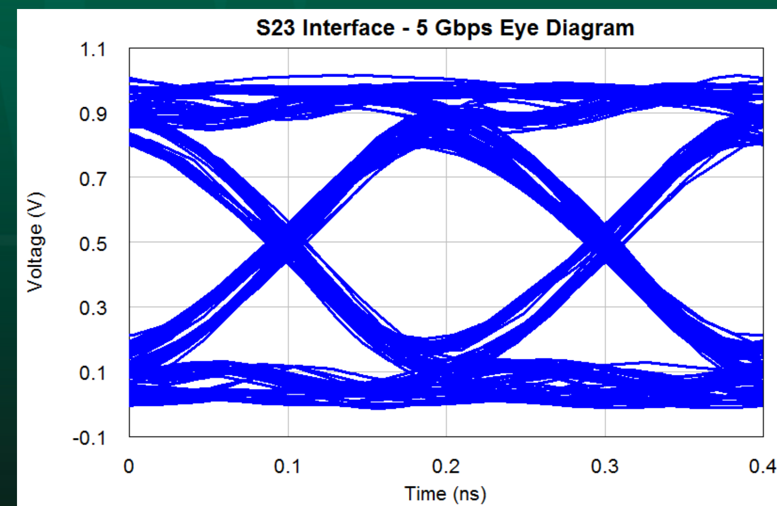
Performance – 5 Gbps Eye Diagram

- Optimized Interface with Probe Head
- Results Reflect Worst Case Signals

S22



S23



- Interface can Pass Most 5 Gbps signals

Performance Overview

- **Performance Varies Based on Level of Optimization and Configuration (S22/S23)**
- **Each Application has Different Requirements**
- **A Single Specification Cannot Describe all Configurations**
- **Approximations for Optimized Configurations:**
  - Analog: -3 dB Bandwidth Around 2 GHz
  - Digital: 5 Gbps Maximum Data Rate

Conclusion

- Results show that both the S22 and S23 Designs are Adequate for Passing Frequencies into the GigaHertz
- Simulation can be Used to Improve the Performance of the Interface
- Further Investigation Will Include Modeling the MLC