IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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Full wafer probe cards for mixed signal products

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Motivation and history

From theory to practice

Feinmetall D32 full wafer probe card

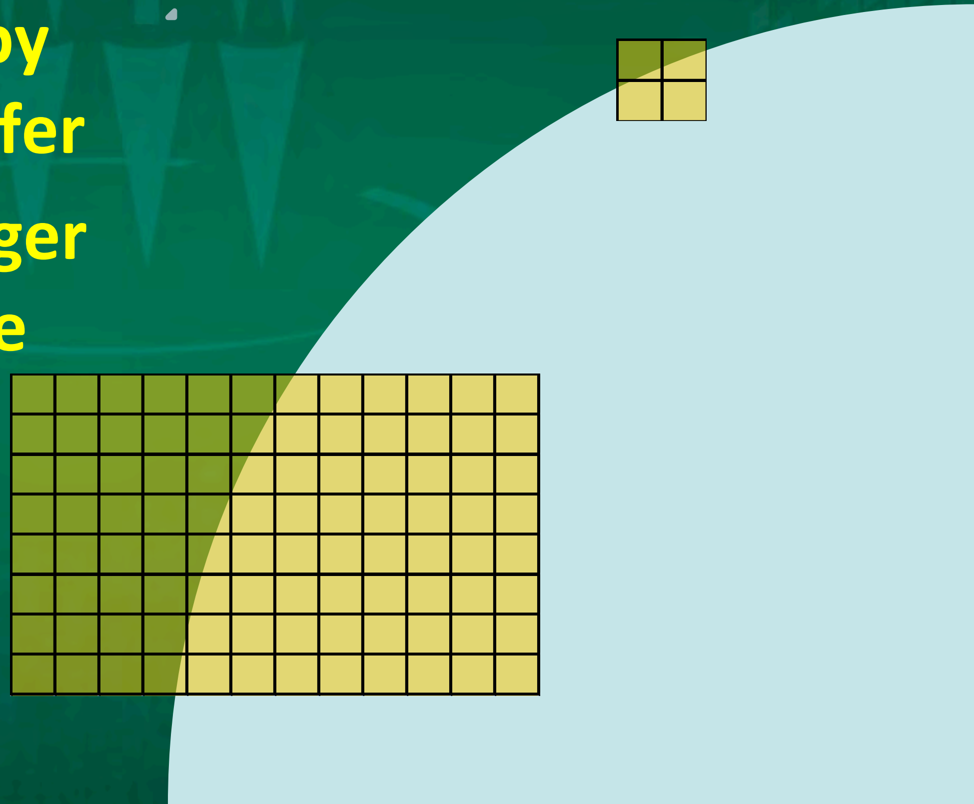
NXP operational first data

Summary and future step

Motivation

- With multi site probe cards there is efficiency loss by probing outside the wafer
- The loss grows with larger dies and larger multisite count

- How do we increase efficiency?

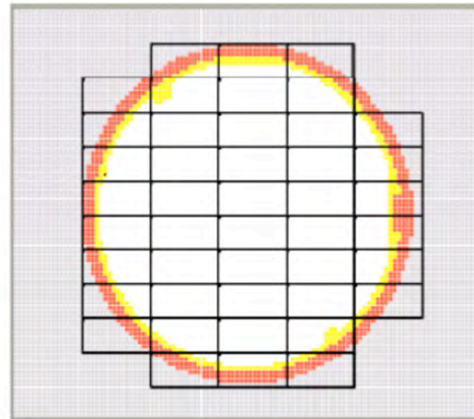


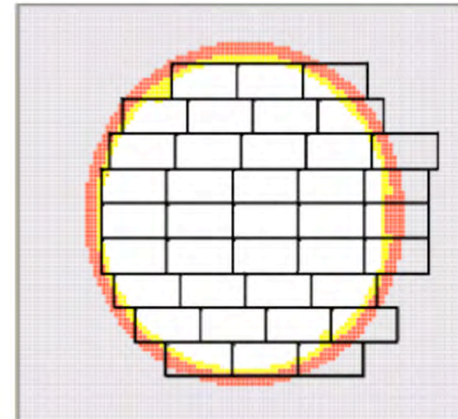
SWTW

SWTW History I – Optimal stepping pattern

http://www.swtest.org/swtw_library/2011proc/PDF/S07_01_Fredriksen_SWTW2011.pdf

MINIMIZE TOUCHDOWNS





Prober: 44 Tochdowns → MSO: 38 Touchdowns

Technology: automatic column / row shift

= 14,6 % TD reduction!

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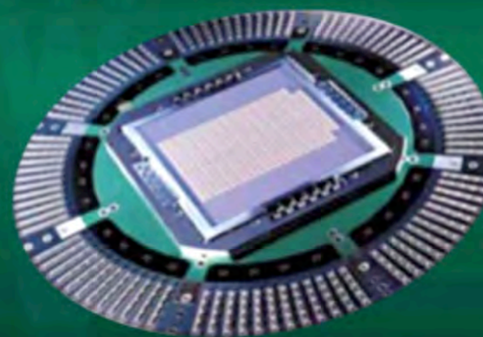
SWTW History II – Optimal array layout

http://www.swtest.org/swtw_library/2012proc/PDF/S01_01_Breinlinger_SWTW2012.pdf

When does it make sense to use a Full Wafer Contactor??

Probe Head

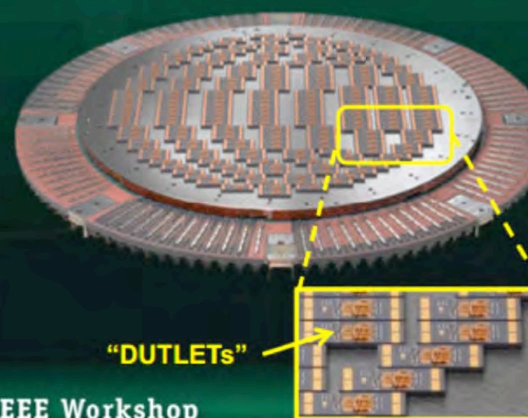
- Multiple sizes from 50mm to 150mm.
- Depending on the die can do:
  - Brick wall (no gaps between tested die)
  - Skip R or C (a 1 die gap in one direction)
  - Skip R & C (a 1 die gap in both directions)



Full Wafer Contactor (FWC)

- Touches the entire wafer at once (200mm or 300mm)
- DUTlet based system uses the same routing on all sites
- Initial cost is higher than PH, but ROI is worth it when parallelism is high enough.

But when is the parallelism high enough??



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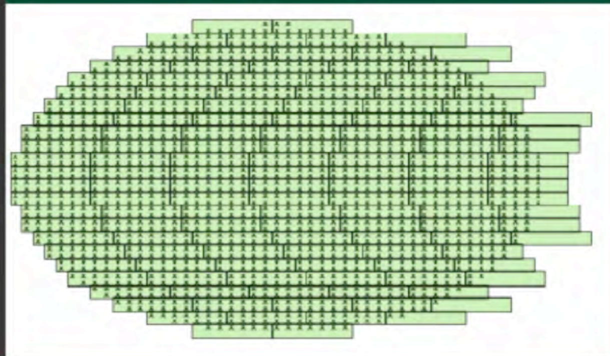
SWTW History III – „Ghosting“

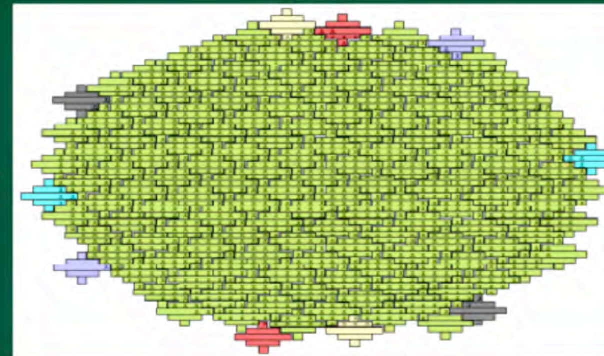
http://www.swtest.org/swtw_library/2011proc/PDF/S09_01_Avidar_SWTW2011.pdf

Ghosting Concept

2nd example – 8% TD reduction (2010)
Ghosting layout is based on known partial dies

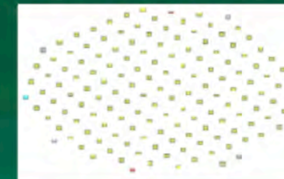


14TD FWA solution



13TD FWA/ghosting solution

PC layout



PC layout

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Increasing efficiency

1) Identify the optimal stepping pattern for a given probe card array →2011 Fredriksen et al
2) Identify the optimal multi site array layout for a given die size, do I need a full wafer probe card?
   → 2012 Breinlinger et al
3) Identify probe card sites which can share tester resources, called „Ghosting“
   → 2011 Avidar et al

Now we use these ideas!

Motivation and history

From theory to practice

Feinmetall D32 full wafer probe card

NXP operational first data

Summary and future step

From theory to practice

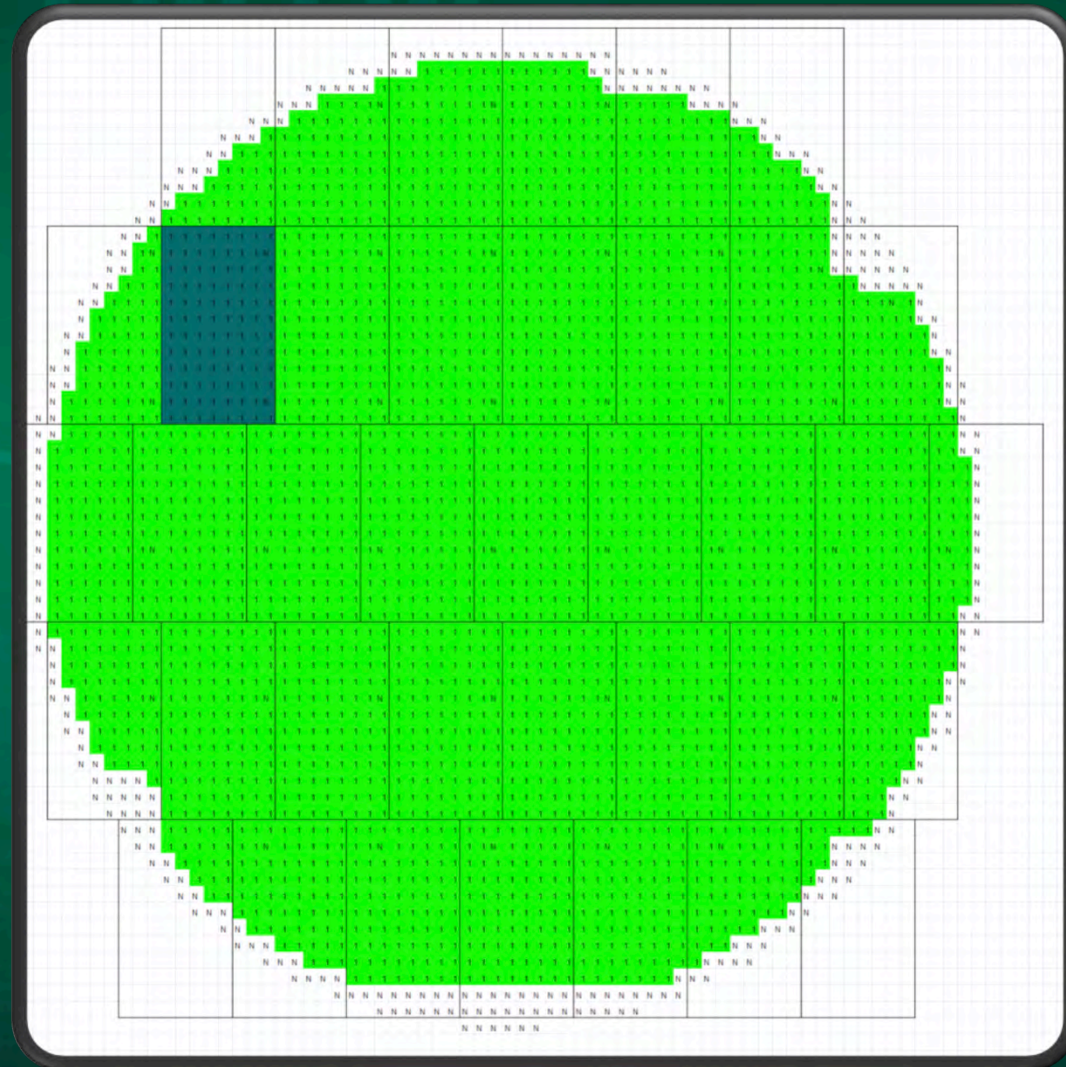
- **First time approach for a NXP full wafer probe card** (first time for SOC manufacturer???)
- **What challenges do we face in production?**
  - FPC manufacturing
  - FPC maintenance
  - Wafer test probing process, cleaning, alignment, etc.
- **What additional costs are generated in the real process; is there enough saving?**

Case study

- Potential Good Dies per Wafer: 2841
- Needs 38 TDs with 96x solid array probe card
- Needs 32 TDs with 96x full wafer probe card incl. 4 ghosting sites
- Potential saving 16% test time reduction

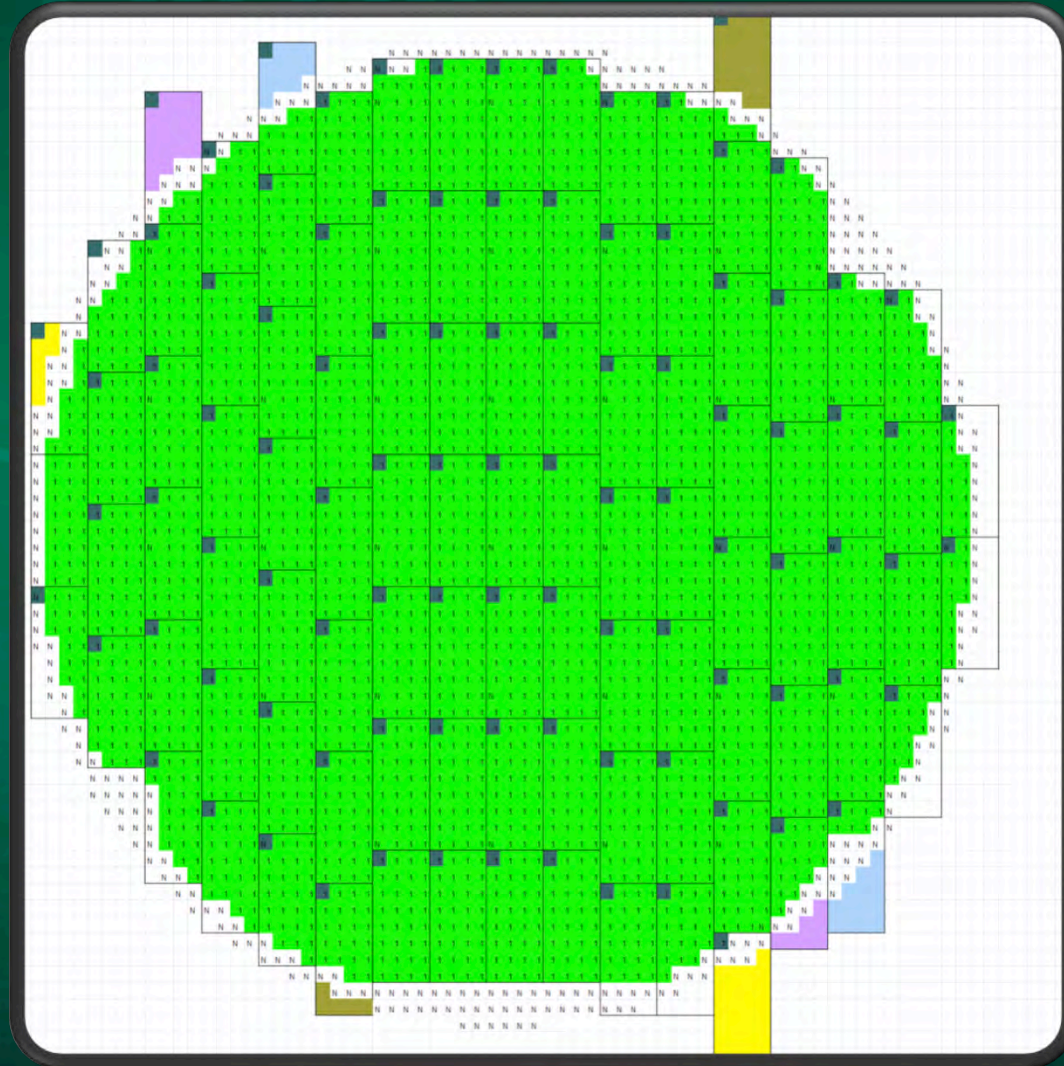
Solid Array probe layout

- 38TDs
- 96x
- 8x12 dies
- Solid array
- 78% eff.



Full Wafer Array probe layout

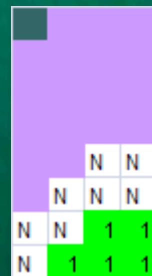
- 32TDs
- Full array
- 100x probing
- 96x resources
- 4x shared res.
- 92.5% eff.



Ghosting / Shared resources

- One set of channels/resources in the tester is split into two sets of channels/probes on the probe card
- Both sets are located at the wafer egde
- While one side touches active silicon the other probes are without contact beside the wafer edge
- Site A Site B Combination

+



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18TDs 5TDs 23TDs

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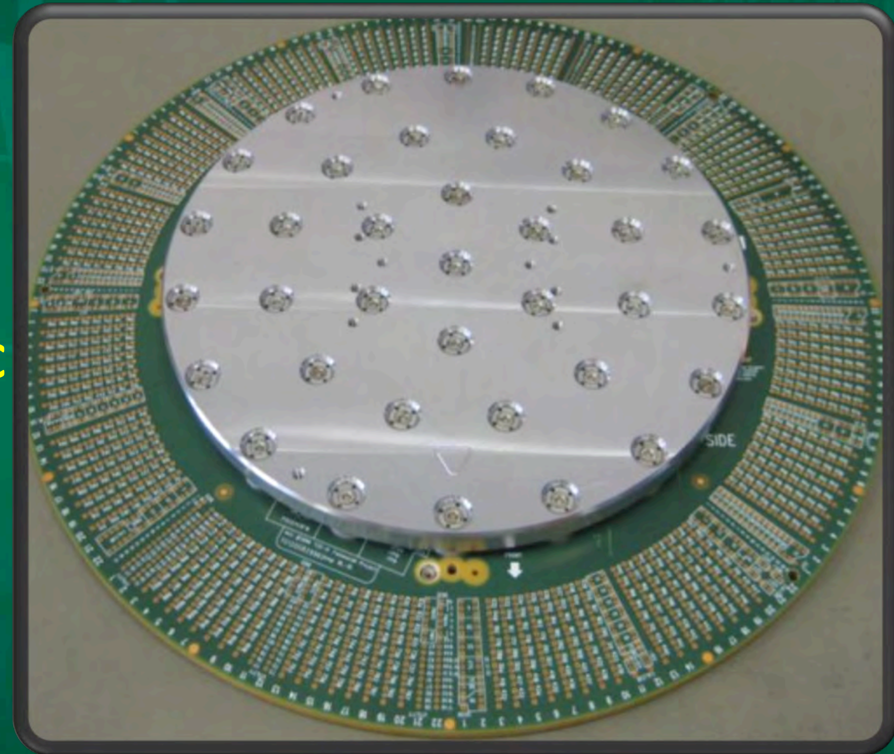
NXP requirements to FM

- Must fit to Teradyne J750 12inch Tester
- Probe card changing by Automatic Probe Card Changer
- Hot and cold test
- Sufficient spacing for components on PCB
- DUT arrangement flexible on complete wafer area

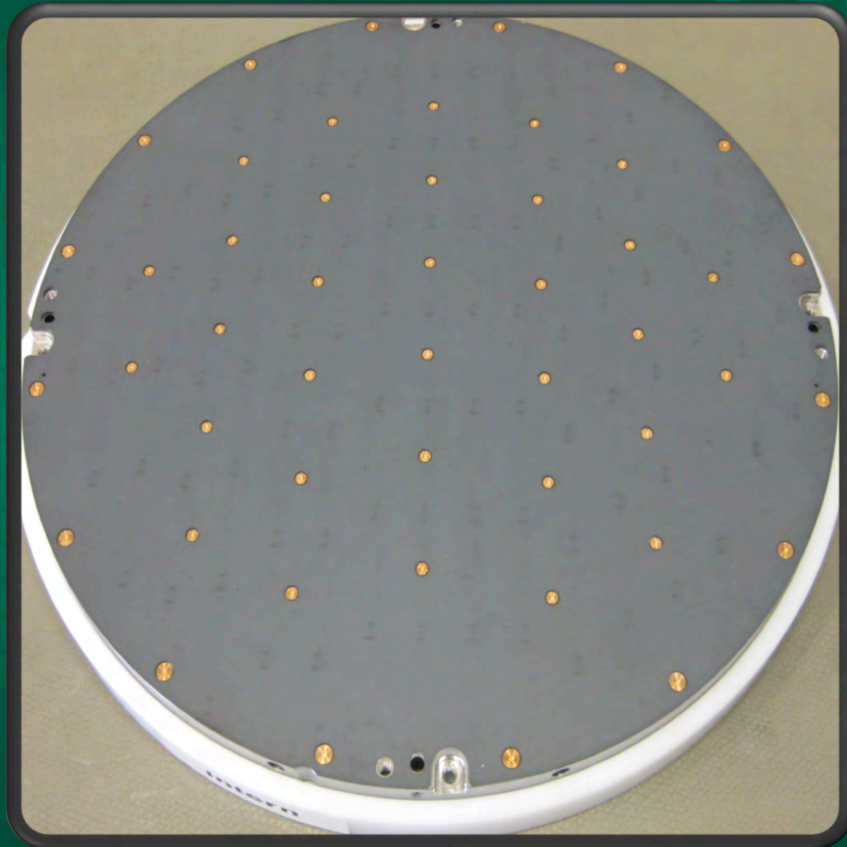
Feinmetall D32 Specification

- Active Area: 213mm
- Outer Dimension Head: 215mm
- Head exchangable
- Beams exchangable onsite
- Temperature Range: -43°C to 125°C
- Max. Pin Count: 5000
- Min Pitch: 86µm
- Min Pad Size: 70µm x 70µm
- XY-Alignment: <15µm
- Z-Planarity: <50µm

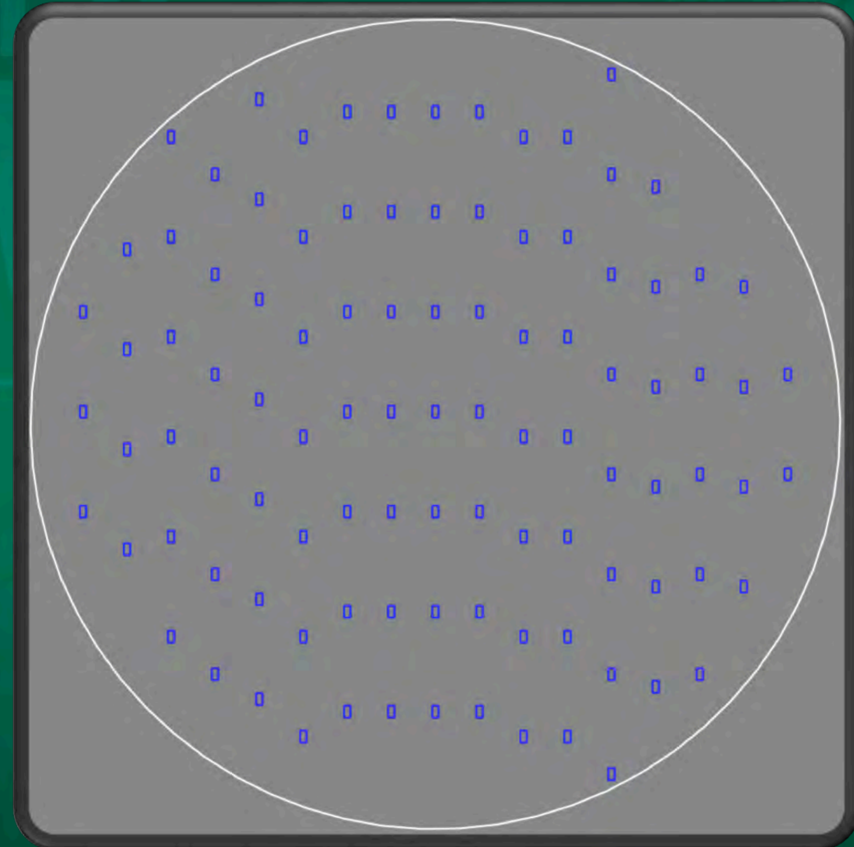


FM D32 case study for NXP

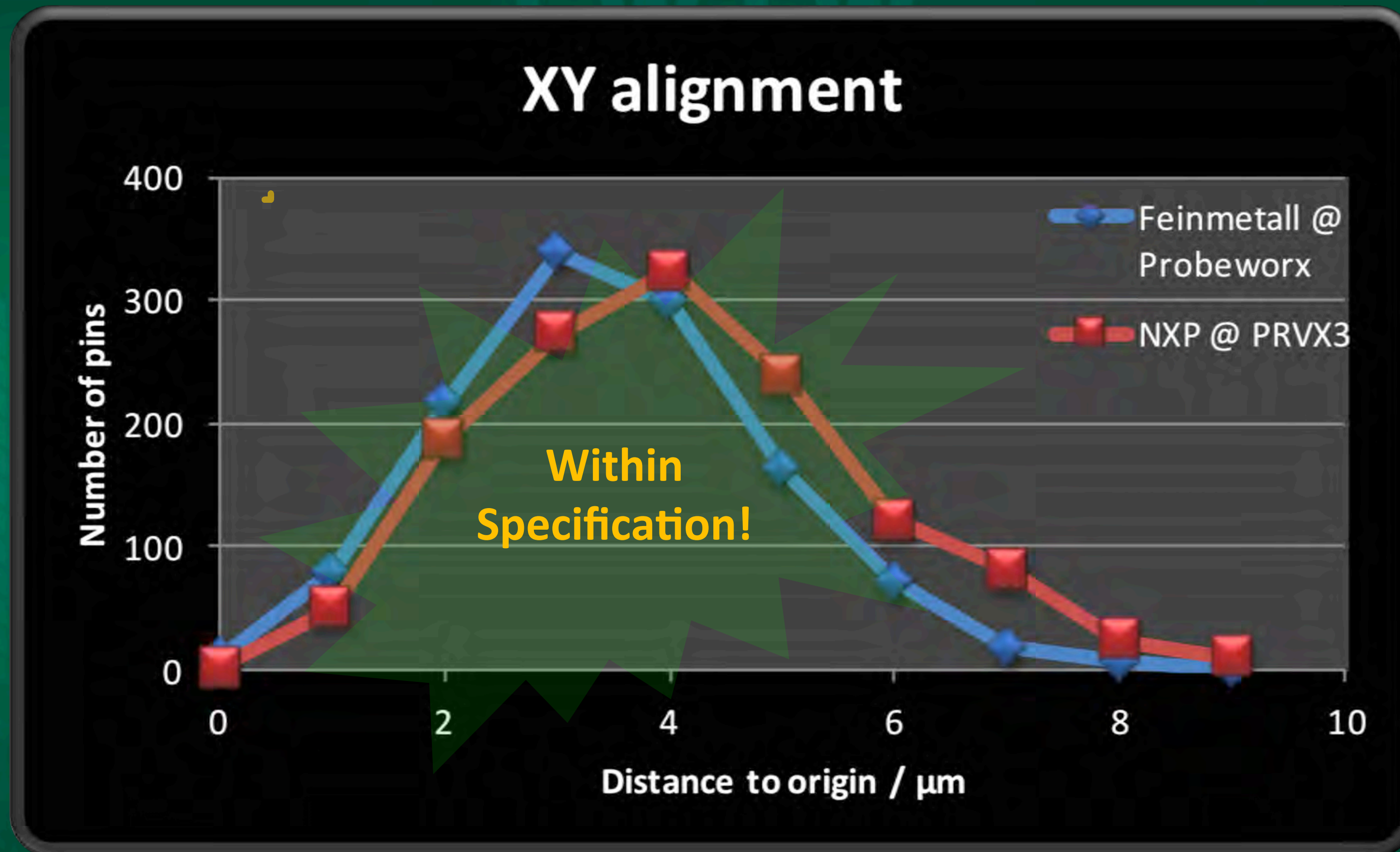
Probe head



100x DUT arrangement



XY alignment accuracy (ProbeWoRx®)



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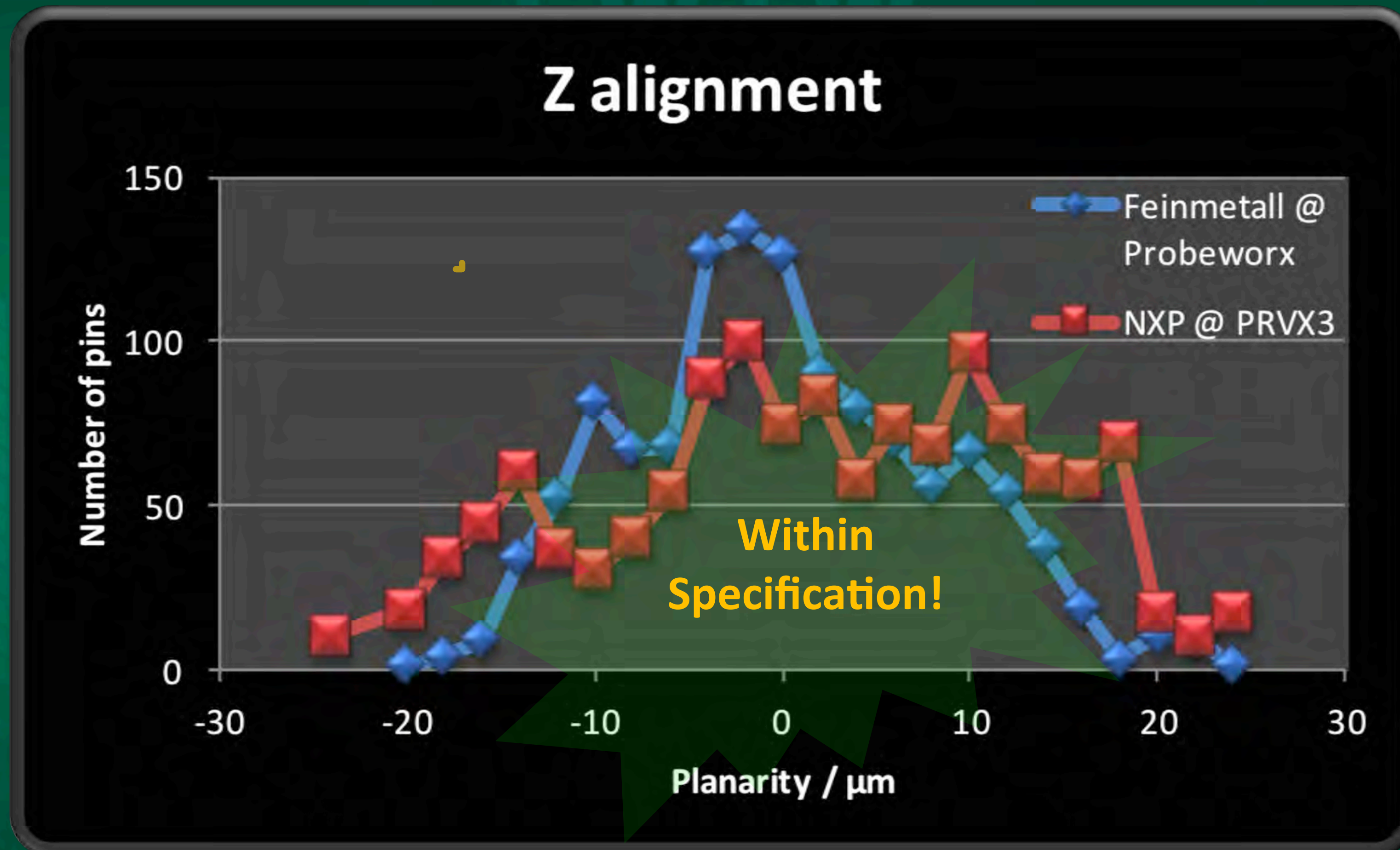
Planarity alignment (ProbeWoRx®)



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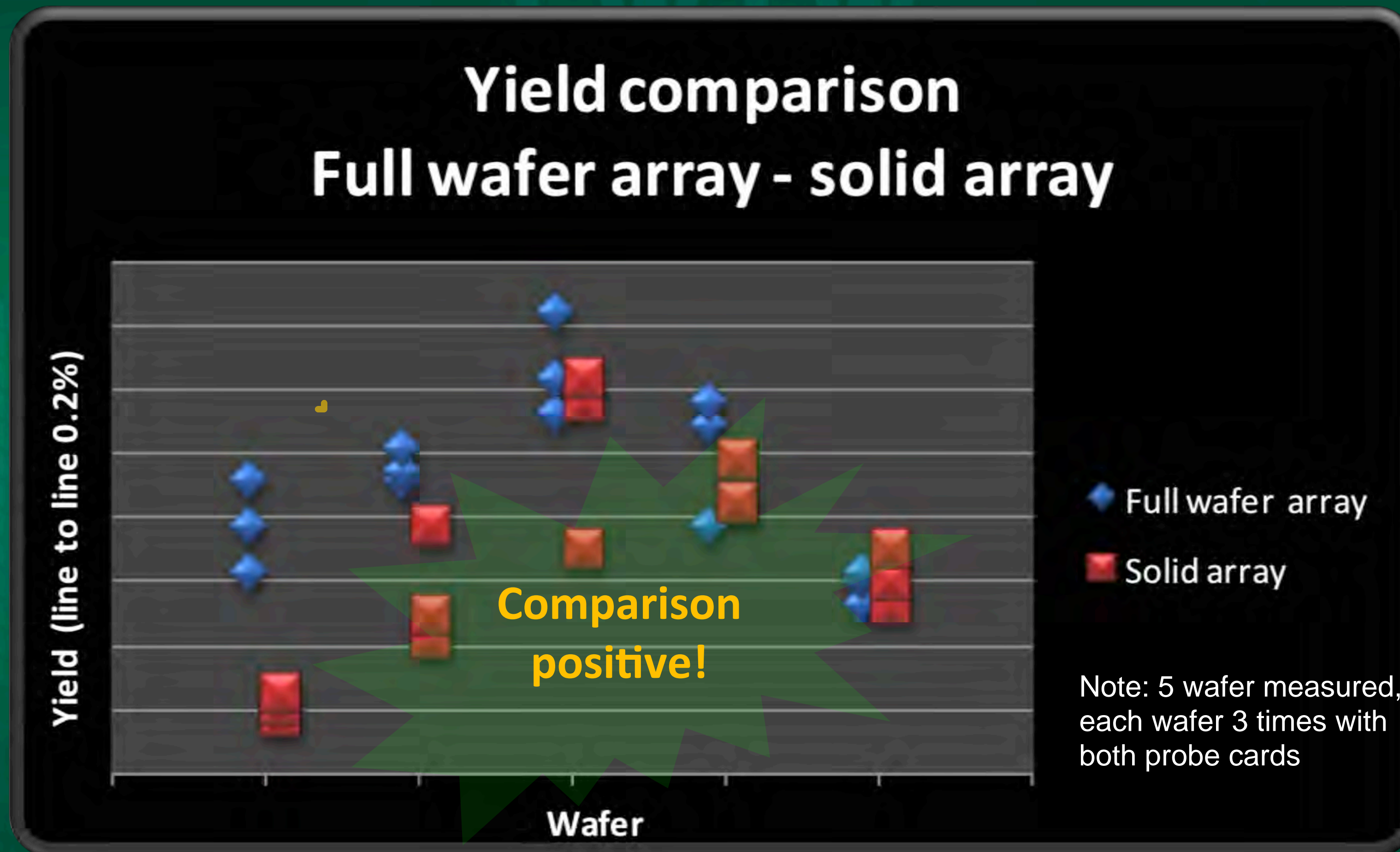
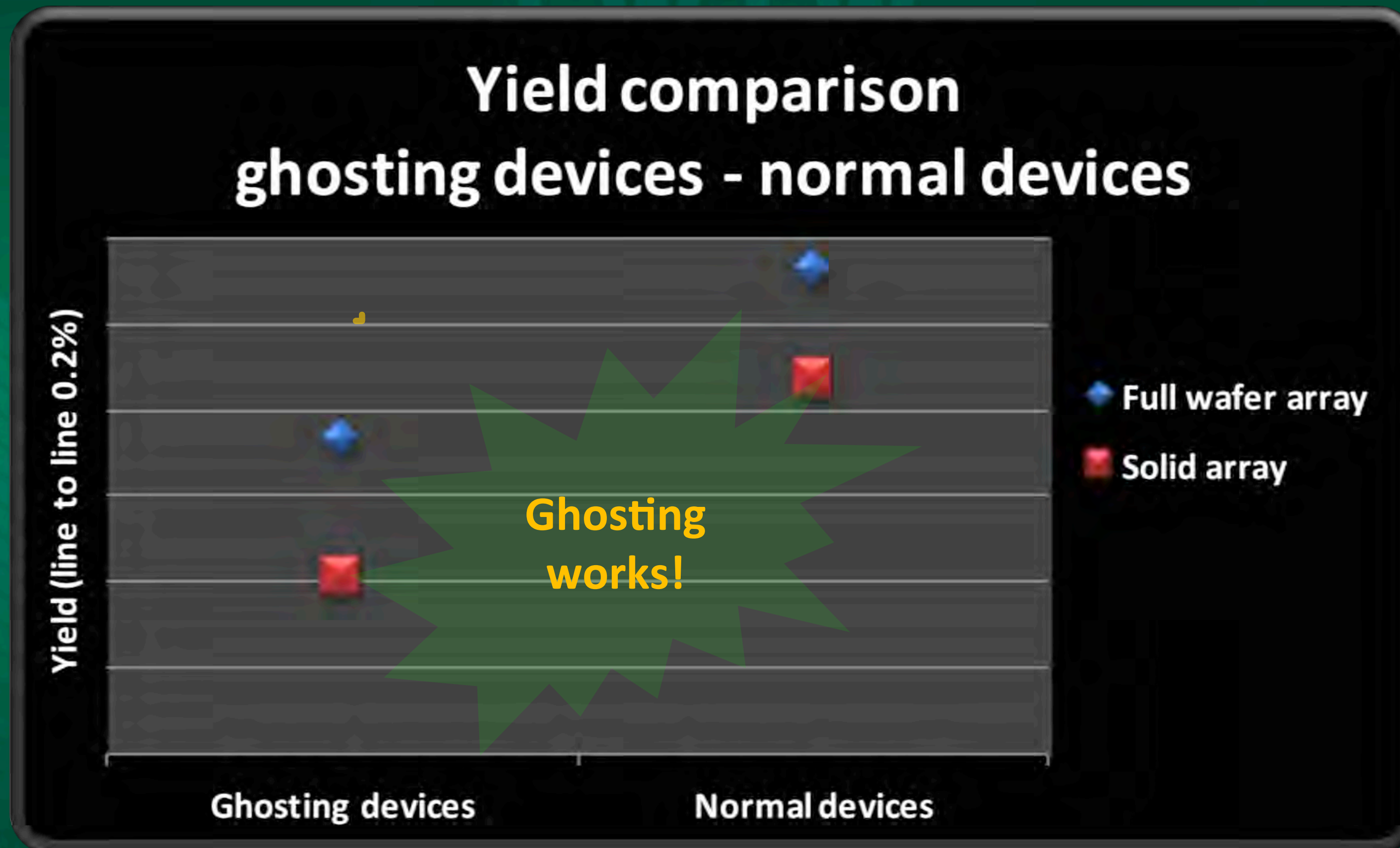
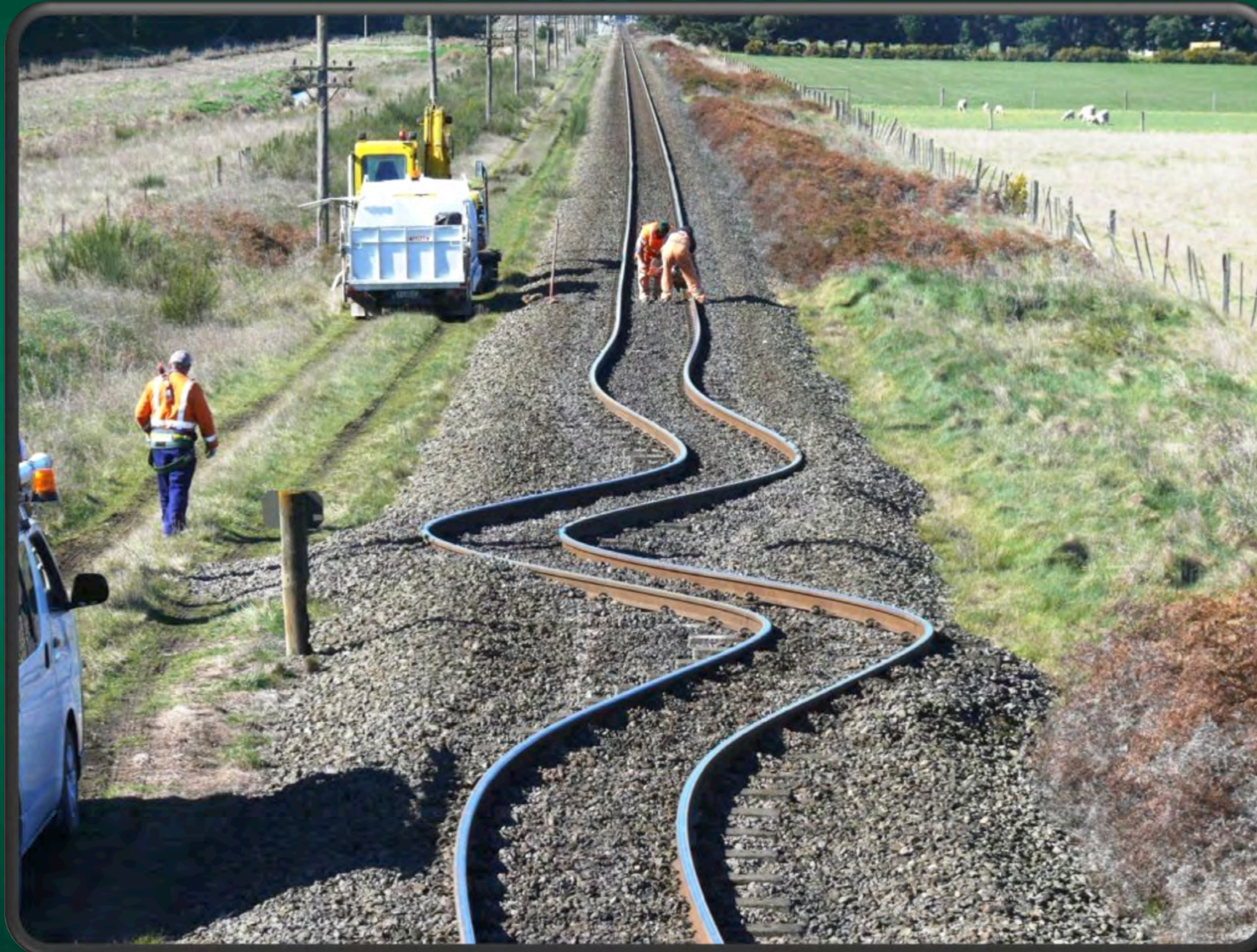
Yield comparison full array/solid array



Yield comparison of ghosting areas

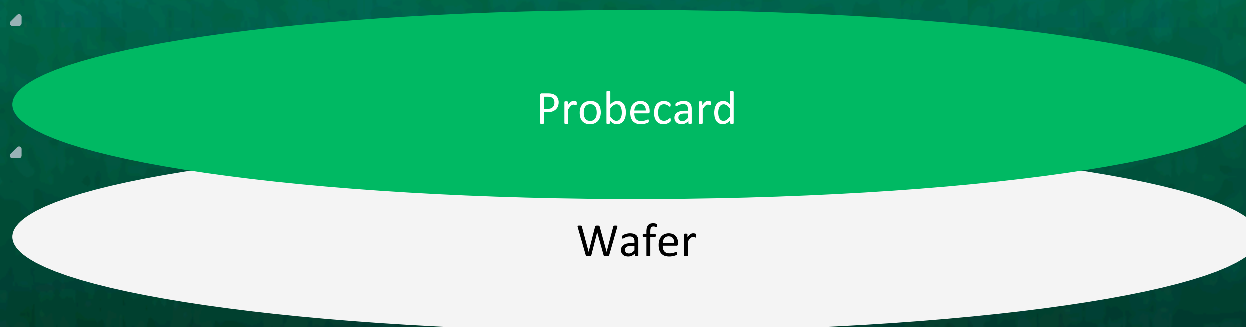


Probe to pad alignment challenge

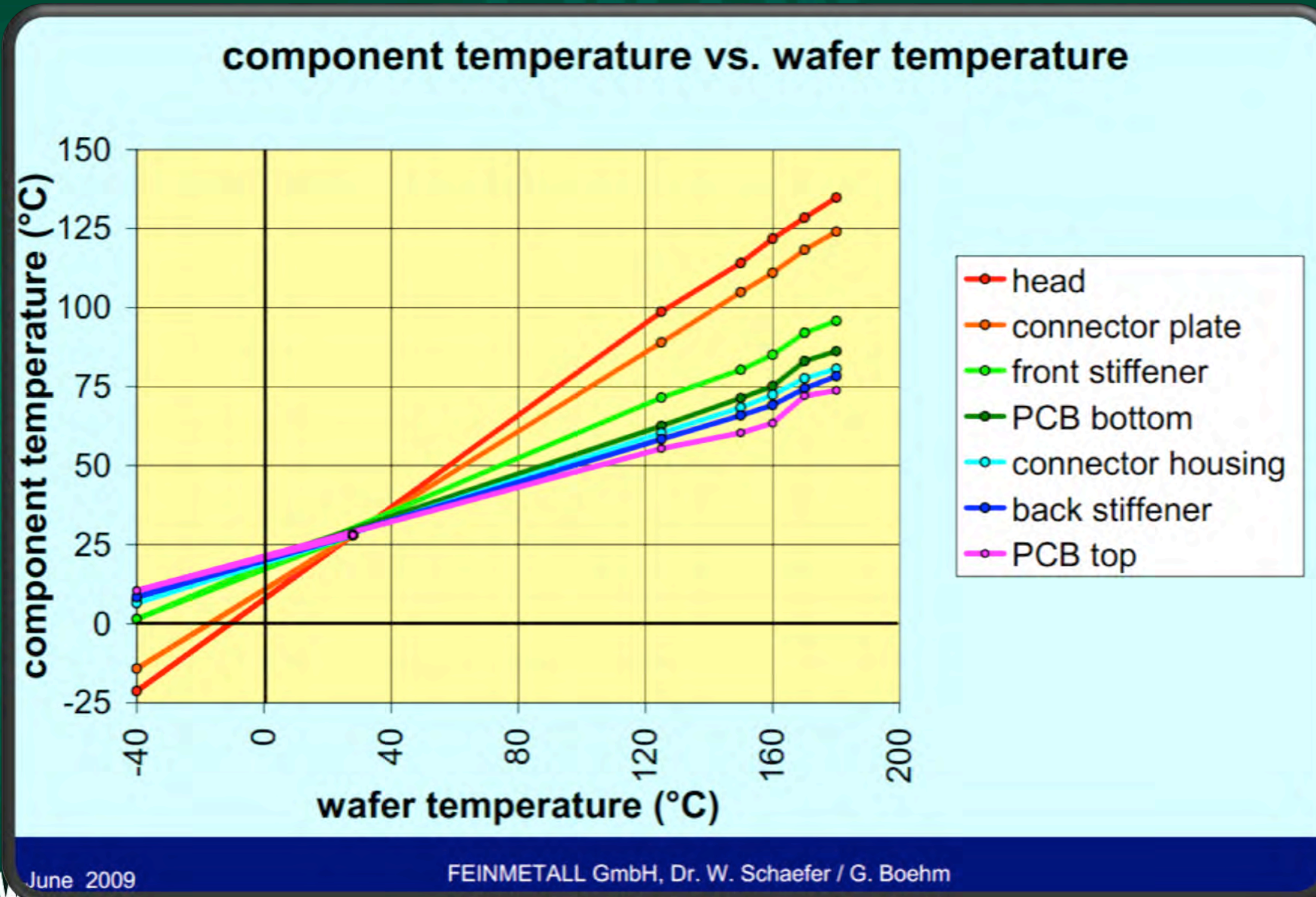


Probe to pad alignment challenge

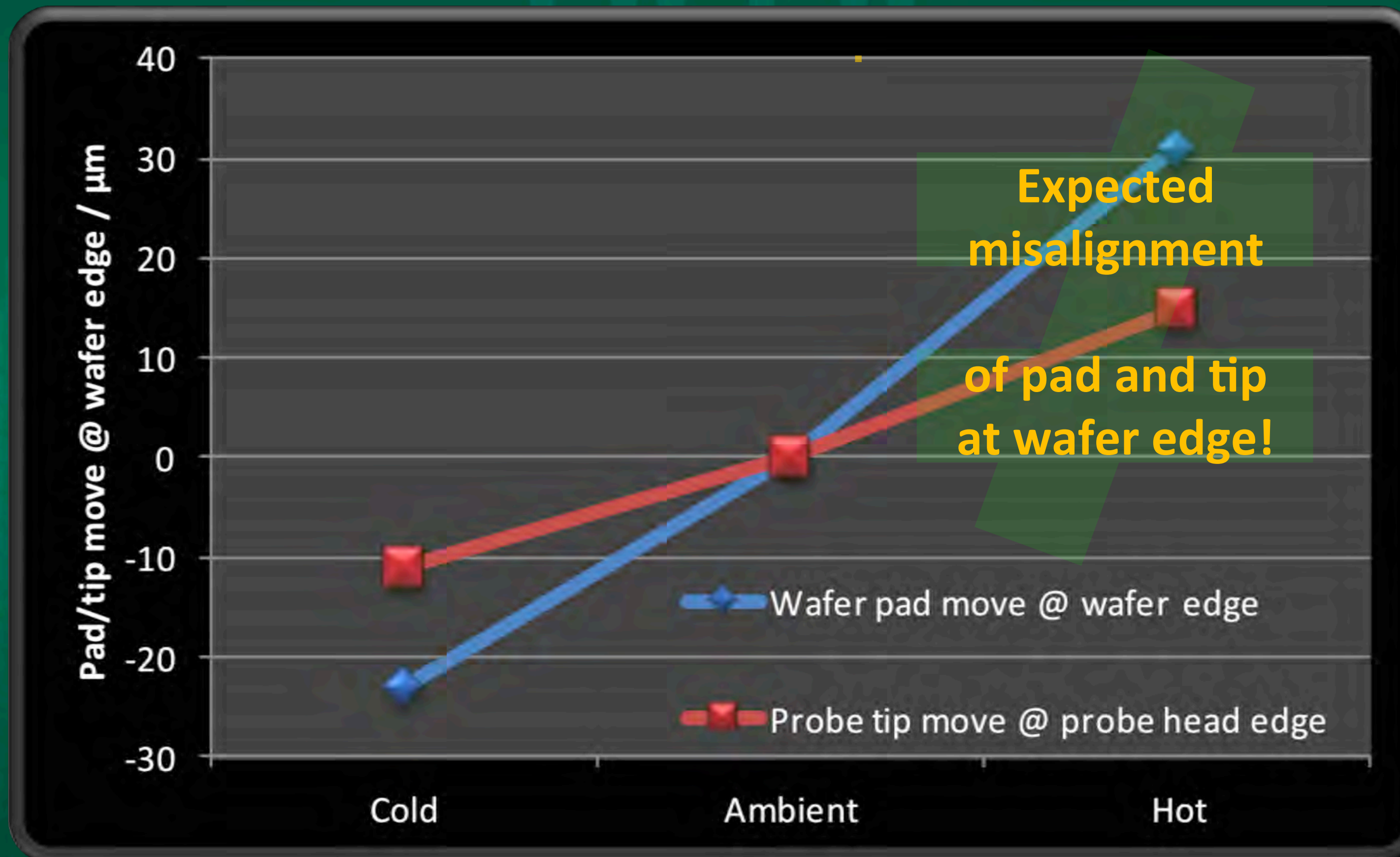
- **Wafer size immediately changes with coefficient of thermal expansion (CTE)**
  - Pads at wafer edge move related to the CTE of Si
  - Wafer reaches chuck temperature within seconds
- **Probe card adapts temperature over longer time scales**
  - Probes at wafer edge move with the CTE of the probe head material
  - Probe head never reaches chuck temperature, saturation needs minutes
  - Mismatch expected after saturation because of CTE_{Si}>CTE_{FPC}



Temperatures of the probe card



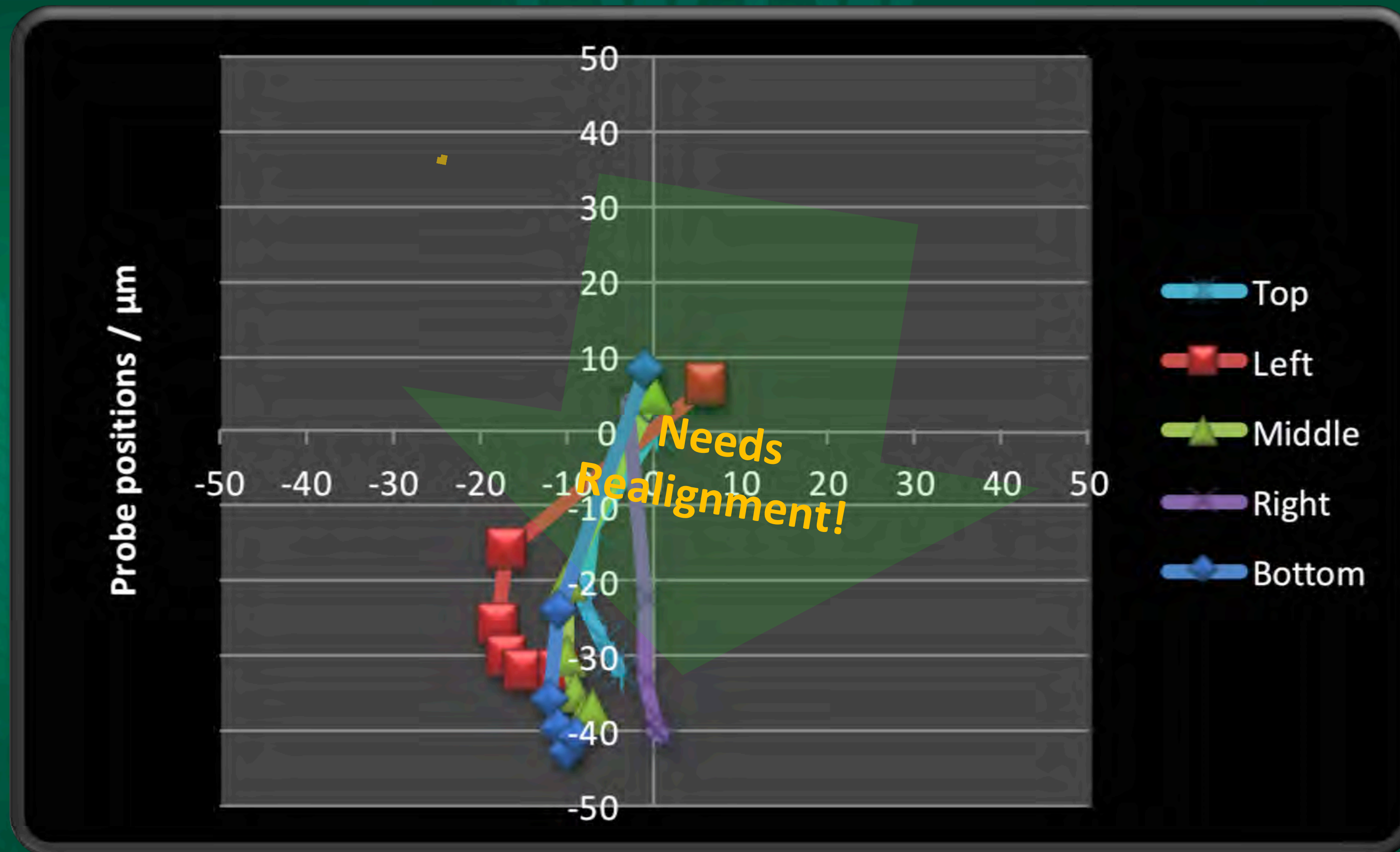
Expected wafer and probe head expansion



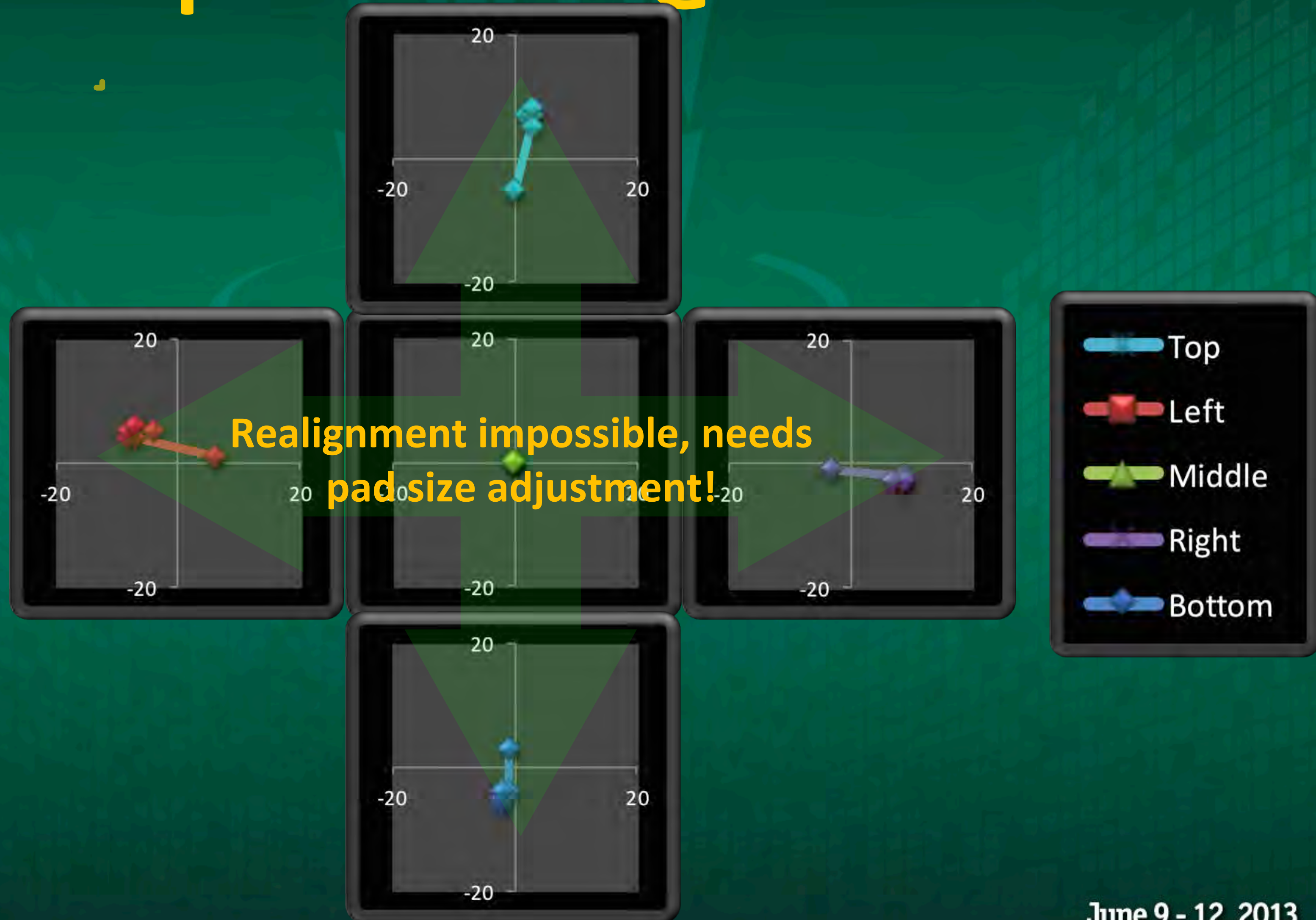
Alignment measurement on prober

- Full wafer probe card installed in prober
- 2h soak @ -43°C/125°C
- Probe realignment after 0, 20, 50, 80, 120 min
- 5 needles measured
  @top, left, middle, right and bottom of the card

Absolute XY movement @ +125°C



Relative XY movement to middle of the probe card @ +125°C



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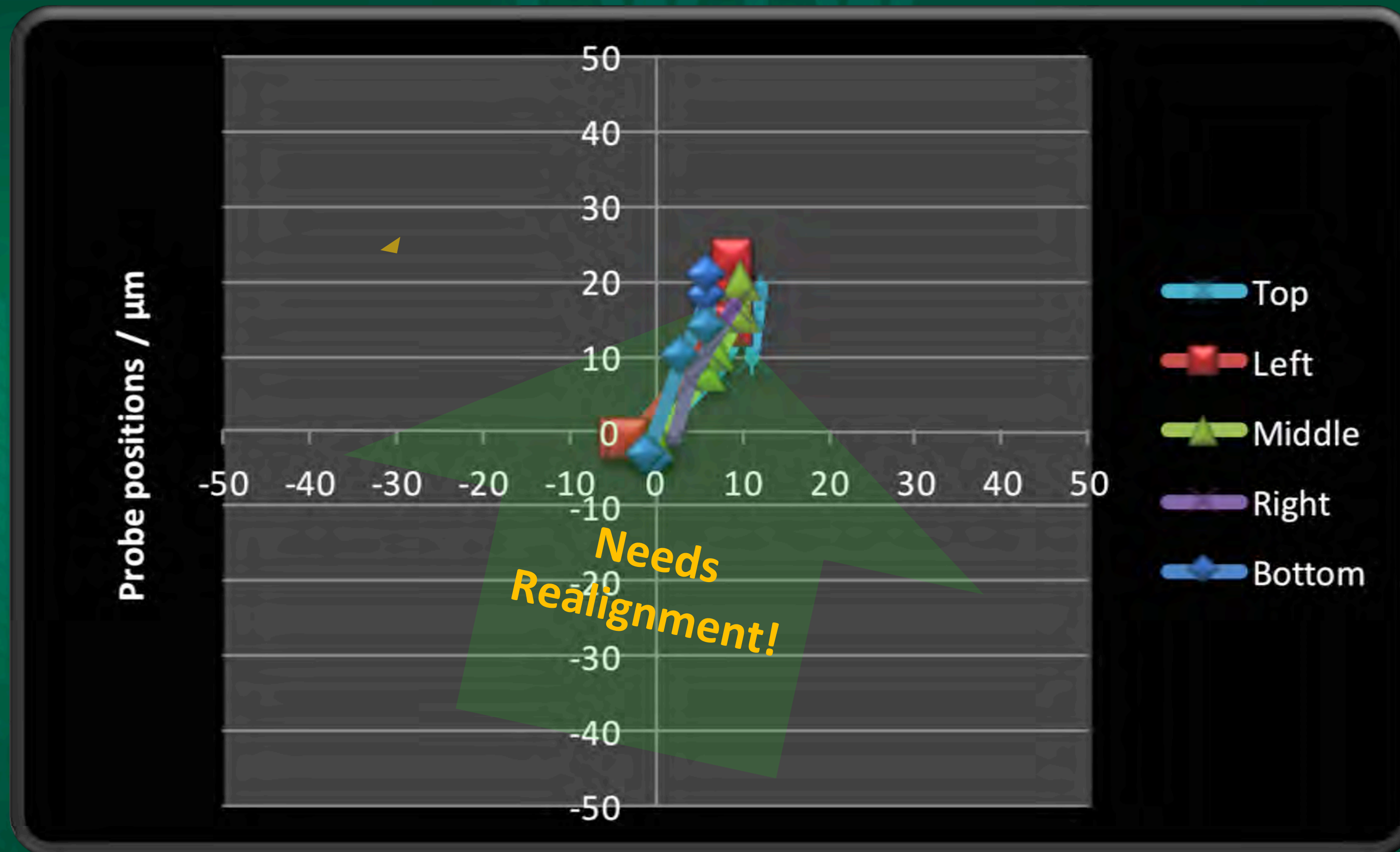
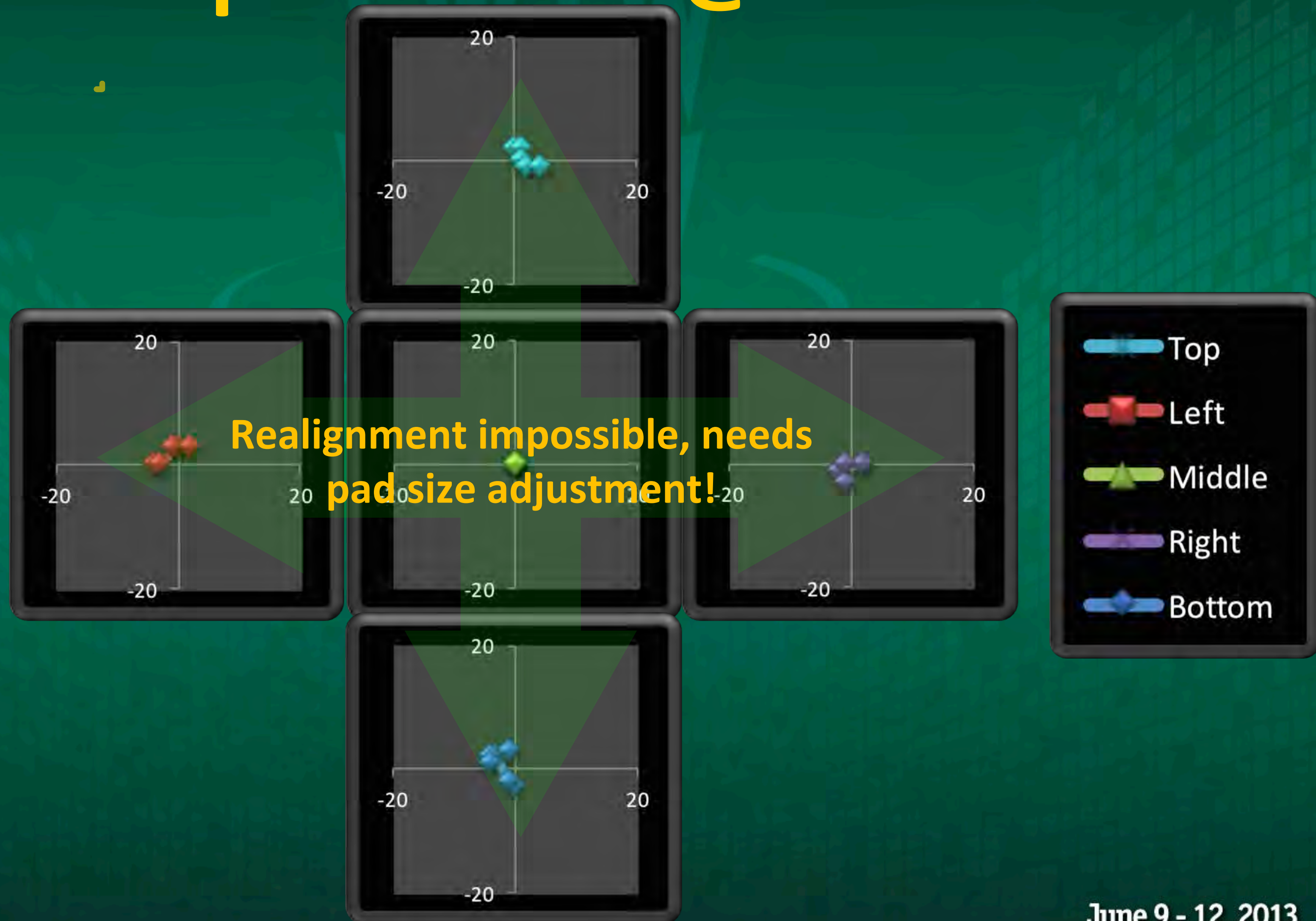
Absolute XY movement @ -43°C



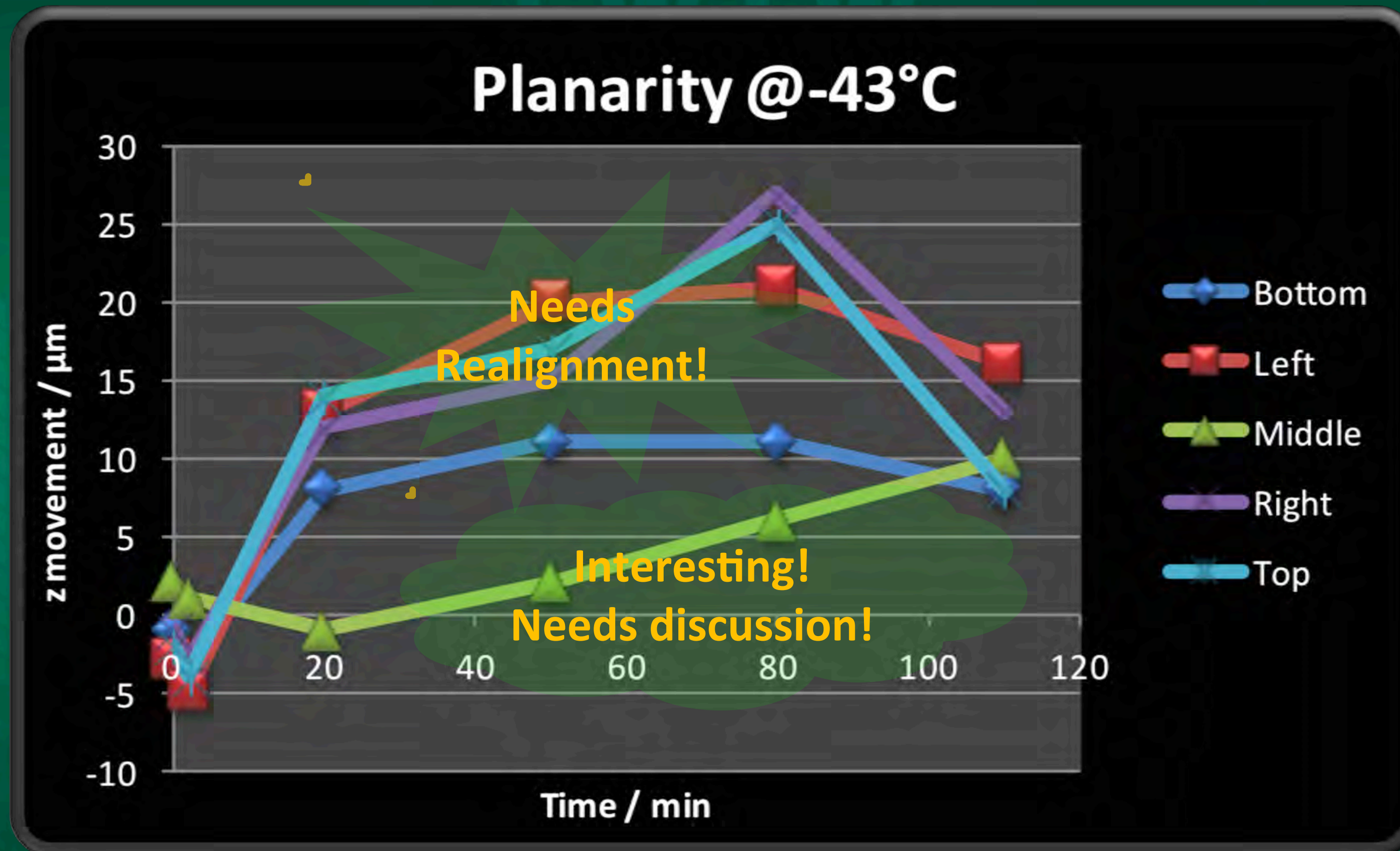
SWTW

Relative XY movement to middle of the probe card @ -43°C

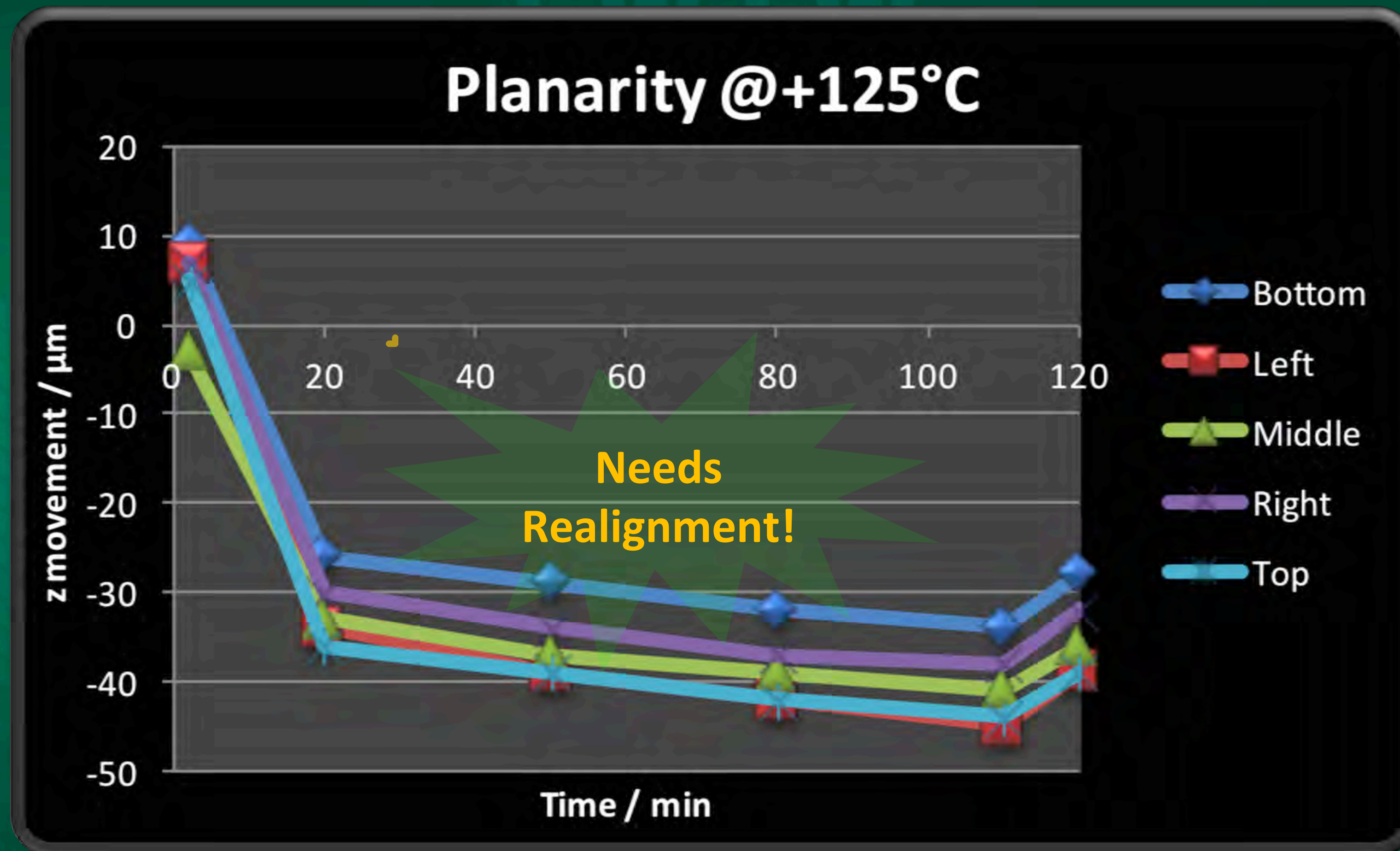


SWTW

Absolute z movement @ -43°C



Absolute z movement @ +125°C



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Other NXP process challenges

- Electrical start up procedure:
  Change from area to shorting wafer
- Probe card cleaning procedure:
  Change from cleaning block to cleaning wafer
  ➔ Use of more than one fixed tray
- Multi site array beyond 2048x (array 64x64)
  ➔ Upgrade of prober software
- No automatic stepping by prober
  ➔ Offline generated stepping pattern
- Probe card analyzer (PRVX3®) process adaption
  ➔ Split full wafer array into several measurement zones.

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Summary and future step

Summary

- Successful test time reduction of 16%
- FM successfully adapted NXP requirements
- Planarity and alignment within specification
- Temp. XY movement at wafer edge requires pad size adjustment– needs further attention
- Yield comparison positive
- Ghosting / Sharing tester resources works – no yield loss

Future steps

- **Probe to Pad alignment data on real pads and at temperature – soak optimization**
- **Long term production experience**
- **Optimizing probe card maintenance**
  - Specifically for legacy probe card analyzers
- **Industrialization needed for 12“ products**

Acknowledgements

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  - Maik Ehlen

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THANK YOU!

QUESTIONS?