IEEE SW Test Workshop
Semiconductor Wafer Test Workshop
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Ideal 3D Stacked Die Test

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Feldman Engineering Corp.

Overview

- Introduction
- Probe Challenge
- Contact Solutions
- Implications
- Conclusion

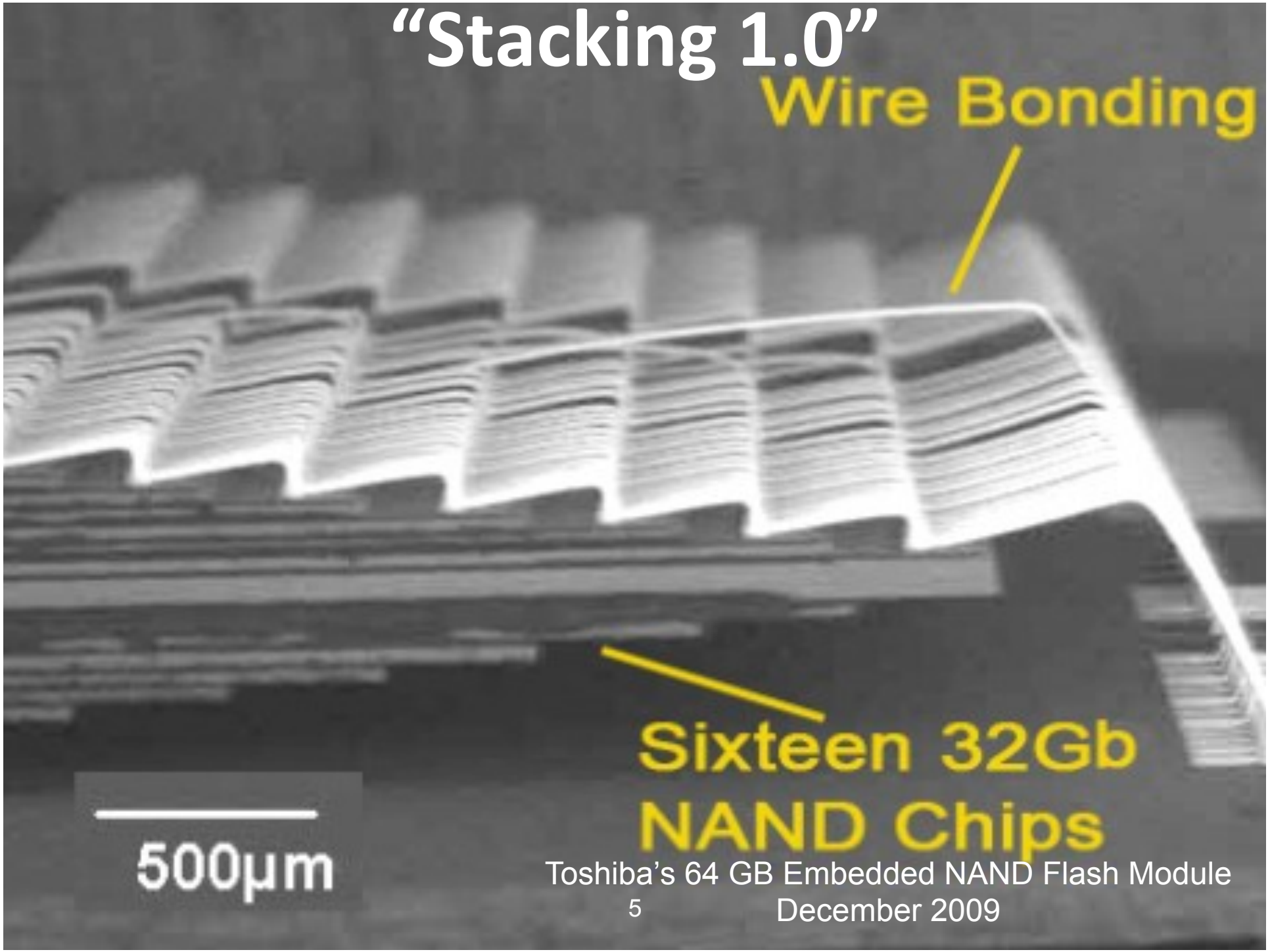
Cost of Test	≤	Cost of No Test
• Yield loss (materials & labor)		
• Test development cost – test engineering, non-recurring engineering/expenses (NRE), etc. • Test operational cost – operator labor, test equipment, test consumables (wafer probe cards, sockets, load boards), maintenance, floor space / facility expenses, etc. • Test equipment / cell depreciation • Rework cost • Work in Progress (WIP) inventory cost • Over stress or intrinsic device damage? • Other damage (eg. probe)?		• Subassembly rework cost. If non-reworkable, cost of subassembly. • Test escapes – warranty or contractual cost, customer dissatisfaction / brand damage • Possible infant mortality? • Greater downstream test complexity and cost for similar or greater coverage? • Loss of device characterization or process data?

Test "Coverage"

Controllability

Observability

“Stacking 1.0”



Toshiba’s 64 GB Embedded NAND Flash Module

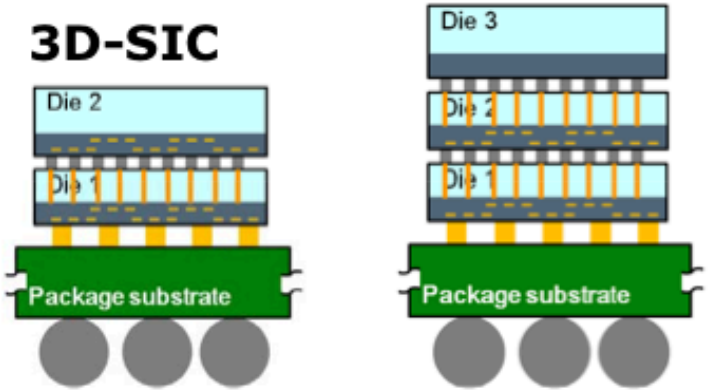
December 2009

Die Stacking

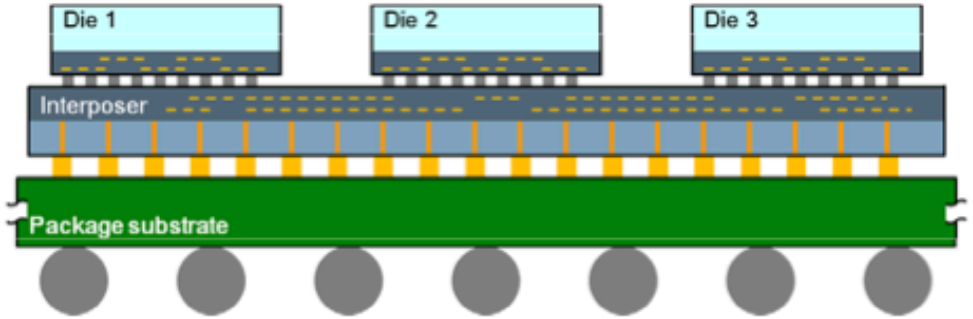
Endless Stacking Opportunities

"Whatever your children can make using Lego bricks"

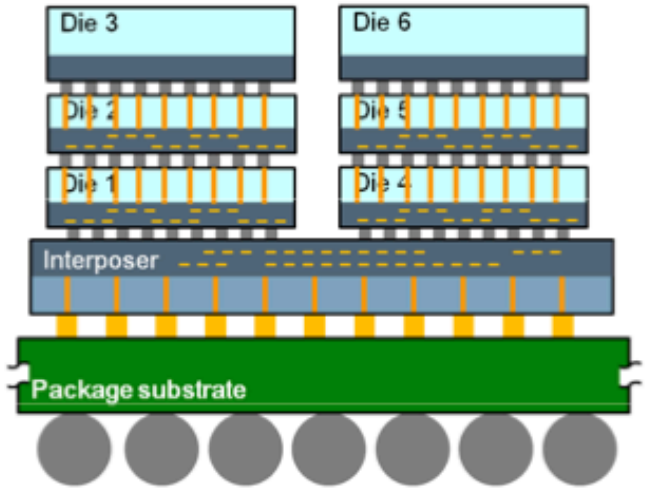
- **3D-SIC**



- **2½D-SIC**



- **2½D + 3D = *5½D-SIC***



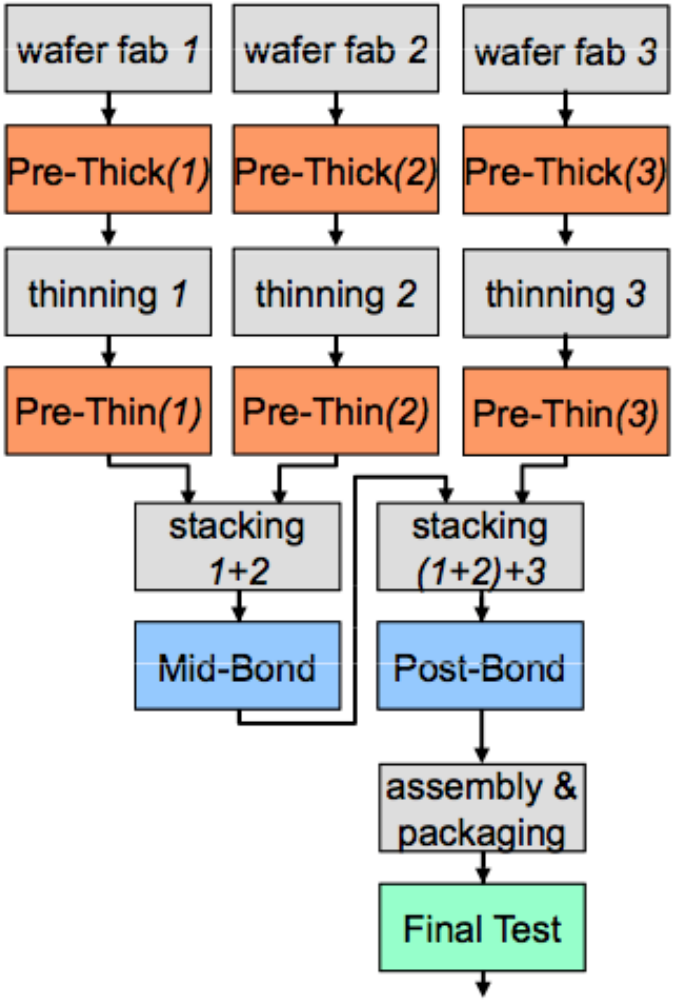
"Wafer Probing on Fine-Pitch Micro-Bumps for 2.5D- and 3D-SICs", Erik Jan Marinissen (IMEC), Peter Hanaway (Cascade Microtech), et. al.

2. Test Challenges

Challenge 1: 3D Test Flows

Potential Test Moments:

- **Pre-Bond Test**
  - Content : die (+ TSVs)
  - Access : wafer probe 
- **Mid- and Post-Bond Test**
  - Content : interconnects (+ dies)
  - Access : wafer probe  + DfT 
- **Final Test**
  - Content : dies + interconnects
  - Access : socket  + DfT 



- Many more natural wafer test moments
- Pre-Bond and Post-Bond tests are distinctly different in test access
- Disintegrated production flow more likely: KGD / KGS testing
- Integrated flow: test benefits need to exceed costs ⇒ cost modeling

"Wafer Probing on Fine-Pitch Micro-Bumps for 2.5D- and 3D-SICs", Erik Jan Marinissen (IMEC), et. al. [Taouil et al. - ATS'10]

Bumps on the Road to 3D IC HVM

- Availability of commercial 3D EDA tools
  - Especially thermally aware design tools
  - Floorplanning
  - Routing
  - Power/signal integrity
- Micro bumping and assembly for finer pitch
- Wafer thinning, specifically the debonding step in the temporary bonding process
  - Higher yields required
- Thermal, where logic is part of the stack
- Test methodology and solution
  - KGD
  - Yield
  - Test methods
- Infrastructure related issues
  - Logistics
  - Supply chain handoff
- Cost reduction compared to alternatives

"Bumps on the Road to 3D ICs", E. Jan Vardaman (TechSearch International, Inc.), RTI Technology Venture "3-D Architectures for Semiconductor Integration and Packaging" December 13, 2012.

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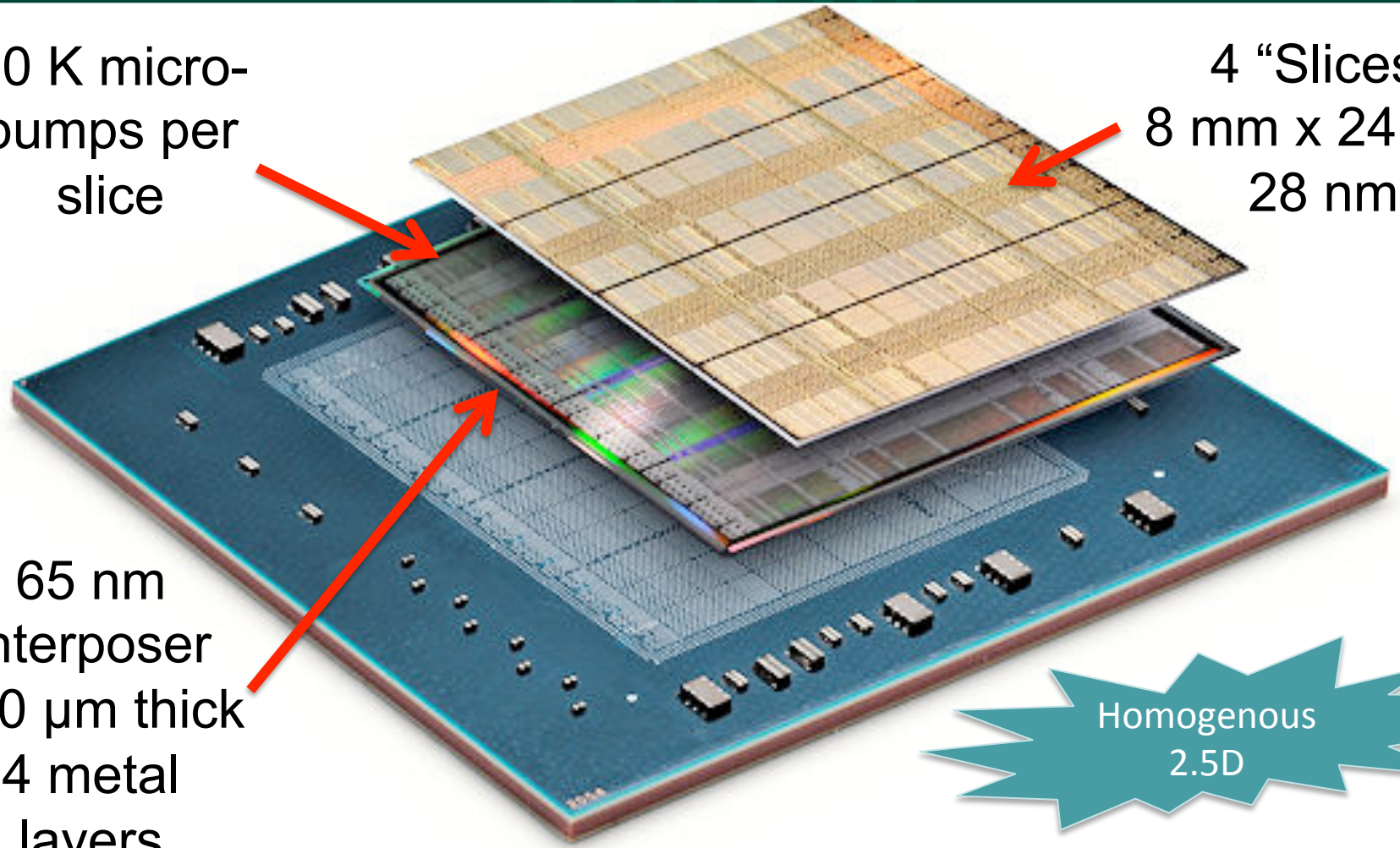
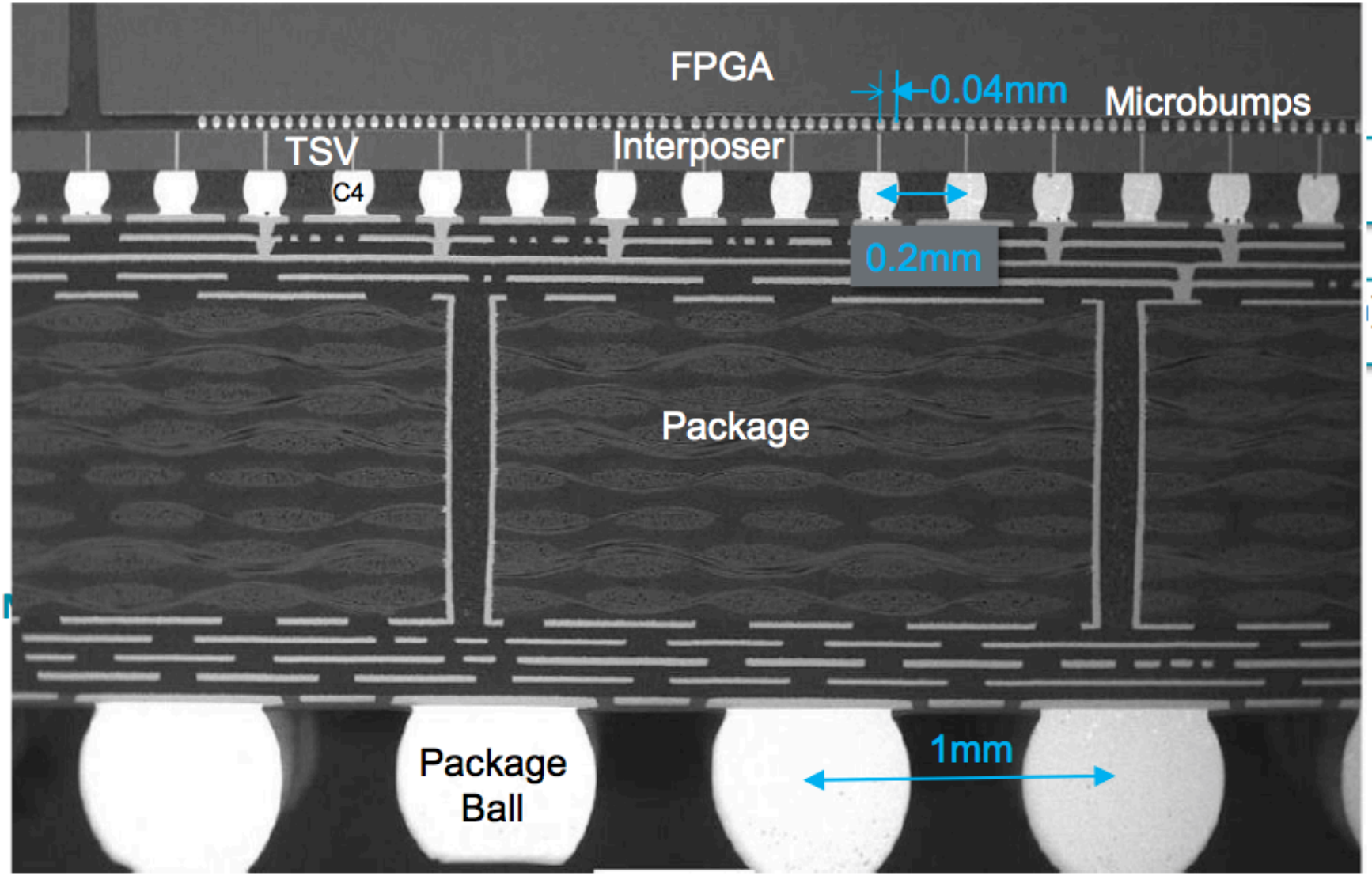
Xilinx Virtex-7 2000T FPGA (Oct '11)



Ref: [Leibson] [Patterson]

Elements of SSIT [Stacked Silicon Interconnect Technology]



Liam Madden (Xilinx). “Heterogeneous 3-D stacking, can we have the best of both (technology) worlds” International Symposium on Physical Design, March 25, 2013.

Microbumps

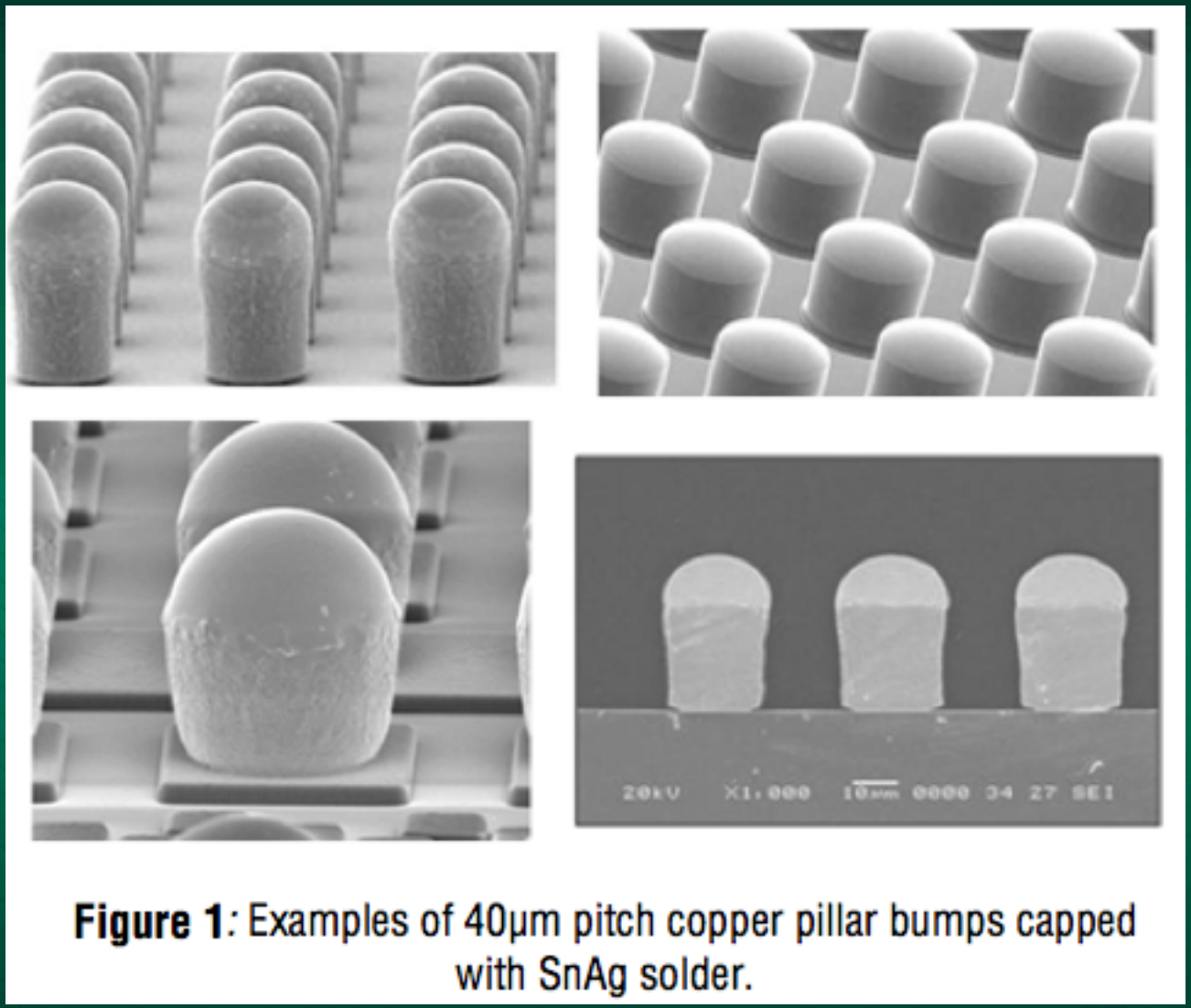


Figure 1: Examples of 40µm pitch copper pillar bumps capped with SnAg solder.

Ref: [Patterson]

Microprocessor Example

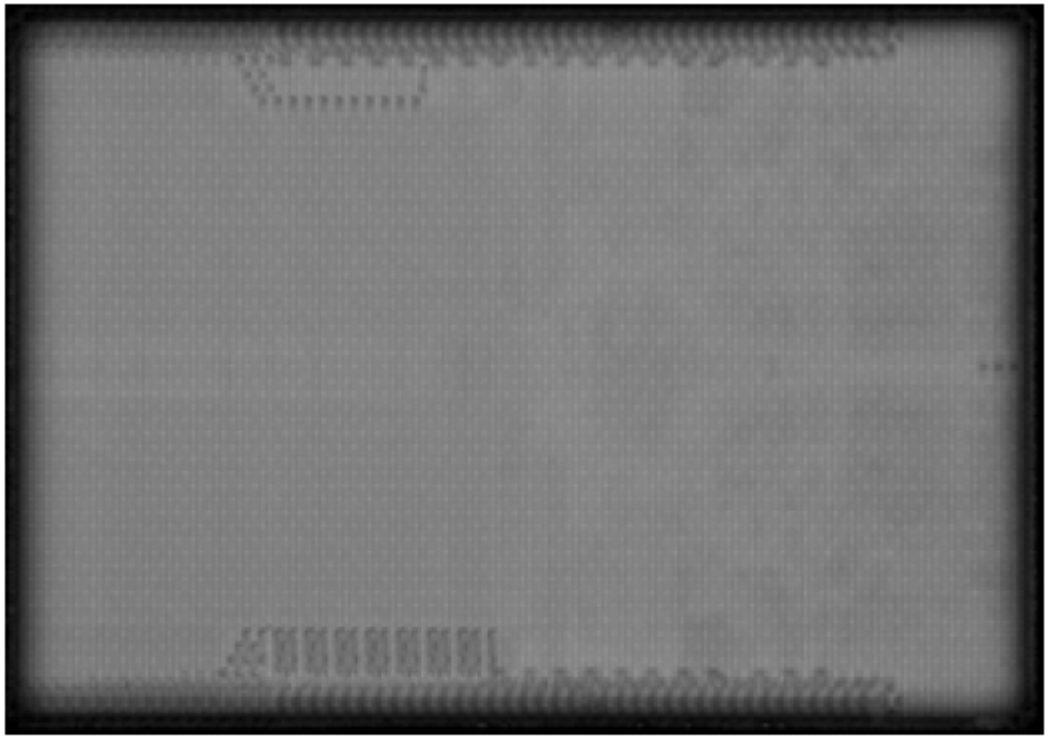
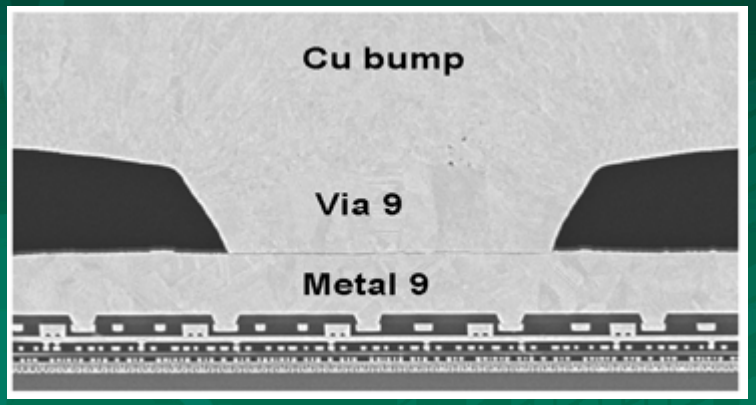
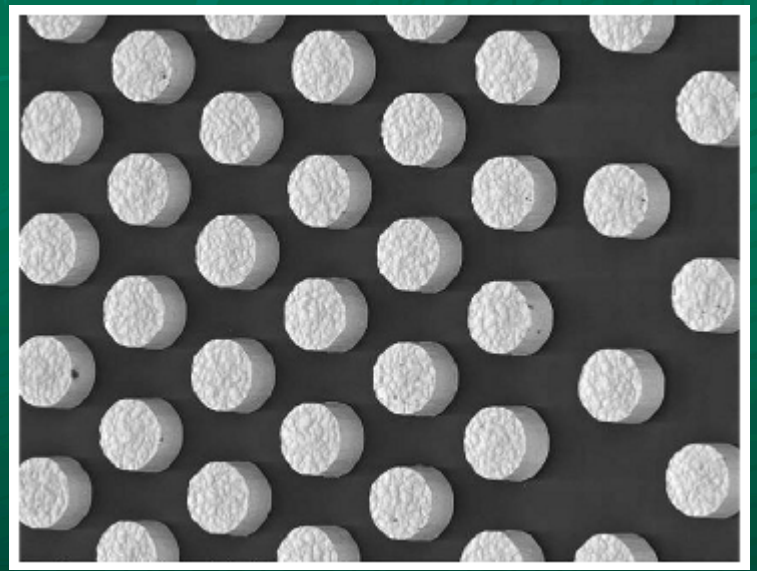


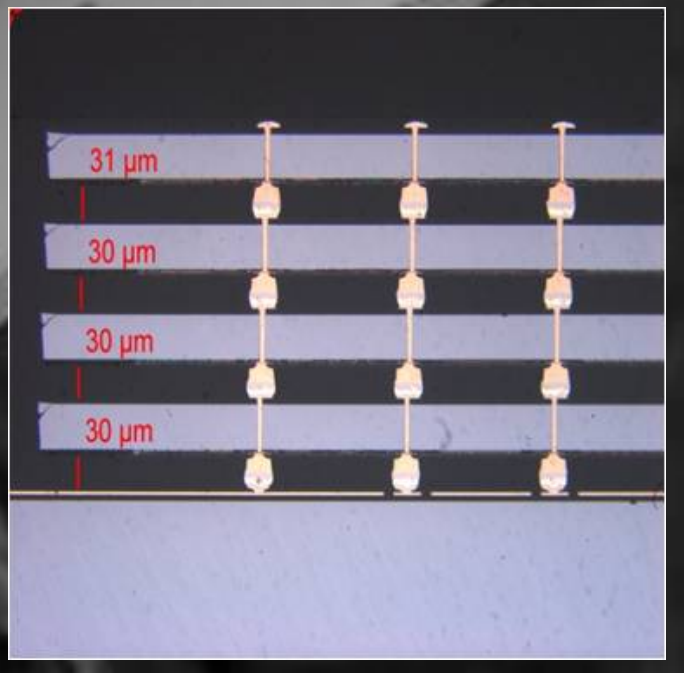
Figure 9: CSAM image of a production unit post packaging





Intel Technology Journal (6/2008):
45 nm process ~50 µm tall Cu bumps

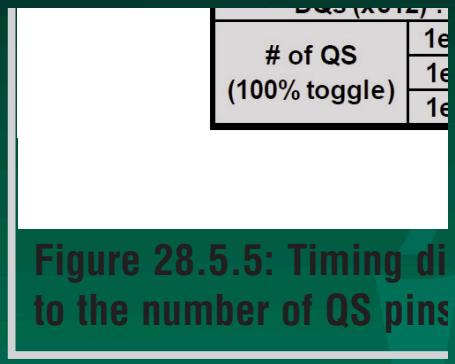
3D Hybrid Memory Cube - Micron

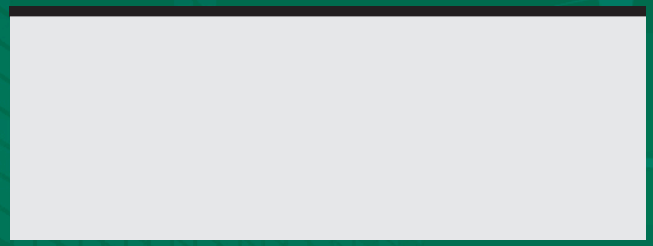


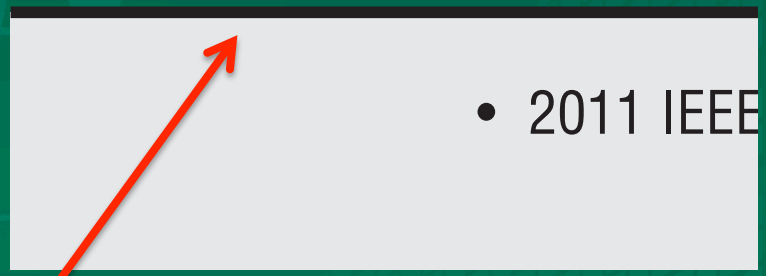
500 µm

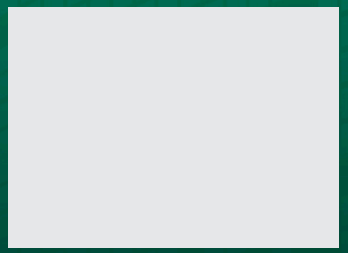
Justin Rattner (Intel CTO) Keynote @ IDF 2011

Mobile DRAM predecessor to Wide I/O









Al pads (muxed) to test with existing probe technology

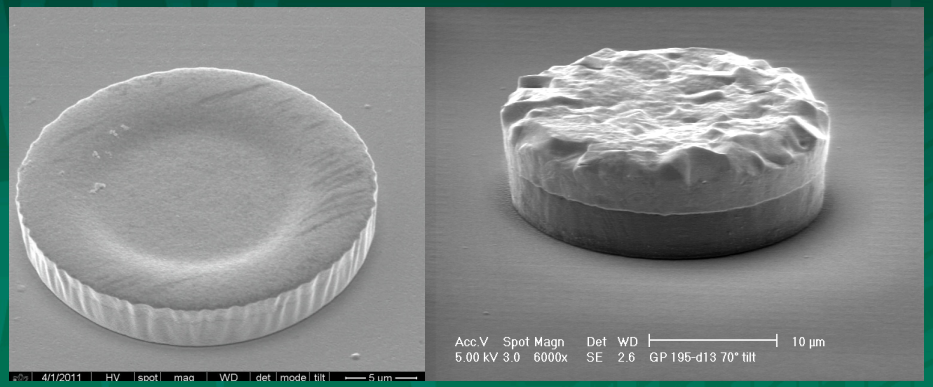
> 1000 micro-bumps 50 µm pitch array

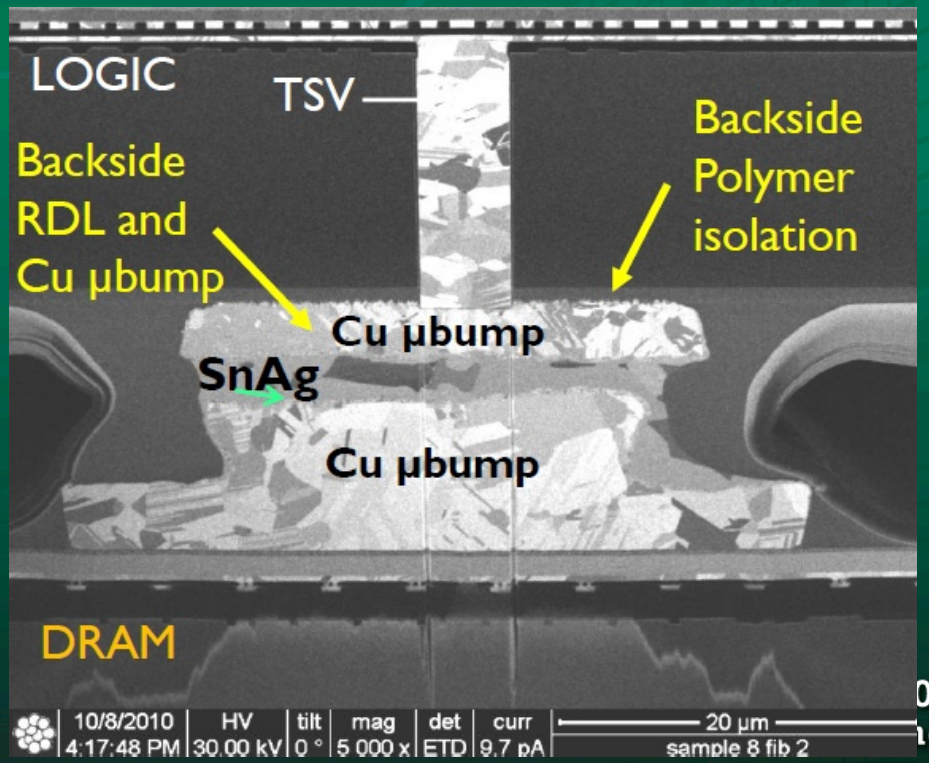
"A 1.2V 12.8GB/s 2Gb Mobile Wide-I/O DRAM with 4×128 I/Os Using TSV-Based Stacking" Jung-Sik Kim, et.al., Samsung Electronics, ISSCC 2011

Electroplated Micro-Bump Bonding

- Cylindrical bumps
  Side1: Cu (5 µm)
  Side2: CuSn (5 µm + 3.5 µm)

- Size (today)
  Diameter : 25 µm
  Pitch : 40 µm
  Scaling down…



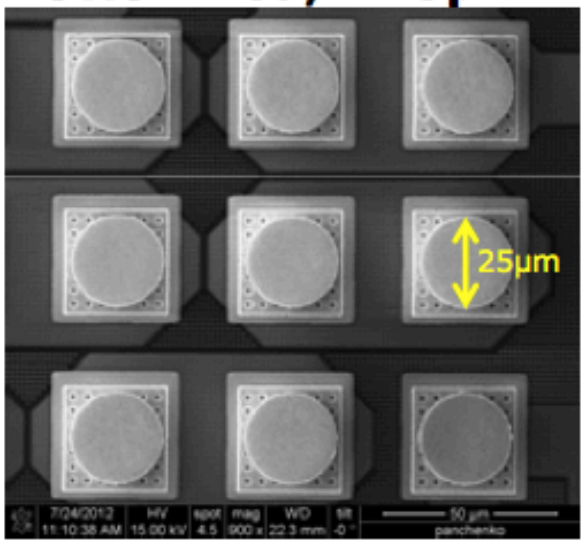


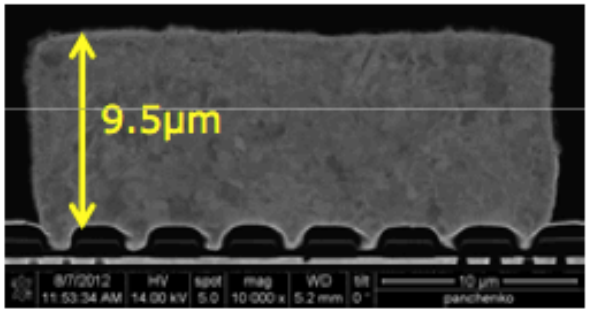
Cascade Microtech & IMEC
(SWTW 2011)

5. 3D Test Access: 3D Probing

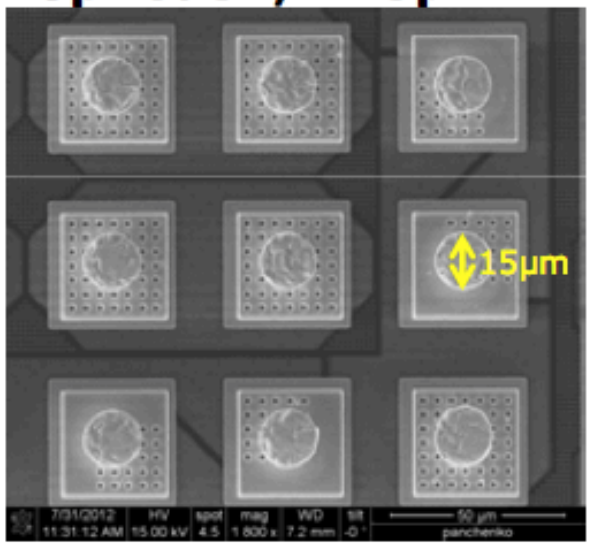
Fine-Pitch Micro-Bumps at IMEC

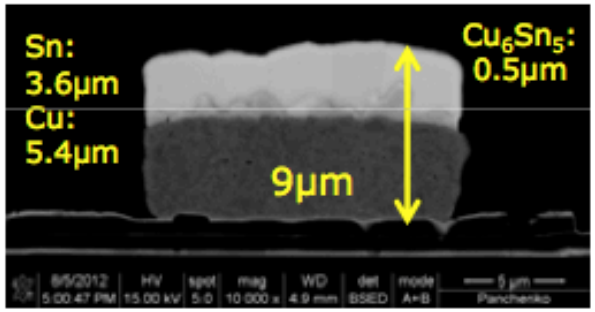
Bottom: Cu, ∅25µm



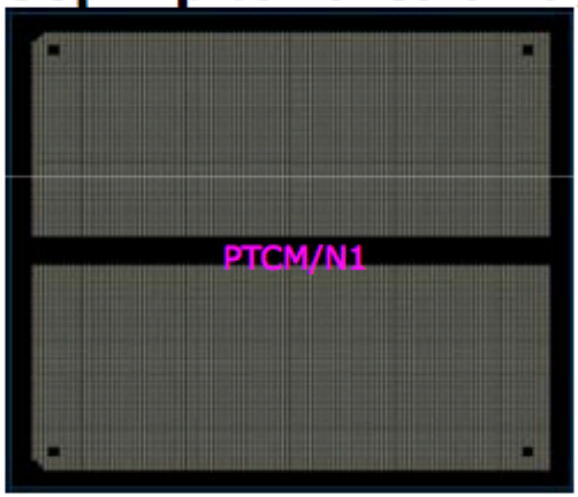


Top: CuSn, ∅15µm

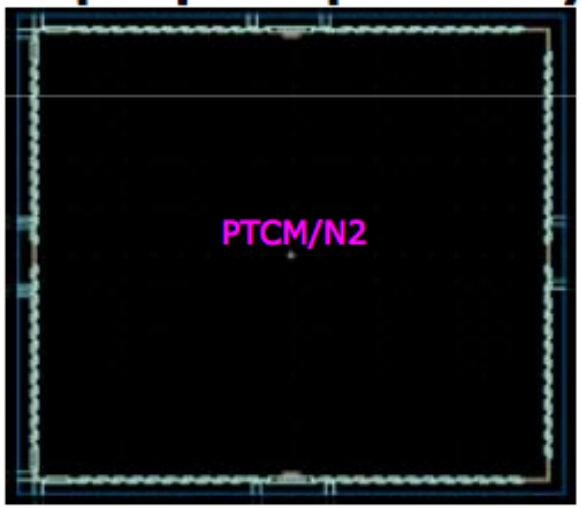




50µm pitch area array

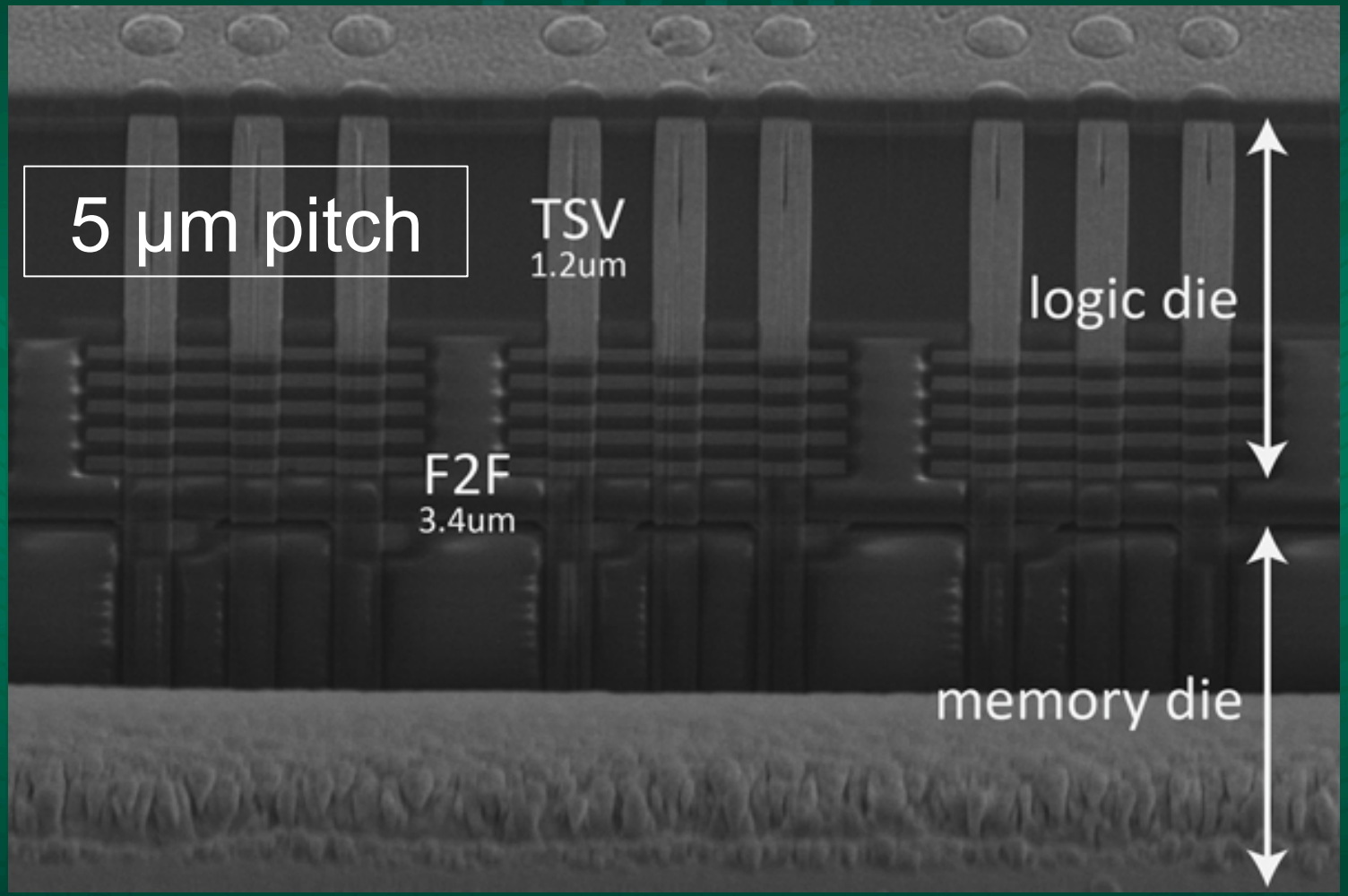


40µm pitch peri array



Erik Jan Marinissen (IMEC). “Testing 3D-Stacked ICs“, RTI Technology Venture “3-D Architectures for Semiconductor Integration and Packaging” December 12, 2012.

Tezzaron



Georgia Tech: The 3D-MAPS Processors
http://www.gtcad.gatech.edu/3d-maps/

Approximate Specifications

	Microprocessor	Wide I/O DRAM	FPGA "slice"	Tezzaron "SuperContact IV"
Die Size	149-295 mm^2		24 mm x 8 mm	
Bumps - **Signals** - **Total**	~1/3 of total	872 1,200	> 20,000 50,000	> 2 M
Pitch	90 µm	50 µm x 40 µm	40 µm	1.2 µm
Bumps / mm^2	123	< 20 (8 mm sq.) 500 core	260	694,444

Ref: [Patti]

By the numbers…

PPM	Cpk	Sigma Level	Assembly Total Microbumps						
			1,000	1,200	10,000	100,000	200,000	1,000,000	10,000,000
10			1.0%	1.2%	10.0%	100.0%	200.0%	1000.0%	10000.0%
5			0.5%	0.6%	5.0%	50.0%	100.0%	500.0%	5000.0%
1	1.67	5	0.1%	0.1%	1.0%	10.0%	20.0%	100.0%	1000.0%
0.5			0.1%	0.1%	0.5%	5.0%	10.0%	50.0%	500.0%
0.1			0.0%	0.0%	0.1%	1.0%	2.0%	10.0%	100.0%
0.05			0.0%	0.0%	0.1%	0.5%	1.0%	5.0%	50.0%
0.002	2.00	6	0.0%	0.0%	0.0%	0.0%	0.0%	0.2%	2.0%
0.001			0.0%	0.0%	0.0%	0.0%	0.0%	0.1%	1.0%

Two scenarios to consider:

1. Defect rate too high, therefore all units have interconnect failures requiring rework or internal repair mechanism.
2. Defect rate 6 sigma or better, therefore unlikely to see failures at test.

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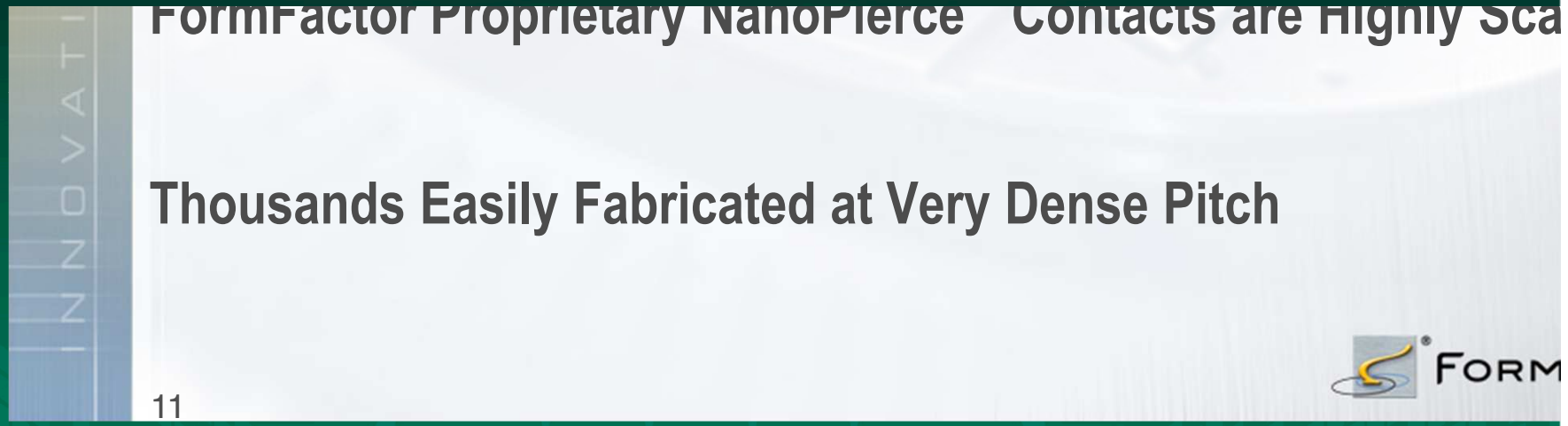
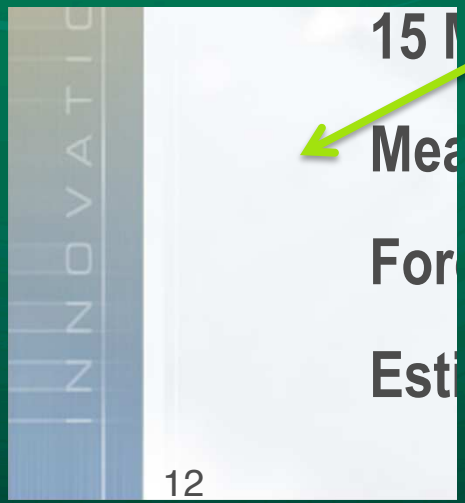
FormFactor: NanoPierce Contact



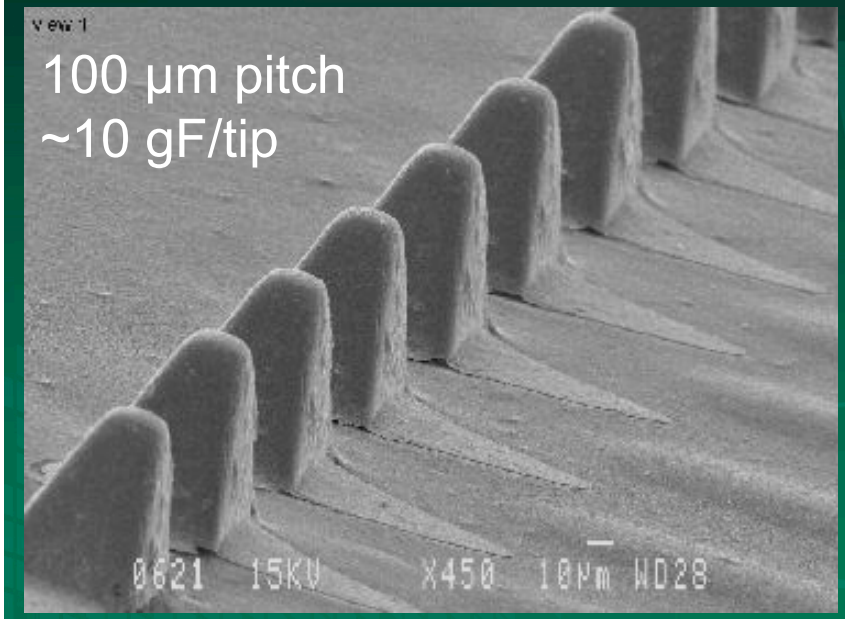
Metal "NanoFiber" contact element



Advantest: MEMS Probes

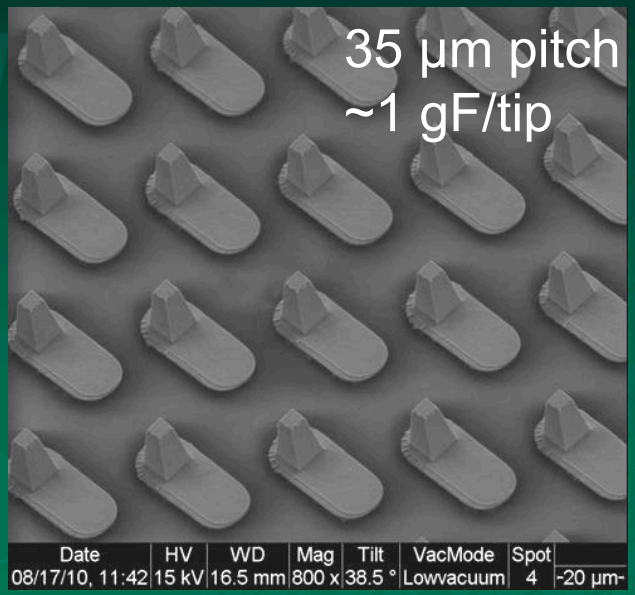
100 µm

Cascade Microtech: Lithographically Printed

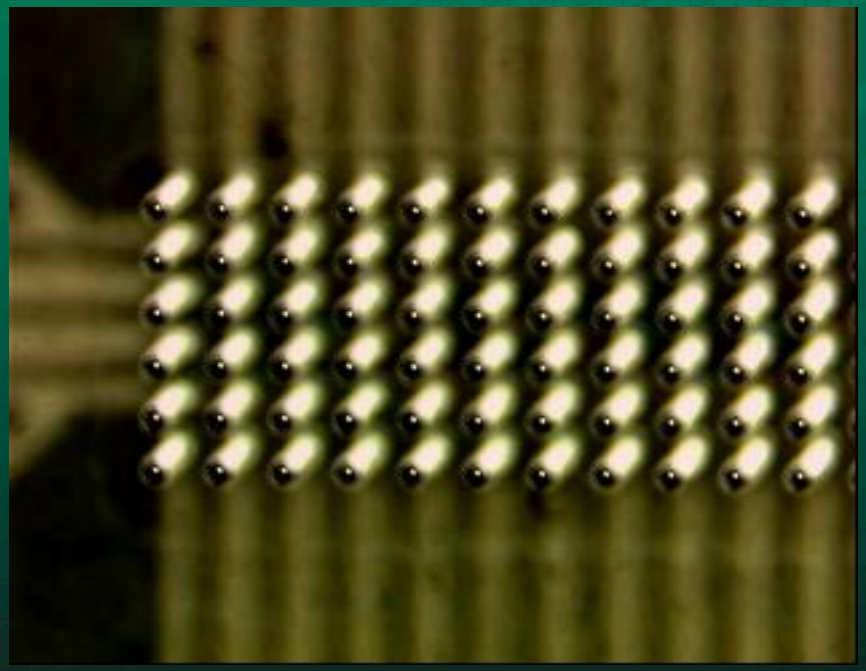


Scale by K

XYZ/K
Force/K²



Fully-routed 6 x 50 array at 40 x 50 µm pitch
New space transformer technology



"Probing Strategies for Through-Silicon Stacking", Eric Strid, et. al, 3D Test Workshop 2011

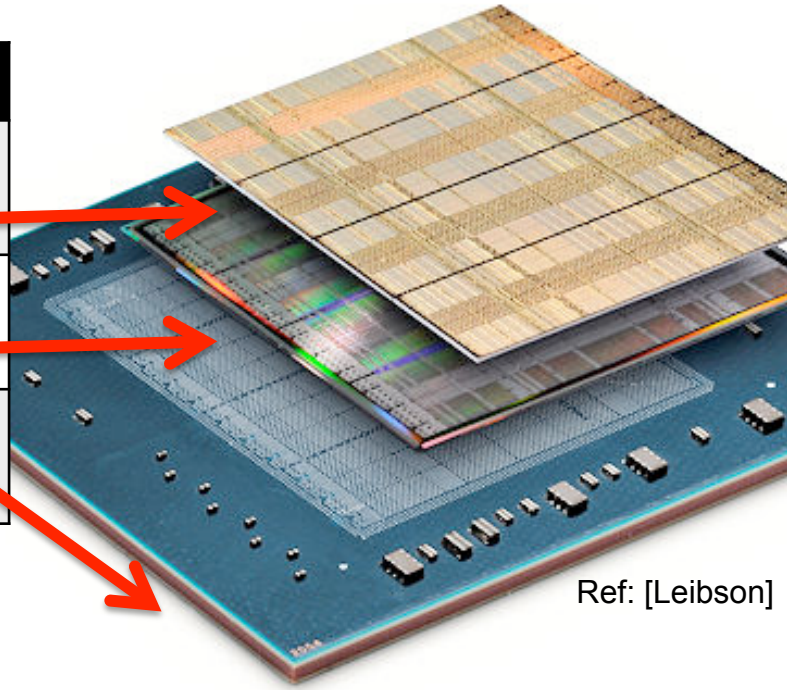
Many Challenges

- **Contact Technology**
  - Force & damage
- **Probe Card Signal Routing**
- **Tester Resources**
- **Power Delivery**
  - At speed & DFT
- **Weak IO Drive Current**

Ref: [Smith2012]

Signal Density Pyramid

Level	Connections	Pitch	Density
Microbumps Die to Substrate	200,000	40 µm	260 / mm^2
C4 Die to Package	24,000	180 µm	31 / mm^2
BGA Package to PCB	1,760	1 mm	1 / mm^2



Ref: [Leibson]

Typical Probe Card Signal Density

Level	Connections	Pitch	Density
Tester to PCB	20,000	~ .8 – 2.54 mm	.16 – 1.6 / mm^2
PCB to Space Transformer	> 20,000	~ .8+ mm (PTH)*	1.6 / mm^2
Space Transformer to ?	> 20,000	90 ~ 180 µm	31 ~ 123 / mm^2
? Interposer ?		90 µm → 40 µm	
Probe Contactor ? to Die	50,000	40 µm	260 / mm^2
Microbumps Die to Substrate	200,000	40 µm	260 / mm^2

* 0.25 mm fan-out possible but with selective lamination / advanced fab technology to achieve typical ATE board thickness. However, not likely for full array due to signal count.

Ref: [Feldman2011]

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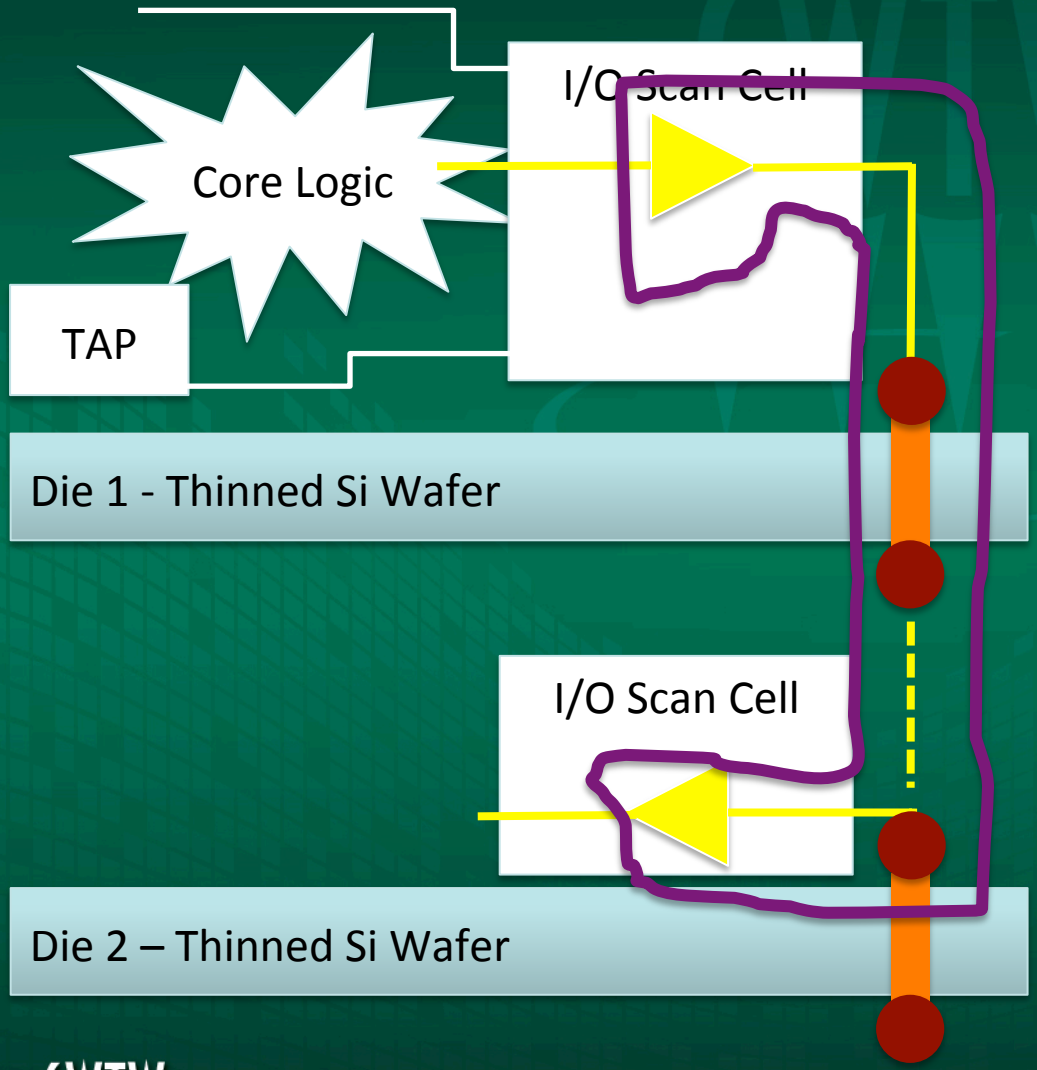
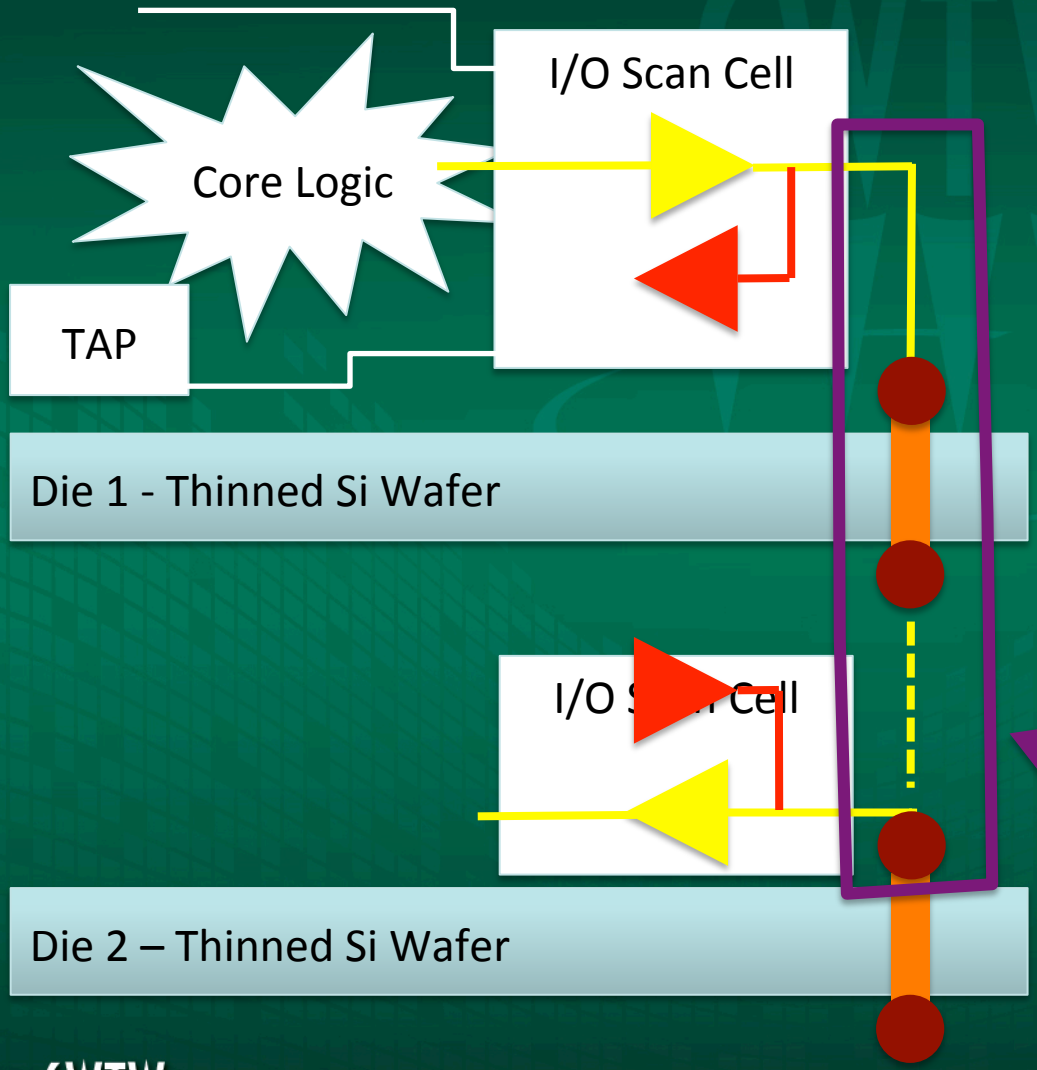
Outside of Wafer DFT Coverage



Inter-die connectivity (final driver, receiver, and interconnect) not tested during DFT wafer level probe.

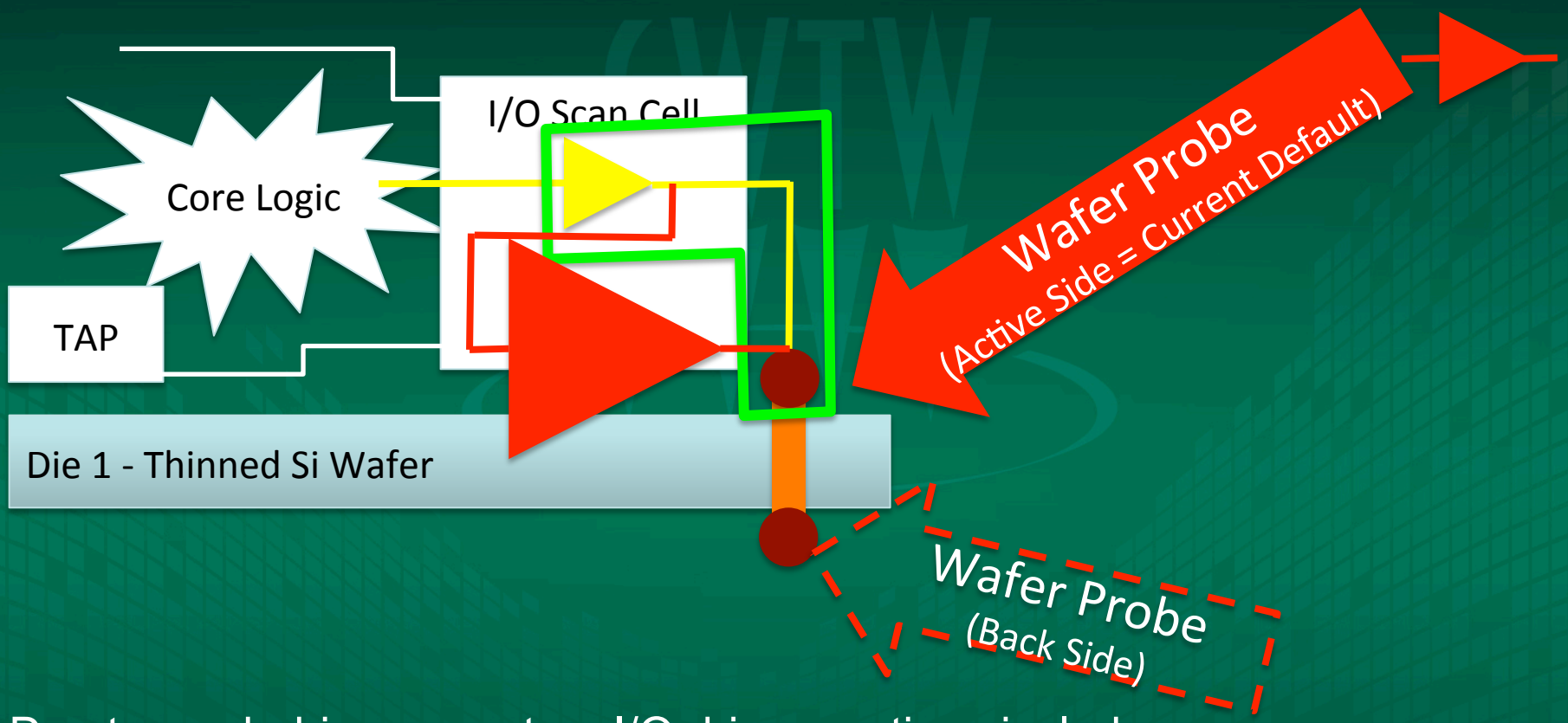
Improved DFT Coverage



Add “feedback” structures to boundary scan cell to check drivers and receivers at wafer level to increase coverage.

Not Covered at DFT wafer level test

Signal Probing @ Wafer Coverage



Due to weak drive current on I/O drivers options include:

1. Add “non-mission mode” high current transistor to drive signal to ATE
2. Add amplification to probe card as close to contact as possible
3. Use drive into load as “signature”

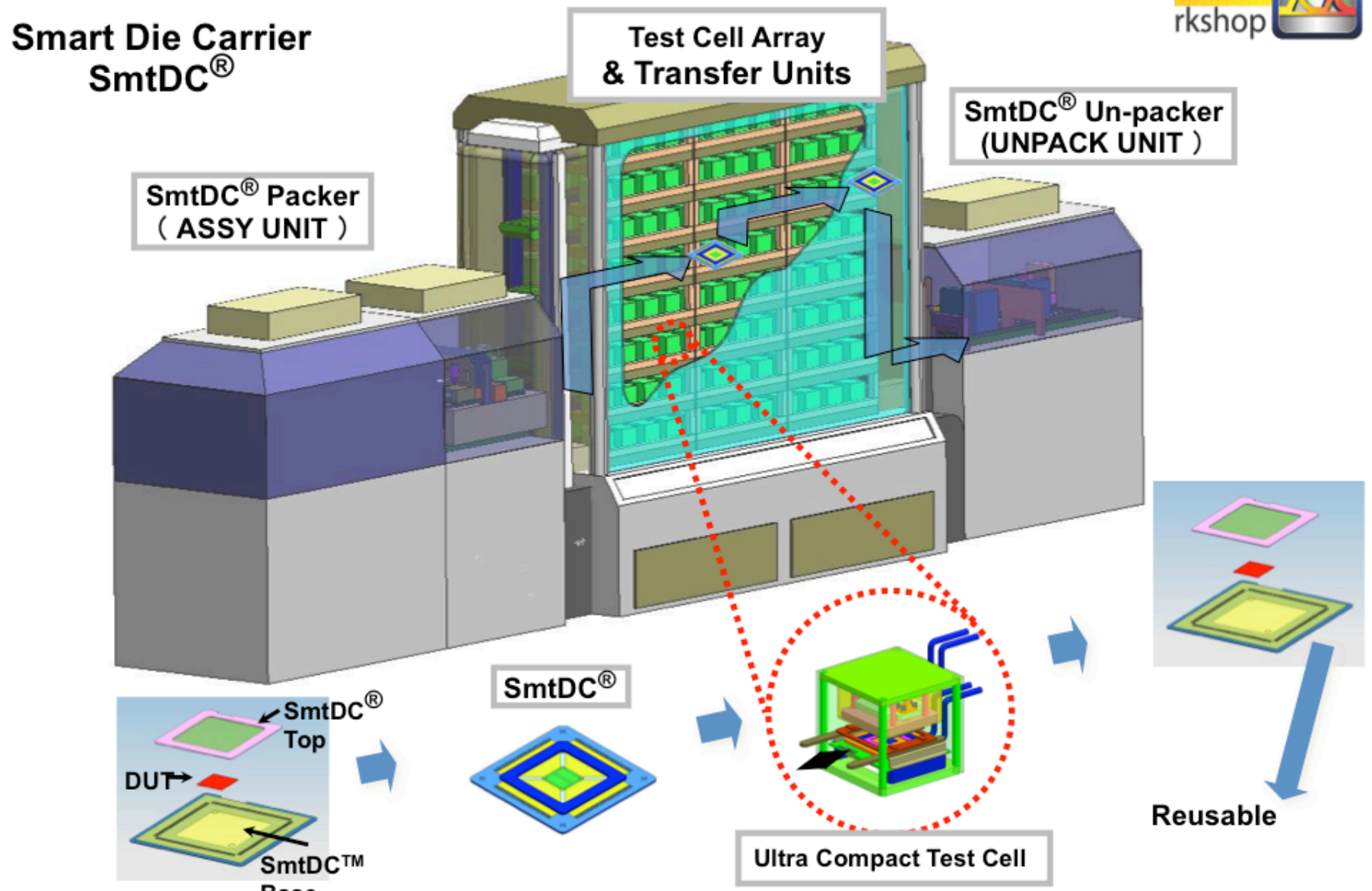
Microbump Probe Avoidance?

Examples:

- **Wide I/O like DRAM**
  - No BIST
  - Test compression & added test pads
- **Si Interposer**
  - Optical inspection
  - Indirect test

Yield loss due to microbump damage concerns?

HVM Stacked Devices




“Known Good/Device”
“Not Known Bad Device”

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It Depends…

3D Stacked Die Test

- **Is Not**
  - Universal tool to use everywhere in die flow
  - Possible for all design technology
  - Done “after design release”
  - Inexpensive
- **~~Is~~ May Be**
  - Needed based upon yield
  - Cost effective

Test Engineers & Managers

- **Need to engage early for DFx – die & system**
  - DFT coverage
  - Special drive and scan cells?
  - Repair / rework mechanisms
  - Test strategies
- **Become experts in cost models**
  - Failure modes estimated
  - ROI analysis on all test activities
  - Continuous process monitoring & improvements

"In God we trust; all others must bring data."

(incorrectly?) attributed to:

W. Edwards Deming & Robert W. Hayden

http://en.wikipedia.org/wiki/W._Edwards_Deming

Acknowledgments

- Colleagues from the International Technology Roadmap for Semiconductors (ITRS)
- Advantest
- Cascade Microtech
- FormFactor
- Teradyne

References #1

- Ben Eldridge (FormFactor). "Challenges and Solutions for Testing of TSV and MicroBump Devices by Direct Connection", IEEE 3D Test Workshop 2011.
- Ira Feldman (Feldman Engineering Corp). "Probe Card Cost Drivers from Architecture to Zero Defects", IEEE Semiconductor Wafer Test Workshop (SWTW) June 2011.
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References #2

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- Liam Madden (Xilinx). "Heterogeneous 3-D stacking, can we have the best of both (technology) worlds" International Symposium on Physical Design, March 25, 2013.
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Thank You!

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