

# IEEE SW Test Workshop

#### Semiconductor Wafer Test Workshop

June 9 - 12, 2013 | San Diego, California

#### Small contacts, high currents, short pulses



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#### **Problem**

- Device pad sizes and pitch decrease
- Device voltages decrease
- Device power decreases
- But ......
  - p=v\*i, so if v decreases and p were to remain constant, i must increase
  - Under the assumption that contact cross section decreases roughly quadratically with pitch dimensions it follows that current handling will also decrease similarly
  - Device current decrease does not generally follow this trend



#### **Objective**

- Provide insight into contact behavior
  - At DC
  - Under short pulse loading (single pulse)
- Point out potential design improvements
- Explore impact of power delivery network

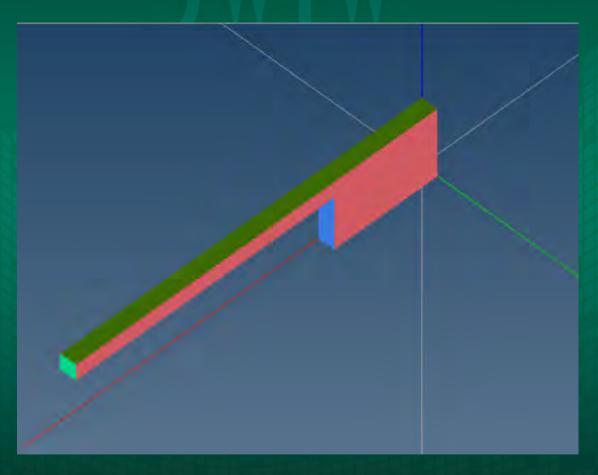


#### **Approach**

- Examine contact thermal response via coupled electrical-thermal simulation
- Select a specific short pulse condition (electrical pulse length = 10% of thermal time constant) since longer pulses approach DC behavior



## Geometry

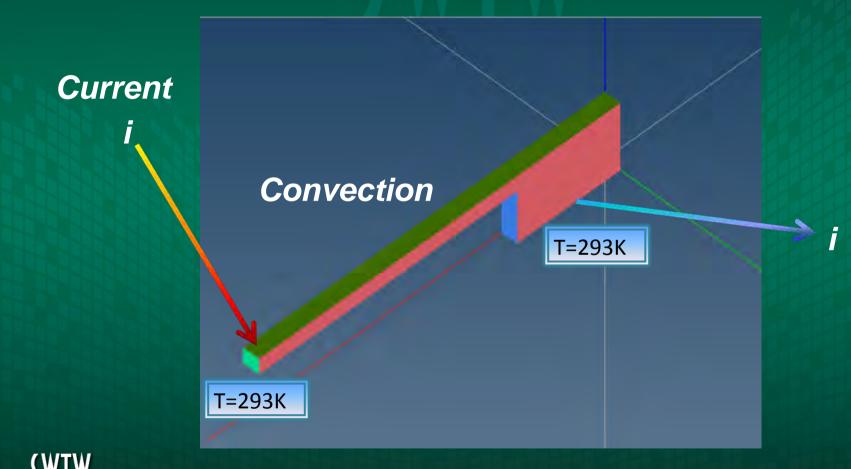




Generic probe

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# **Boundary conditions**





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#### Temperature dependence

R=Ro\*(1+alpha\*(T-To))

ki=k300\*(Ti/300)^alpha\*T

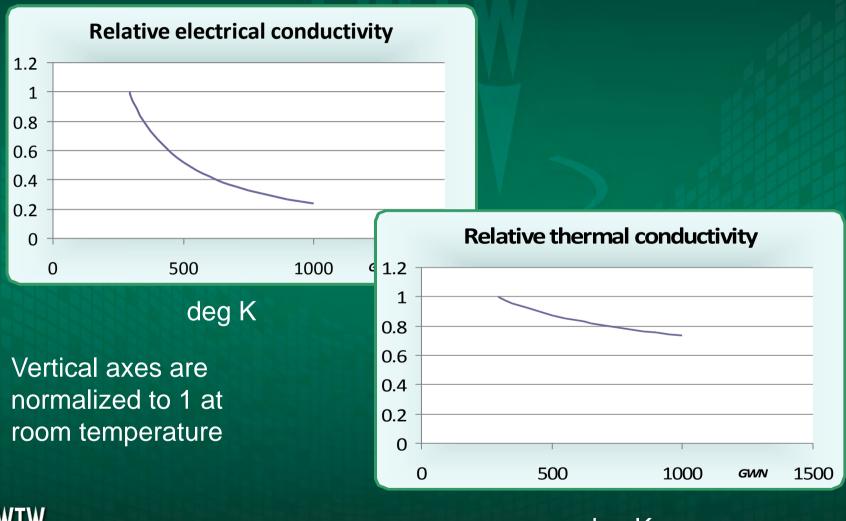
Source: Wikipedia

There are many different ways to describe temperature dependence of thermal and electrical resistance.

In general, resistance increases with increasing temperature.



## Temperature dependence



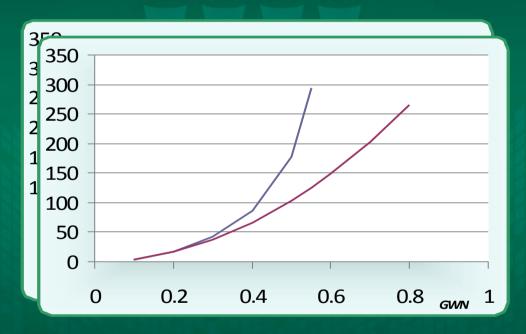


deg K

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#### Constant vs. T-dependent properties



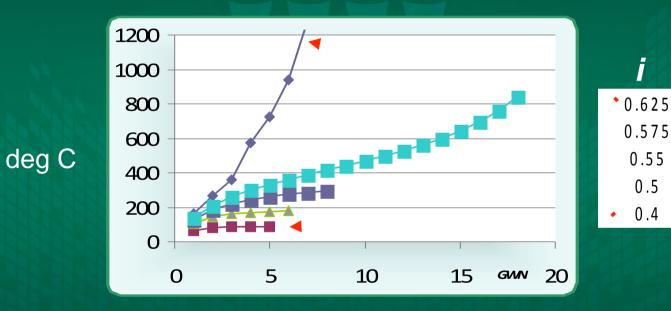


current

Temperature dependent materials properties must be included in model



#### Temperature rise, DC



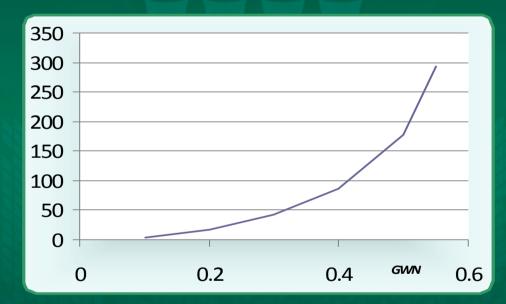
Number of iterations in model

Temperature dependent materials properties necessitate a sufficient number of iterations in the model



## Temperature rise Tr, DC





Current



#### Pulse current parameters

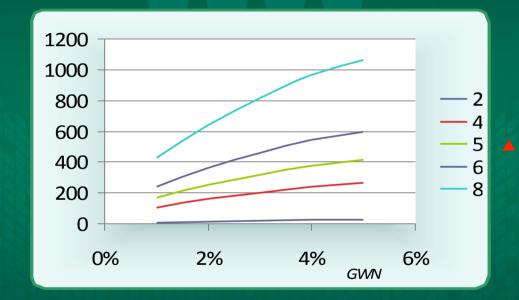
- Pulse length vs. Time constant
- Duty cycle
  - In a linear system with constant conductivities the energy delivered to a contact increases linearly with duty cycle as well as with pulse length
  - This does not hold true for temperature dependent parameters



#### Pulse length, Tr=f(%)

Single pulse





Pulse length [% of thermal time constant]

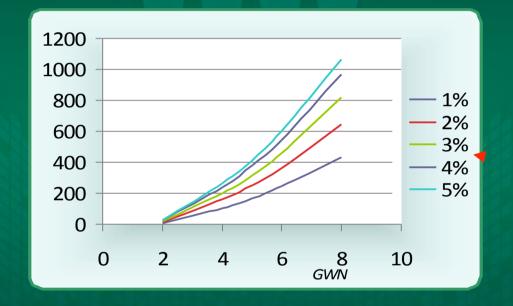
Temperature rise does not increase linearly with pulse length as current levels increase



#### Pulse length, Tr=f(i)

Single pulse

deg C



Pulse length in % of thermal time constant

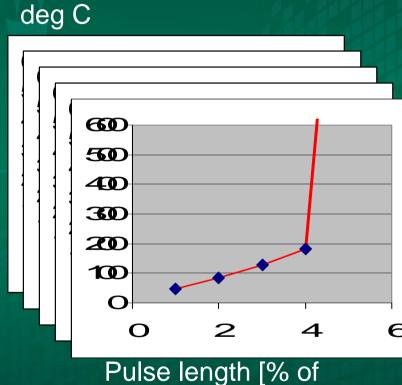
Current

Temperature rise does not increase linearly with pulse length as current levels increase



#### Temperature distribution

Visualization of temperature rise during pulse loading



Pulse length [% of thermal time constant]

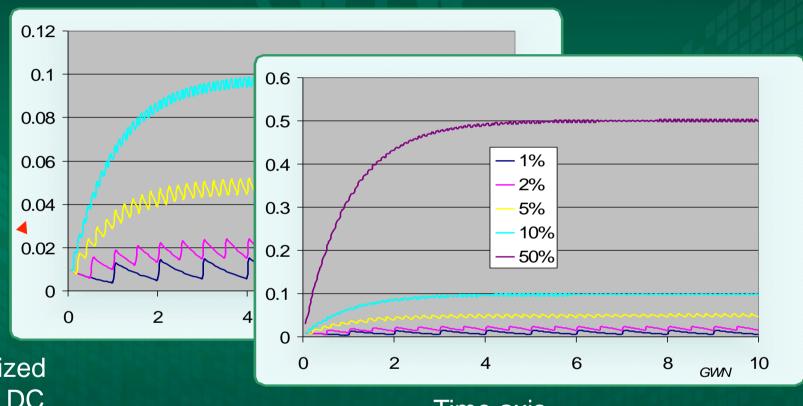
Color gradient is normalized to maximum temperature in each individual image

SMIM THTT

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#### **Duty cycle dependence of Tr**

Pulse length = 10% of thermal time constant



Normalized to peak DC temperature

Time axis



Temperature as a function of time\*

(\*linear electrical model)

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#### **Material options**

# Improvements should be available from engineered materials:

- Higher melting point of materials at hot spot
- Less dependence of electrical resistance R(T)
- Lower temperature coefficient of thermal conductivity
- Layered structure with temperature insensitive materials



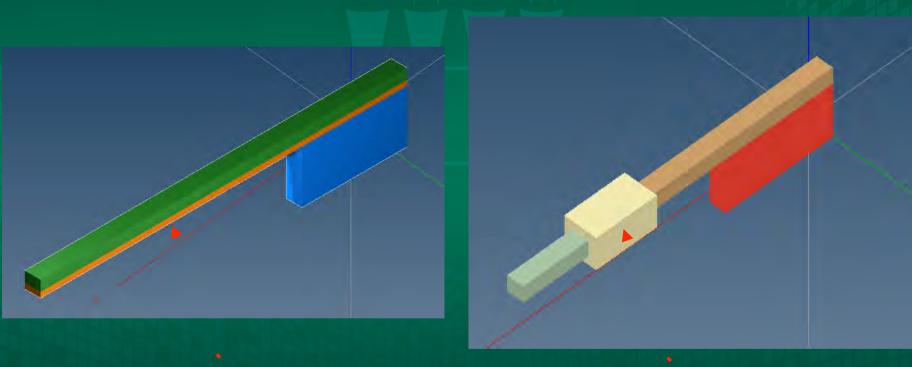
## **Design options**

Improvements should be available from geometry:

- Forced (air) cooling
- Better heat sinking at ends, in particular tip
- Shorter contacts
- More bulk at hot spot



# **Examples**



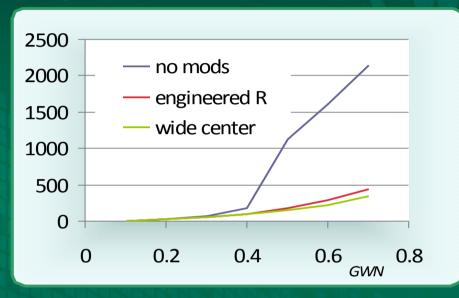


More bulk at hot spot

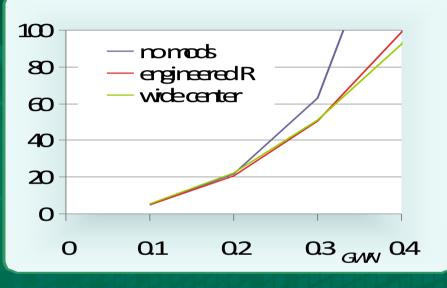


#### Temperature rise Tr, DC current

deg C



deg C



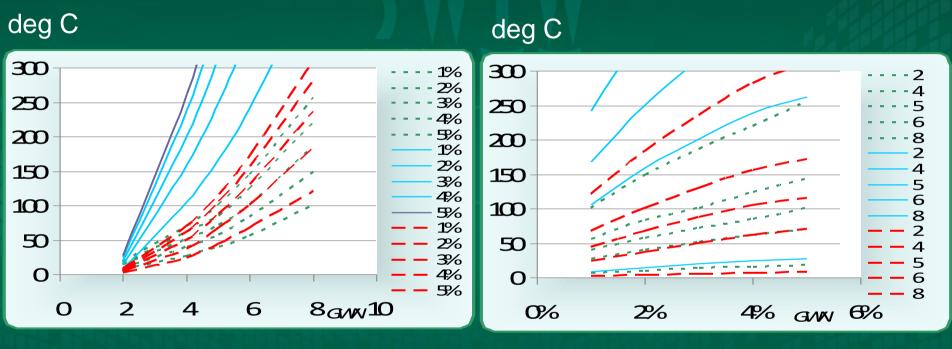
Current

Current



Shape as well as materials engineering can improve maximum DC current handling performance

## Temperature rise, pulse current



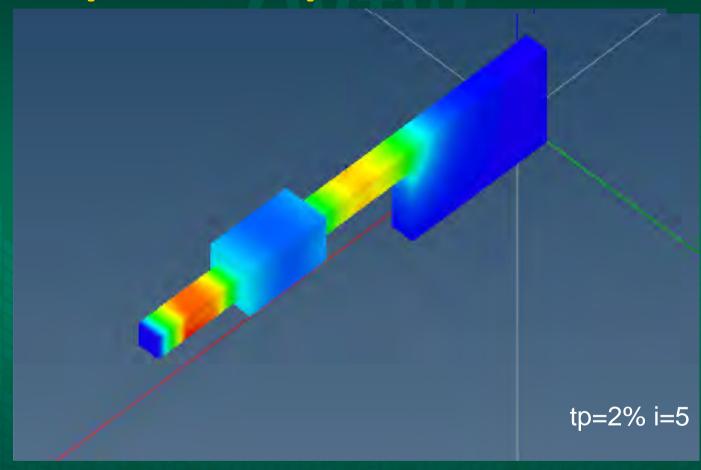
Current constant]

Pulse length [% of thermal time



Shape as well as materials engineering can improve performance especially for short, high current pulses

#### DC and pulse temperature distributions



The presence of additional mass delays heating up of the center portion

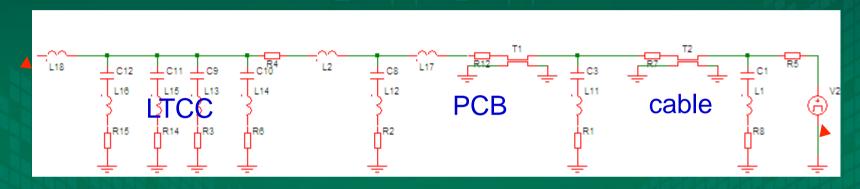


# What about the impact of ever improving power delivery networks?

- Low series resistance
- More capacitors near device under test (DUT)
- On-board regulators



## PDN schematic example

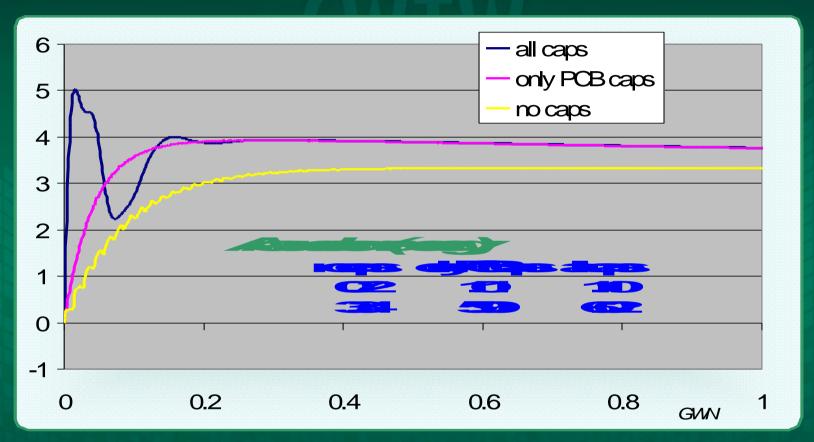


DUT

Simplified power delivery network equivalent circuit



#### **Current pulse from a short circuit at DUT**



Examples for a short circuit at DUT condition are 'hot' touchdown and device failure during test



#### Conclusions

- Contact material and shape can have a significant impact on pulse current handling capabilities.
- Simulations have to be set up and monitored very carefully in order not to overlook divergences
- Energy storage in bypass capacitors near the contacts does not appear to be a major concern

