IEEE SW Test Workshop
Semiconductor Wafer Test Workshop
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The Cost of Quality – Challenges of High-Volume Memory Wafer Test

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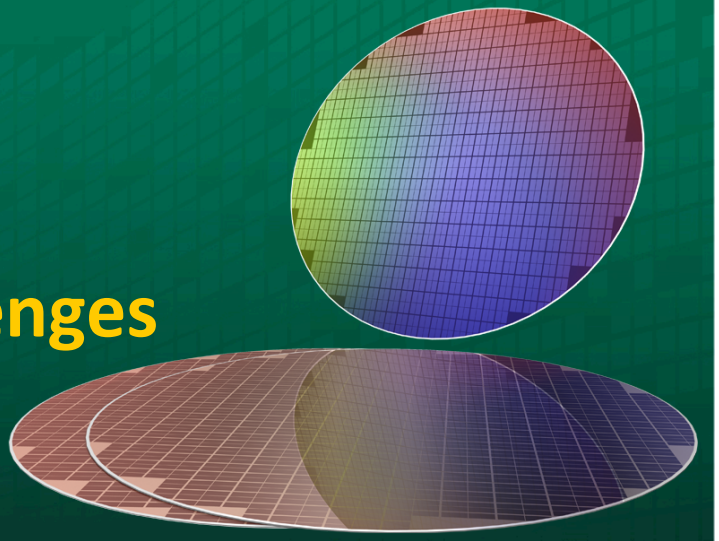
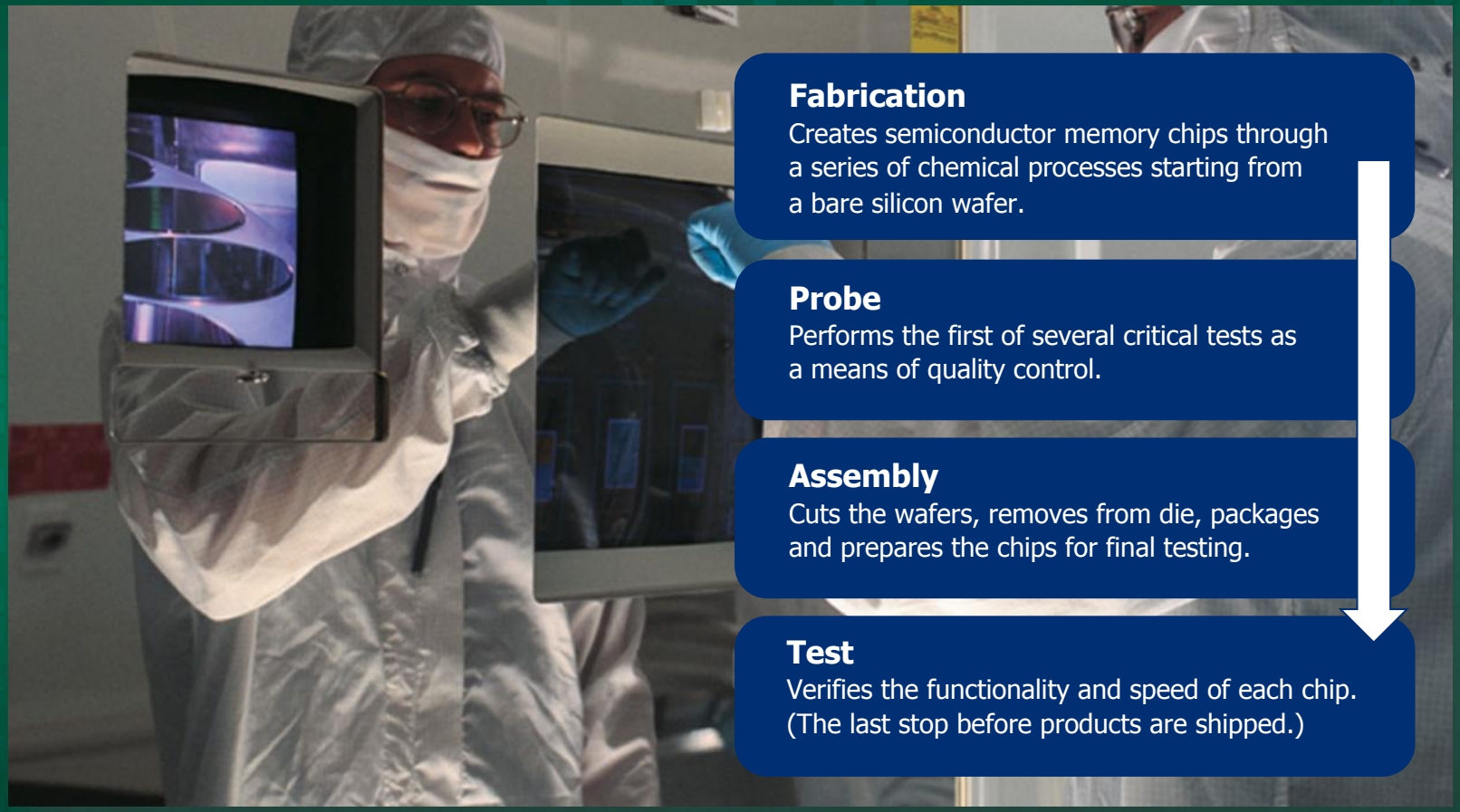
Agenda

- Basics: Making of a Micron Memory Chip
- Product Portfolio and Industry Landscape
- Cost of Quality (Cost of Poor Quality)
- High-Frequency Wafer Test
- Bond Pad Damage
- Test Cell Stacking Tolerances
- Thermal Management
- Future Memory Product Challenges
- Conclusions



Basics: The Making of a Micron Memory Chip



Fabrication
Creates semiconductor memory chips through a series of chemical processes starting from a bare silicon wafer.

Probe
Performs the first of several critical tests as a means of quality control.

Assembly
Cuts the wafers, removes from die, packages and prepares the chips for final testing.

Test
Verifies the functionality and speed of each chip. (The last stop before products are shipped.)

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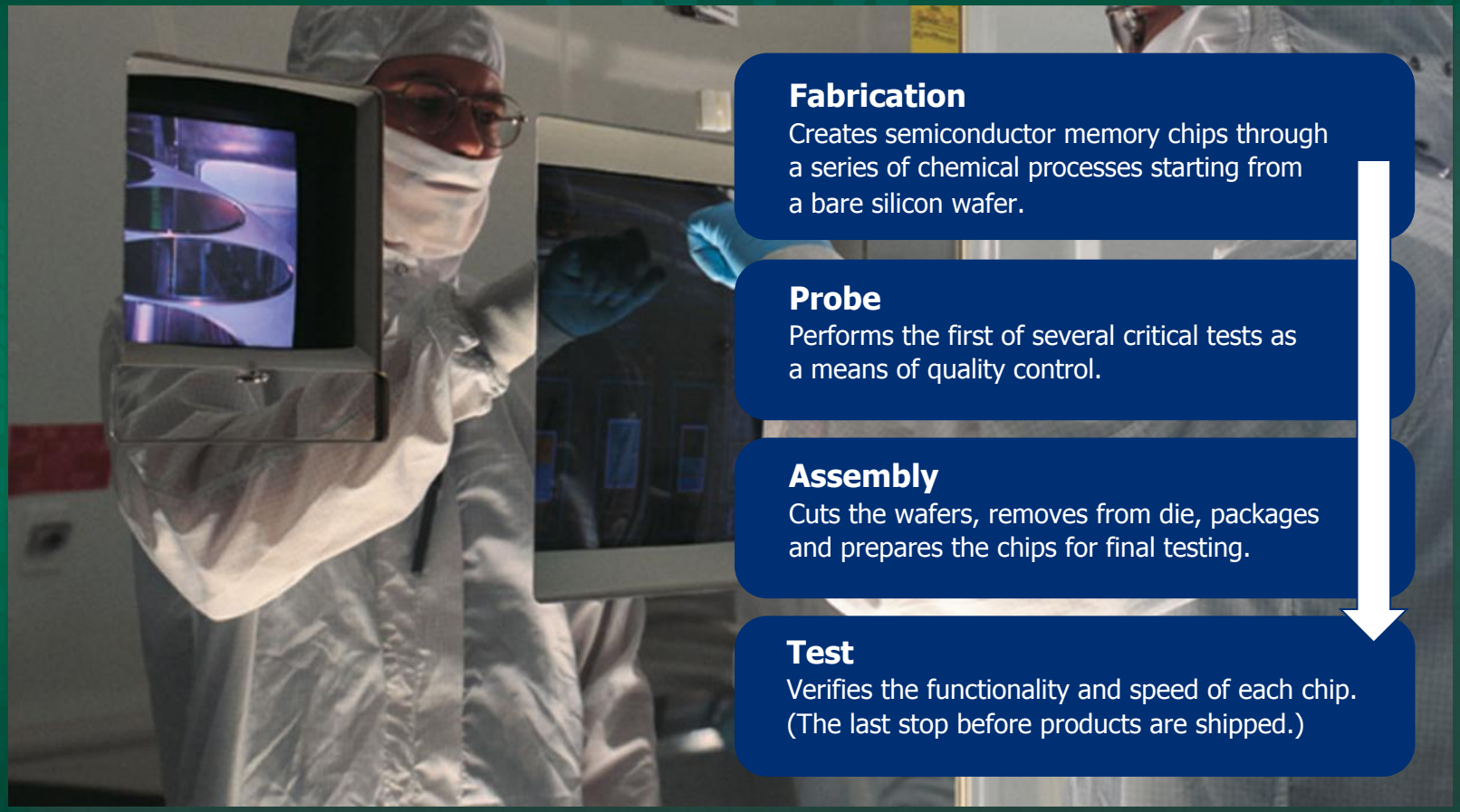

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In reality its not that simple

Diversifying Memory Markets

Automotive Storage Graphics/Consumer Networks





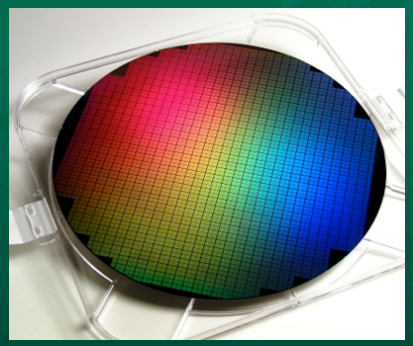


Server Mobile Personal Computing IMM

A New Industry Landscape

Equipment Suppliers[1]

Memory Producers[2]



Customers[1]

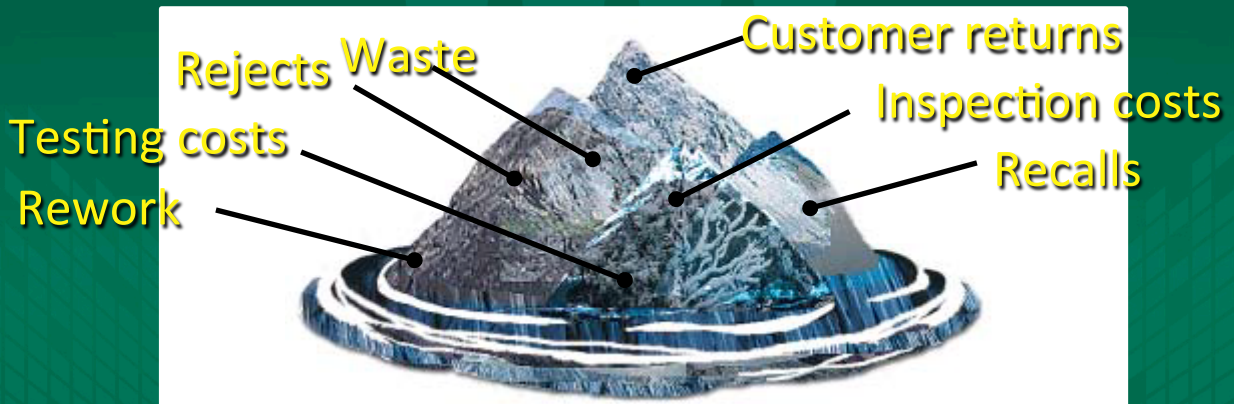
Source: Gartner, Micron Market Research Estimates

[1] Number of companies making up 60% or more of revenue

[2] Total memory producers

Traditional View of Quality Costs

- Initial quality costs typically include only the most visible factors, i.e. above the iceberg

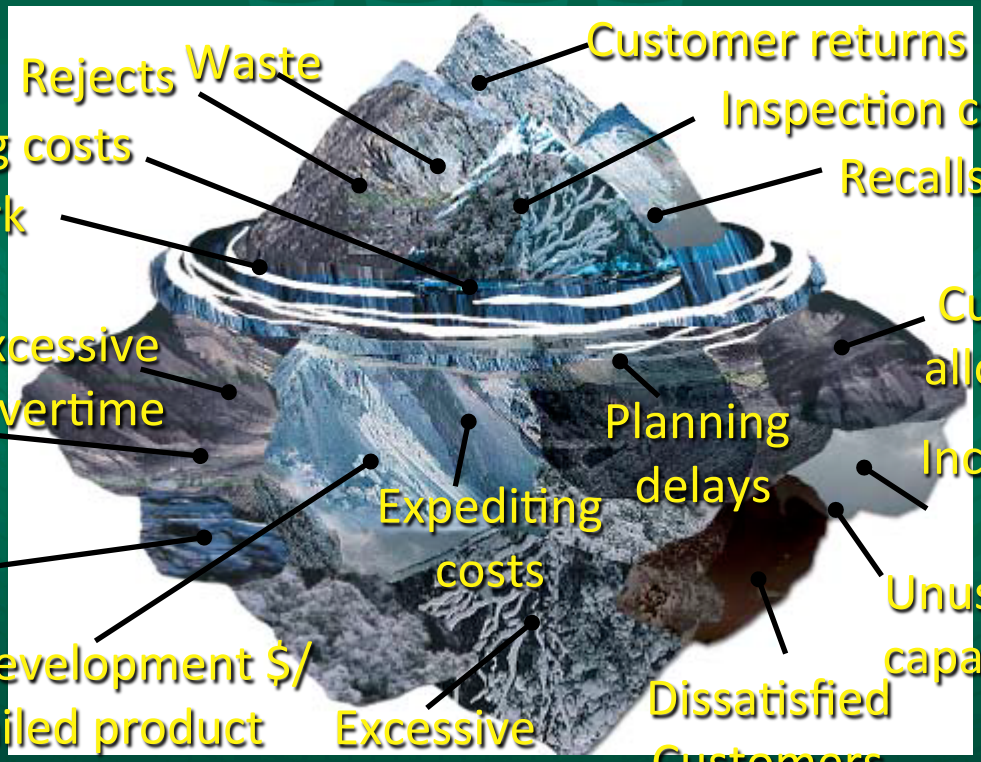


(4–5% of sales)

Reference: "The Tip of the Iceberg" by Joseph A. DeFeo, Quality Progress, May 2001

Cost of Poor Quality (COPQ)

- When gaining a broader definition of poor quality the hidden portions of the iceberg becomes apparent



COPQ ranges from 15−25% of total cost.

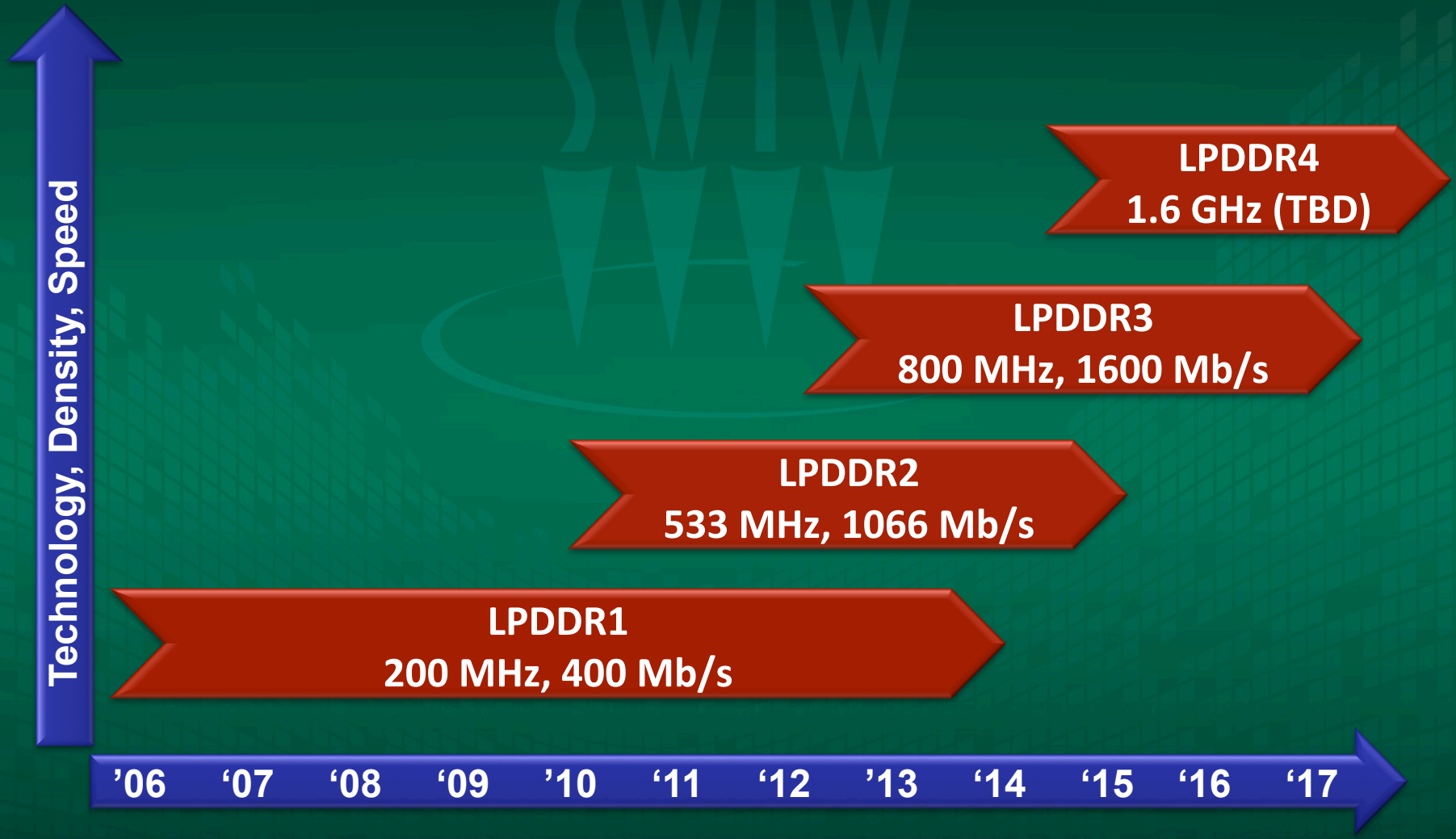
Reference: "The Tip of the Iceberg" by Joseph A. DeFeo, Quality Progress, May 2001

KGD, High-Frequency, High-Parallel DRAM Wafer Test

Typical Memory Test Flow

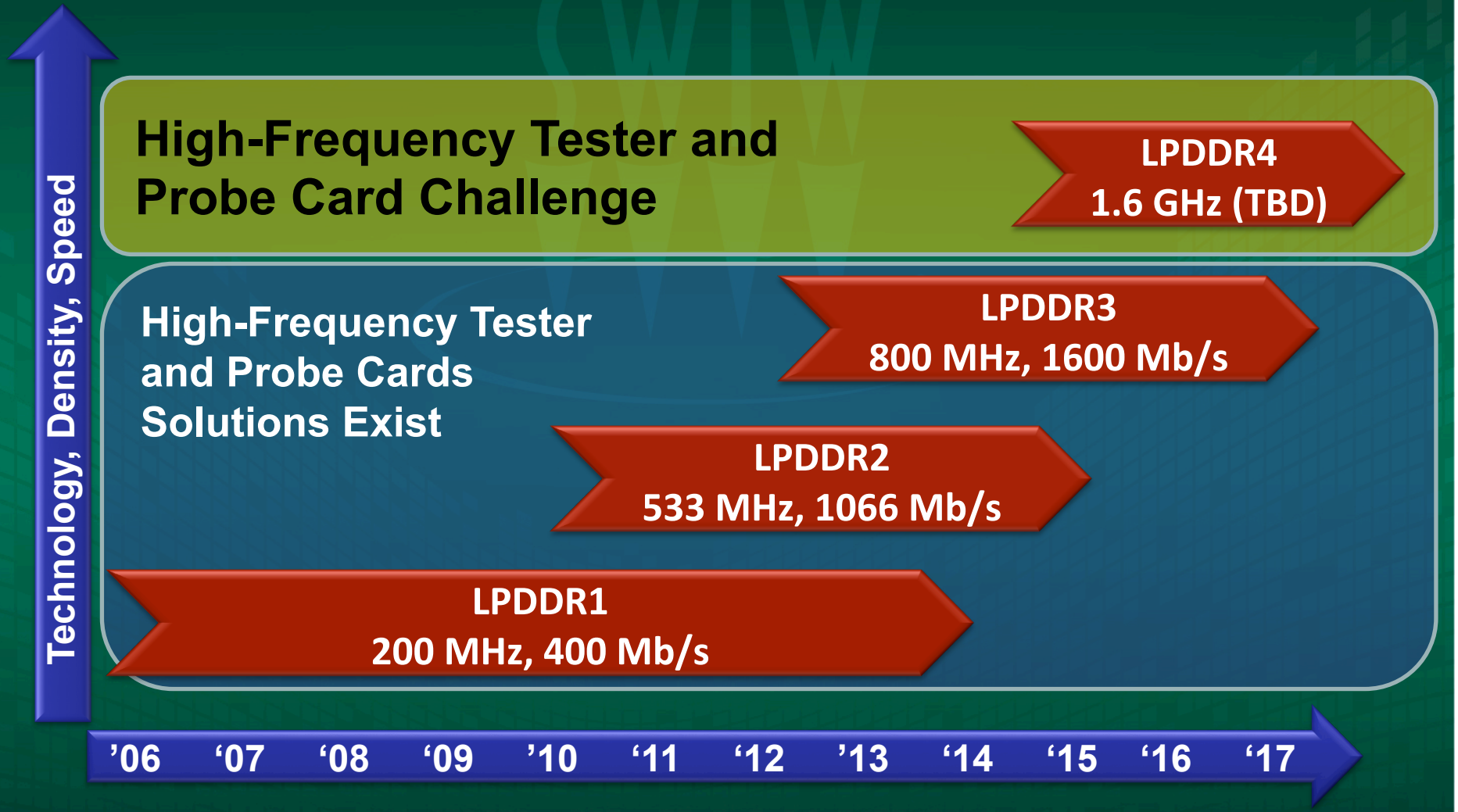
- **SORT**
  - Lower pin per DUT
  - High parallelism
  - Lower test frequency
  - Full wafer contact
  - Probe mark inspection
- **KGD**
  - Higher pin per DUT
  - Low parallelism
  - Higher test frequency
  - Increased probe mark quantity

Mobile LPDRAM Trend



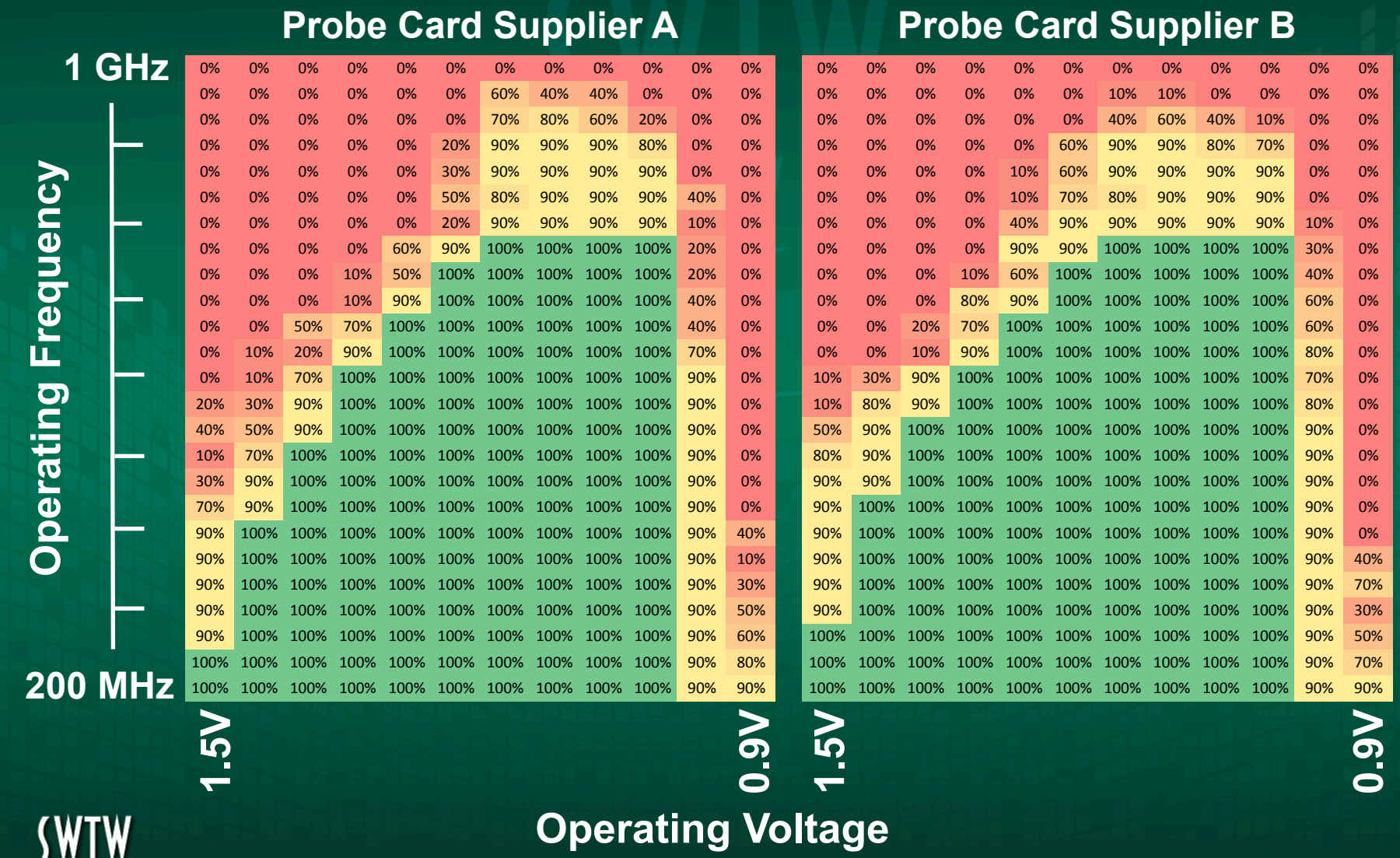
Source: JEDEC

Mobile LPDRAM Trend



Source: JEDEC

Operating Frequency vs. Voltage Shmoo



Probe Card Supplier A											
0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
0%	0%	0%	0%	0%	0%	60%	40%	40%	0%	0%	0%
0%	0%	0%	0%	0%	0%	70%	80%	60%	20%	0%	0%
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0%	0%	0%	0%	0%	50%	80%	90%	90%	90%	40%	0%
0%	0%	0%	0%	0%	20%	90%	90%	90%	90%	10%	0%
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100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	80%
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	90%

Probe Card Supplier B											
0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%	0%
0%	0%	0%	0%	0%	0%	10%	10%	0%	0%	0%	0%
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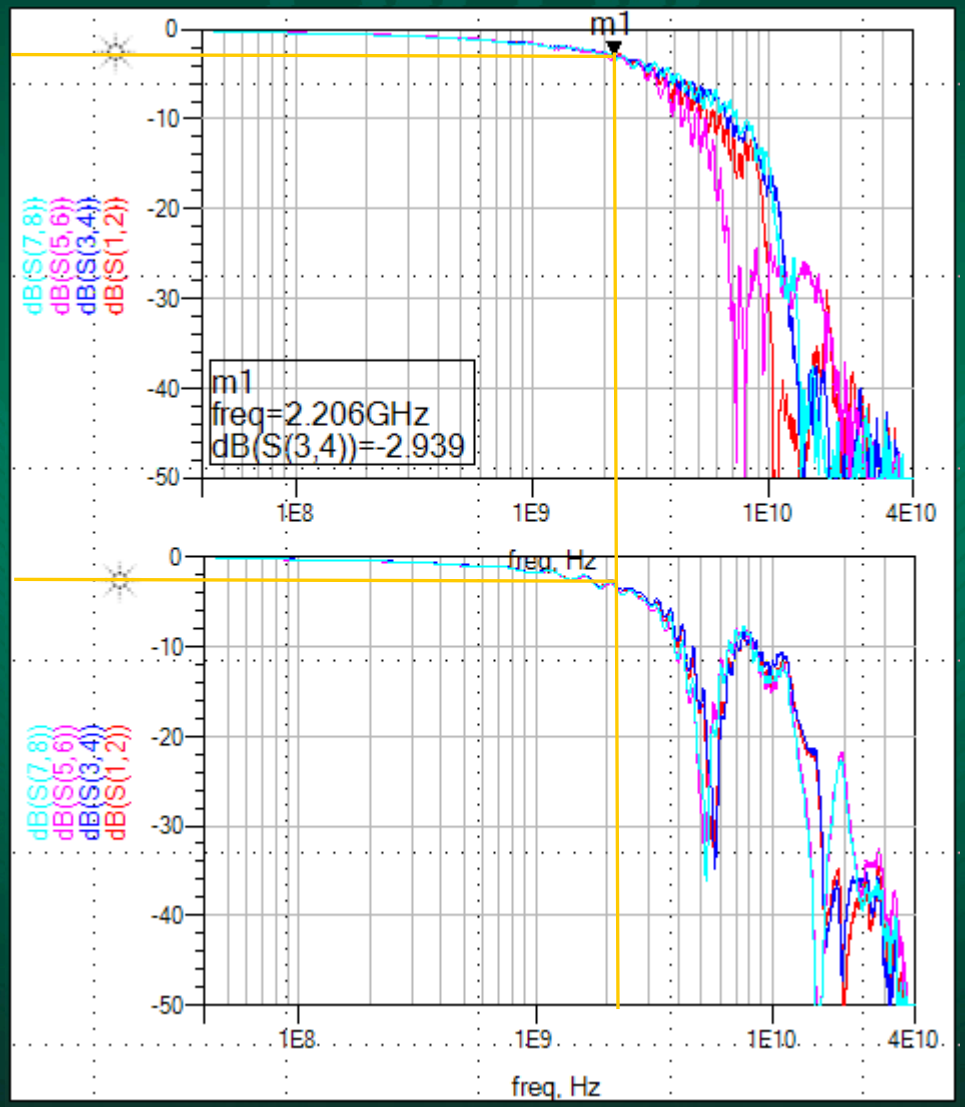
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	50%
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	70%
100%	100%	100%	100%	100%	100%	100%	100%	100%	100%	90%	90%

Insertion Loss 800MHz Probe Card

−3dB Bandwidth



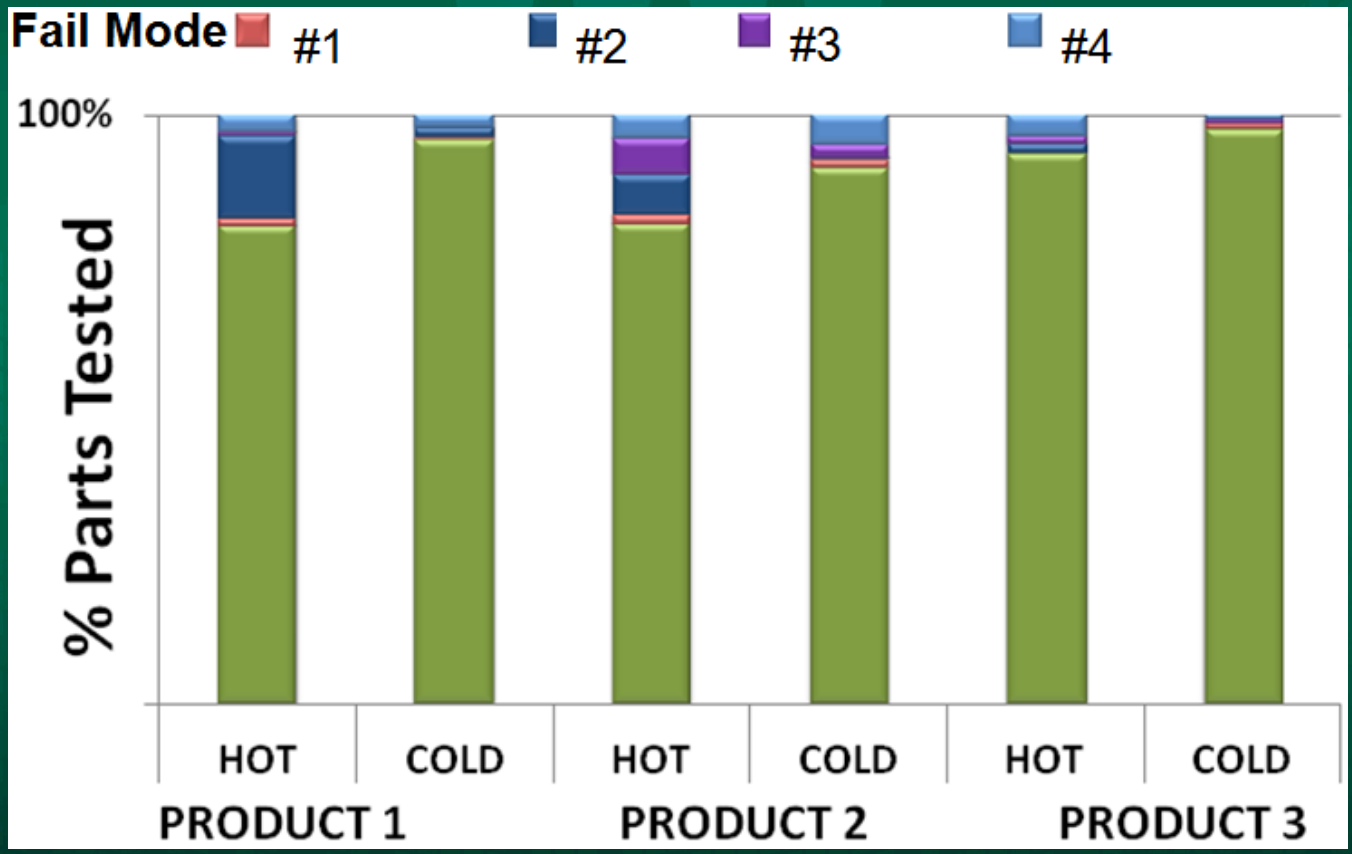
−3dB Bandwidth

Probe Card Supplier A

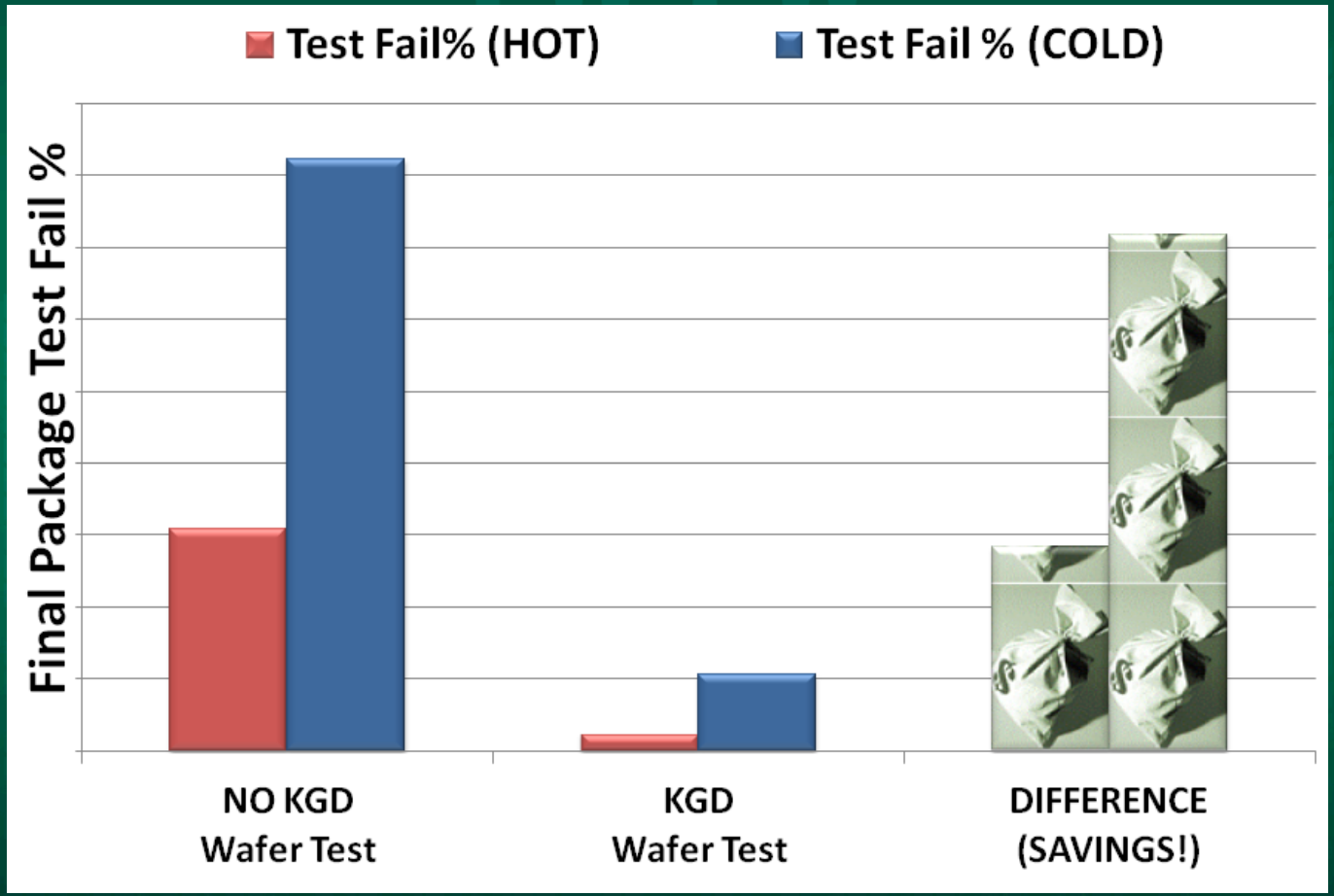
Probe Card Supplier B

KGD1 and KGD2 Wafer Test Fails

- Screening prior to packaging at max LPDDR2 frequency



The Cost of Not Implementing KGD Wafer Test



KGD High-Frequency Solutions

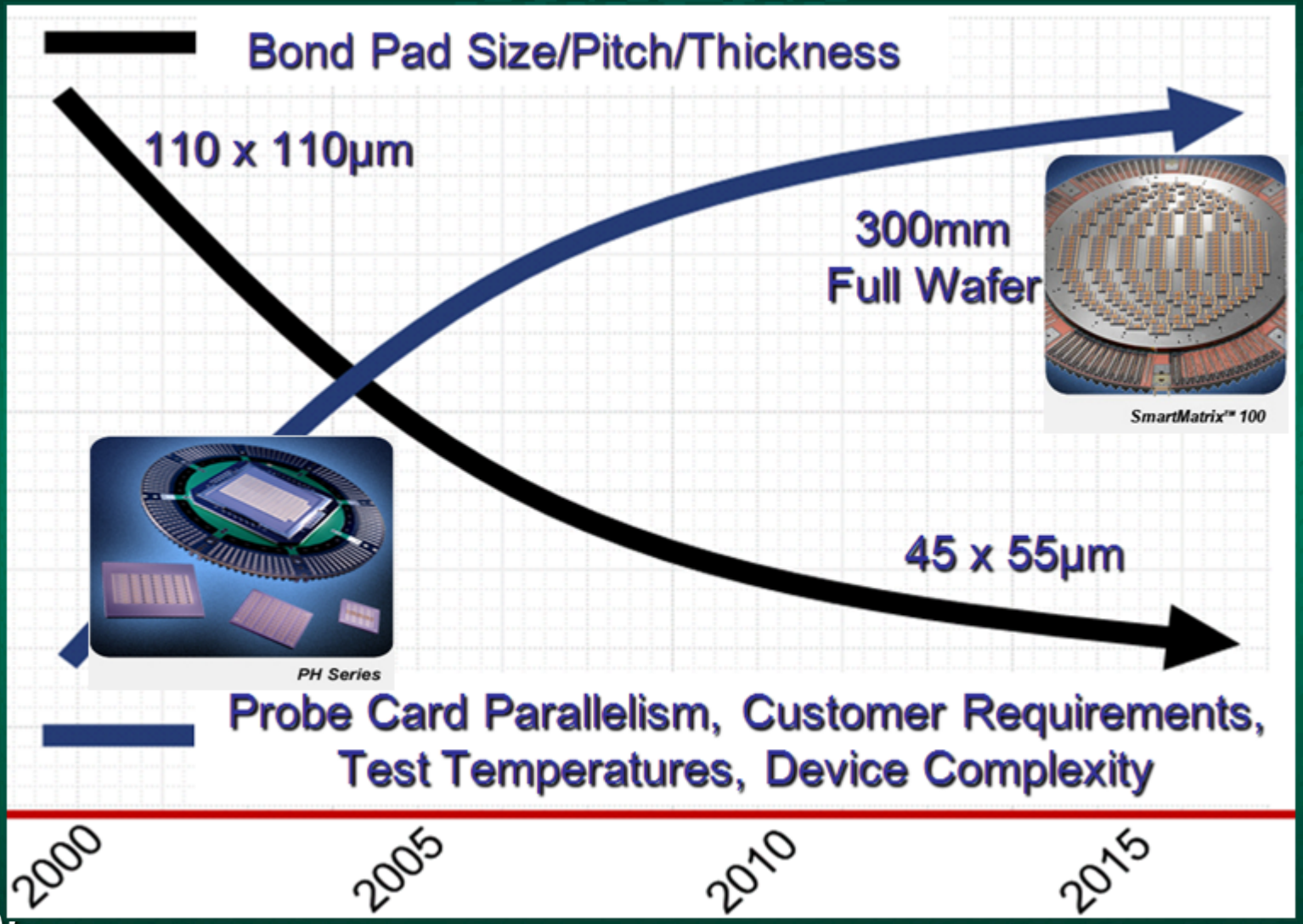
- **Existing tester solutions:**
  - 1.2 GHz (2.4Gbs) to 1.6GHz (3.2Gbs)
- **Existing probe card solutions:**
  - 800 MHz (1.6 Gbs)
  - Signal line bandwidth of >2 GHz @ –3dB
  - Signal line trace length matching of <100ps

What is Needed?

- High-frequency, high-parallelism solutions to enable LPDDR4 markets.

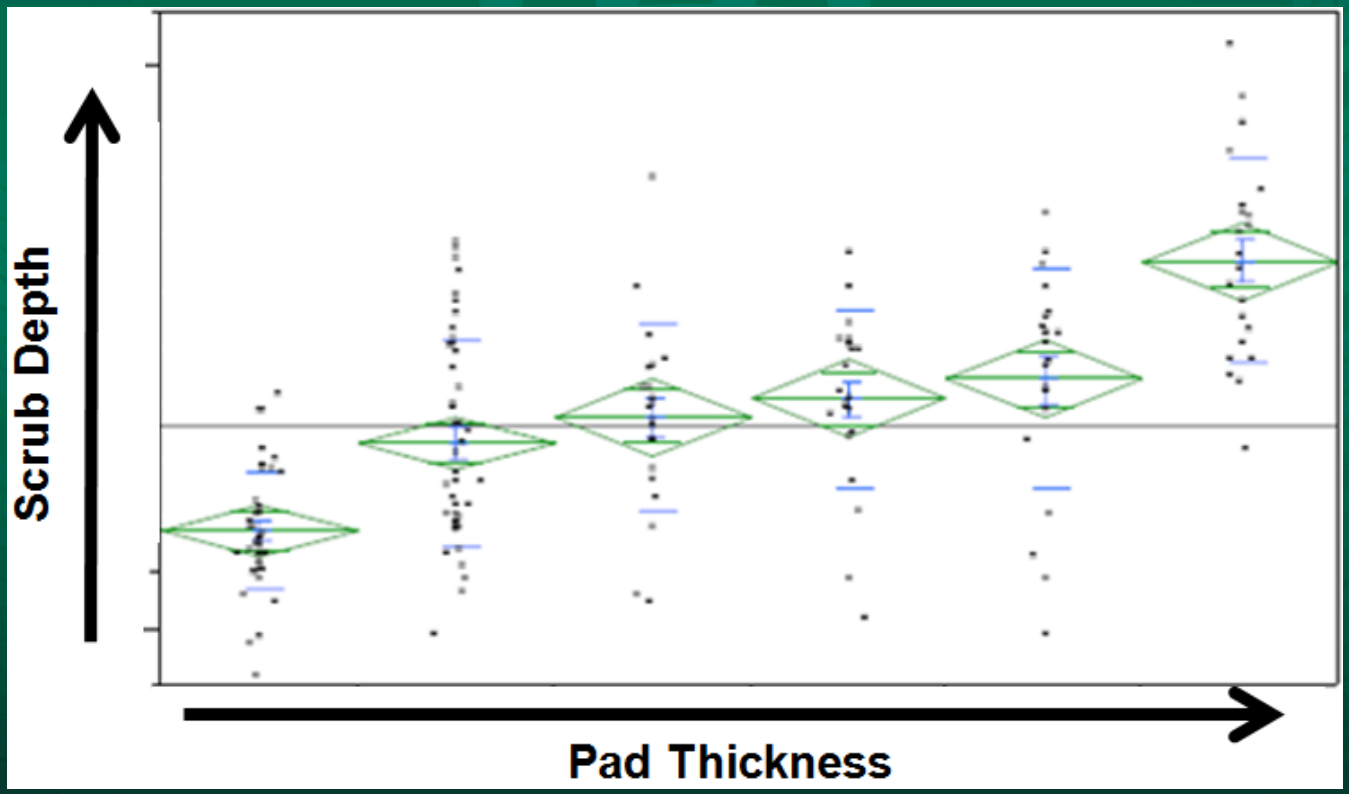
Bond Pad Damage and Scrub Mark Placement

Pad Size/Probe Card Complexity Trend



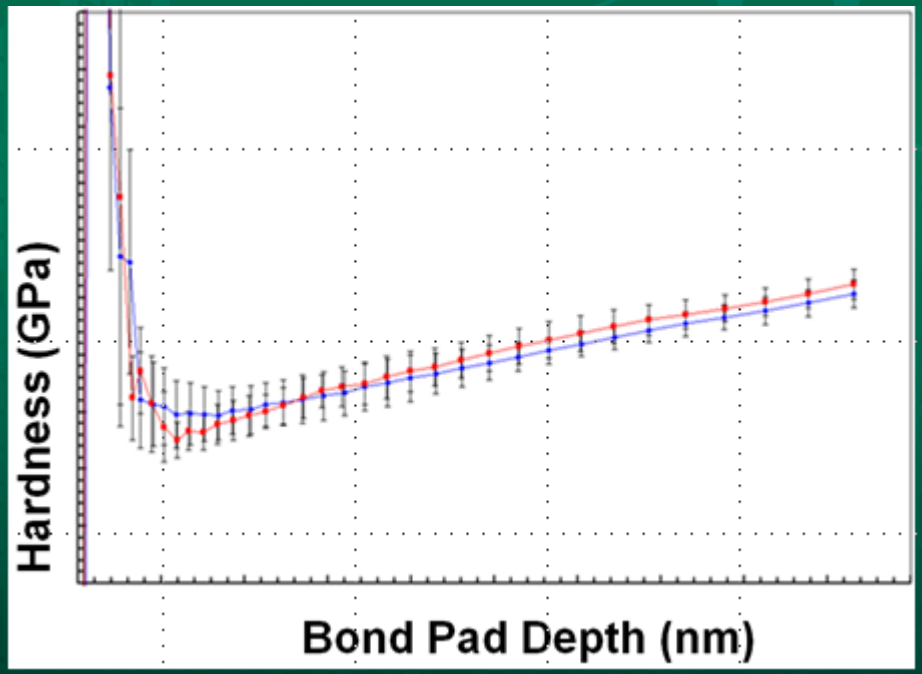
Effect of Metal Thickness

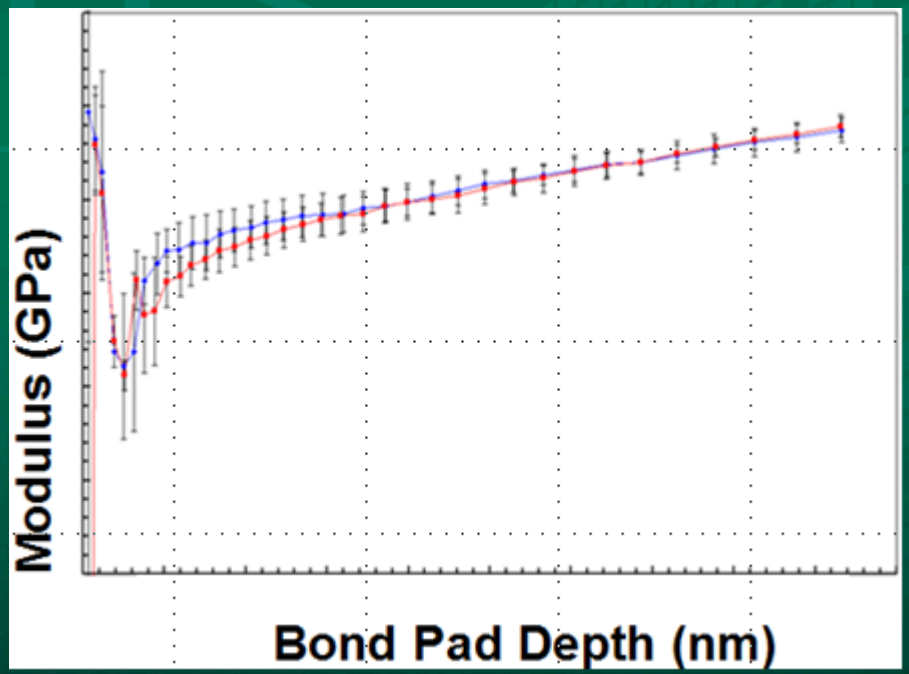
- Scrub depth increases as bond pad material increases
  - Termed **Substrate Effect**: increased metal hardness & modulus in closer proximity to the underlying substrate



Effect of Metal Thickness (cont.)

- Quantifying **Substrate Effect** : measured hardness and modulus of bond pad using nanoindentation
  - **Hardness & modulus increase with measurement tool surface displacement**





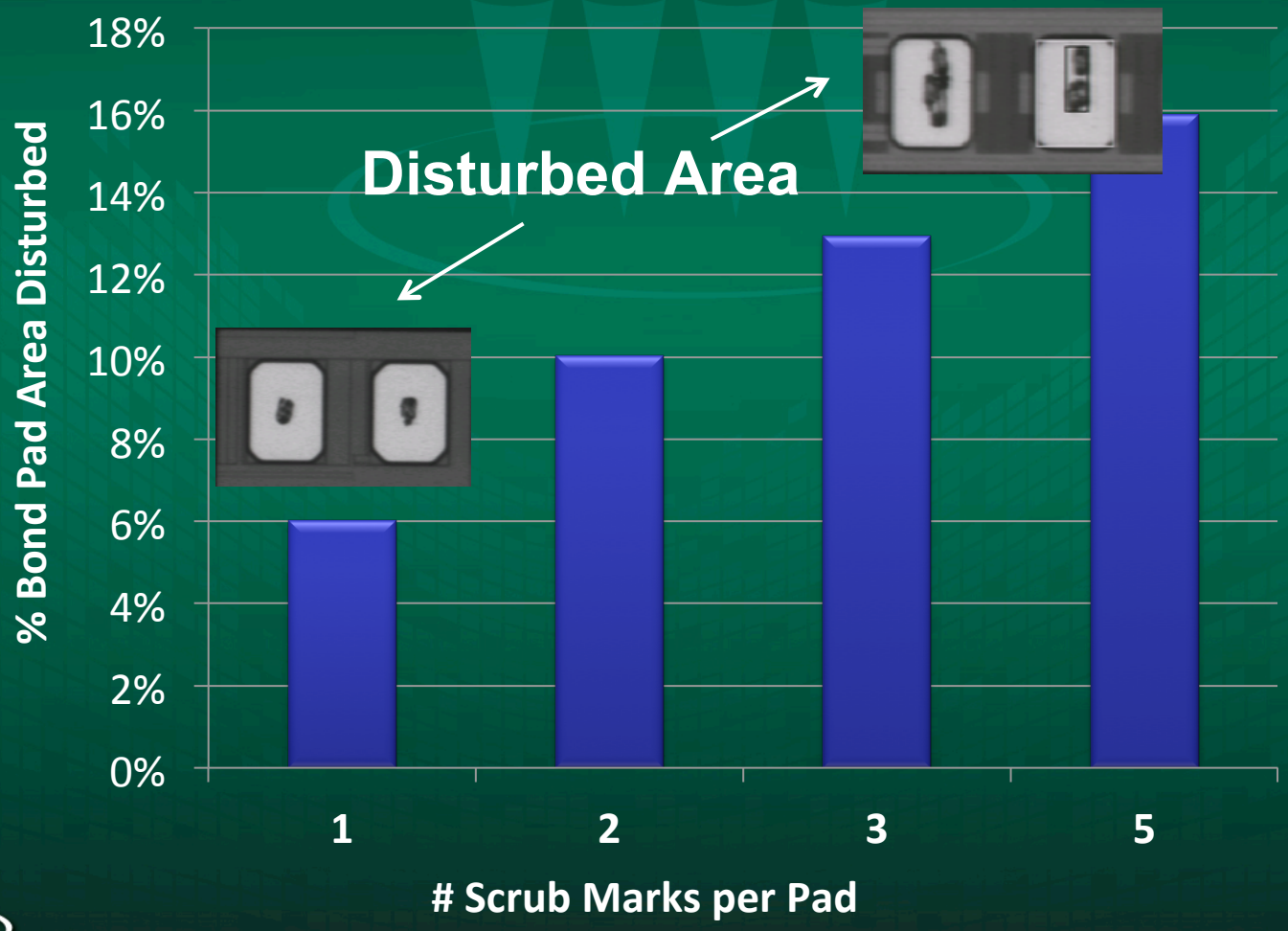
Bond Pad Damage

- **Assembly and customer needs:**
  - No punch through
  - Disturbed area <25% of pad area
  - Limit on maximum number of touchdowns

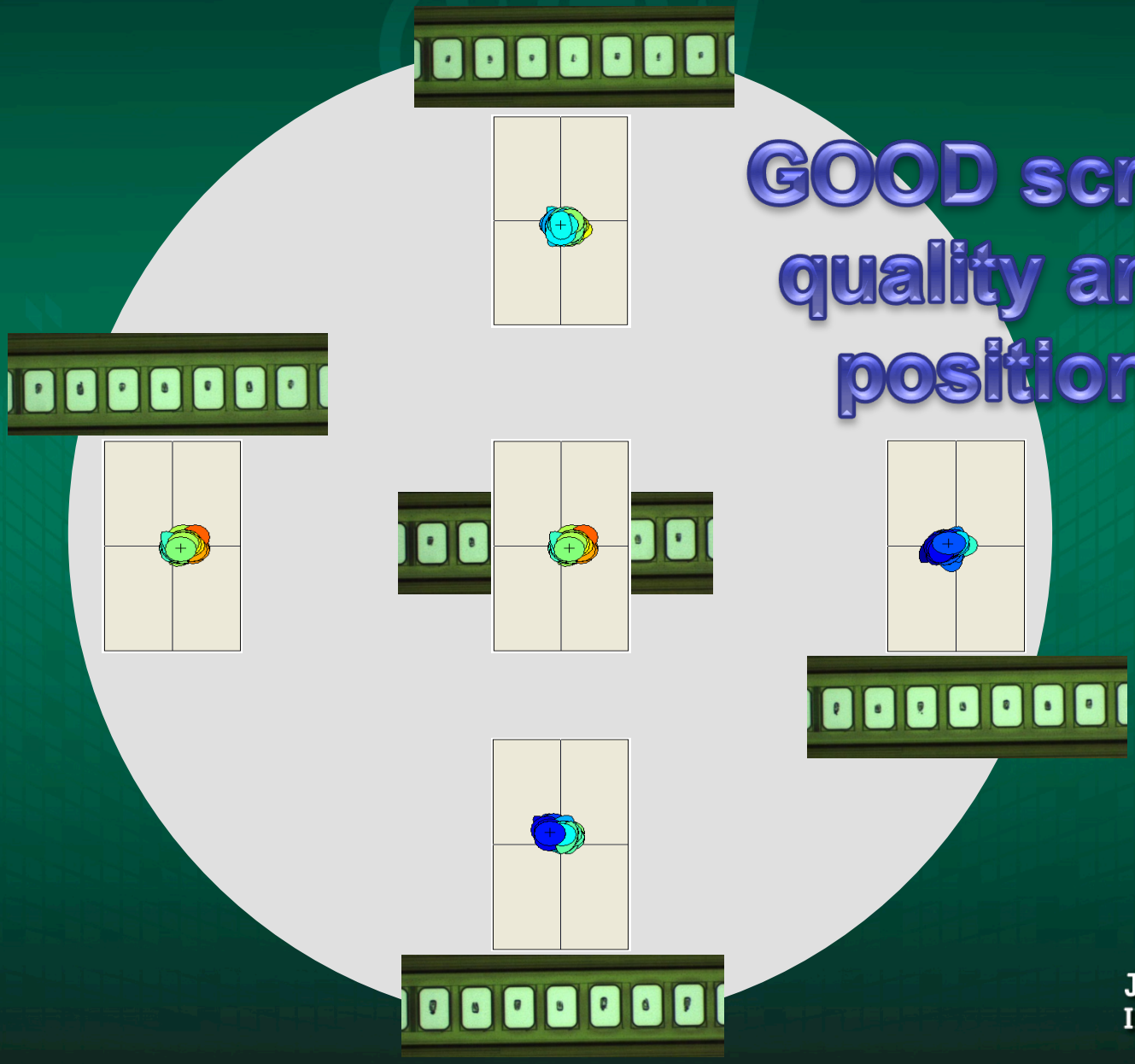
- **Internal design group wants:**
  - Minimum pad size and pitch
  - Reduced pad metal thickness
  - Circuitry under pad (CuP)

Bond Pad Damage

- Pad area consumed by multiple wafer test steps

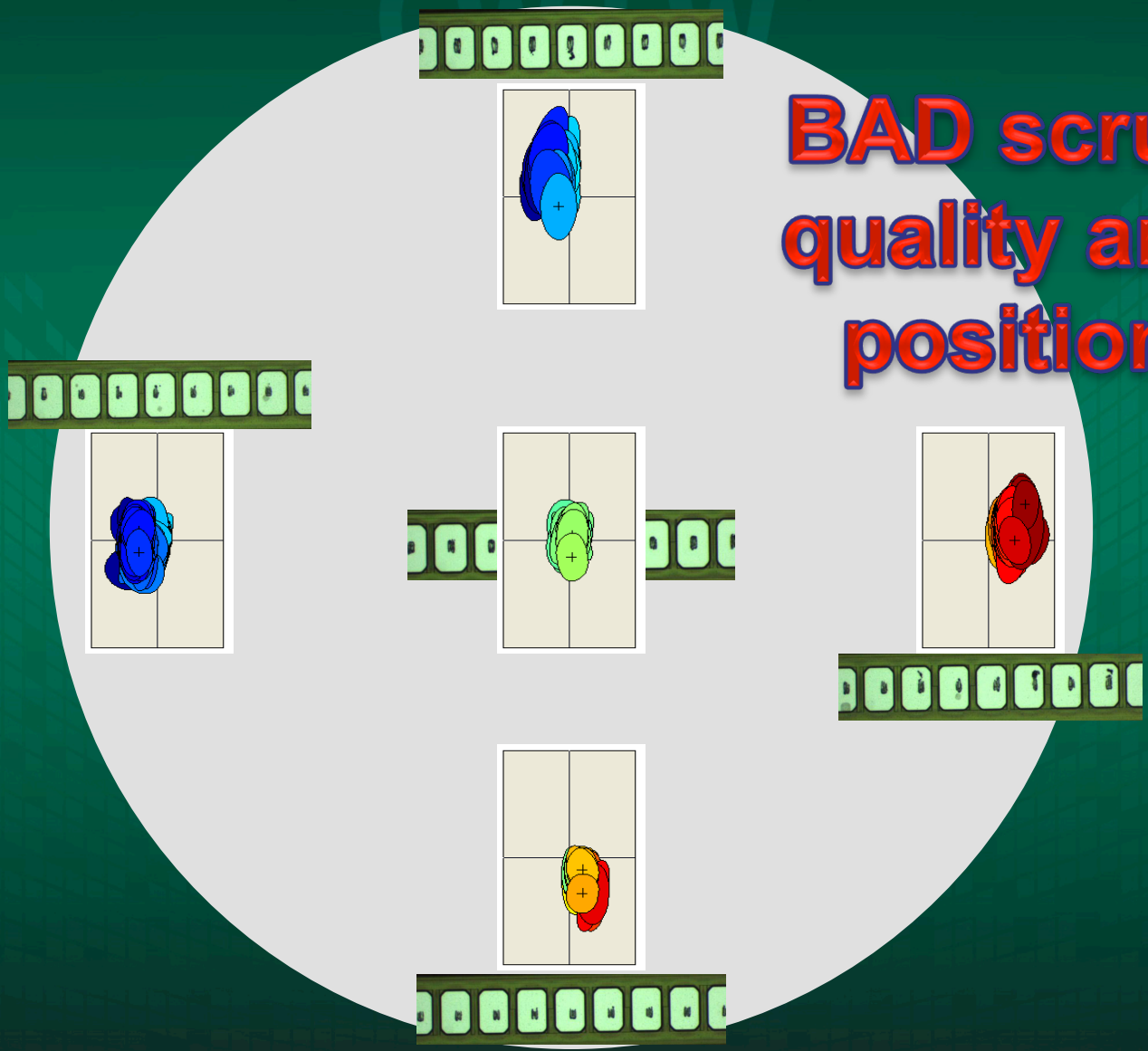


Full-Wafer Scrub Mark Placement



GOOD scrub quality and position

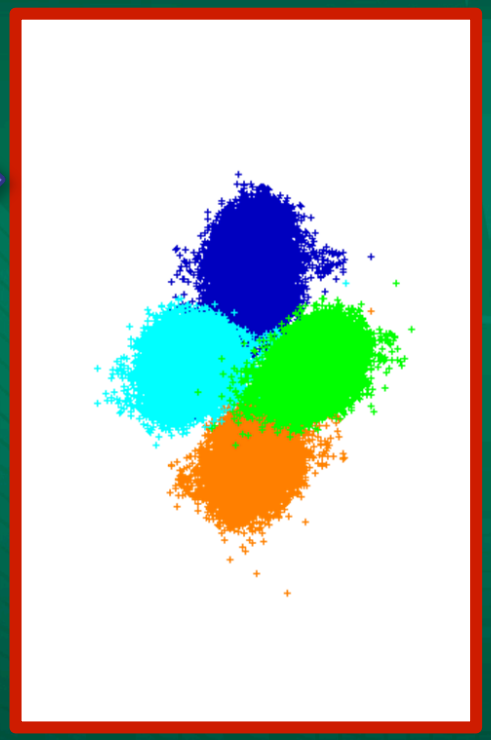
Full-Wafer Scrub Mark Placement



BAD scrub quality and position

Bond Pad Damage – TBLR Analysis

GOOD!

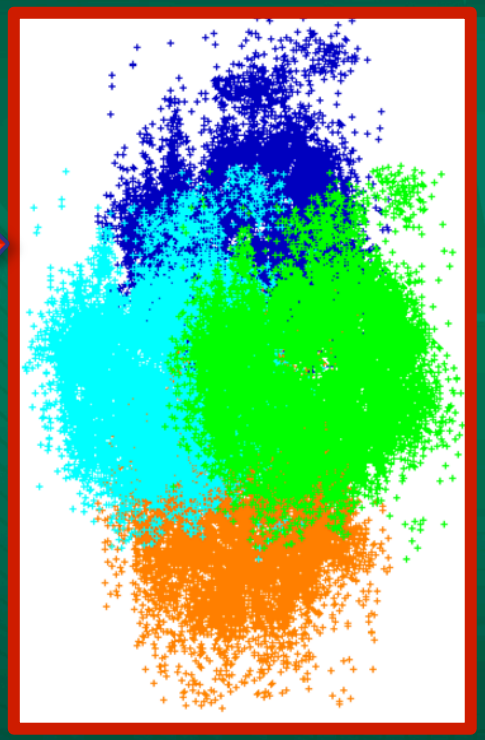


- Bond Pad Edge
- Extent of Scrub Mark Top
- Extent of Scrub Mark Bottom
- Extent of Scrub Mark Left
- Extent of Scrub Mark Right

- >20K scrub mark data overlay
- Good centering and tight distribution

Bond Pad Damage – TBLR Analysis

BAD!



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- Extent of Scrub Mark Right

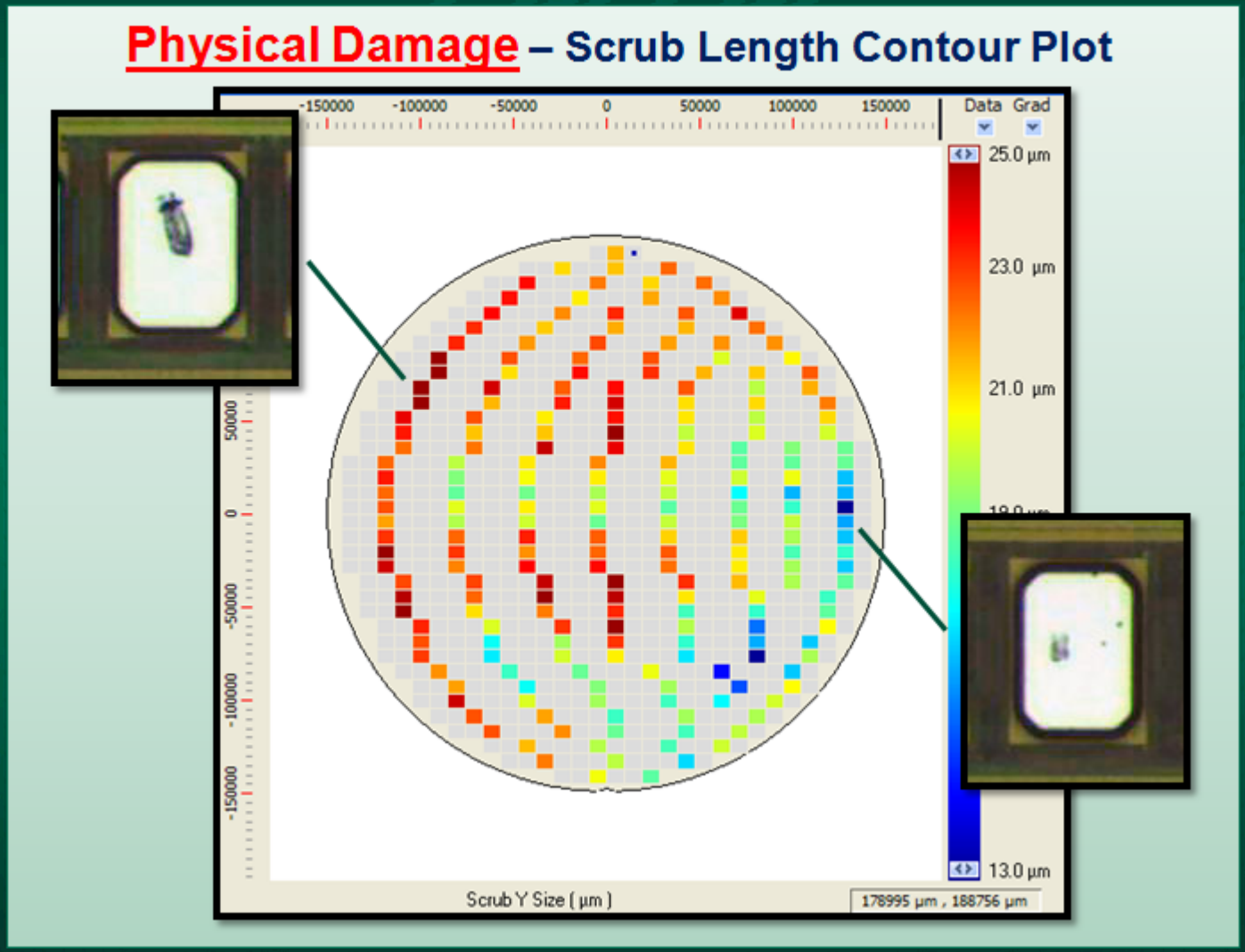
- >20K scrub mark data overlay
- Good centering and tight distribution

What is Needed?

- **Reduced pad damage**
  - Low force probes
  - Reduced scrub length
- **Greater probe card z-compliance (Max OD)**
- **Efficient inline probe mark inspection methods**

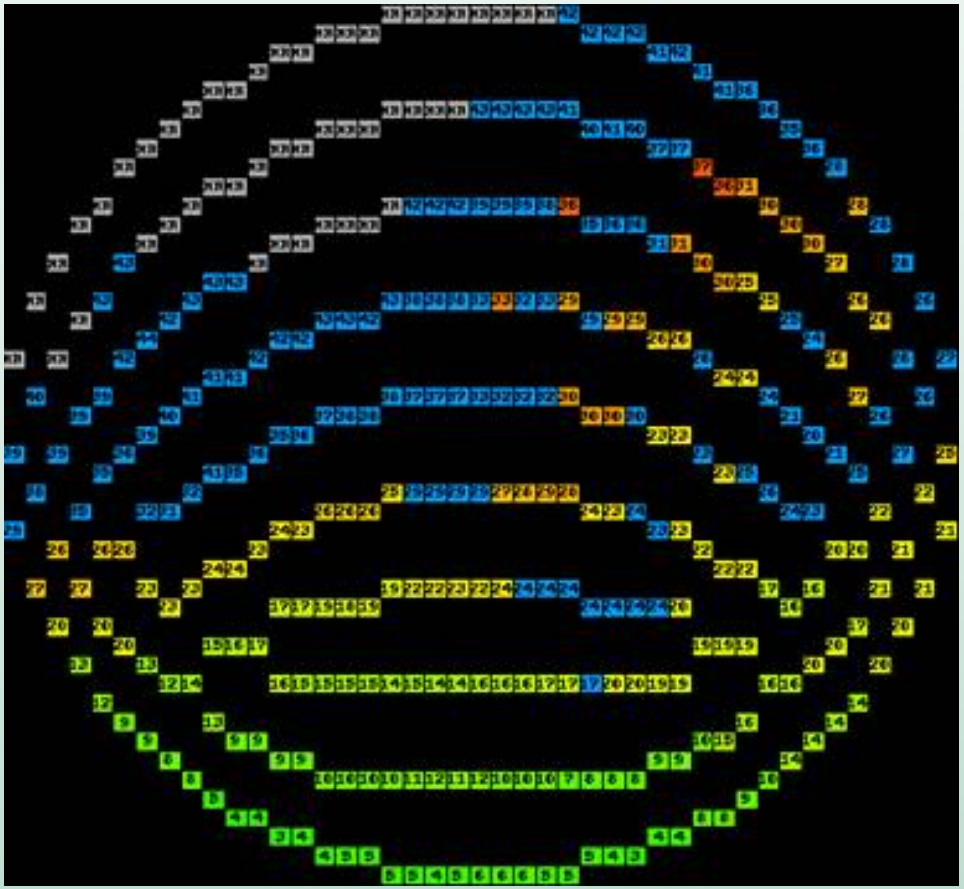
Test Cell Mechanical Tolerance Stackup

Cost of Increased Planarity Variation

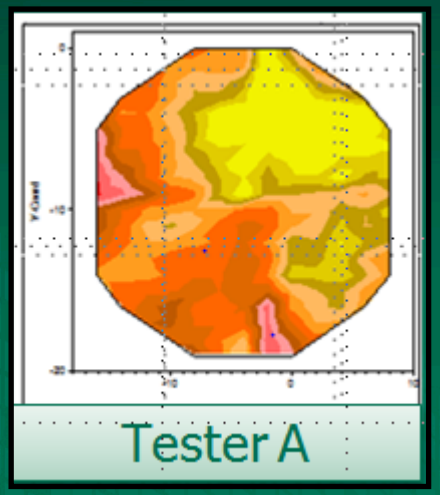


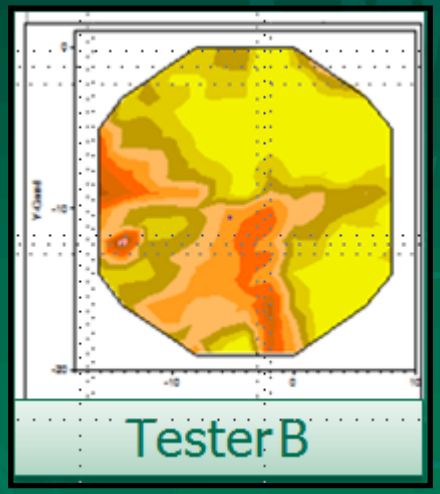
Cost of Increased Planarity Variation

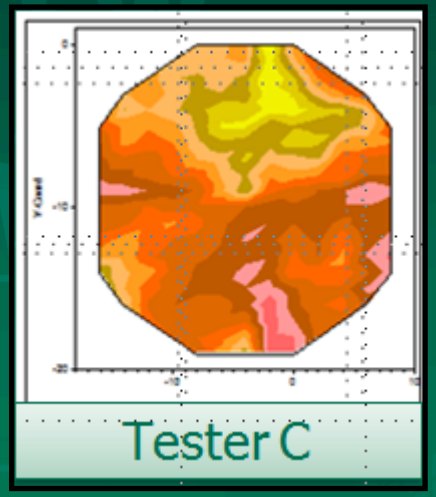
Electrical Performance – Continuity Contour Plot

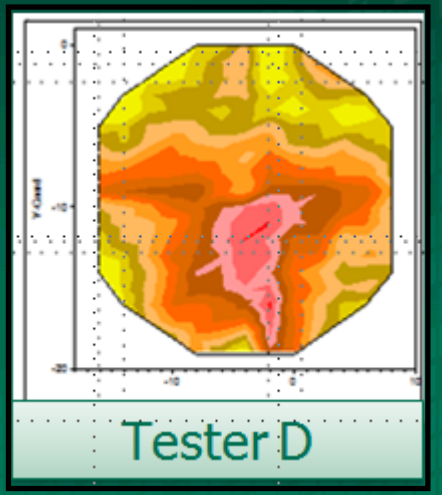


Cost of Manufacturing Support

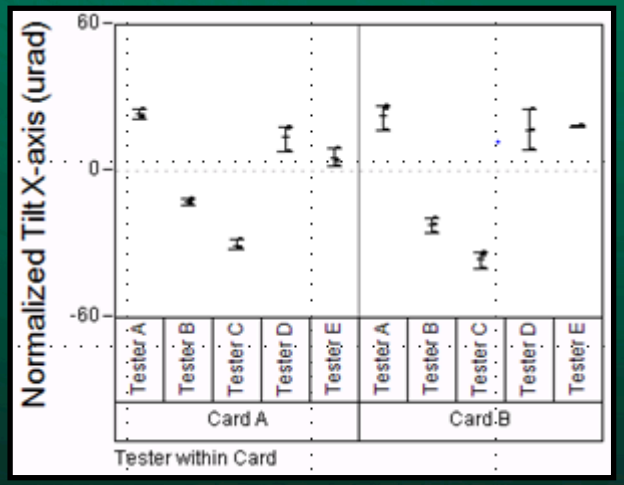


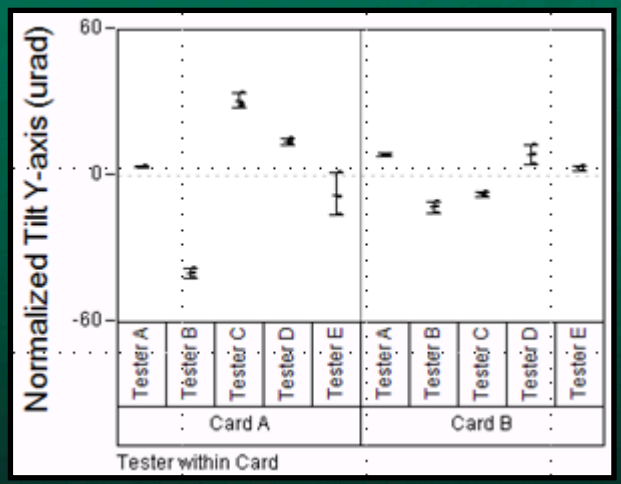




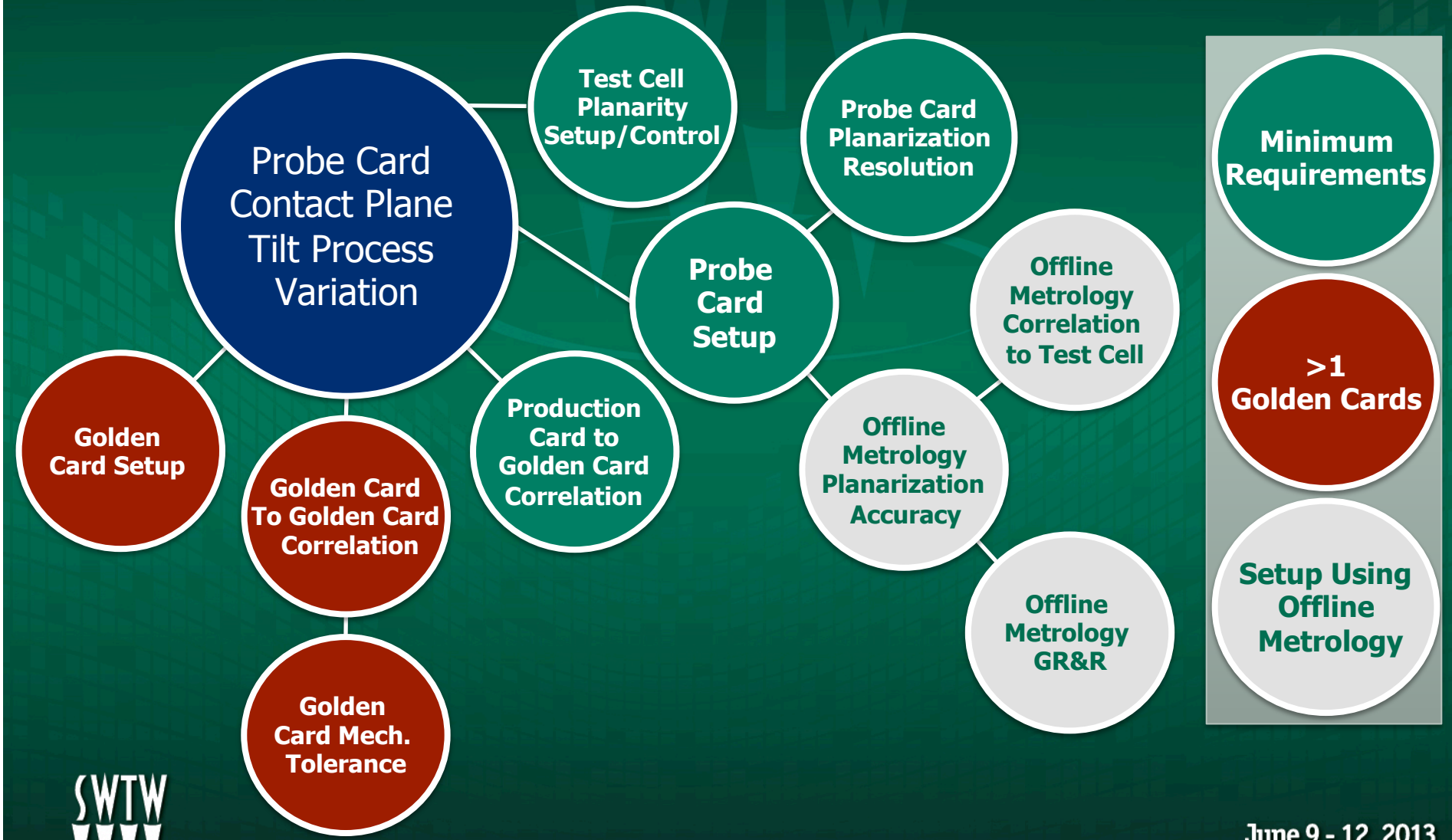


Tester-to-Tester Planarity Variation





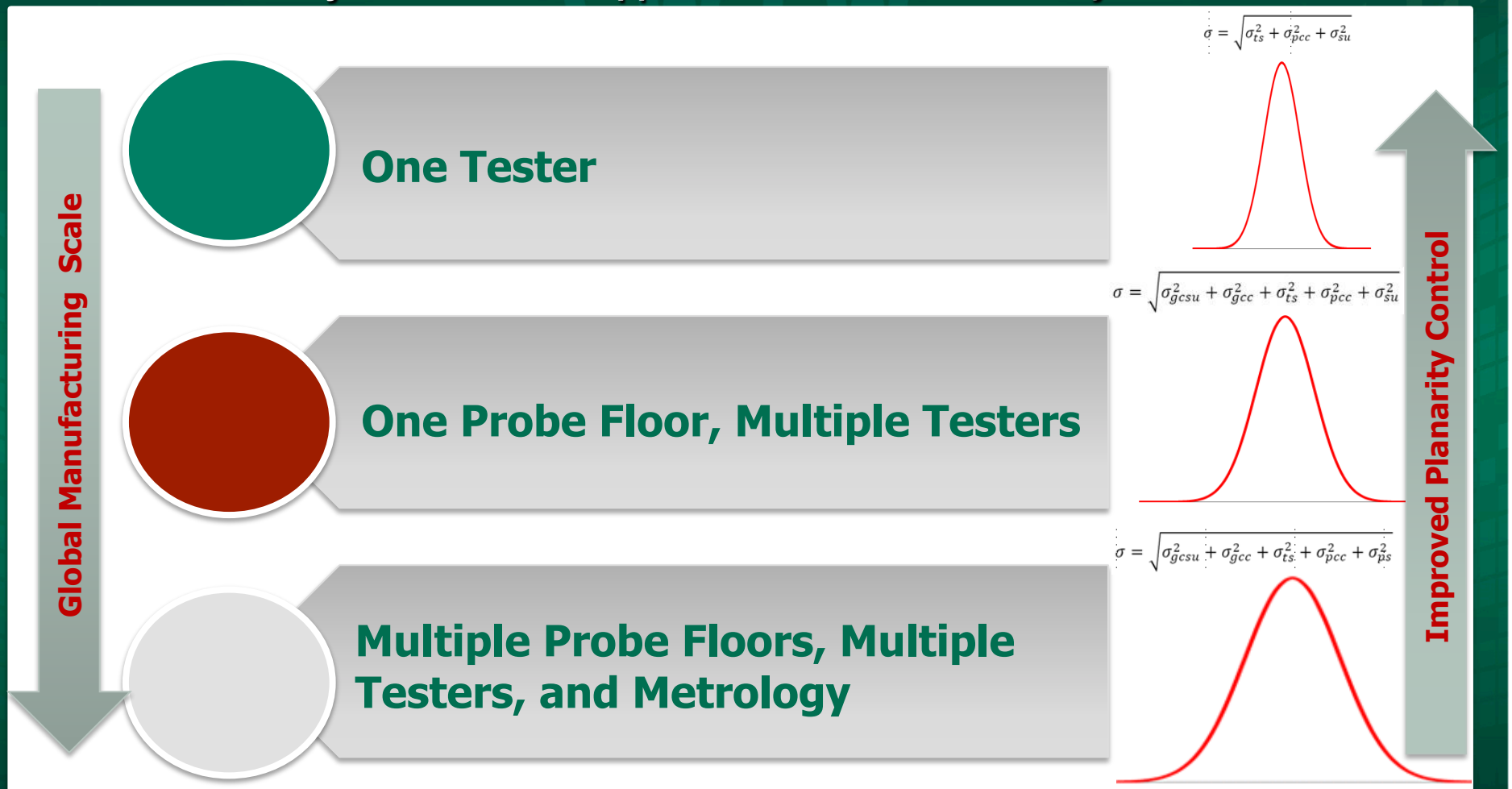
Test Cell Planarity Process Control



Test Cell Planarity Support Model

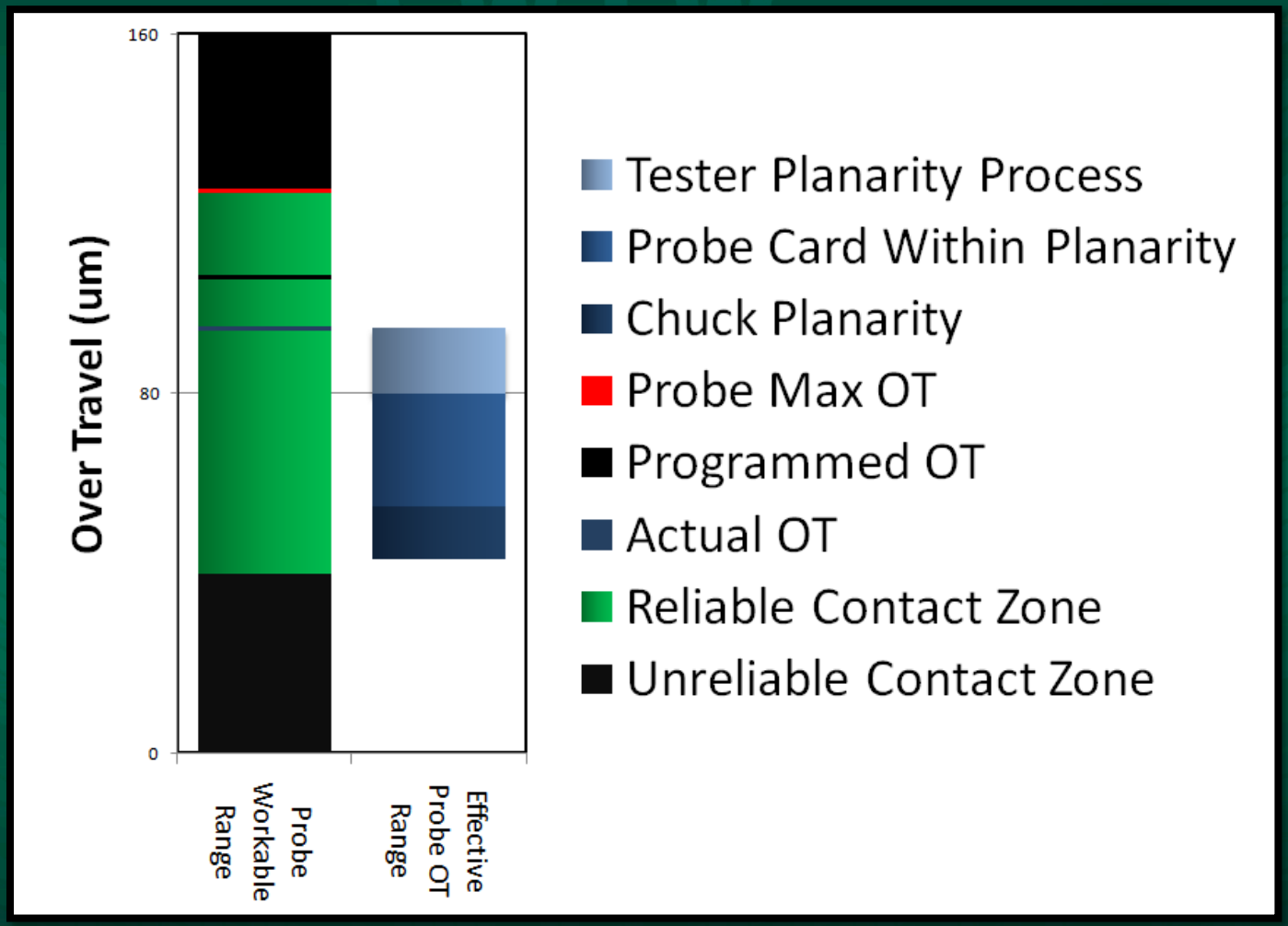
Planarity Maintenance/Support Model

Planarity Variation Probe Floor



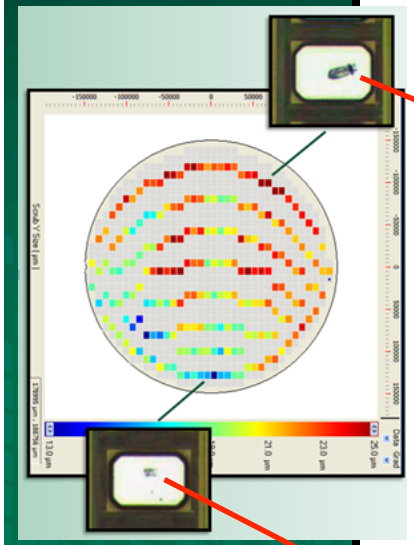
Probe Range vs. Test Cell Planarity

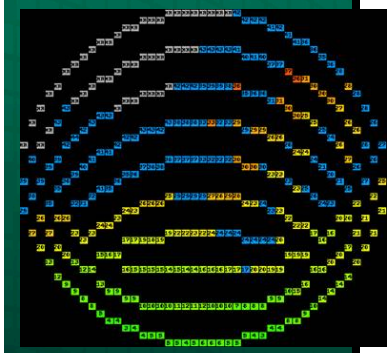
1 Golden Card, Probe Planarized on Tester Cell

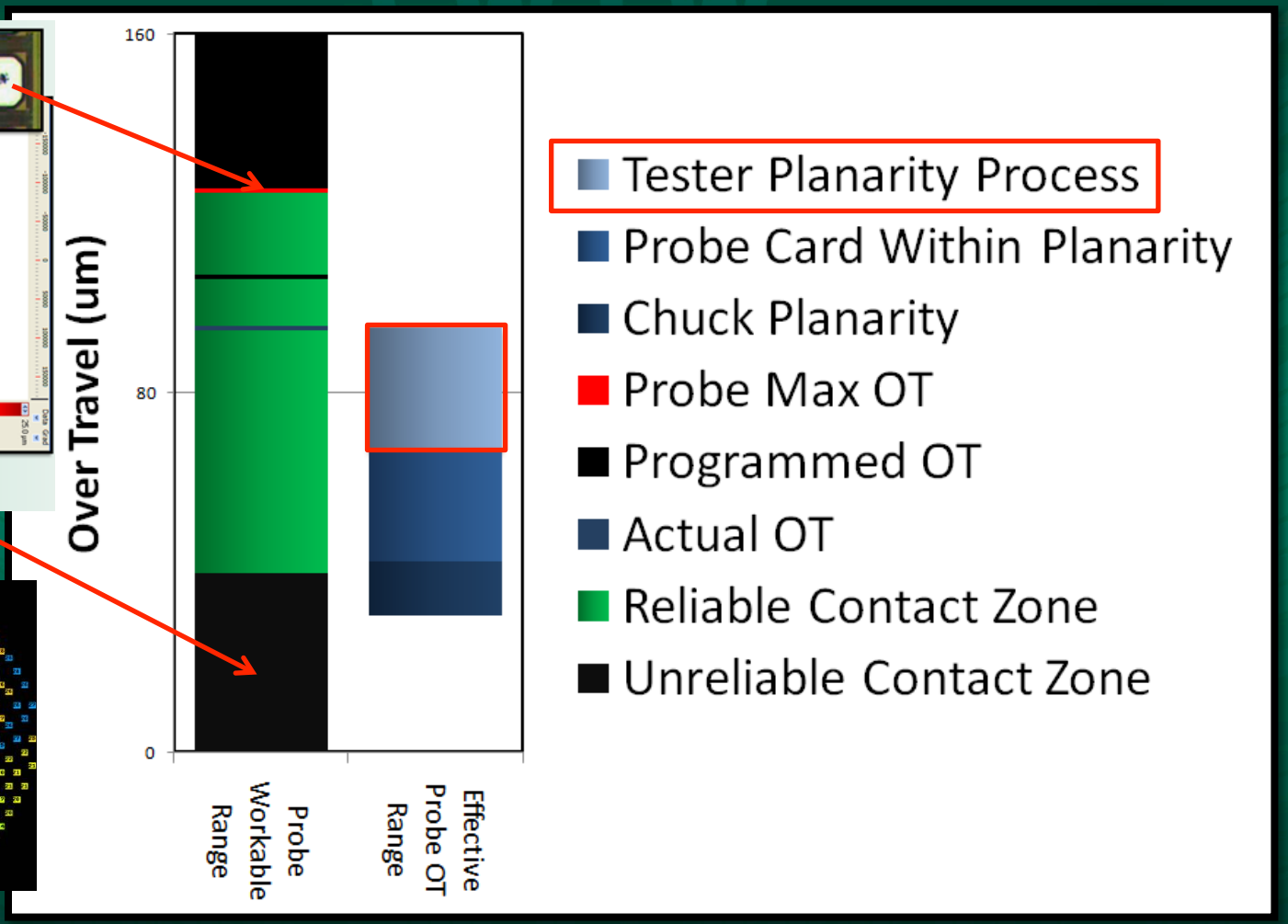


Probe Range vs. Test Cell Planarity

Offline Metrology Probe Card Setup + >1 Golden Cards





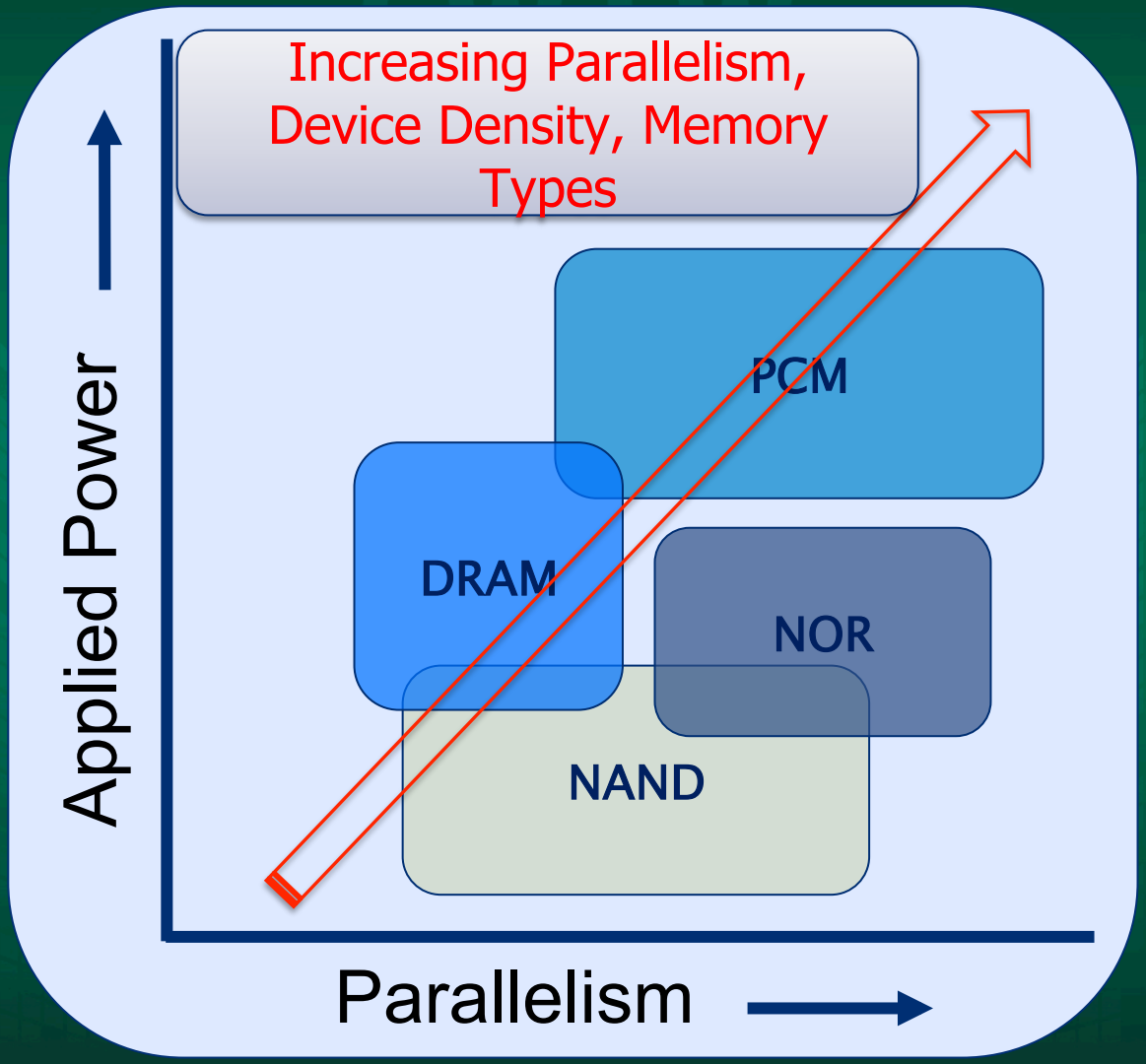


What is Needed?

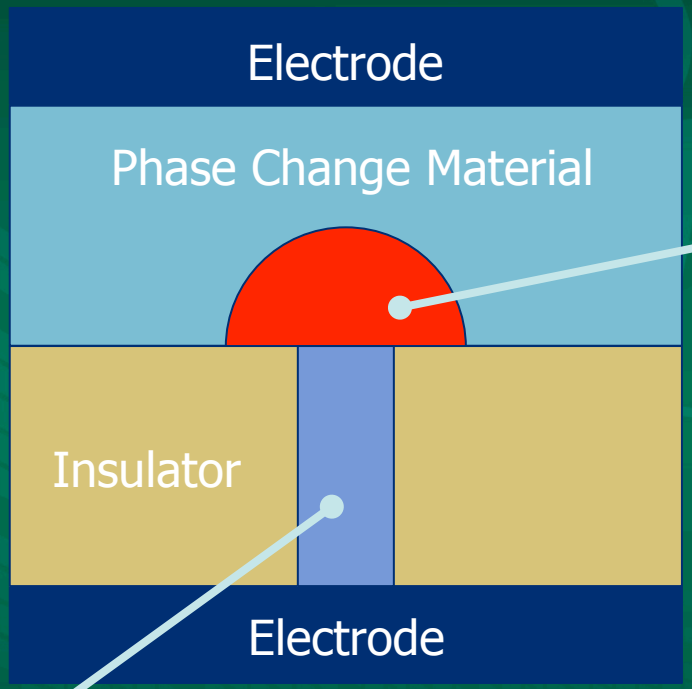
- **Equipment Designed for Manufacturing (DFM)**
  - Innovative, integrated test cell solutions
  - Tighter probe card planarity
  - Greater probe card z-compliance

Thermal Management

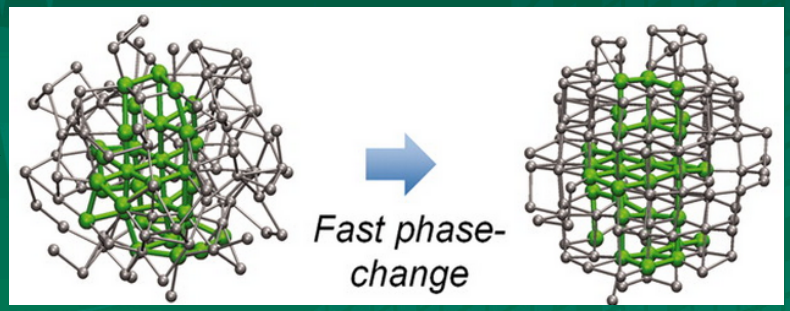
2013 Memory Landscape

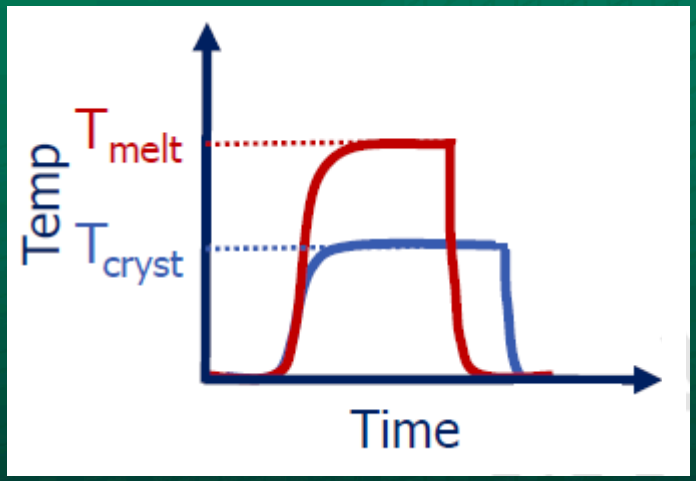


Phase Change Memory (PCM)



Cell Region →

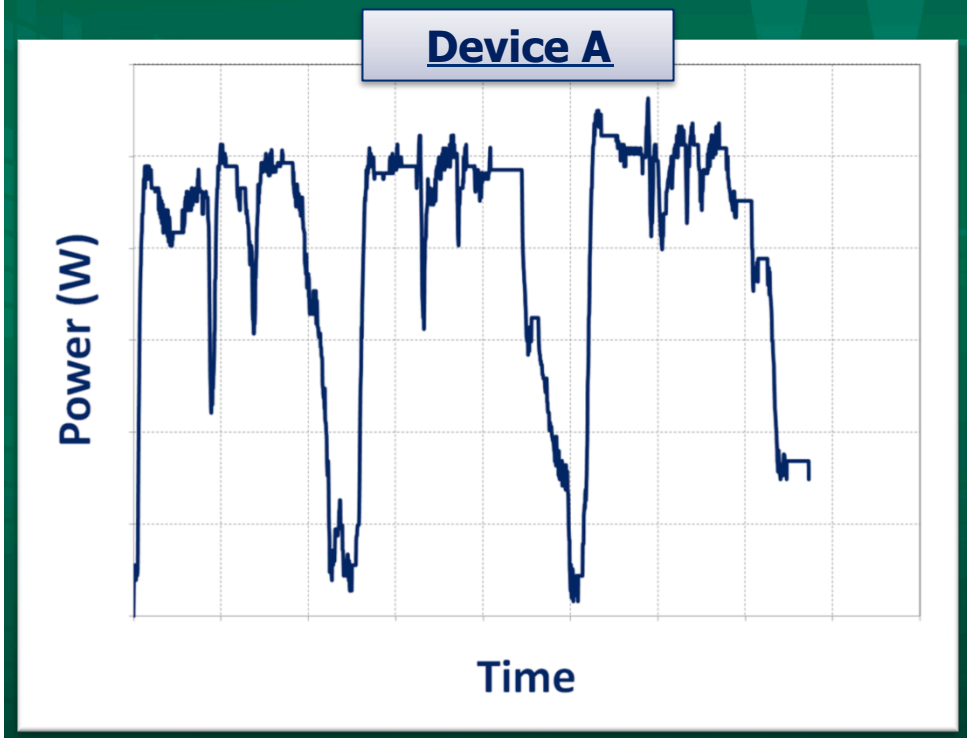


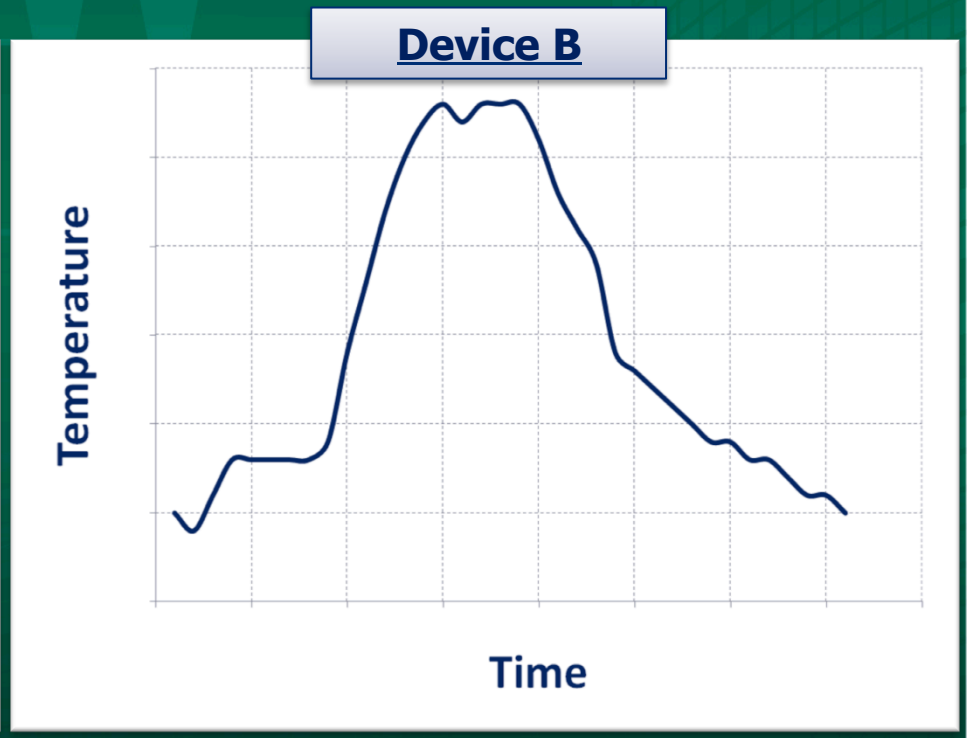


D Loke et al. Breaking the Speed Limits of Phase Change Memory. Science (2012) 1566-1569.

Device Characterization

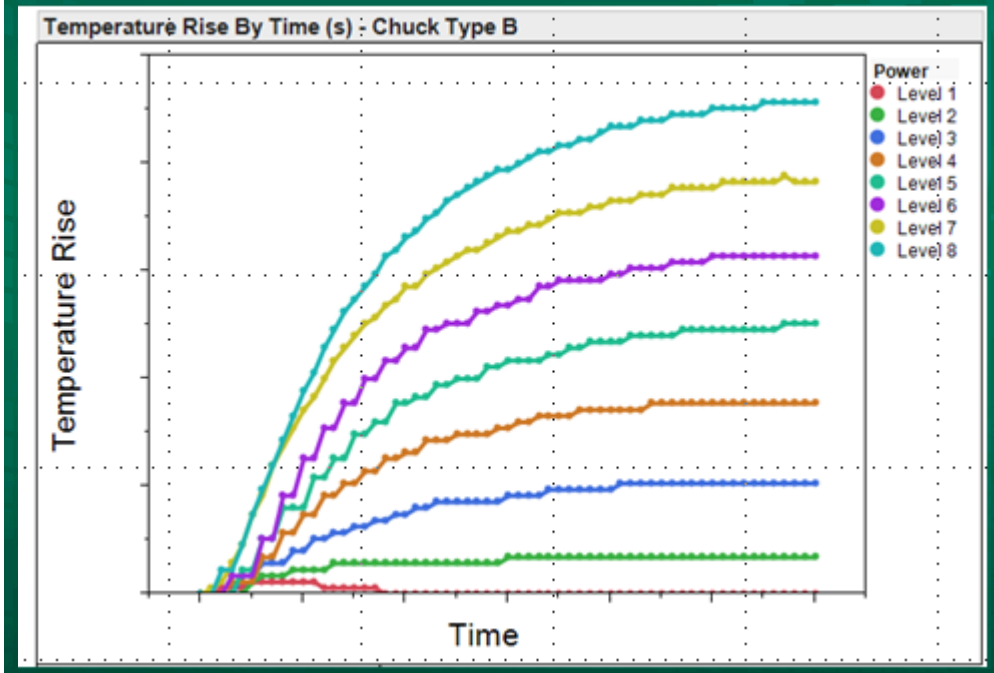
- Characterize **power curves** and **device temperature** during functional test flow

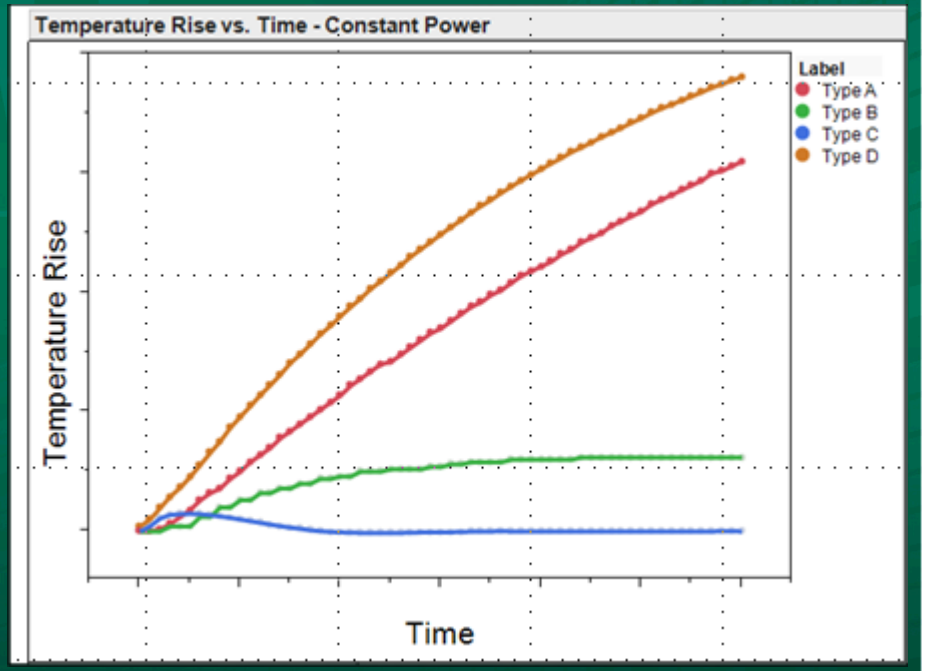




Equipment Characterization

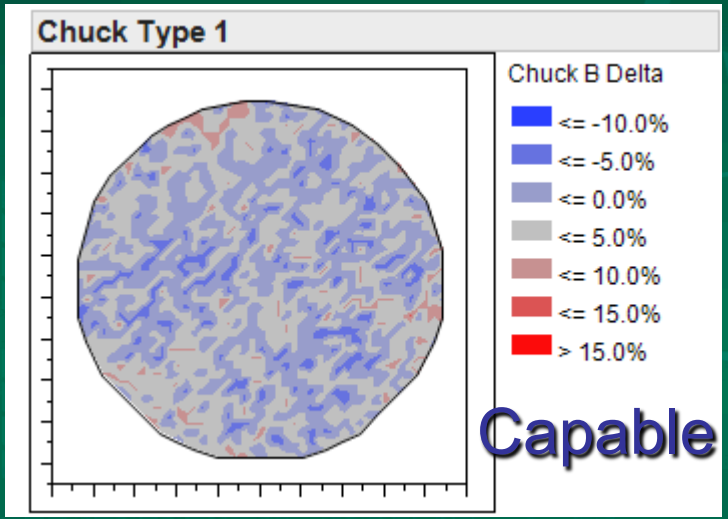
- Characterize **chuck response** to **applied power** and benchmark performance

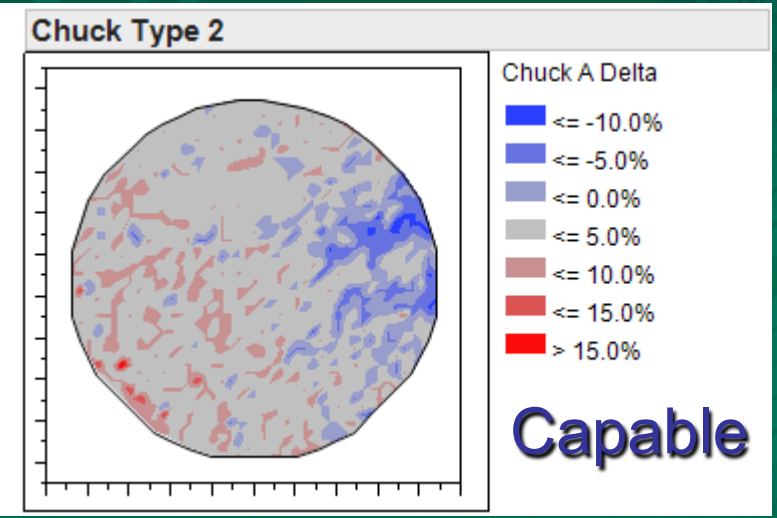


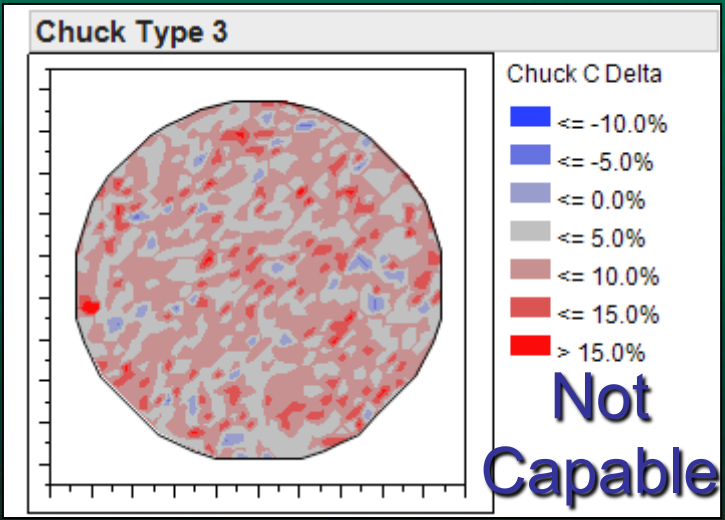


Analyze Test Data

- Die temperature vs. chuck temperature







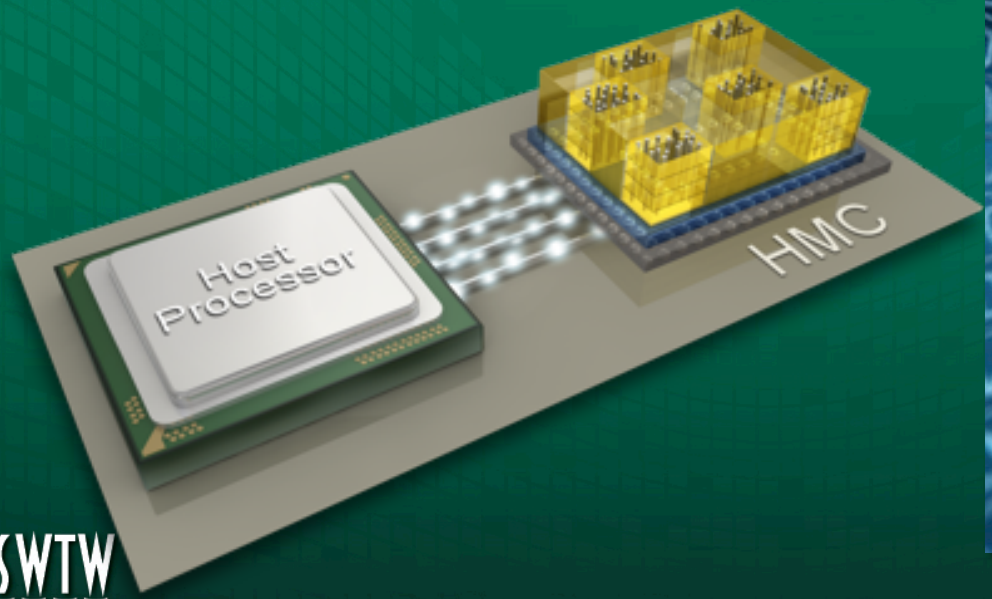
What is Needed?

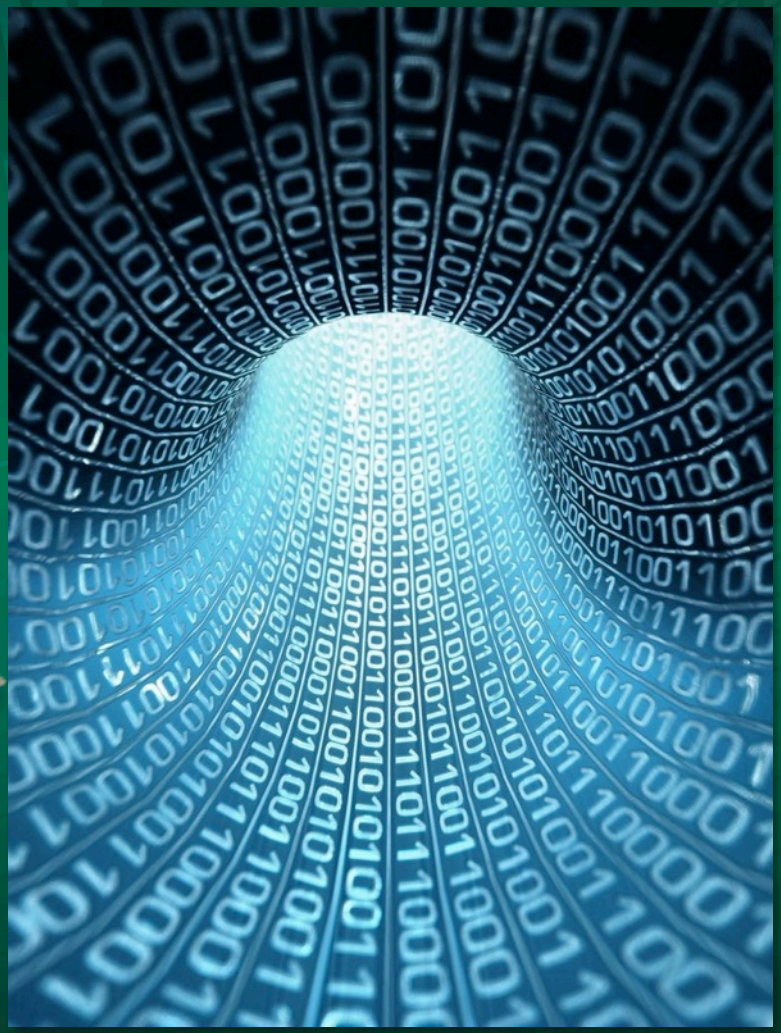
- Innovative power/thermal management solutions for high-parallel applications.
- Diligent characterization of device power dissipation requirements to allow informed equipment selection.

Future Memory Product Challenges

Future Challenges - Memory Revolution

- Global demand for mobility, exponential data growth, cloud service requirements, storage server capabilities





Conclusion

- **LPDDR4 challenges** current probe roadmap. Opportunity exists to enable new capability.
- **Integrated test cell** solutions (DFM) Designed for Manufacture, (metrology, prober, probe card)
- **Emerging memory** devices are driving demanding thermal management solutions.
- **Cost of Quality** has to be addressed through industry collaboration (standards around test for manufacturing).

Thank You!