

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 9 - 12, 2013 | San Diego, California

Spansion, Inc.

Probe Card Improvements to Resolve Customer-Specific Issues



Mohamed Eldessouki, PhD Rehan Kazmi, PhD SV Probe, Inc. Mark Ojeda

Presentation Overview

- Motivation
- Objective
- Noise Sources & Bandwidth
- Modular Space Transformer (MST) Solution
- Probe Head (PH)
- Customer Measurement
- Summary & Conclusion



Motivation

- Customer Feedback WST-based Probe Cards
 - Customer Noticed High Noise on Both Signal & Supply Measurements
 - Average Percent of Wafer Test Yield Loss with Standard WST Technology was 3.83%
 - Customer Noticed PWR Pin Deformation Due to High Currents

Wired Space Transformer (WST) Probe Card



June 9 - 12, 2013 IEEE Workshop

The Goal

- To Keep WST Advantages:
 - -Quick Turn Around Time
 - Easy
 - Economical
- To Address WST Shortcomings:
 - -High Noise Coupling between Signal Channels
 - Power Plane Noise Coupling
 - -Low Bandwidth



Specific Objectives

- Signal Integrity (SI) Related
 - Increase ST Bandwidth
 - Reduce Signal to Signal Crosstalk
 - Reduce Signal Loss
 - Better Noise Decoupling from Supply Line
 - Reduce PWR/GND Impedance
- Power Integrity (PI) & Power Capability Related
 - Increase Current Carrying Capacity
 - Introduce Low Stable Contact Resistance
- Productivity Related
 - Keep Turn Time Short by Introducing Modular Solution



Noise Sources:

- Reflection Noise
- Crosstalk Noise
 - Radiation
 - Coupling
- Power/GND Noise

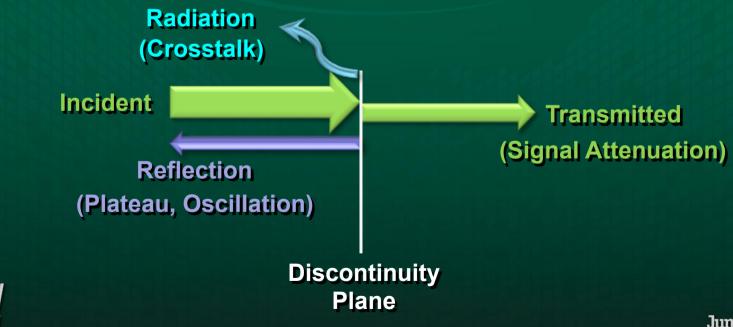
• Bandwidth:

- Transmission Line (TL) Type with a Low Pass Filter (LPF) Characteristic
 - Parallel Wire TL



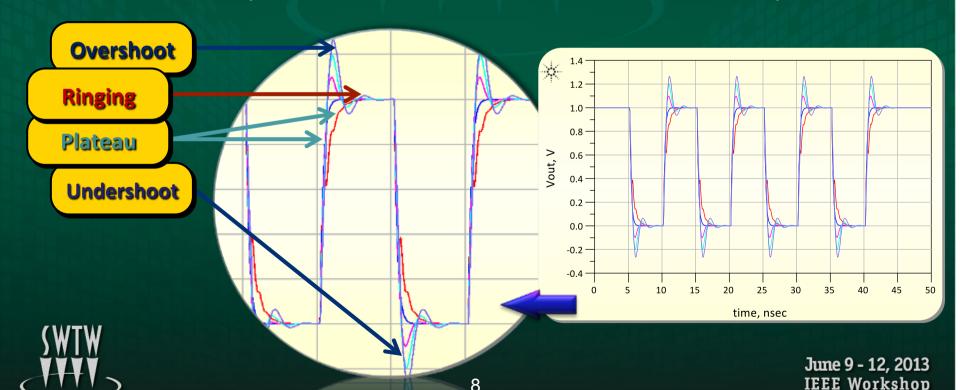
• Strip Line, Micro-strip

- Reflection & Multiple Reflection Noise
 - Impedance Mismatch Discontinuity & TL Delay
 - Return Path Discontinuity
 - Transition (Wire to Pin Connection, Connectors, etc)



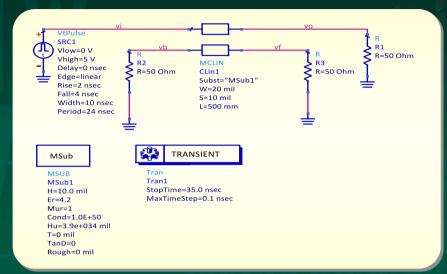


- Reflection & Multiple Reflection Noise
 - Impedance Mismatch Discontinuity & TL Delay
 - Return Path Discontinuity
 - Transition (Wire to Pin Connection, Connectors, etc)

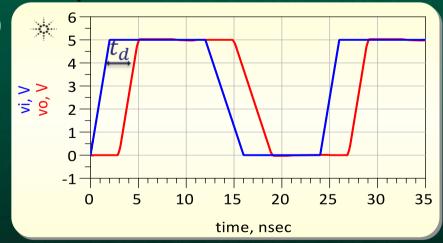


• Crosstalk:

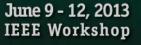
- Source of Crosstalk:
 - Capacitive Coupling
 - Inductive Coupling
 - Radiation
- Crosstalk Types
 - NEXT (TL Delay Time Related)
 - FEXT (*tr* and *tf* Related)



Coupled Lines

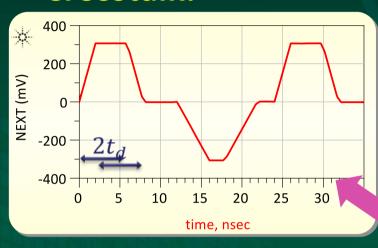


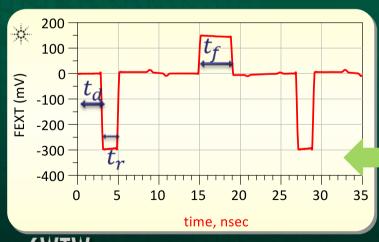


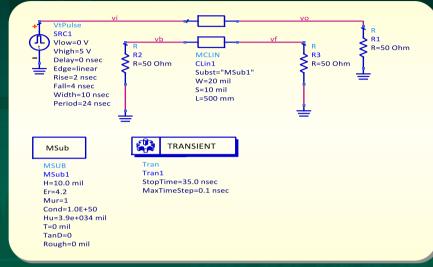




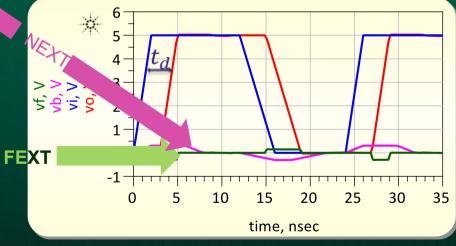
Crosstalk:







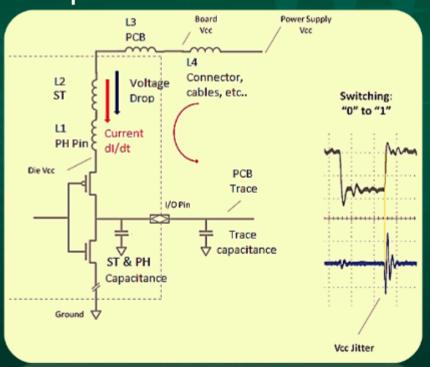
Coupled Lines

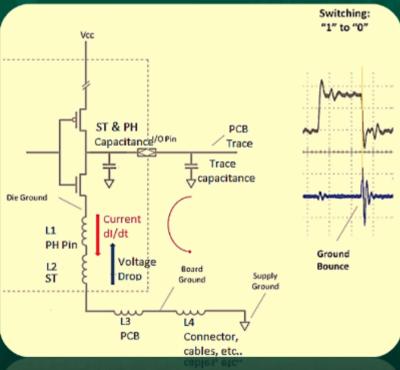


Input, Output NEXT & FEXT Signals

June 9 - 12, 2013 IEEE Workshop

- Power/GND Noise:
 - Higher Impedance of the Power/GND Plane at Higher Frequencies





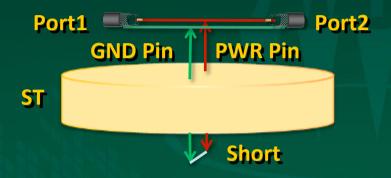


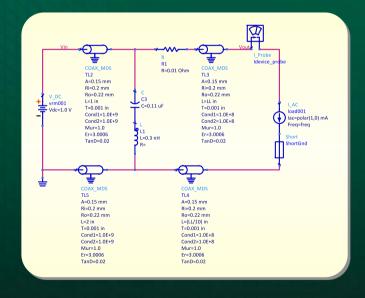
VCC Drop Jitter

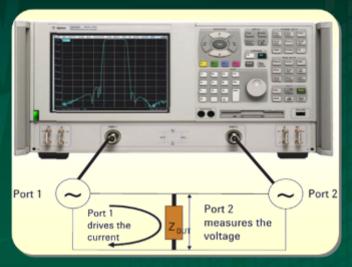
Ground Bounce

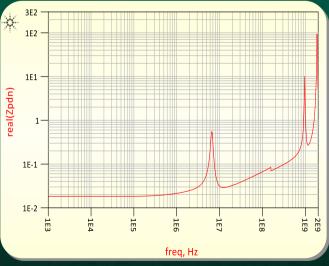
June 9 - 12, 2013 IEEE Workshop

Power/GND Noise:





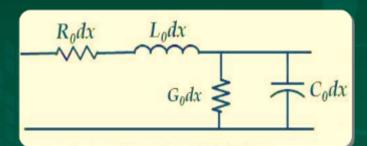






Bandwidth:

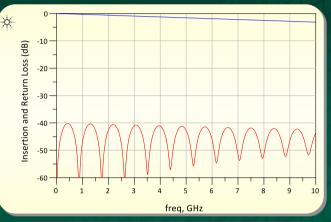
TL Type with a LPF Characteristic



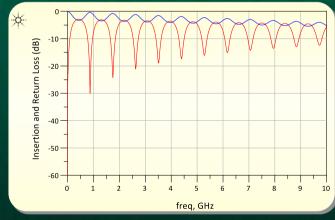
TL Equivalent Circuit Model

$$\frac{L_0 dx}{C_0 dx}$$

 $f_c = \frac{1}{2\pi\sqrt{LC}}$



Matched TL



Mismatched TL

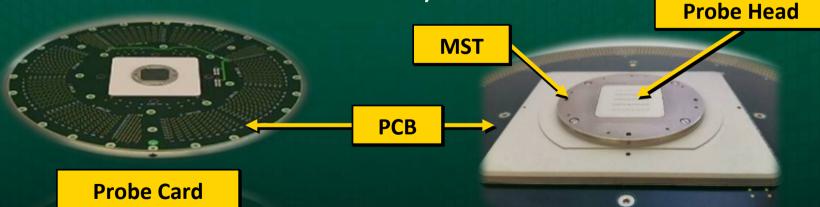
June 9 - 12, 2013 IEEE Workshop

Loss-less TL Equivalent Circuit Model

Action Items:

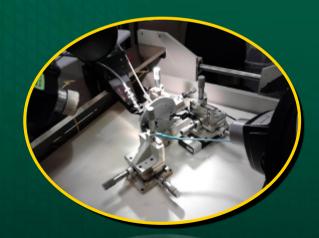
- Minimize Discontinuity for Signal Path
- Provide Continuous Return Path
- Bring Decoupling Capacitors as Close as Possible to the DUT PWR Pad

Reduce Inductance for PWR/GND Path





- Experimental Methodology
 - Bandwidth Measurement
 - PWR/GND Path Resistance Measurement
 - TD Analysis



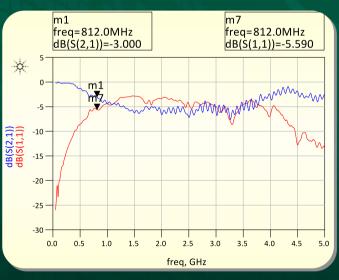


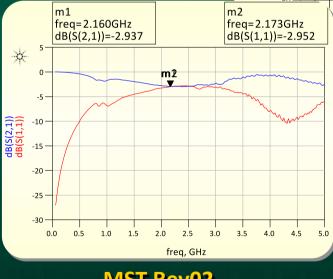


Probe Card using MST



- FD Measurements:
 - -50Ω Single Ended & 100Ω **Differential Channel** Measurement





* m4 Insertion and return loss (dB) freq, GHz

freq=8.392GHz

50 Ω Single Ended **MST Rev02**

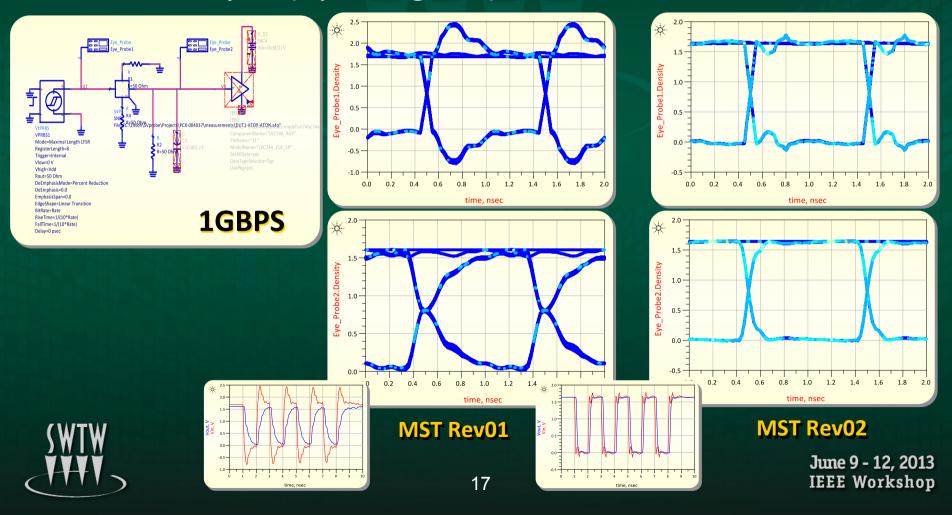
MST Rev01

MST Rev02

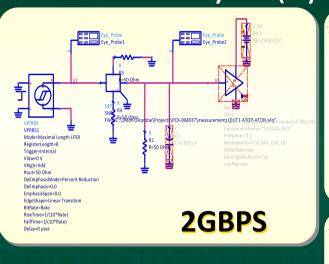


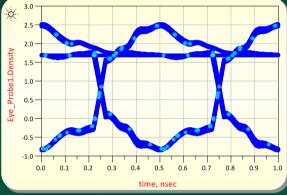
100Ω Differential

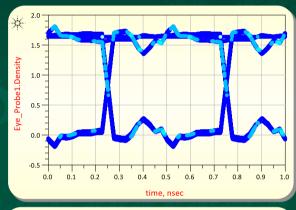
- Measurements:
 - TD Analysis (Eye Diagram)

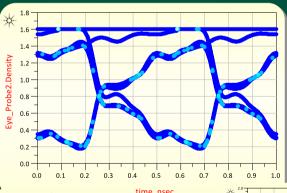


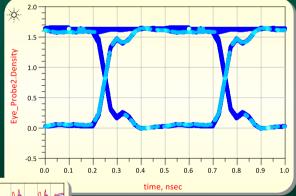
- Measurements:
 - TD Analysis (Eye Diagram)



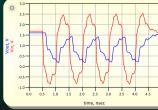












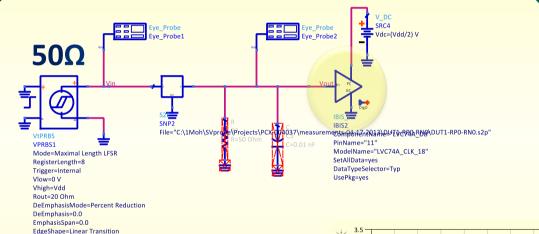
MST Rev01

18

MST Rev00

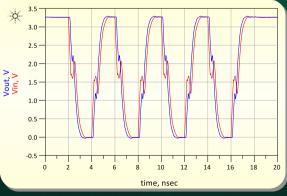
June 9 - 12, 2013 IEEE Workshop

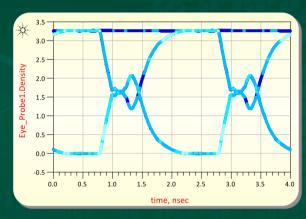
- Measurements:
 - TD Analysis (Eye Diagram)

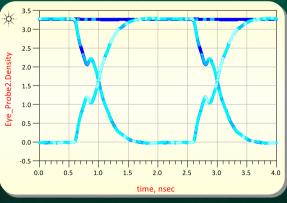


MST Rev02

500MBPS





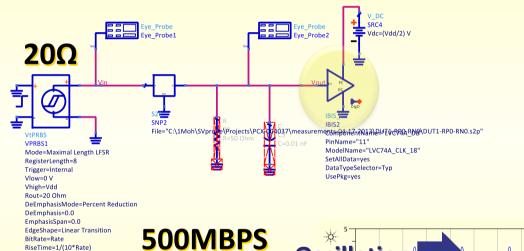




RitRate=Rate

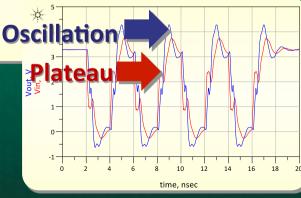
RiseTime=1/(10*Rate)
FallTime=1/(10*Rate)
Delay=0 psec

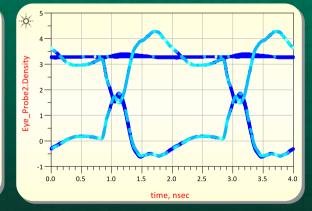
- Measurements:
 - TD Analysis (Eye Diagram)



2.0 2.5

MST Rev02







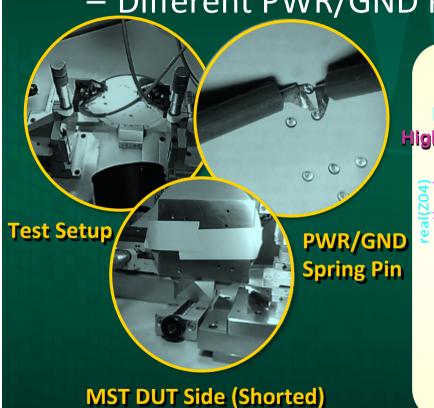
RitRate=Rate RiseTime=1/(10*Rate)

FallTime=1/(10*Rate) Delay=0 psec

> June 9 - 12, 2013 IEEE Workshop

Power/GND Measurements:

Different PWR/GND Plane Measurements



High Supply Line Inductance
High Supply Line Inductance

NST Low Inductance for Both
Return & Supply line

1E-1
High Return Path Inductance

1E-2

1E8

1E9

2E9

freq, Hz



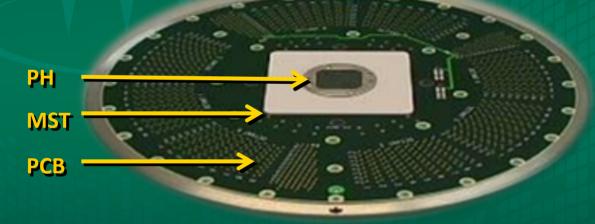
- Validated Advantages:
 - Higher Bandwidth
 - Low Noise Coupling
 - Higher Bit Rate Capability
 - Low Path Resistance for Both PWR & GND



Power Capability

• Reduce Path Resistance & Increase CCC

Bottleneck for CCC



Probe Card



Probe Pin

• P7 & PowerPlus™(PP) Properties Comparison:

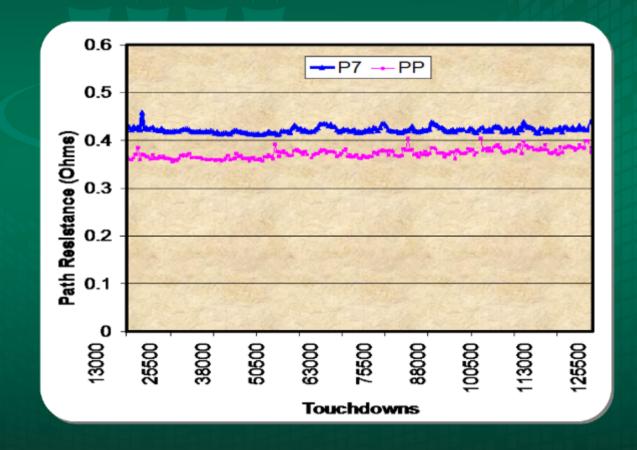
	Paliney 7	PowerPlus™
Resistivity	32 μ Ω -cm	12 μ Ω -cm
Oxidation at 25°C	Low	Low
Oxidation at 150°C	Low	Low
Melting Temp	1015°C	960°C



Probe Pin

• P7 & PowerPlus™(PP) Performance Comparison:

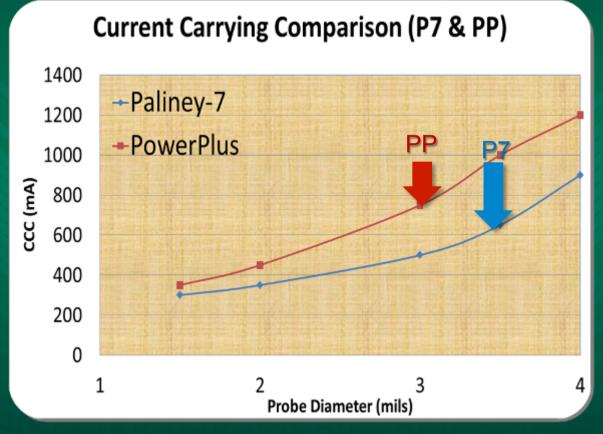
Path Resistance Measurement





Probe Pin

• P7 & PowerPlus™(PP) CCC Comparison:

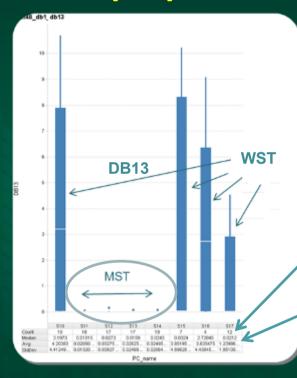




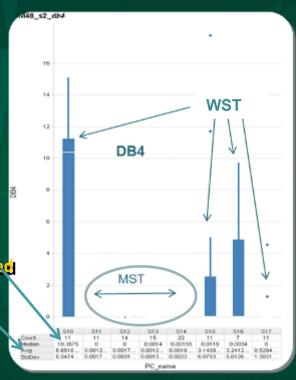
10% Force Drop Methodology

Customer Results

• MST (PP) VS WST (P7) Data



Number of Wafer Tested
Avg. Yield Loss



98M48 Sort-1 DB13

98M48 Sort-2 DB4

The Average Yield Loss was Reduced from 3.83% to Almost <u>Negligible</u>

Summary & Conclusion

- Summary
 - ST Enhancement
 - MST Shown to Overcome WST Drawbacks
 - Reduce Discontinuities
 - Establish a Return Path for Signal Channels
 - Reduce Path Resistance
 - Reduce Inductance Between Decoupling Caps & GND
 - PH Enhancement
 - Increase Current Carrying Capacity
 - Reduce Path Resistance



Summary & Conclusion

Conclusion

- Reduce Discontinuity
 - Minimize Reflection Noise
 - Increase Bandwidth
- Establish a Return Path
 - Minimize Crosstalk Noise Caused by Radiation
 - Minimize Signal Loss by Radiation
 - Minimize Reflection Noise
- Decoupling Caps Close to the DUT
 - Reduce Path Resistance & Reduce PWR Drop (SSN)



Summary & Conclusion

Conclusion

- Connecting Coupling Cap GND to MST Reference GND
 - Reduce GND Inductance & Minimize GND Bounce (SSN)
- Reduce Pin Resistivity
 - Increase CCC
 - Reduce Voltage Drop

With the implementation of MST & PowerPlus™ probes, significant performance improvements were made to the probe card which resulted in higher yield at customer site.



Customer Issue Resolved!



IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 9 - 12, 2013 | San Diego, California

Probe Card Improvements to Resolve Customer-Specific Issues



Mohamed Eldessouki