
IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 9 - 12, 2013 | San Diego, California

# Wafer Translators

## An Alternative to Probe Cards

An Introduction

ADVANCED INQUIRY

Morgan Johnson CTO, Founder

# Translator Definition

## A typical Translator is:

- A thin, but air tight, two-layer-metal substrate
- Large, robust, regularly distributed pads covering the whole tester side
- Laser blind-vias connecting both sides
- Contact points exactly matching the wafer die pads on the wafer side

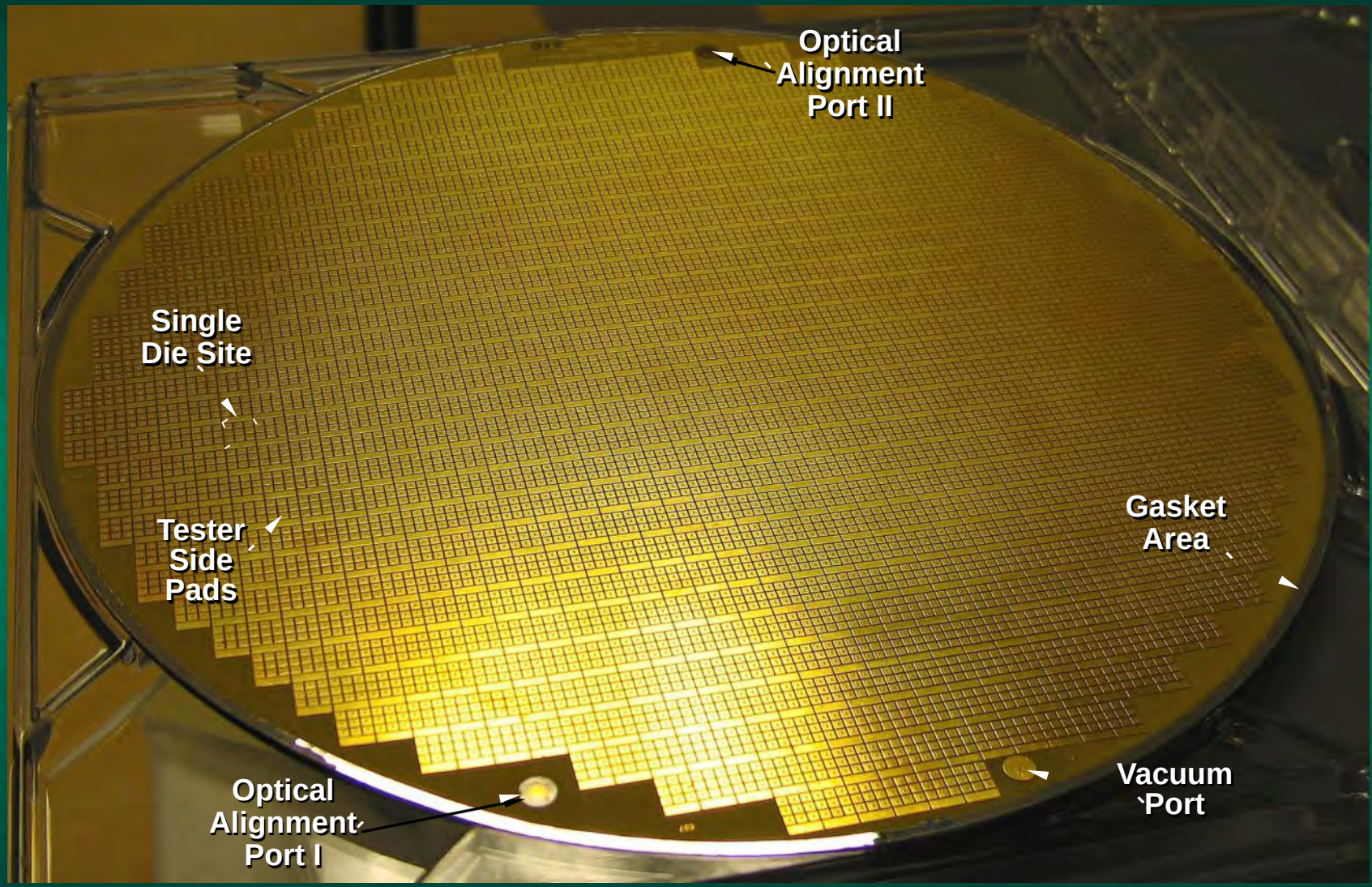
# THE PROBLEM

## Wafers Are Difficult To Test Because:

- Die pads are tiny and close together
- Die pads are delicate - 1 micron thick metal
- There are often a lot of them - per die / per wafer
- Die pads can be inconveniently distributed

# AN ORGANIC PCB BASED TRANSLATOR

**Rogers 4350 Microwave Substrate - .004” Core, 17 Micron Metalization Both Sides Ni & Au – Laser Blind Vias**

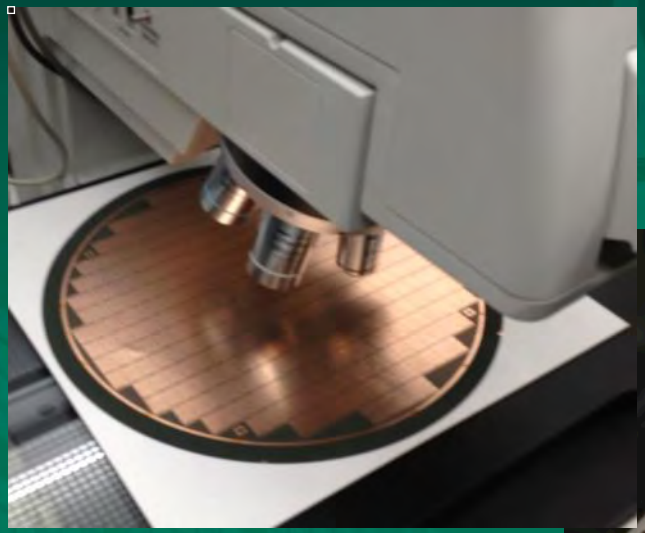


# What does a wafer “Translator” do?

- Translates tiny pads to big pads
  - 65 microns sq. to 800 microns sq. – 150 times the area
- Translates delicate pads to robust pads
  - 1 micron thick Al to 9-20 micron Cu-Ni-Au
- Translates inconvenient to symmetrical
  - Random to square pitch arrays typ. 1 mm x 1 mm

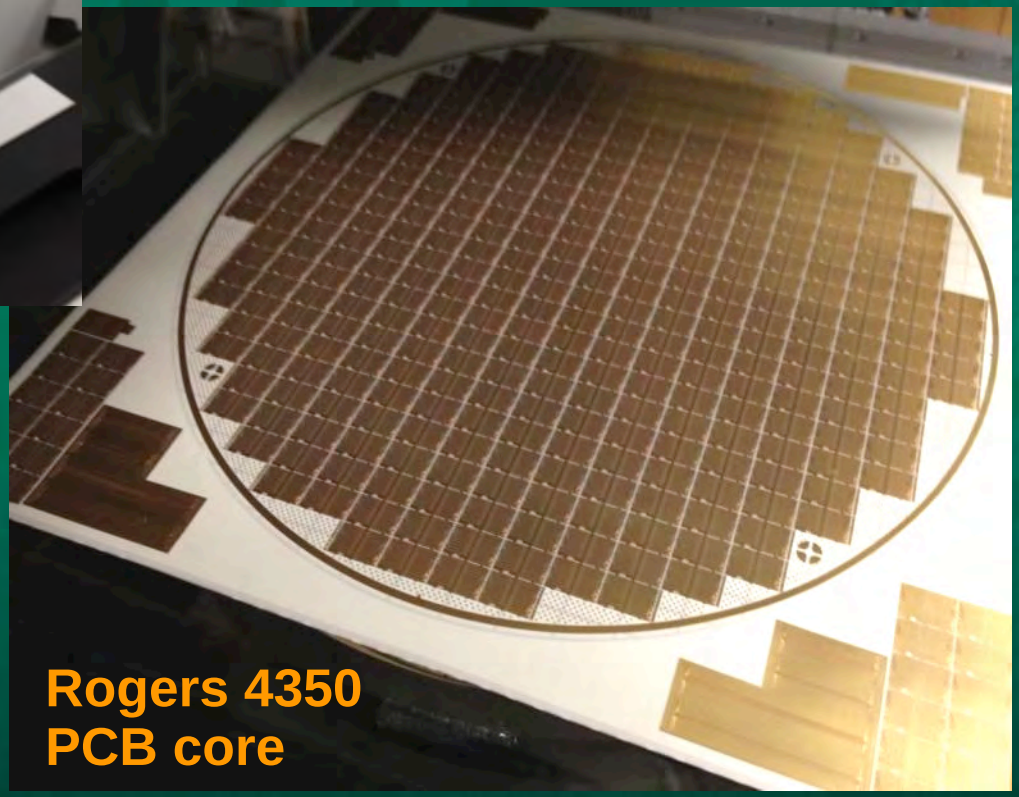
# ORGANIC PCB BASED WAFER TRANSLATORS

**Conventional two layer metal PCB substrate (.004") with ½ oz. Cu and laser blind vias**



**BT Epoxy**

CTE of 7 PPM $^{0}$C

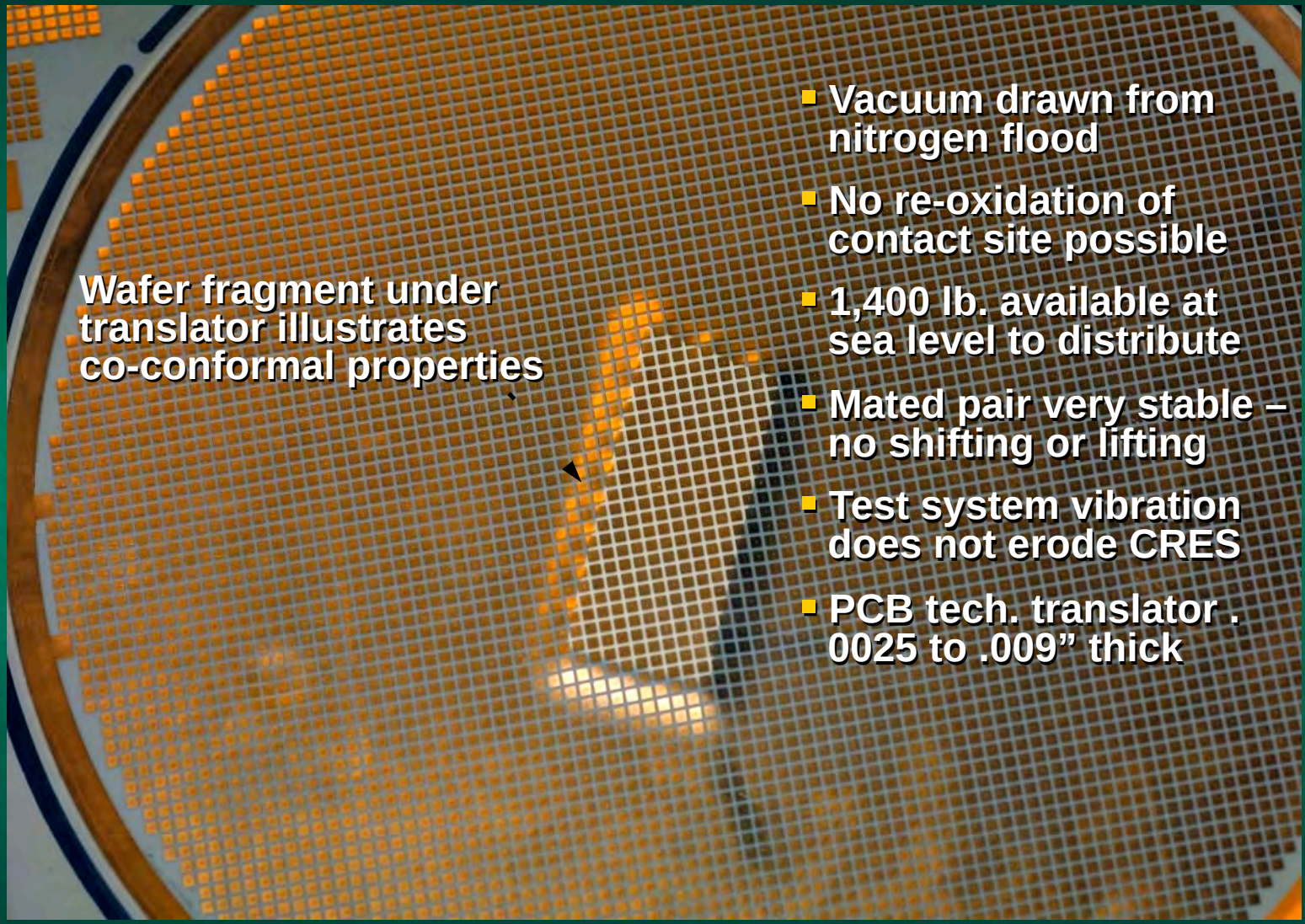


**Rogers 4350**
**PCB core**

# “Translated Wafer™”

- Translated Wafer™ has giant, tough pads with large pitch arranged for easy, low-cost contact
- Now the wafer die pads are never touched more than once
- Translator takes all the punishment
- If desired, all die pads on wafer appear on top of the Translator

# VACUUM MOUNTING OF TRANSLATOR IS CO-CONFORMAL




- Vacuum drawn from nitrogen flood
- No re-oxidation of contact site possible
- 1,400 lb. available at sea level to distribute
- Mated pair very stable – no shifting or lifting
- Test system vibration does not erode CRES
- PCB tech. translator . 0025 to .009” thick

# “Translated Wafer™”

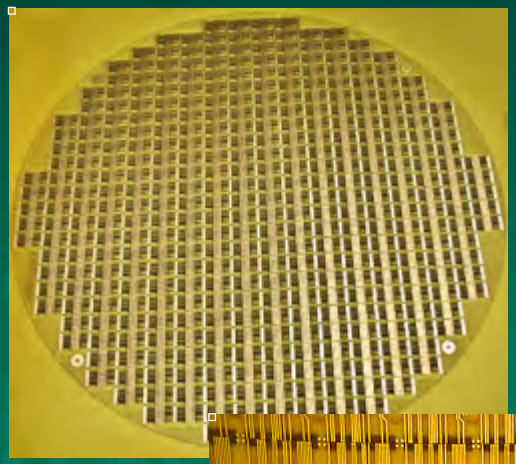
- NO OVERDRIVE - Translator is co-conformal with wafer
- CO-PLANARITY between wafer and Translator is inherent
- CRES using translators is equal to or lower than probe cards

# “Translated Wafer™”

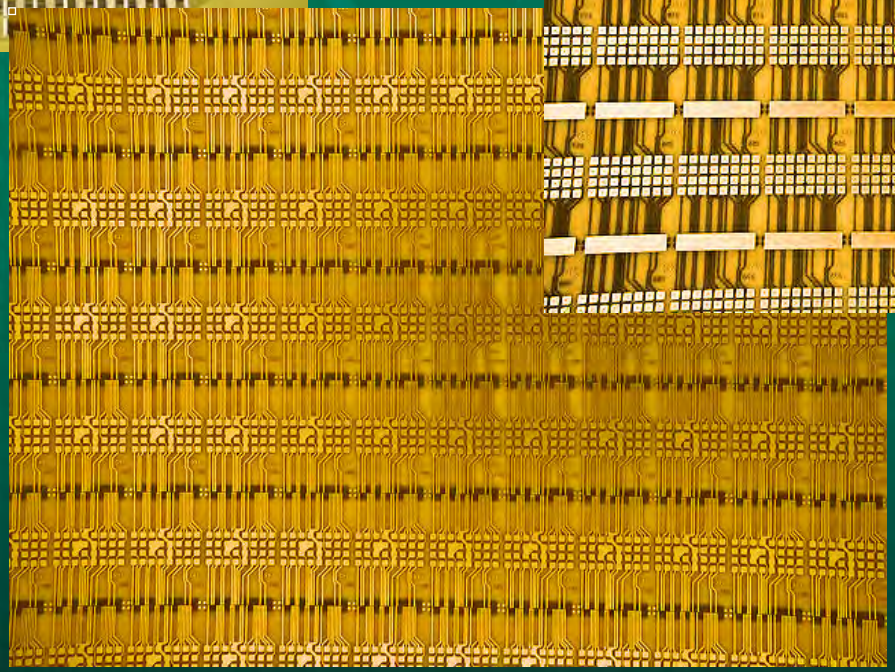
- EVERY LINE currently supports 56 Giga Bits on two-layer BT Epoxy
- Translator bumps are in a near vacuum drawn from a nitrogen flood
- Chaining die happens on Translator and is easy to design and fabricate
- Cleaning probe cards for example, 3 times per FOUP, is irrelevant

# ORGANIC PCB BASED WAFER TRANSLATORS

**Conventional two layer metal PCB substrate (.004”) with ½ oz. Cu and laser blind vias**



Wafer Side



Tester Side

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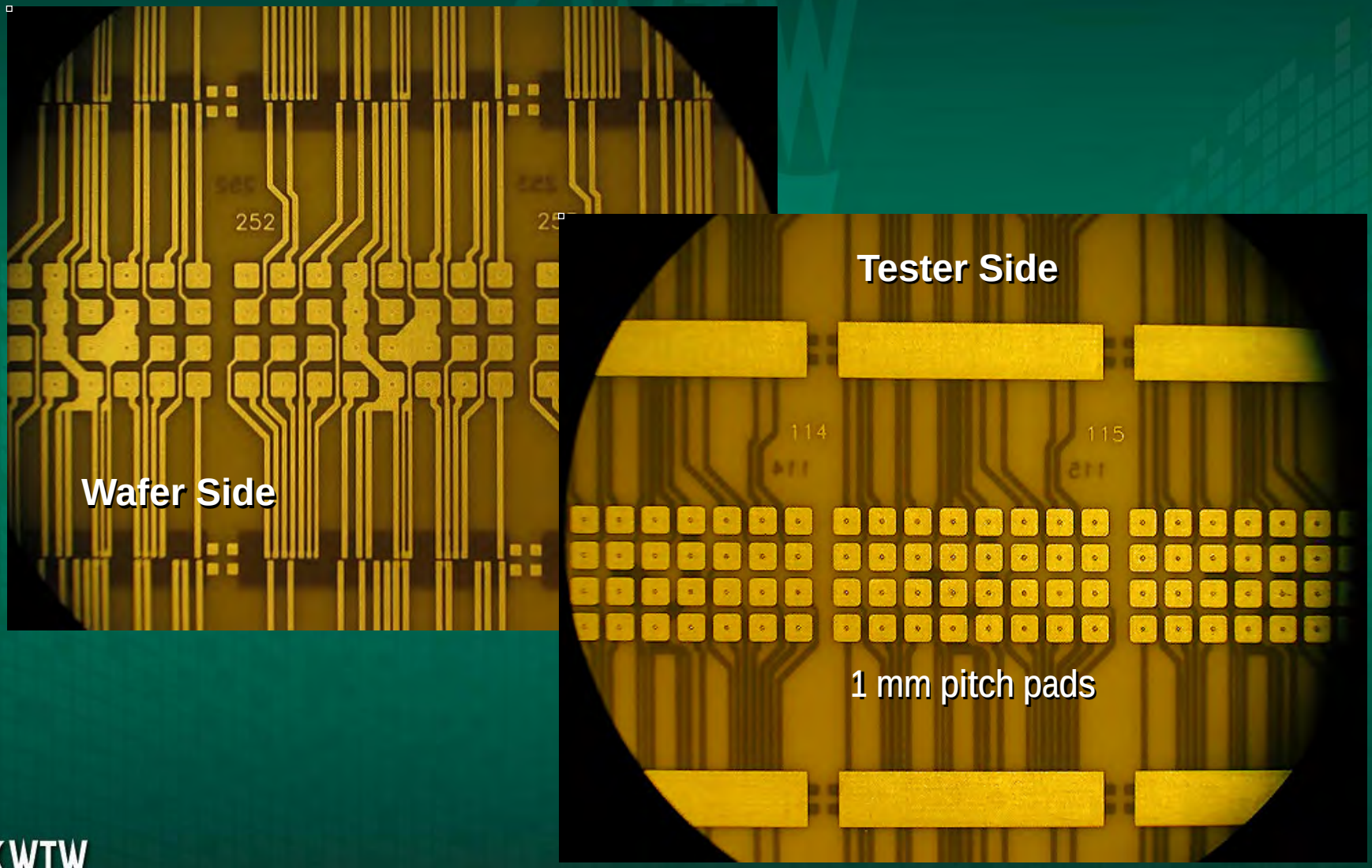
# ORGANIC PCB BASED WAFER TRANSLATORS

**Conventional two layer metal PCB substrate (.004”) with ½ oz. cu and laser blind vias**

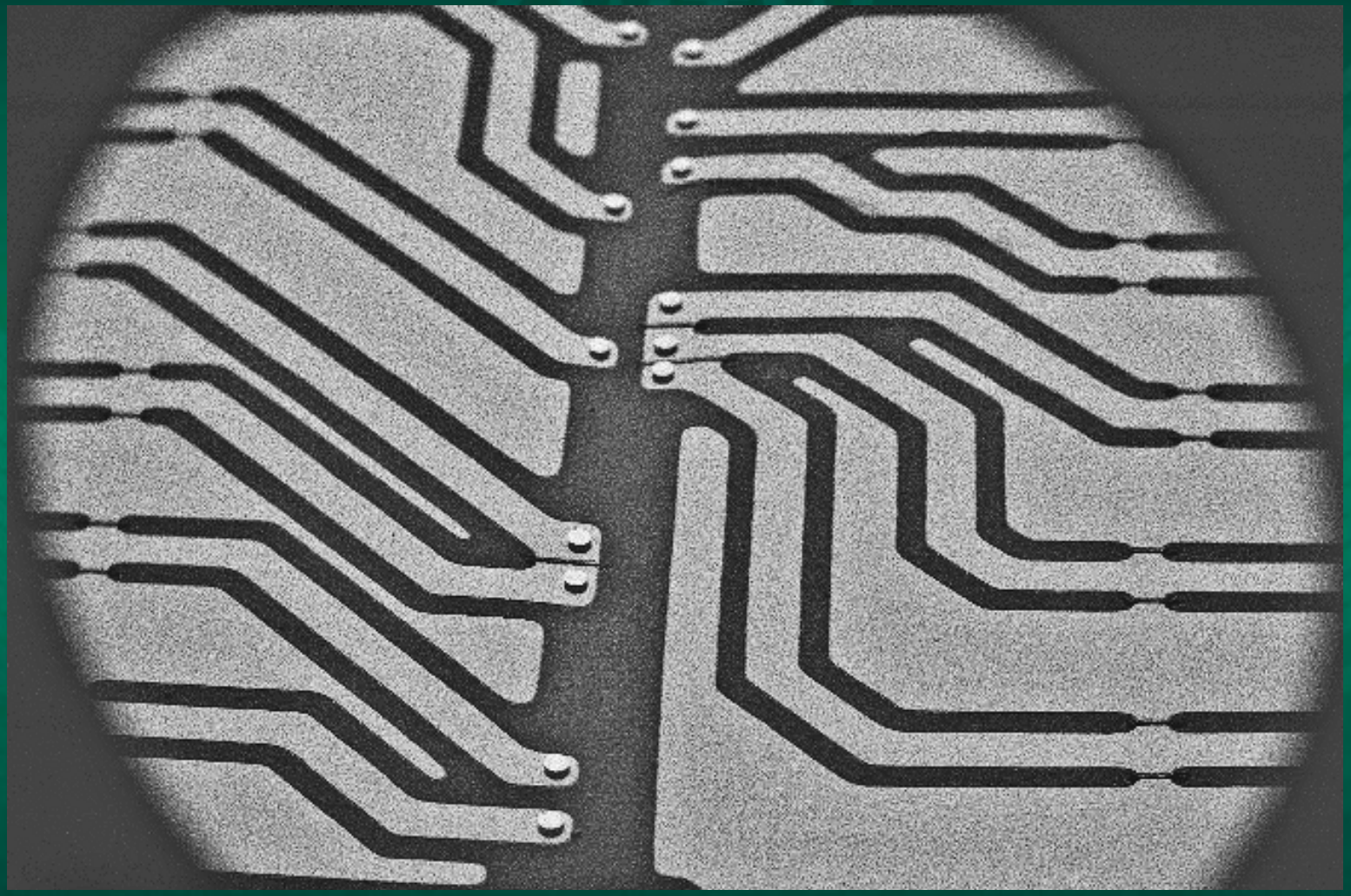


# Wafer Translator Facts

- Translators can be manufactured in
  - PCB / HDI Organic technologies - all types, flex or rigid
  - Semiconductor thin-film technologies – BCB, Poly, Oxide
  - WLCSP redistribution metal technologies
  - Ceramic substrate - etched thick film and thin film
  - Glass, ceramic, silicon, organic and most other substrates
- Translated Wafers™ typically fit in FOUPS
- Translated Wafers™ handle just like plain wafers
- Translators can carry relays, switches, caps etc.

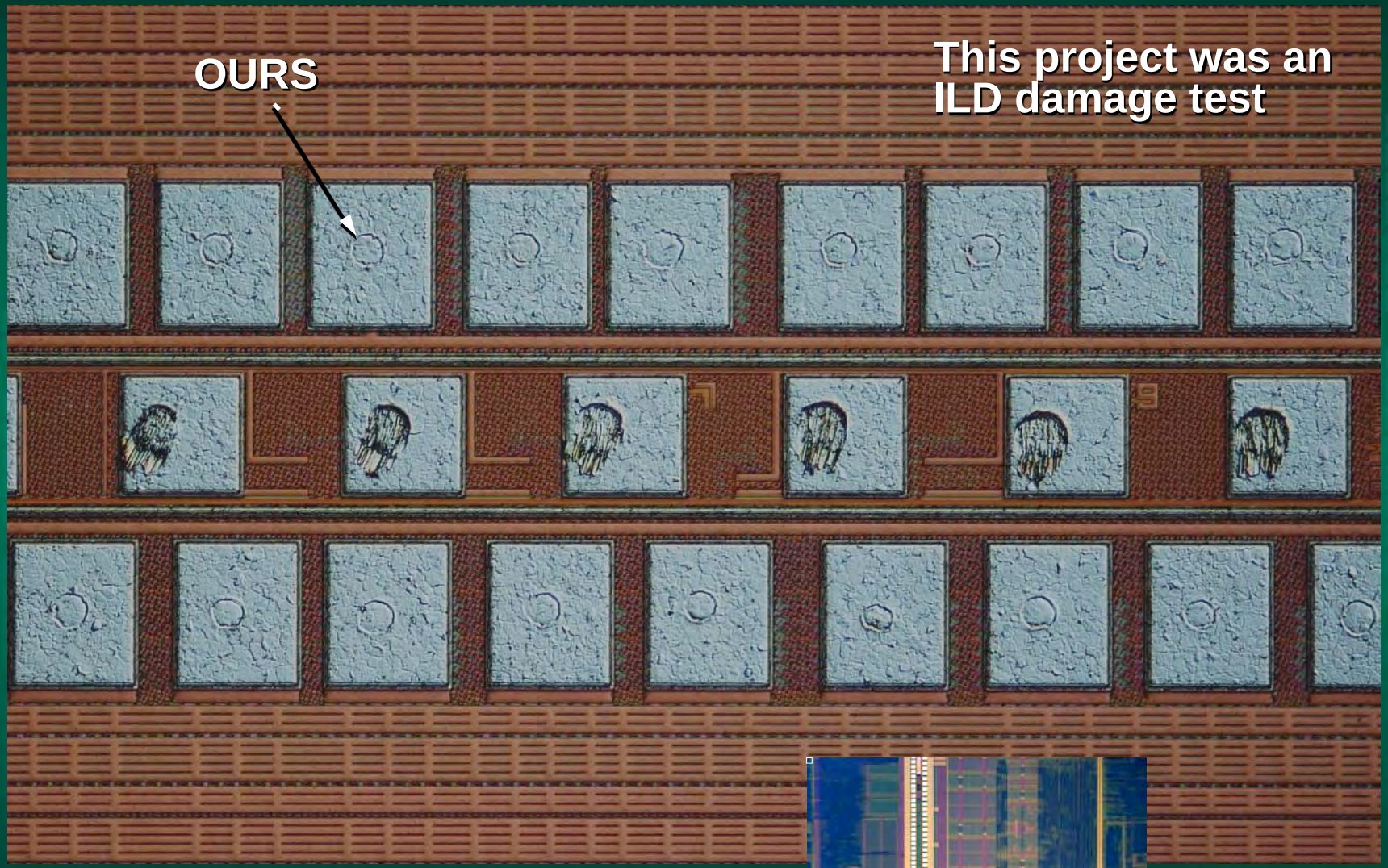
# TWO LAYER METAL BT-EPOXY TRANSLATOR

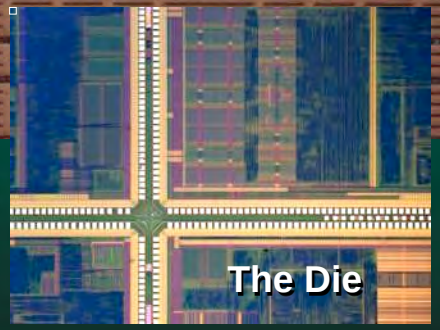
**½ Oz Cu - Controlled Impedance – 100% of Lines Support 56 Gigabit Data Rate**



**Organic PCB Fabrication - Contact Height Variation 1.3 Microns Max – Pre-Coin**

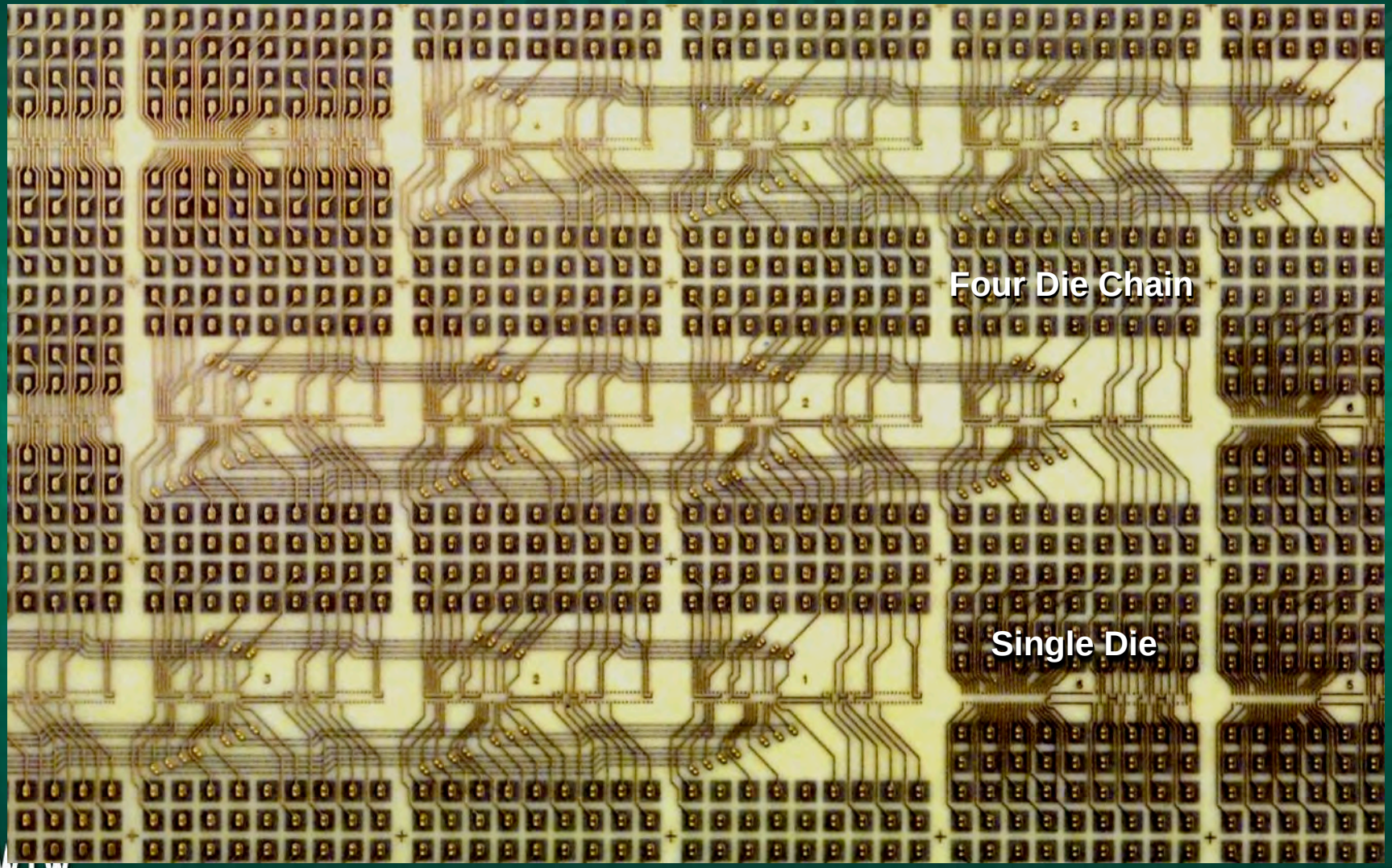
# 225,000 Contacts on a 200 mm logic wafer



# CHAINING DRAM DIE

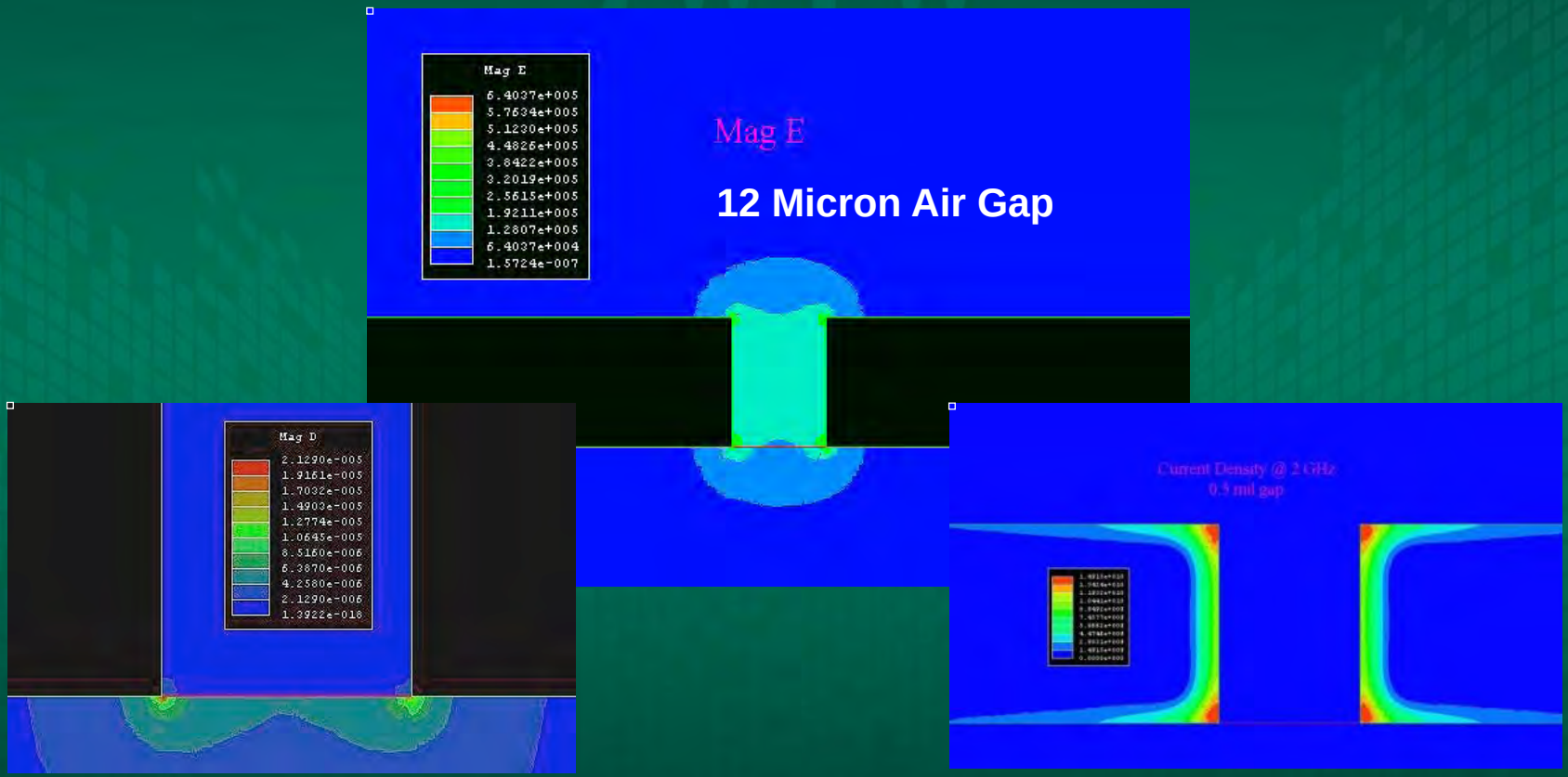
**Two-layer-metal organic PCB Translator supports DRAM chaining for test-channel reduction**



# WAFER TRANSLATORS often use CPW - CoPlanar Wave Guide Circuits

**Two-layer metal substrates gain certain advantages from CPW wiring**

## Some CPW Simulations



# WAFER TRANSLATOR

**Rigid Aluminum Nitride Translator Used As The Carrier Wafer During Wafer Thinning**

## A Tiny Fraction of Translator Patent Claims

**WAFER TRANSLATOR INVENTION**
Claim One

**TRANSLATED WAFER™ FORMED**
Creating
A Portable Assembly
Which then is moved from tester to tester where the Translator pads are probed

**A. Second patent to establish and claim the concept of a translator plate**

**1.** A method of wafer level testing, comprising: disposing a wafer onto a chuck such that a first major surface of the wafer is adjacent the chuck; disposing an anisotropic conductor onto a second major surface of the wafer, the second major surface of the wafer having a plurality of integrated circuits formed thereon, each of the integrated circuits having a plurality of pads; disposing a first major surface of a translator plate onto the anisotropic conductor, such that an electrical pathway is established between at least one of the plurality of pads of each of at least two of the plurality of integrated circuits, and corresponding electrical contact pads on a second major surface of the translator plate; engaging a clamping ring with the chuck and the translator plate; electrically coupling the corresponding electrical contact pads to a ***first tester***, and applying electrical signals from the ***first tester*** to the at least two integrated circuits; wherein applying electrical signal comprises providing power.

**B. First establishment and claim that wafer and translator form a portable assembly**

**C. First establishment and claim of single touchdown on pad even if probed several times**

**19.** A method of ***forming*** a portable assembly including a wafer, the assembly suitable for ***repeated testing of the wafer*** while preserving the integrity of the bonding pads, the method comprising: disposing a wafer onto a chuck such that a first surface of the wafer is adjacent the chuck, the chuck having isolation grooves therein; disposing an anisotropic conductor onto a second surface of the wafer, the second surface of the wafer having a plurality of integrated circuits formed thereon, each of the integrated circuits having a plurality of pads; disposing a first surface of a translator plate onto the anisotropic conductor, such that an electrical pathway is established between at least one of the plurality of pads of each of at least two of the plurality of integrated circuits, and corresponding electrical contact pads on a second surface of the translator plate; engaging a clamping ring with the chuck and the translator plate; electrically coupling the corresponding electrical contact pads to a first tester; and performing at least one electrical test on at least one of the plurality of integrated circuits.

**D. First establishment and claim of moving portable assembly from tester to tester**

**20.** The method of claim 19, further comprising electrically decoupling the corresponding electrical contact pads ***from the first tester***; moving the portable assembly; electrically coupling the corresponding electrical contact pads ***to a second tester***; and performing at least one electrical test on at least one of the plurality of integrated circuits.

**PROBE CARDS:**
Six probe marks
are put down with six tester insertions

**TRANSLATOR:**
One probe mark
is put down with six tester insertions

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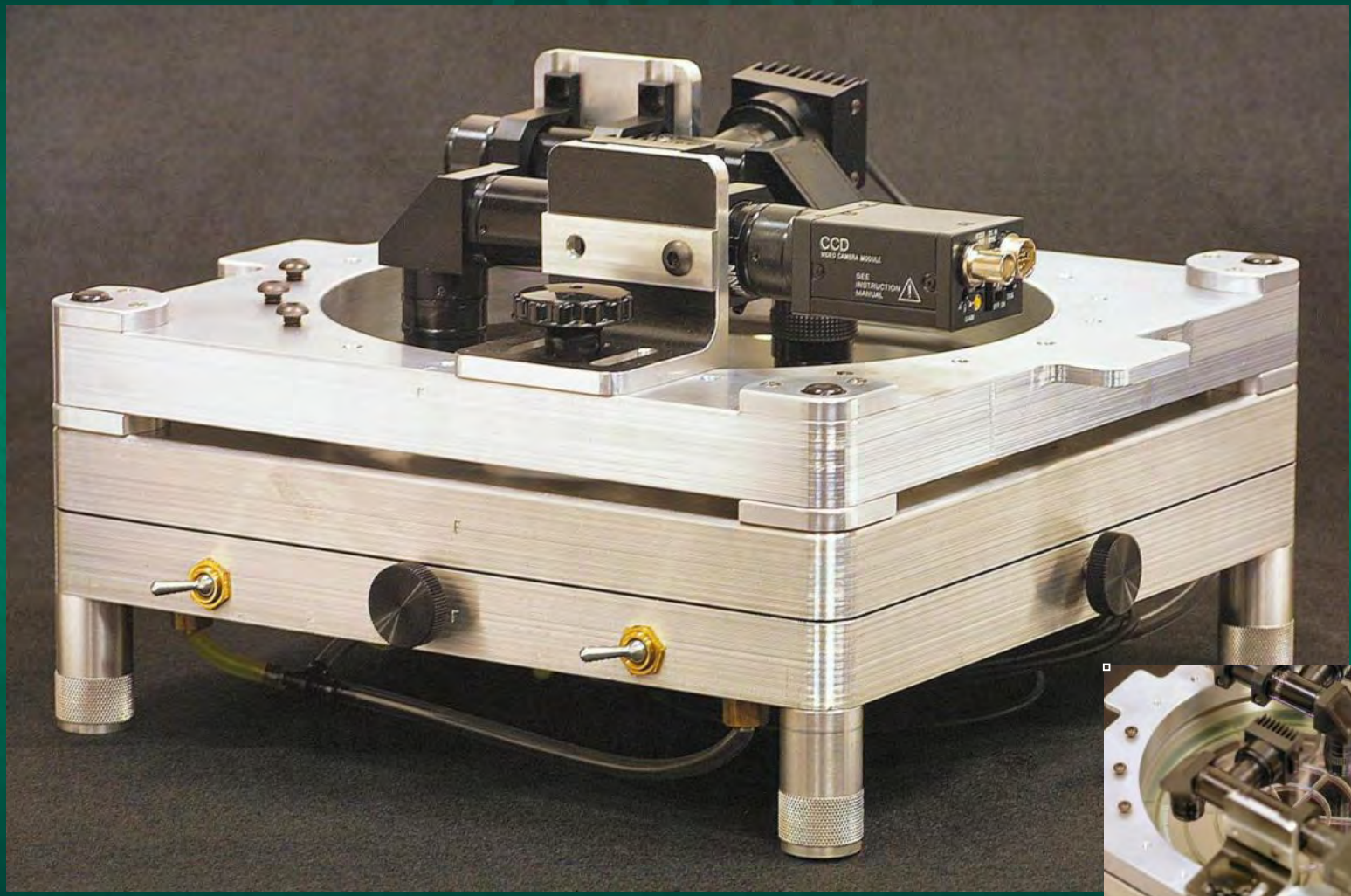
# DESK-TOP TRANSLATOR ALIGNER

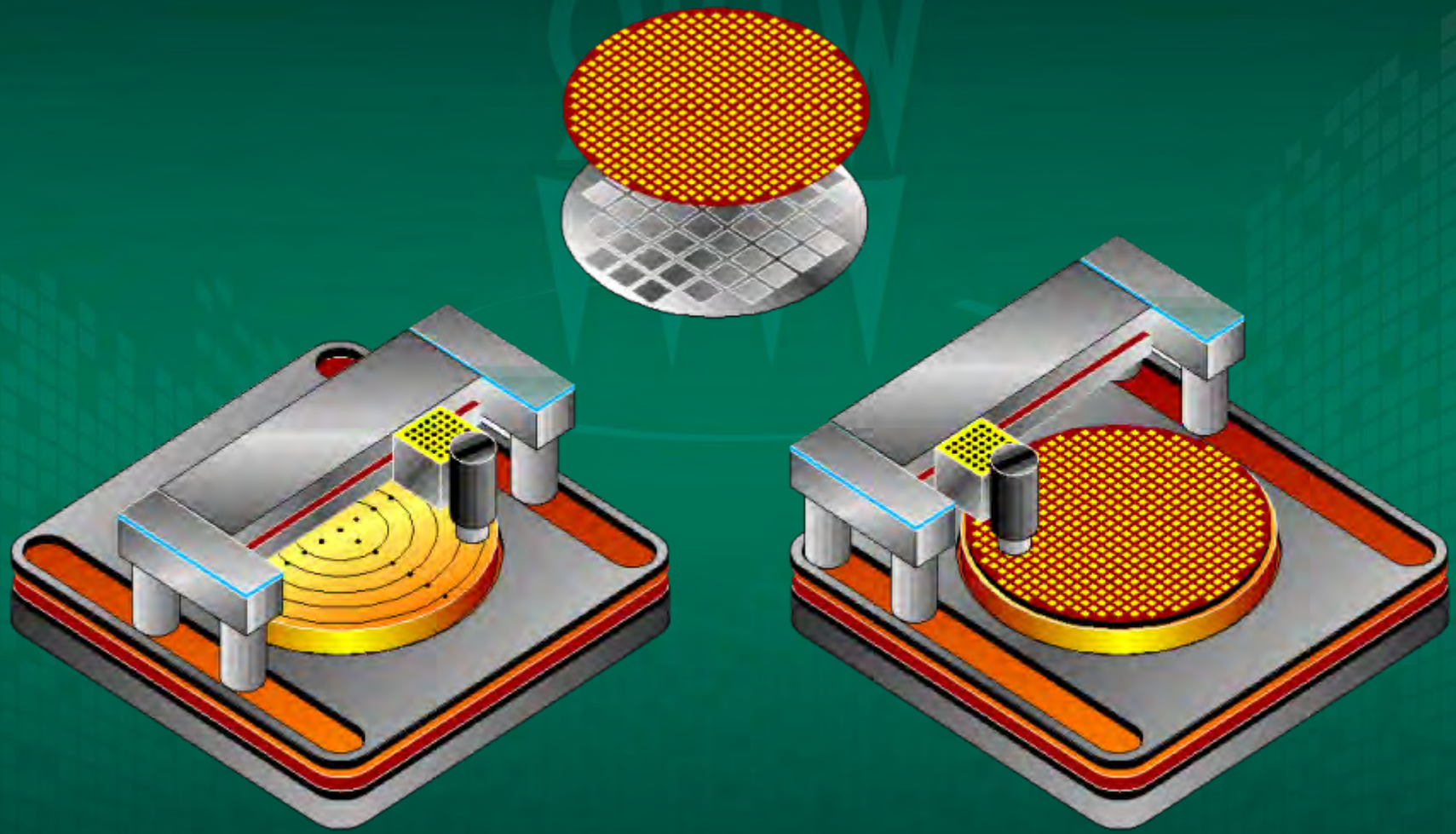
**Enables engineers to create a Translated Wafer™ on the workbench**

**A Translated Wafer™ can be probed with a DMM with no risk to the valuable "First Article" parts.**
**No probe station or probe card required**



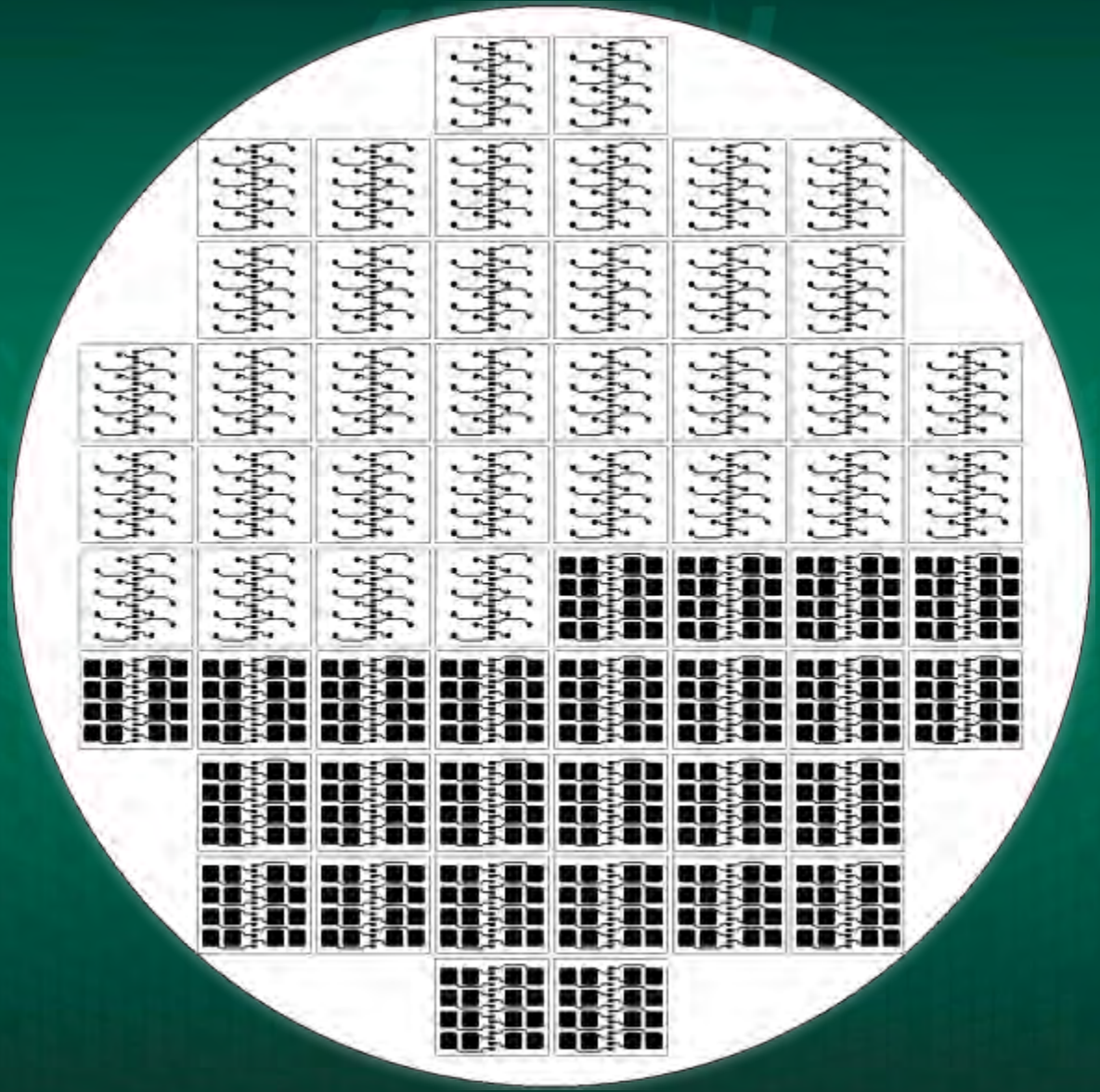
# DESK-TOP AUTOMATIC TRANSLATOR CONTACTOR

**When combined with the Translator Aligner, an engineer can test every die in a short time without probe cards or a prober**



# PRINT-ON, WASH-OFF TRANSLATOR

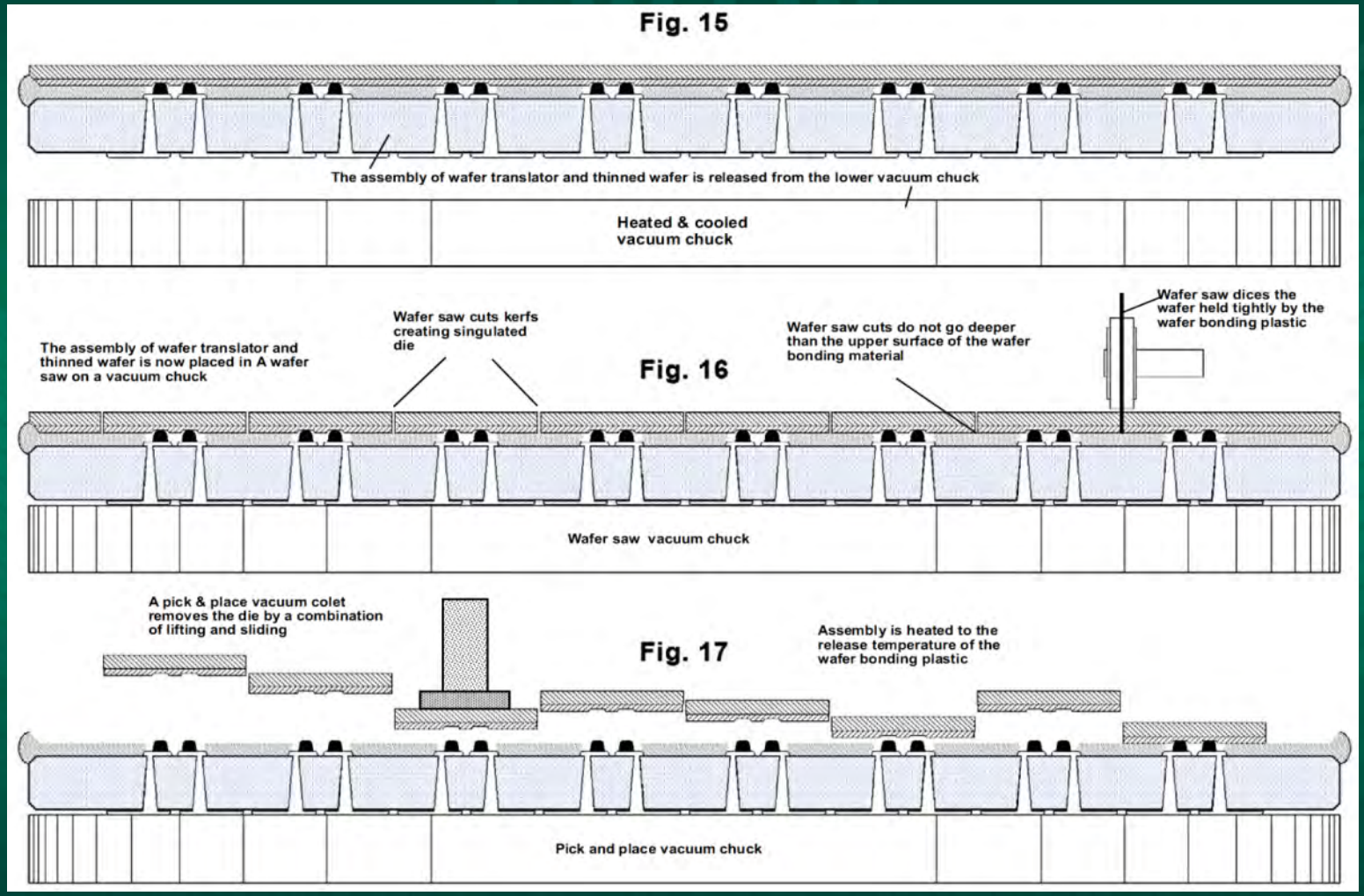
**Conductive Translator pattern is printed on wafer, cured, wafer tested then pattern washed off without marks on pads or residue on wafer**



# TRANSLATOR AS CARRIER WAFER

**Rigid Aluminum Nitride Translator Is Used As The Carrier Wafer During Wafer Thinning**

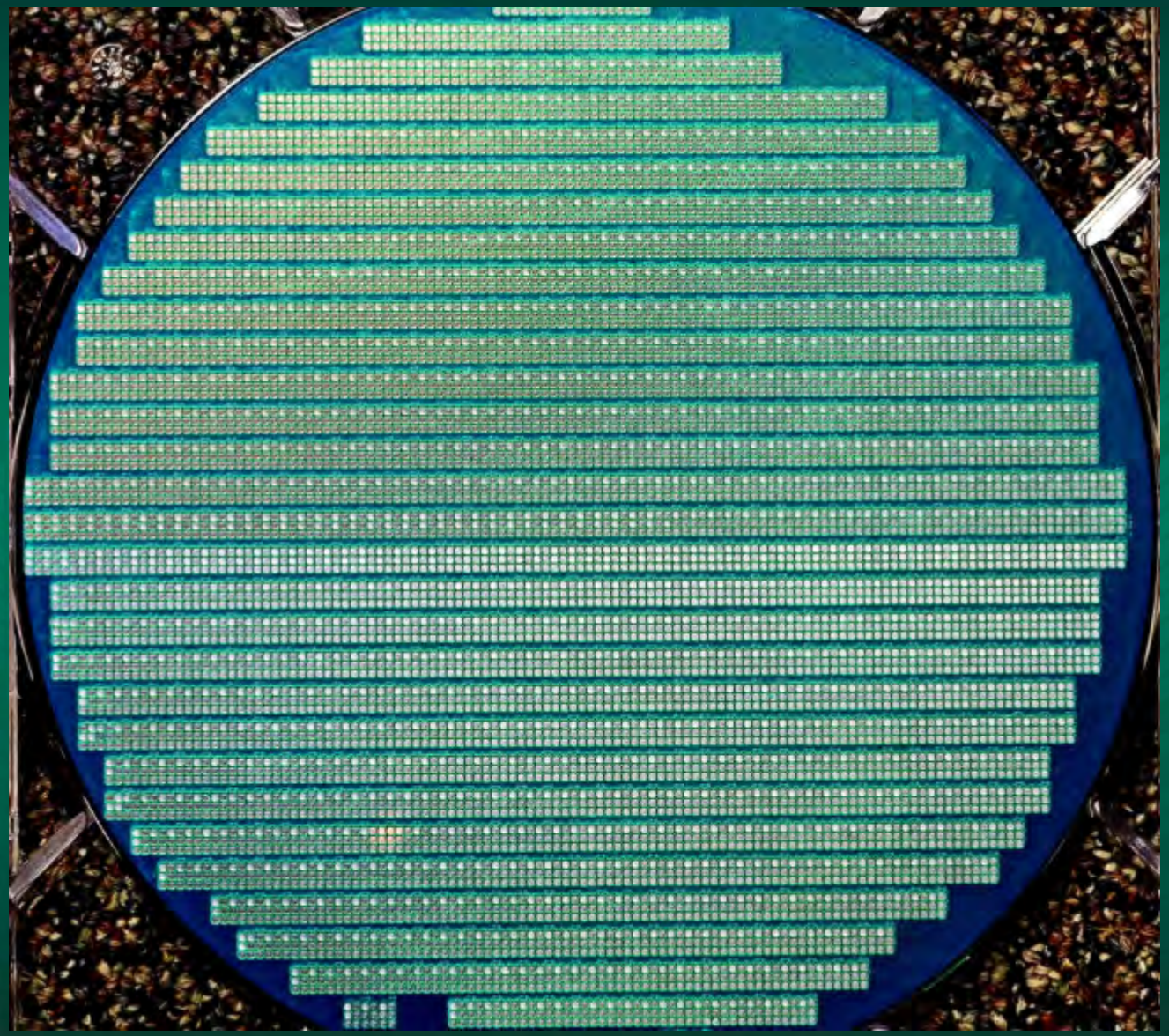
## Translator Enables Testing Of Thinned Die Even After Singulation




**Organic PCB Fabrication - Contact Height Variation 1.3 Microns Max - Pre Coin**

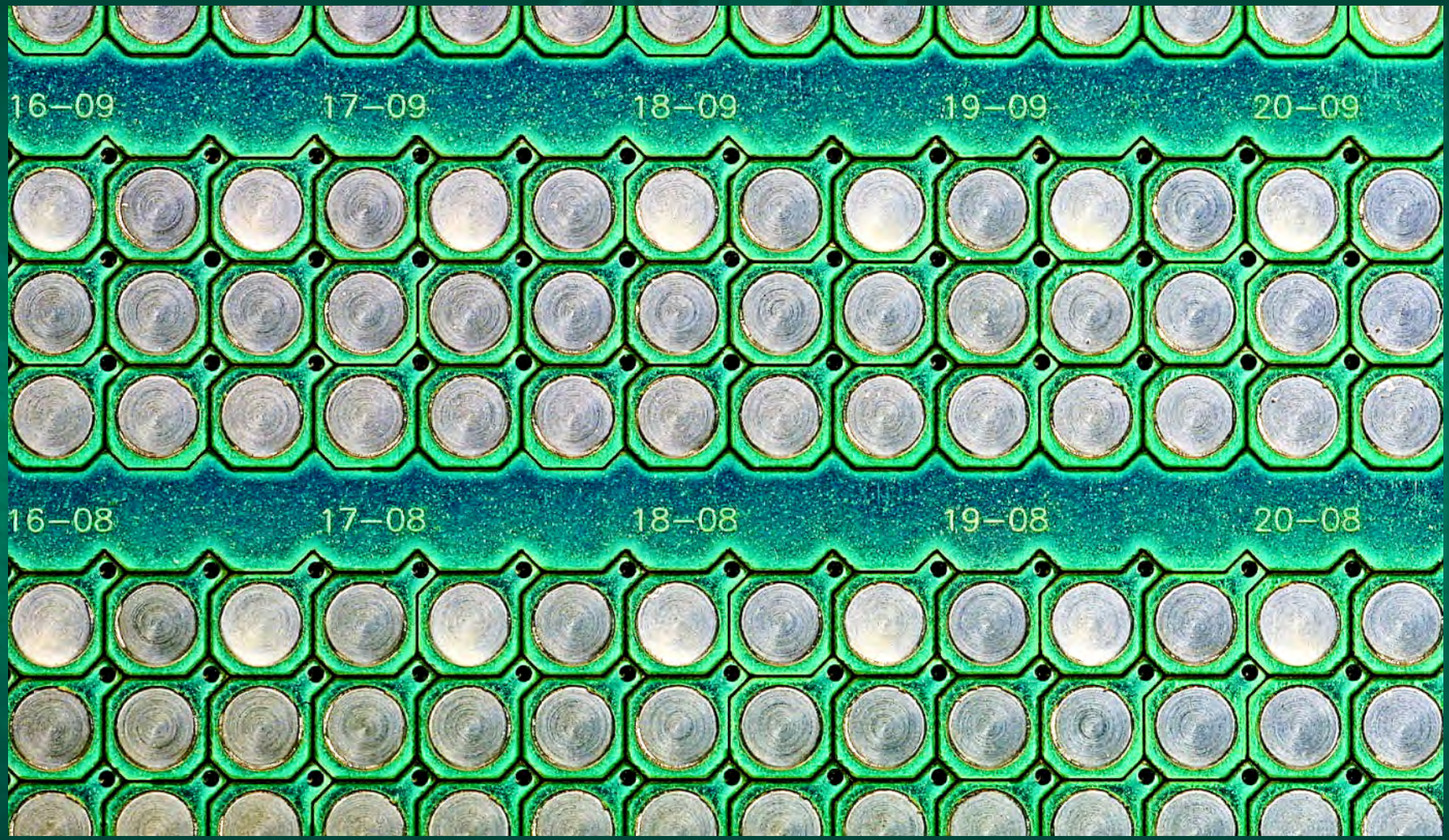
# - 100% Laser Defined Glass Wafer Translator -

**Vias in Mirror wafer with passivation cover as start point**



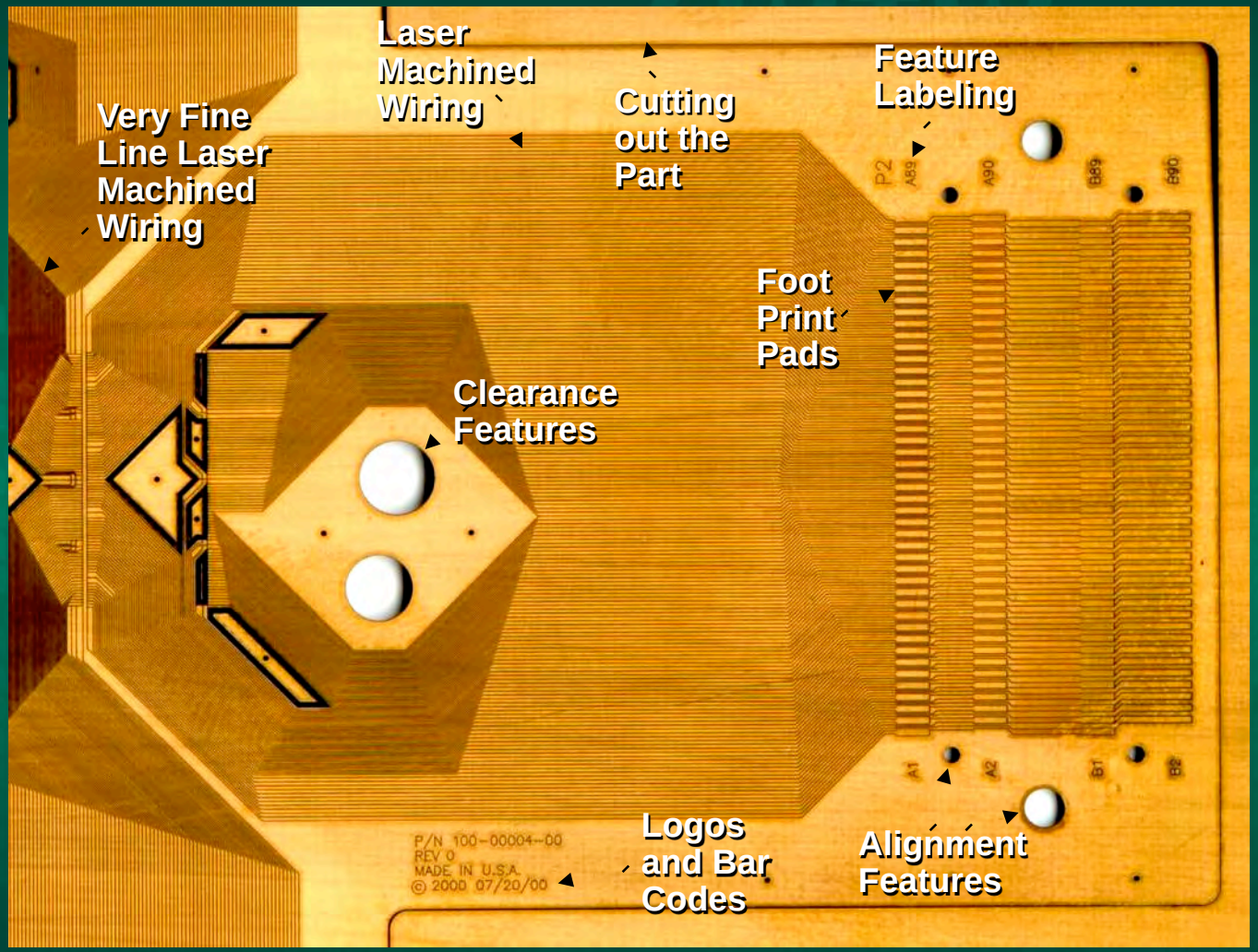
# - Laser Defined Translator -

**Pads Defined, Via Capture Pad Created, Passivation Opened, Sites Labeled, Ready to Test & Ship**



# Laser: Reduced Error Budget – Fewer Entries, Tighter Values

½ Oz Cu - Controlled Impedance CPW – 300 mm Translator takes 20 to 30 min. per side

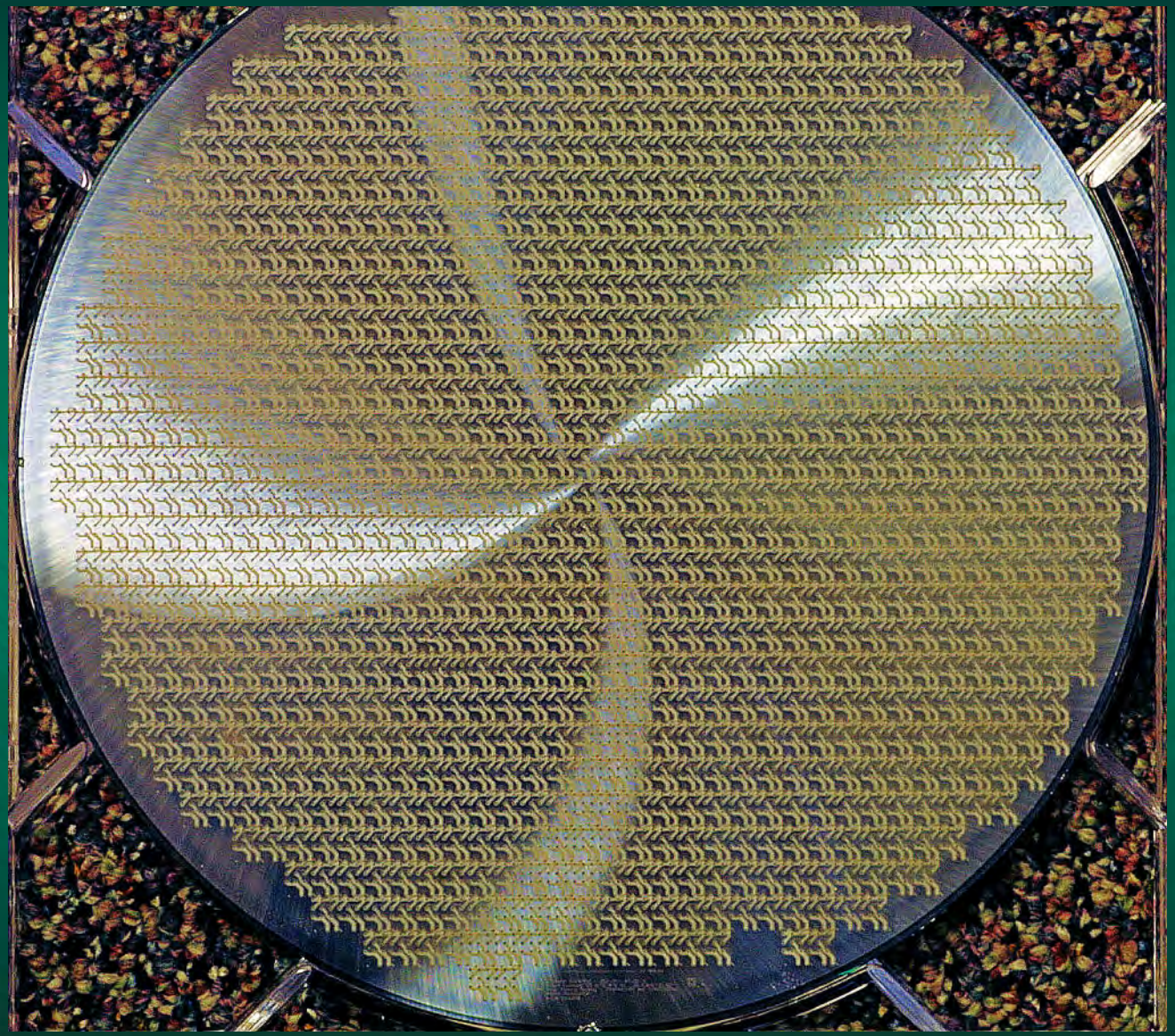



## ALL AT ONCE

- Traces
- Via capture pads
- Alignment features
- Labels
- Fold lines
- Footprint pads
- Logos
- Barcodes
- Clearance features
- Cutting out the fixture
- Single insertion - same coordinate system

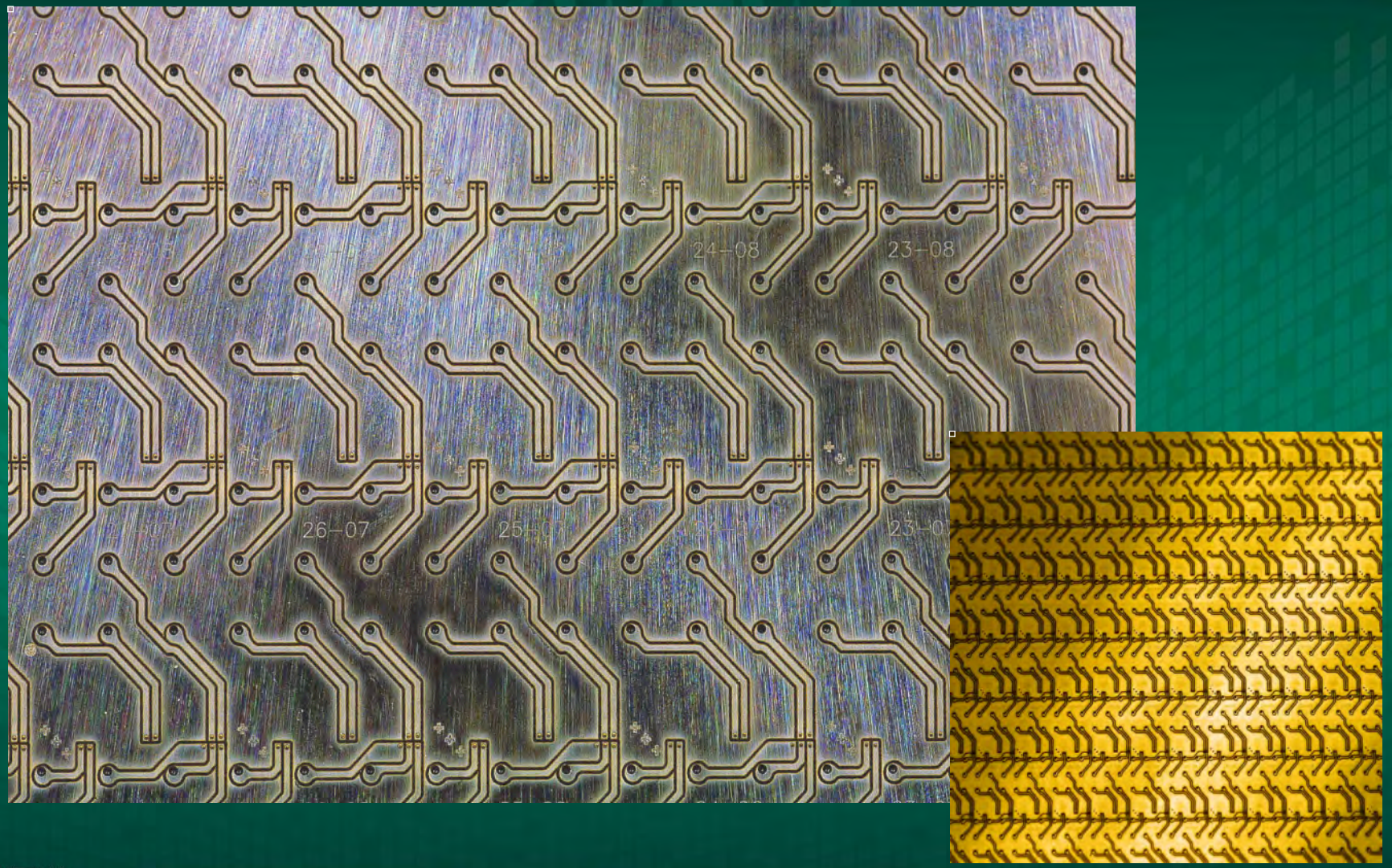
# - 100% Laser Defined Ceramic Wafer Translator -

## Vias in Mirror wafer as start point



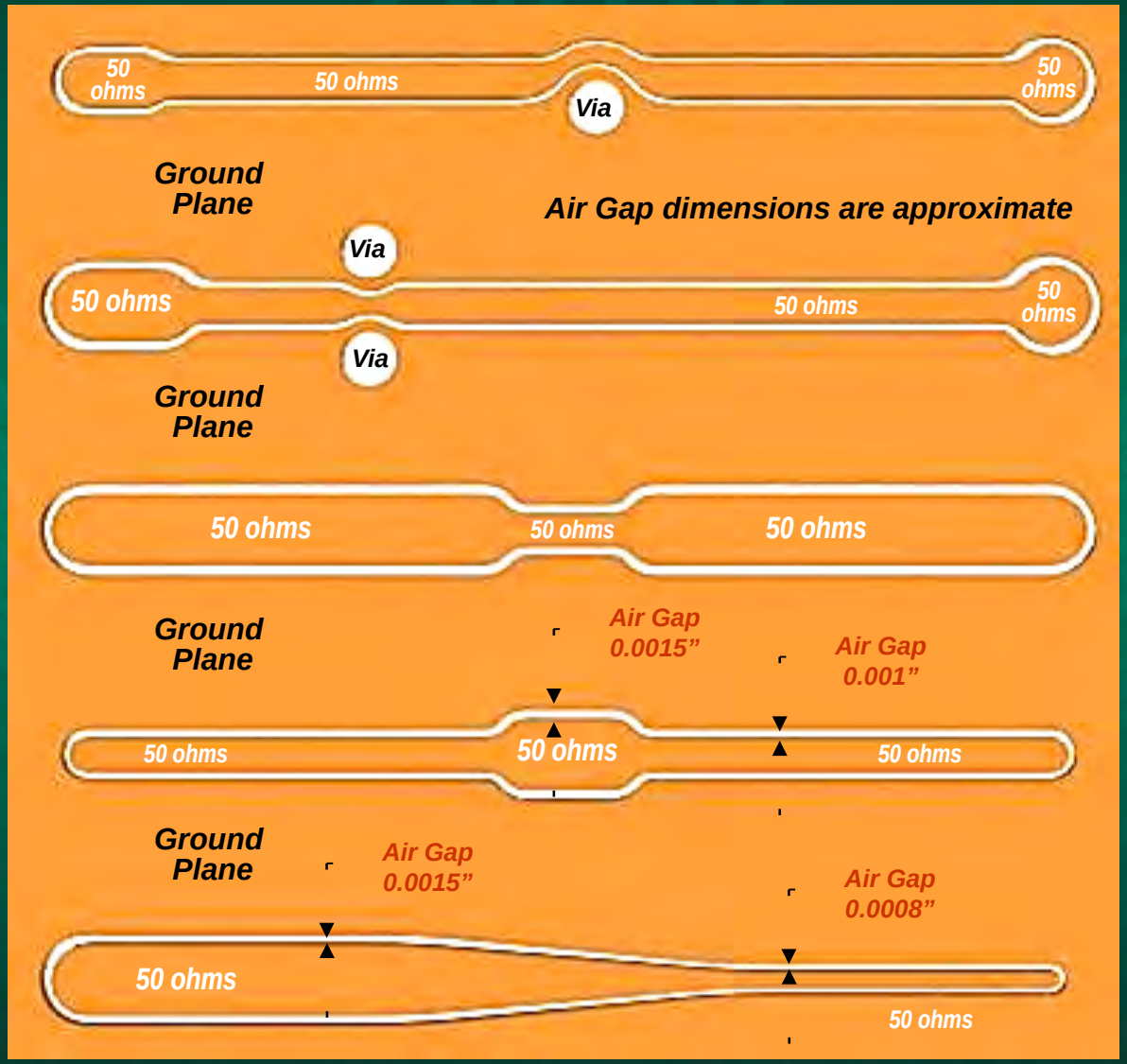
# - 100% Laser Defined Ceramic Wafer Translator -

**Vias in Mirror wafer as start point**



# Variable Line Width – Constant Impedance

**Laser Direct Creation of Wiring on Translator Enables Better Impedance Control +/- 1%**



# Thanks for your attention