IEEE SW Test Workshop

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A Fine Pitch MEMS Probe Card with Built in Active Device for 3D IC Test

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Overview

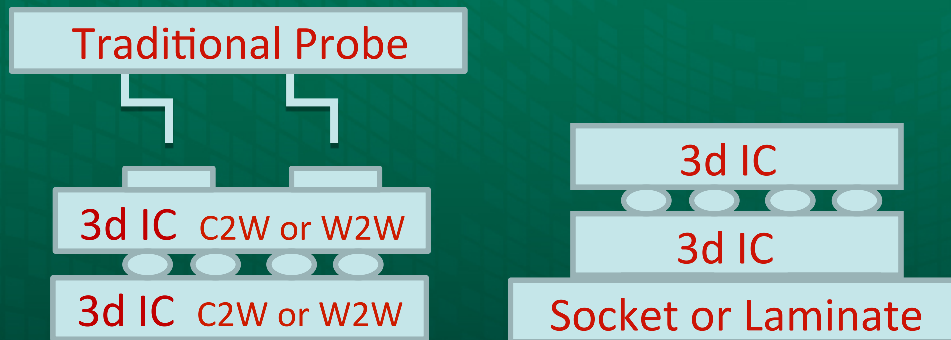
- 3D Silicon Technology: Role of Test
- New Probing Challenges
- Active Test Probe Benefits
- The Probing Solution
- Test Results
- Summary
- Acknowledgements

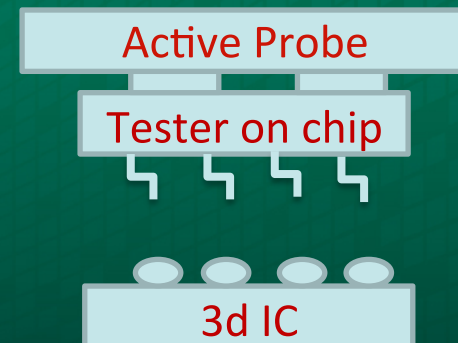
3D Silicon Technology : Role of Test

- **Why test before stacking?**
  - Design verification / Defect isolation
  - Reduce yield loss
  - Enable integration of chips from different suppliers

3D Performance Test
(After stacking - yield loss)

3D Performance Test
(Before stacking - 100% KGD)





New Probing Challenges

- **Silicon and Packaging Technology Scaling**
  - Smaller test contact geometries and finer pitches
  - New materials and handling systems
  - Packaging evolution, Example: CSP and WLP
- **New Test Insertions and More Test Partitioning**
  - New wafer, die, and SOC configurations (C2C, C2W, W2W)
  - Development of new test methods and test strategies
  - In process product functional test with increasing pin counts
  - Invent / redefine silicon debug and fault localization (yield learning)
- **Chip to Probe Centric Design For Test (New on-off chip DFT)**
  - Extend performance testing off chip (chip to chip interfaces)
  - ISIO buffering for ATE pin electronics
  - Need for fast, very high, stack data volume collection and chip repair
  - Dynamic power / thermal monitoring and control
- **Future Requirements**
  - New requirements for Protocol Aware and Application Specific test
  - Start planning for future on chip Optical Transceivers

Active MEMS Probe Card Benefits

- **Mitigate Rising Cost of Test (COT)**

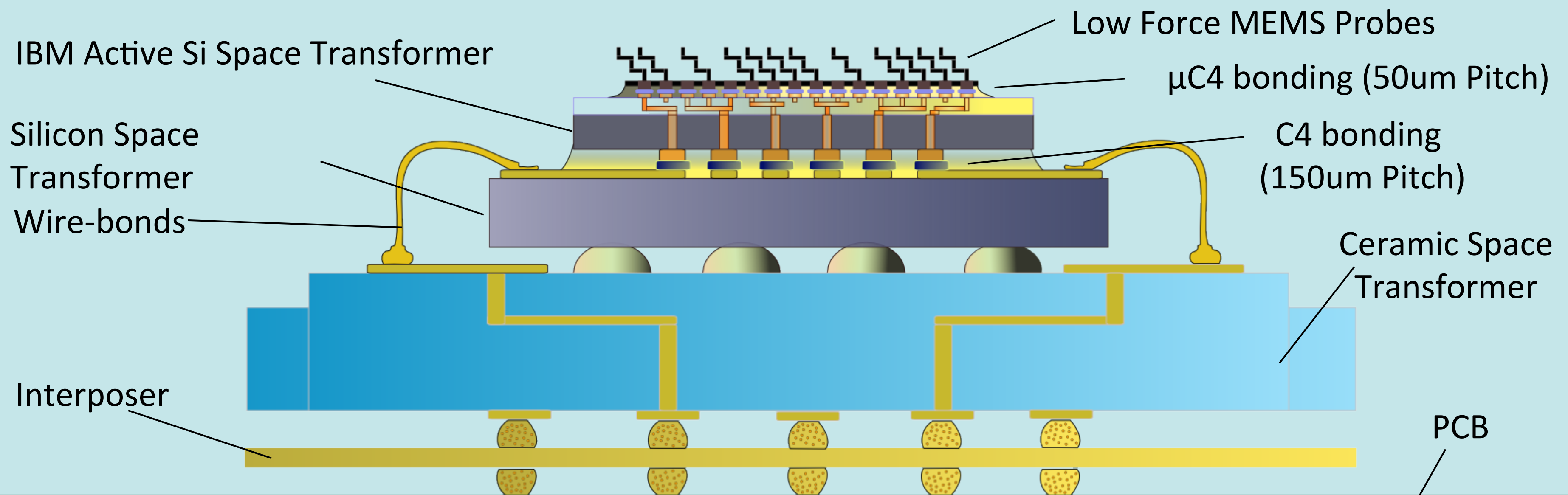
- **Extend ATE and Bench Instrumentation**
  - Enable wafer / die manufacturing test for scaled systems integration into silicon
  - Expand design verification, characterization capability
  - Enhance / enable future silicon debug and fault localization (yield learning)

- **Interstrata In-Out (ISIO) Buffering / Performance Testing**
  - ATE pin electronics and traditional probe loads too large

- **Chip to Probe Centric Design for Test (DFT)**
  - Extended Performance testing off chip and chip to chip

- **Future Active MEMS Probe Features**
  - No limit ABIST fail storage w/fast access time, rapid fail collection and chip repair
  - Customer defined Protocol Aware Functional Test (PAFT)
  - Customer defined Application Specific Integrated Test (ASIT)
  - Fine Pitch Hybrid Wire and Optical Transceiver Probes

Active MEMS Probe Card Architecture



Active MEMS Probe Cross-Section

MEMS Probe

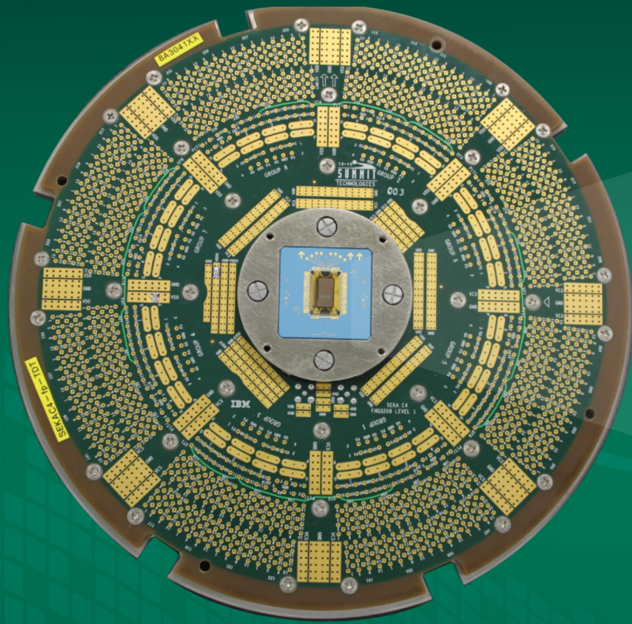
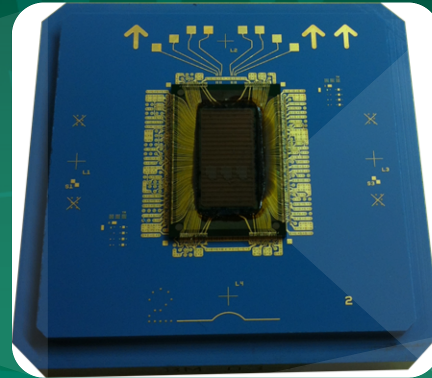
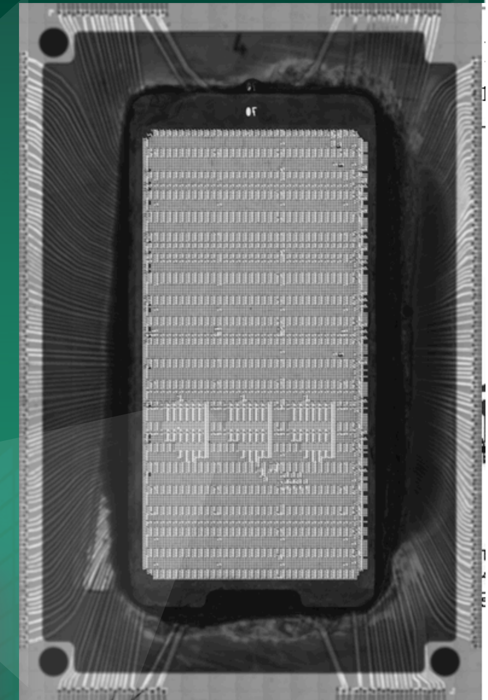
Interconnect µPillars

µC4 Bonding

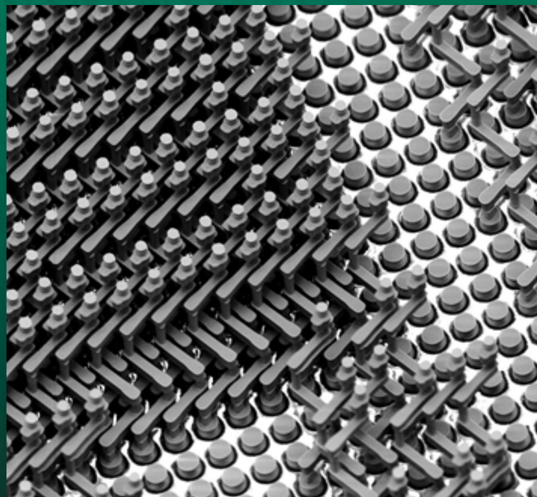
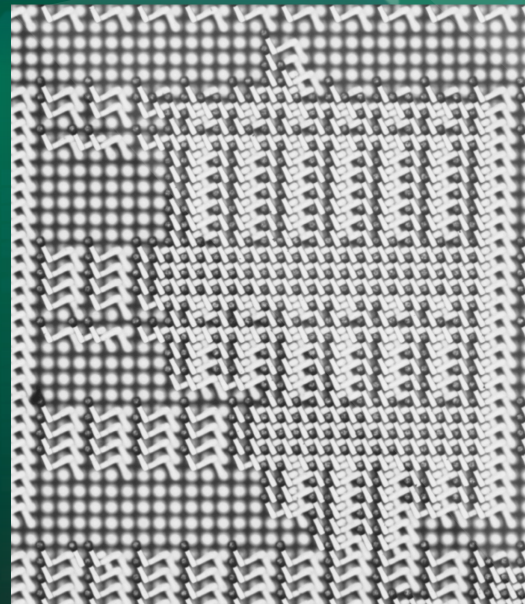
TSVs

Active Circuitry

Active MEMS Probe Card

- Over 1300 IO's
- 50µm min pitch
- 5k Pwr / Gnd
- 4 power planes

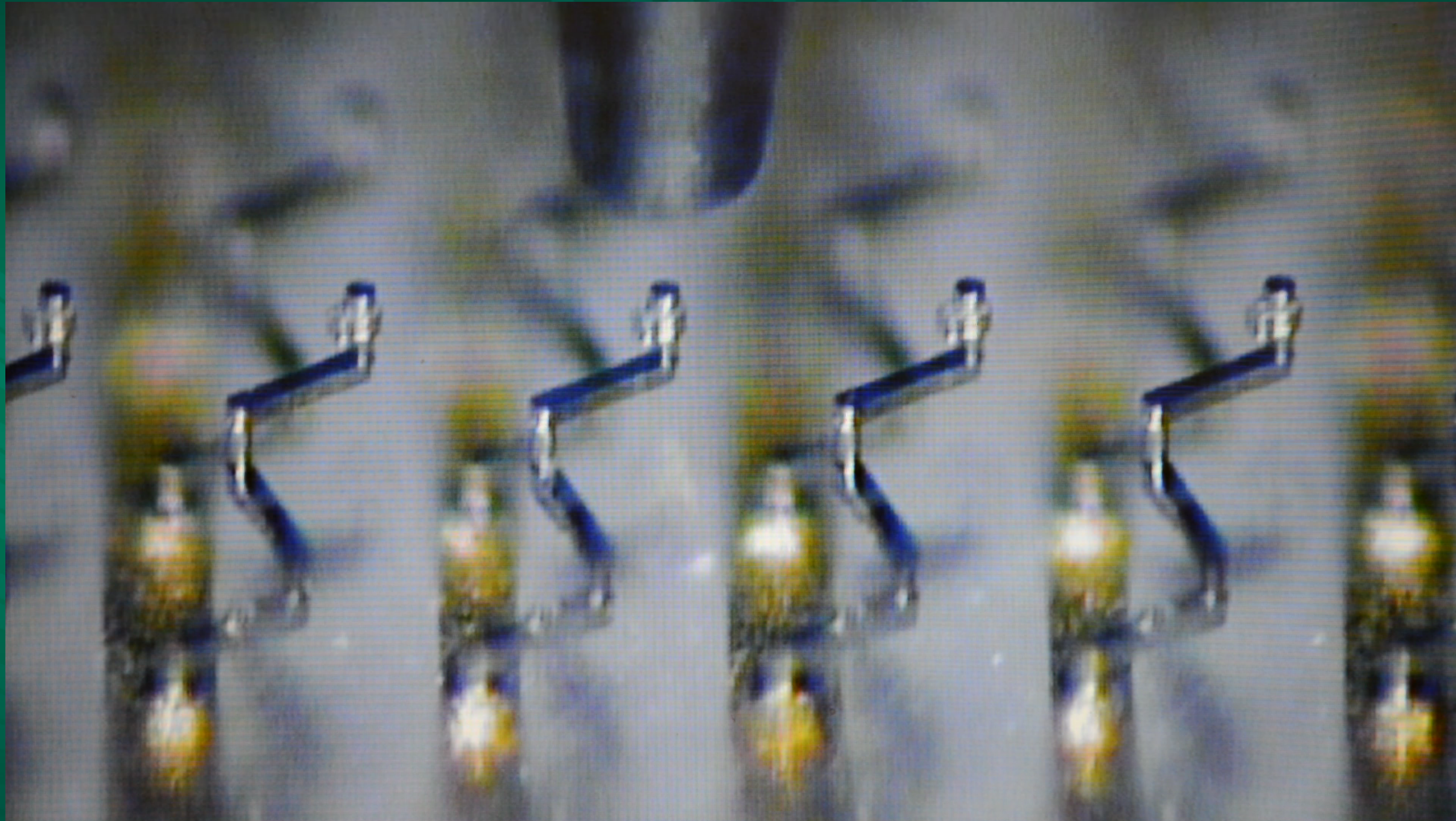



Why Low Force MEMS Probe?

- **Why MEMS?**
  - Wafer Scale manufacturing
  - Lithographic scaling and planarization
  - No probe count limitations
  - Short probe length for better electrical performance
- **Why Low Force?**
  - Minimal damage to all test contact surfaces
  - Thin silicon, thinner test pads, low-k dielectrics
  - Enable inline product test

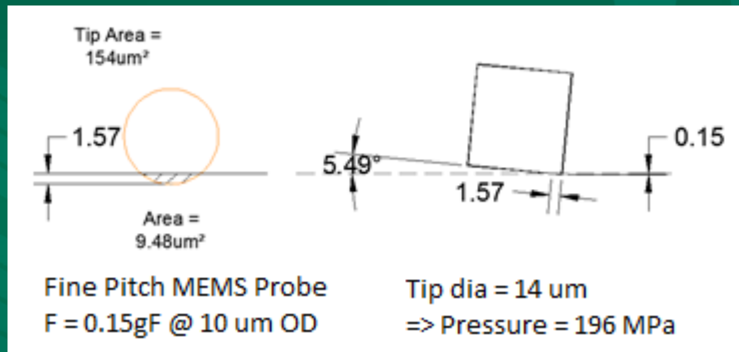
- **Fine Pitch MEMS Probe**
- **Operating OD: 15µm**
- **Scrub Length: 10-15µm**
- **Force: 0.2 gF**

Video of Fine Pitch Probe



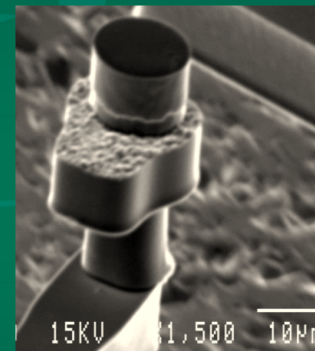
How Low Force MEMS Probe Works

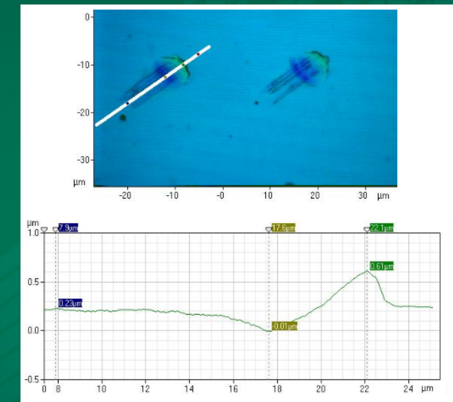
Low profile MEMS probe has shallow scrubbing angle ➔ high scrub pressure



Scrubbing action removes native surface oxide

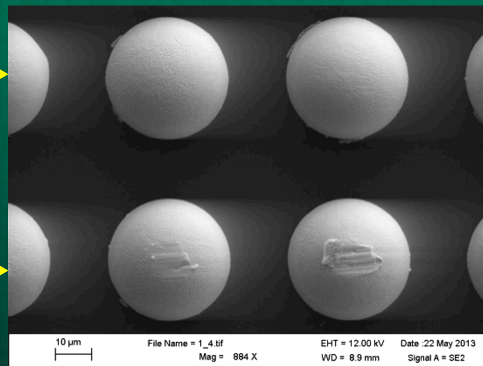
- Example: A 14 µm round tip produces a 0.2 to 0.4µm scrub depth on aluminum pad.

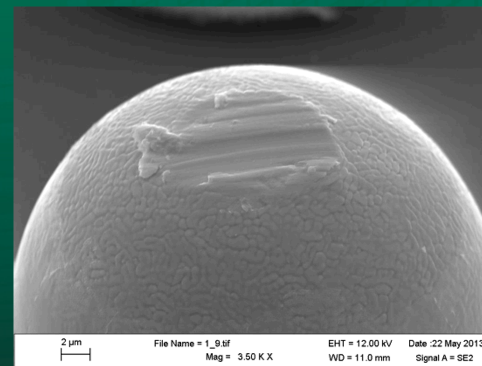


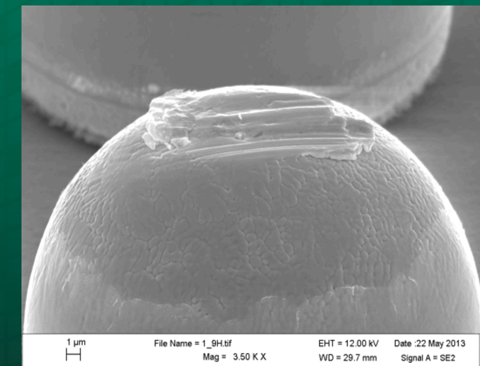


Un-probed µC4s

Probed µC4s



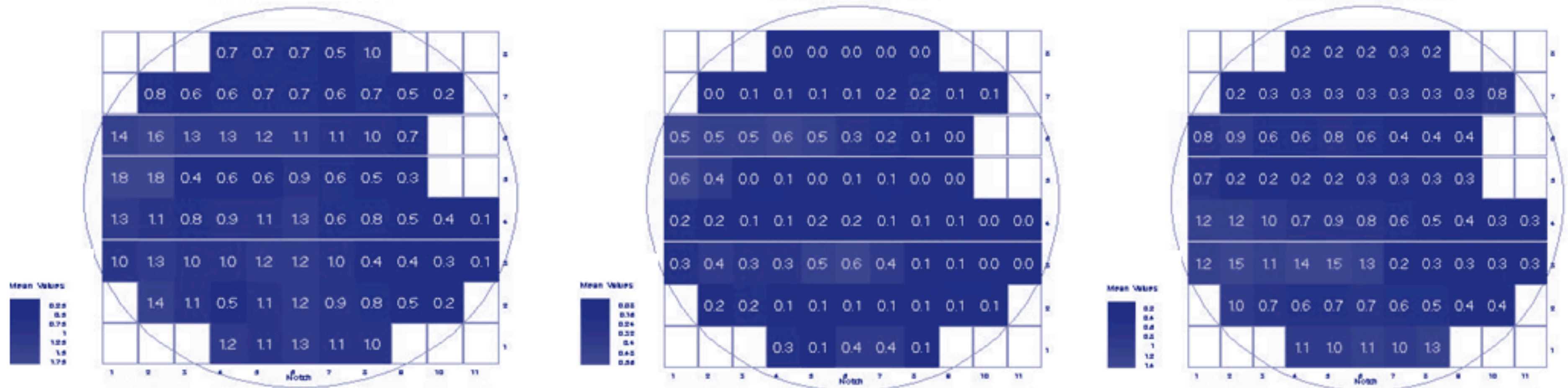




Parametric Test Results

- **Contact resistance on µC4 lead free solder bumps at -10C, 25C, and 85C**

Examples of Mean CRes Value per Die, 52 channels, 100mA current



14µm OD at -10C: <1.8Ω   14µm OD at 25C: <0.6Ω   14µm OD at 85C: <1.5Ω

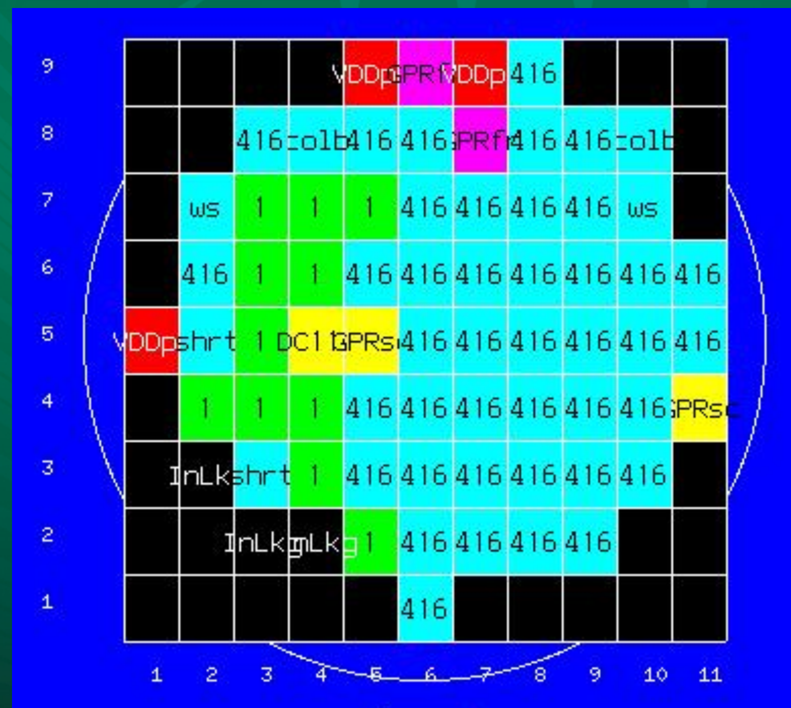
CRes each channel = Resistance on bumps (Path + CRes) – Resistance on Gold (Path + CRes)

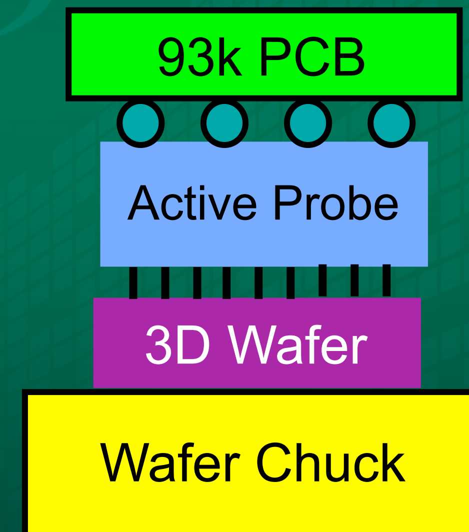
Functional Test Results

- **Wafer Test Flow**
  - External IO and Interstrata IO (ISIO) DC Pin Testing
  - Power Supply Shorts and Standby Current
  - Structural ATPG Scan and Logic Test
  - Array Built In Self Test (ABIST)
  - Performance Interstrata Input / Output (ISIO) Test
- **3D Wafer Level eDRAM and ISIO AC Characterization**
  - Fmax, Vmin / Vmax
  - Stack Power / Thermal
  - Logic , eDRAM, and ISIO Performance Measurements

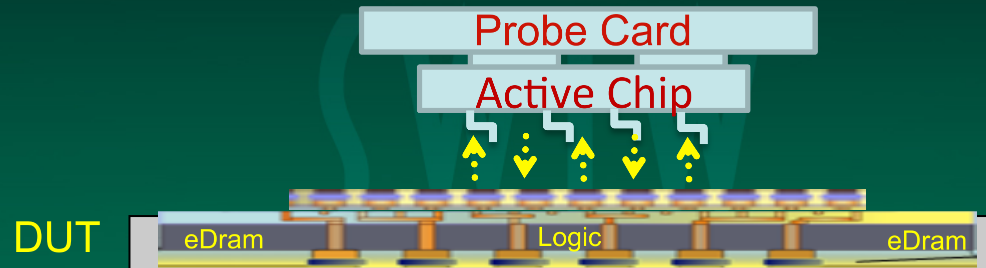
Functional Test Results

- **Superior AC coverage at wafer test enabled by Active MEMS card**
- **Enhanced Known Good Stack (KGS) via KGD sorting**
  - Same results on three µPillar surface metallizations (gold, copper, pb-free solder)





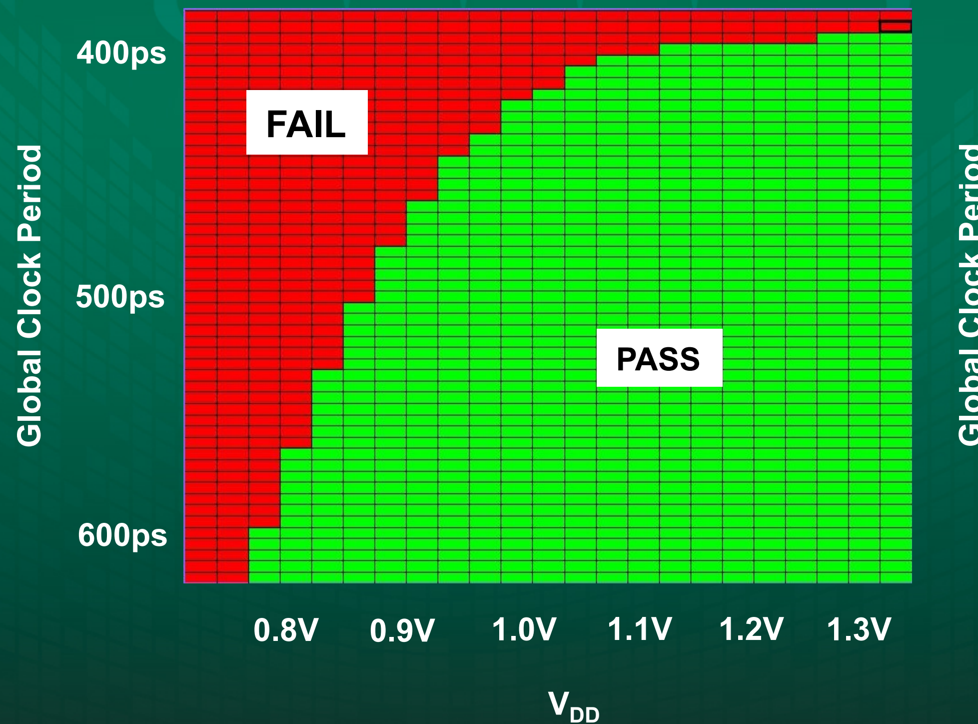
eDRAM and ISIO Performance Test @ Wafer Level



eDRAM, logic, etc. is 100 % tested through TSV, ISIO, C2C interconnects
Pre-stack for KGS

Good TSV Die for Stack

Fmax = 2.2 GHz , Vrange = .7v to 1.4v



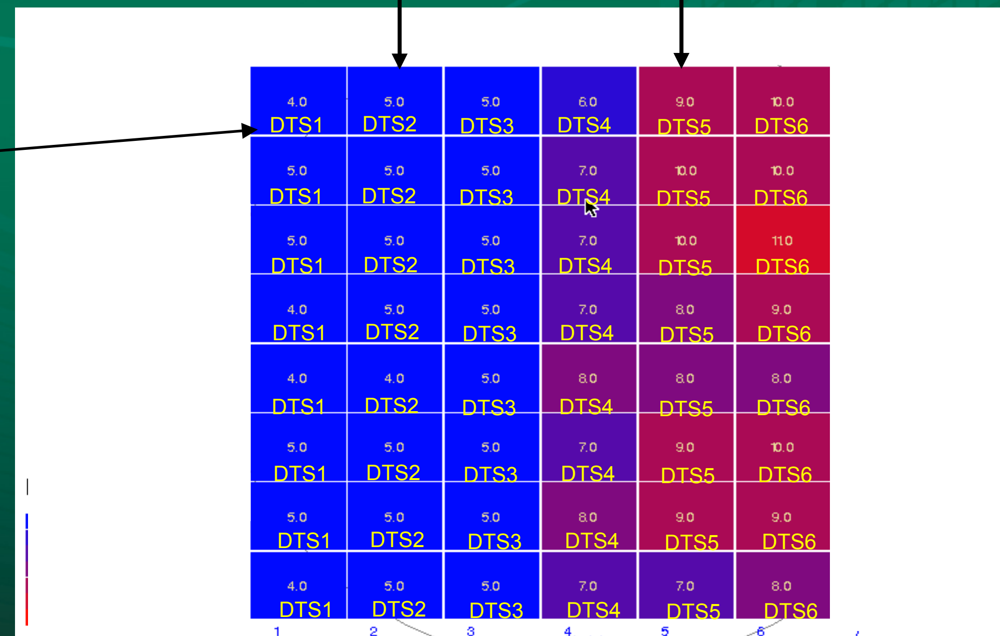
Dynamic Power and Thermal Monitoring

- **Active MEMS Probe enables Very Fast Response Time for Power Switching, Voltage Regulation, and Clock Controls**
- **Flexible for Adaptive Test, Sequential Testing, and Chip Test Partitioning**

Instant Temperature Control by Active Probe Card reducing switching activity

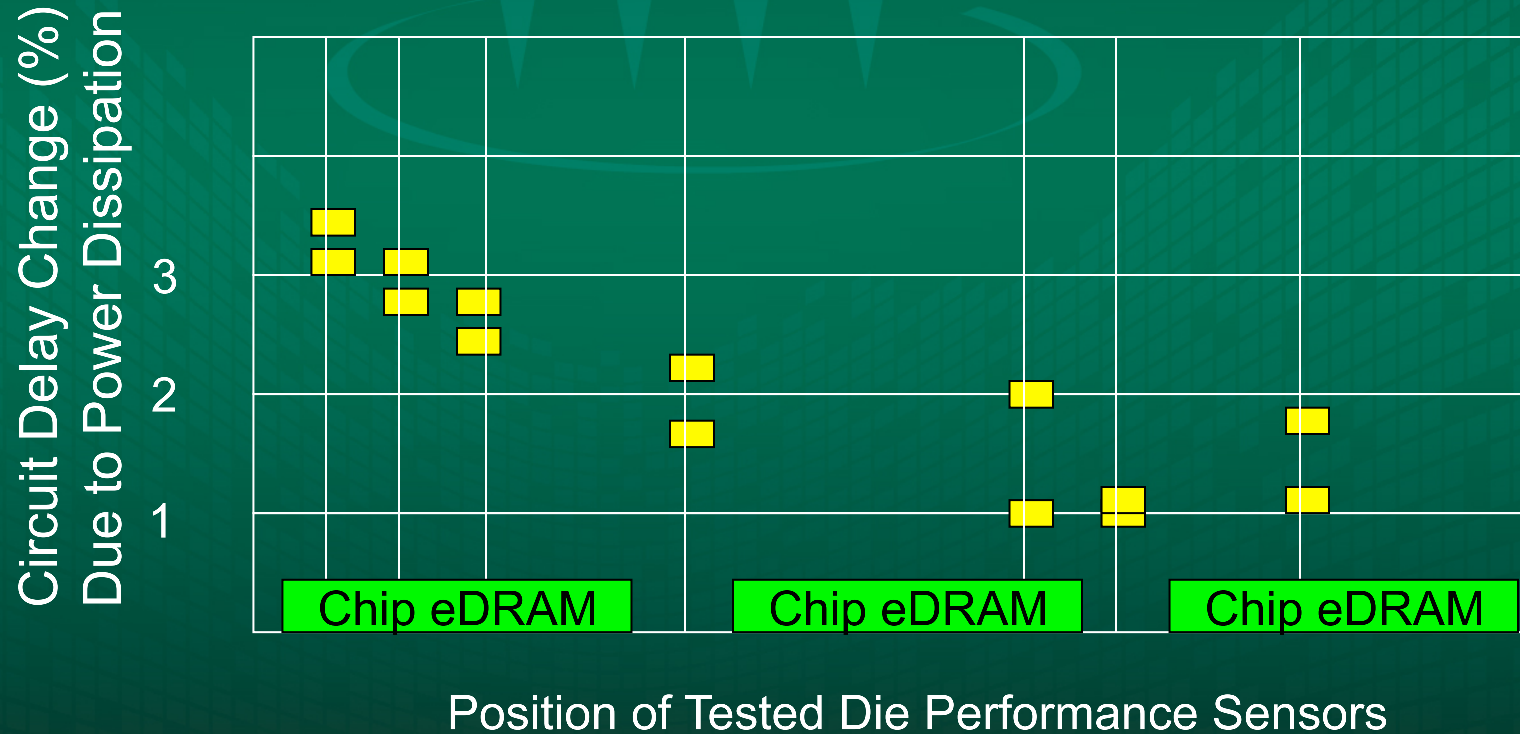
Temperature Rise due to high switching activity

Active Probe Card dynamically monitors die Thermal and Power Sensors



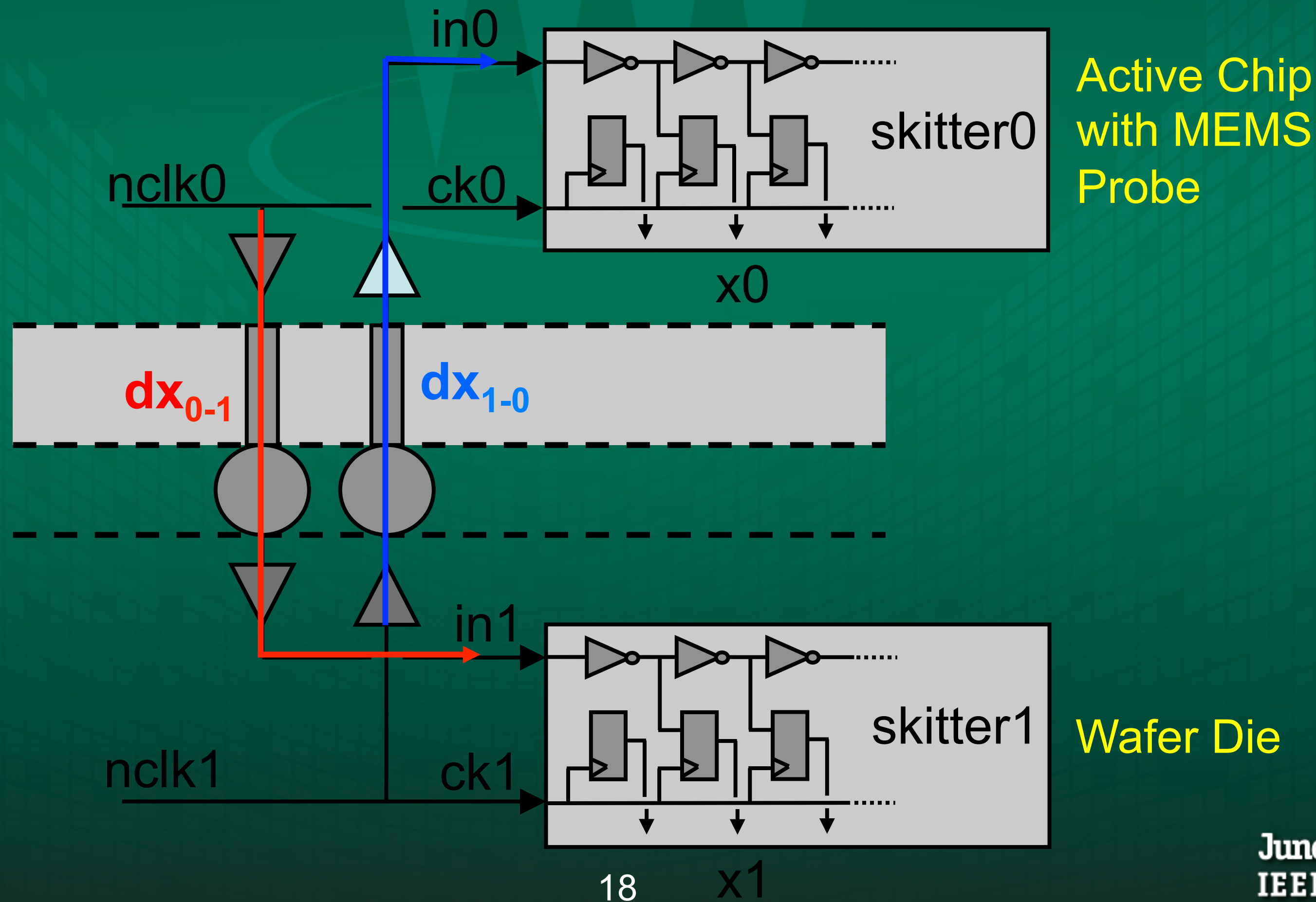
Performance Variation Localization

- **Performance variation can be quickly measured and isolated with Active MEMS probe measurement systems for AC yield learning at wafer test**



Active Probe Instrumentation

- Tested die and probe have pairs of performance measurement circuits
- dx0-1 and dx1-0 are measured for Clock Skew
- Clock Skew through MEMS and Tested Die measured < 15ps @ .8 - 1.3V



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Summary

- MEMS Probes successfully bonded to a thinned Active Device with TSV, attached to a complex space transformer stack in a fully functional probe card
- Demonstrated full DC and AC functional testing on 3D chips with 50µm pitch µPillars using Active MEMS probe card with low force probes

Acknowledgements

- Gary Maier / IBM SRDC project lead, test development
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- Lakshmikanth Namburi / AAI Sr. Director of R&D
- Yong Hong / AAI Probe Applications Engineering Manager
- Ting Hu / AAI Sr. Design Engineer
- Feng Lo / Lithography Manager
- Michael Chang / R&D Engineer
- Shahram Mehdizadeh / Sr. Plating Engineer
- Jane Tran / Packaging Engineer
- AAI Manufacturing & Quality Teams
- Greg Medrick / AAI General Manager , Advanced Probe Cards