IEEE SW Test Workshop
Semiconductor Wafer Test Workshop
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LPDDR2 and LPDDR3 High Speed Wafer Test for KGD

ELPIDA

Tera Probe

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Project Purpose

ELPIDA

High speed wafer evaluation

KGD business

TeraProbe

High speed wafer test service

High speed Probe Card technology development

About Tera Probe

Teramikros

・WLP Process Subsidiary in Japan

Tera Probe Headquarters

Tera Probe Hiroshima Operation Center

・Focusing on D-RAM & Other Memory

Tera Probe Kyushu Operation Center

・Focusing on SOC, CIS, Analog and other devices

TeraPower Technology Inc.

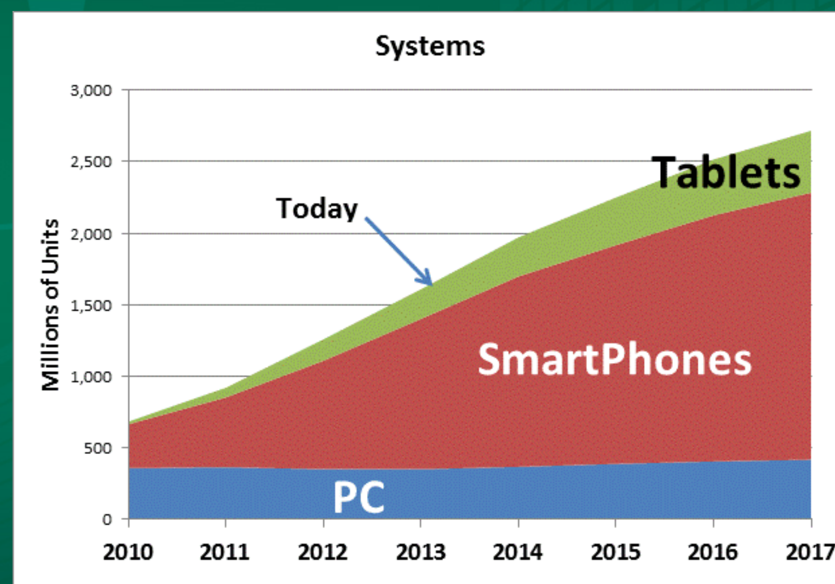
・Subsidiary in Taiwan

Overview

- Background
- Test System
- Probe card architecture
- LPDDR2/LPDD3 evaluation
- Next step
- Summary

Background

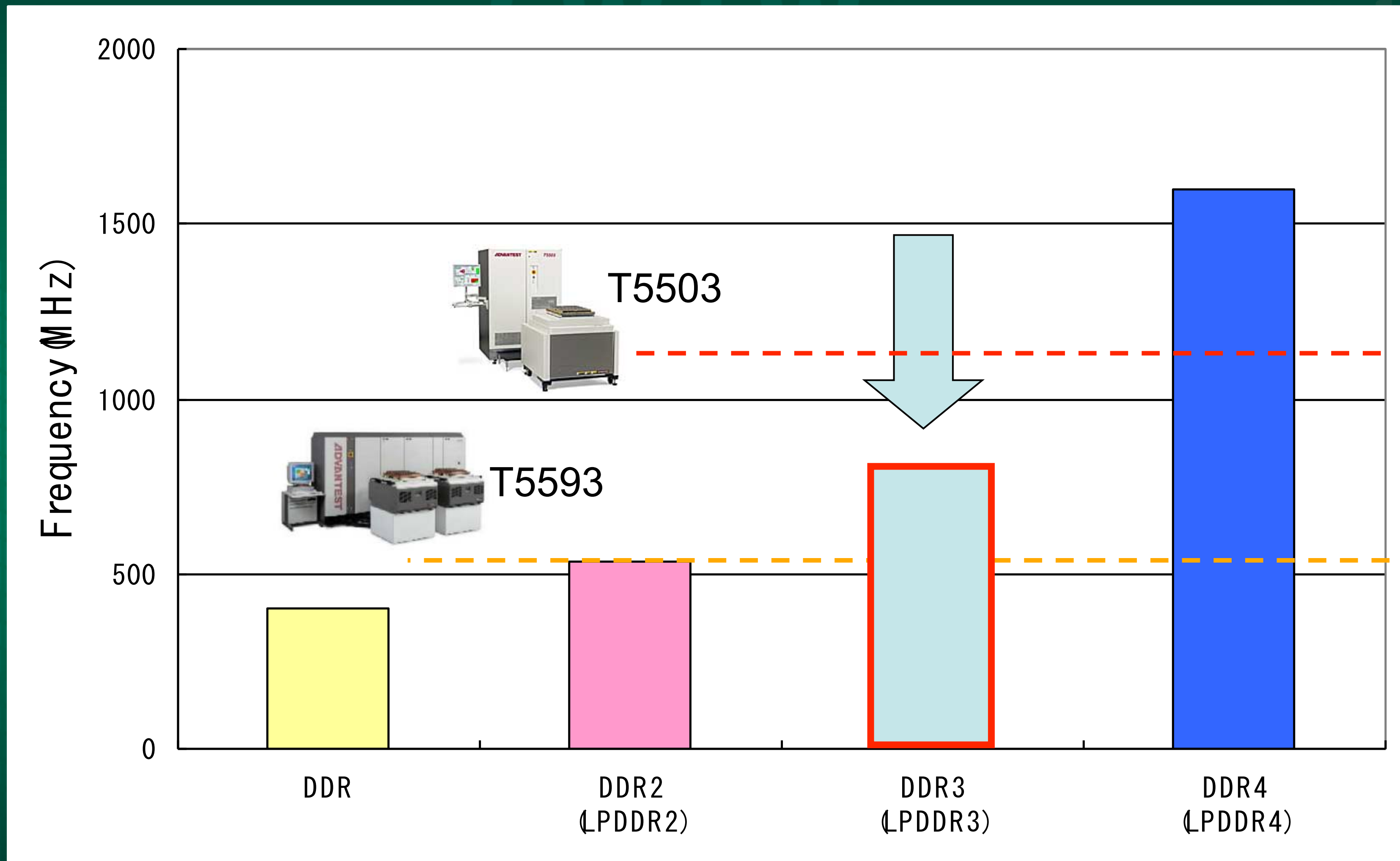
- **LPDDR3 become mainstream**
  - 1.066Gbps(533MHz) to 1.6Gbps(800MHz)



- **KGD Mobile demand is exploring**
  - Smartphone/Tablet market

- **Ramping TSV technology**
  - Memory is stacked with Logic chip in wafer level

Target



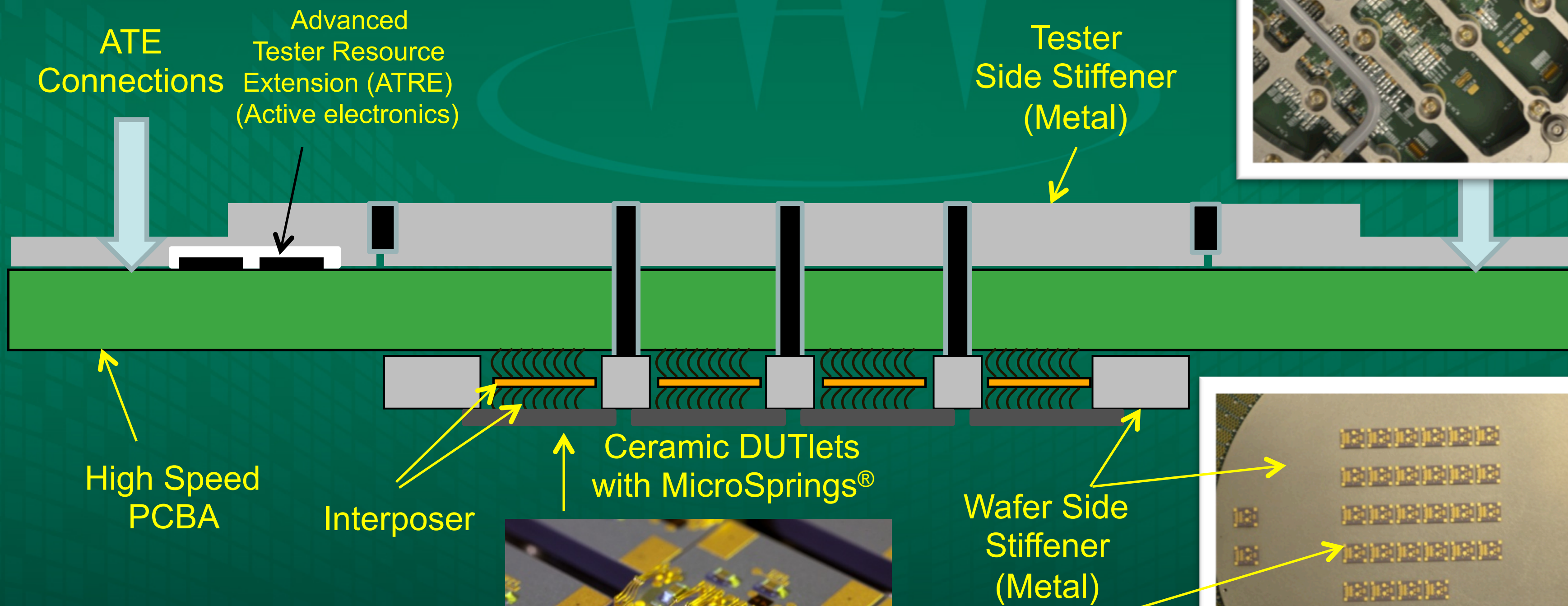
Test System T5503 WS

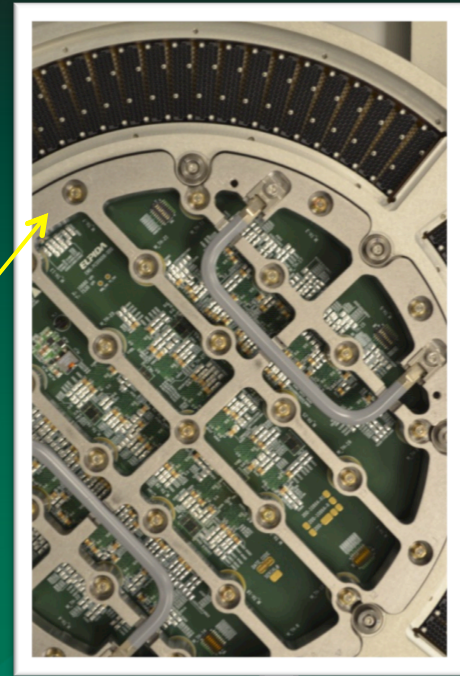
Test System T5503 WS

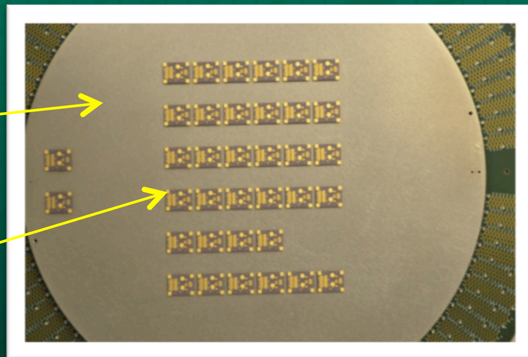
- **T5593WS and T5503WS TEST SYSTEM**

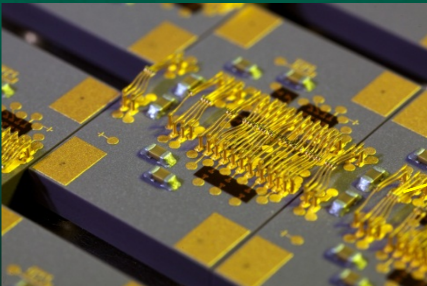
Item		T5593WS (Half)	T5503WS (4Site Half+OpPE)
Speed	Tester Max Freq	533MHz/1,066Mbps 1,066MHz(HSCLK opt.)	1.14GHz/2.286Gbps (actual Freq=depend on PC)
	OTA	±150ps	± 75ps
	DR/CP Skew	p-p100ps	≦ 60ps p-p
PPS	Current Driving	800mA / PPS	1.6A / PPS
	Channel数	160 PPS	256 pps
Channel	DR Channel	672	1152
	IO Channel	704	2688
	LVDR	-	384
Parallelism	**LPDDR2(x32)**	16 para	64 para
	DDR3(x16)	32 para	128 para by 4DR-share
WMB		350ϕ	440ϕ

SmartMatrix 100 XP Full Wafer Contactor Architecture



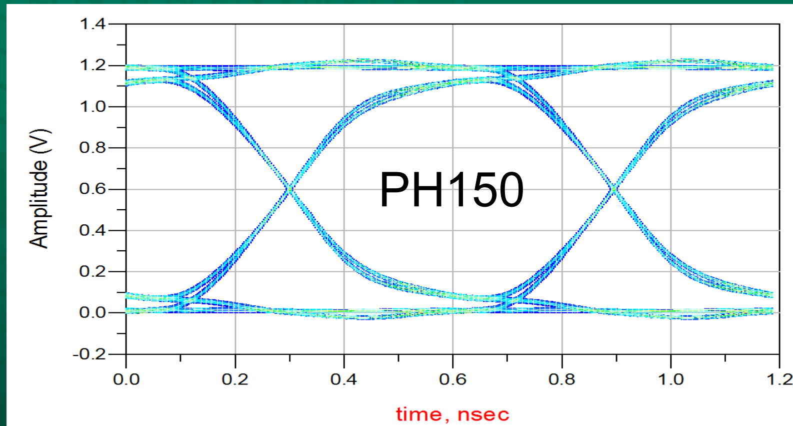


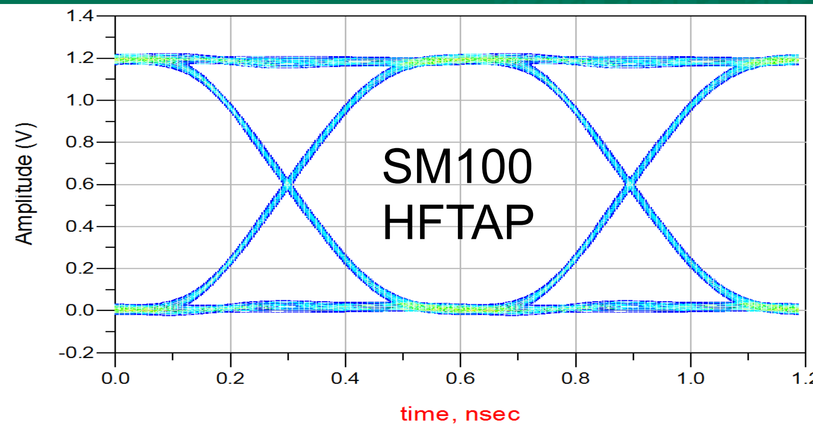




Probe Card Specifications

Parameter	Max Clock (MHz)	Parallelism	Skew Timing (±ps) Single ended / Diff pair	-3dB (70% Vinput) Attenuation (MHz)	-24dB (6% Vinput) Crosstalk (MHz)
PH100 K5 LPDDR2	500MHz	64	75	>1000	>400
SM100 HFTAP K10 LPDDR3	1066MHz	32 non-shared 2 groups of 2 Shared	50/10	>3000	>1100

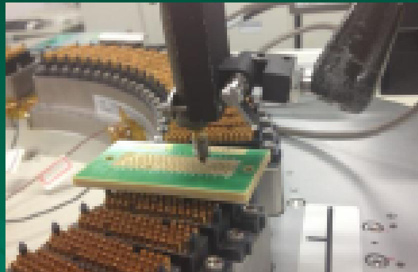




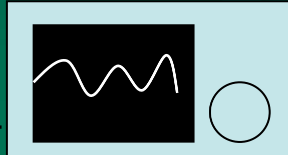
- 1680Mb/s PRBS $2^8 - 1$ Pattern
- Input Risetime = 173ps (20%-80%)
- Does not include effects of crosstalk and other noise factors

WAVEFORM Measurement

Wafer Mother Board Waveform

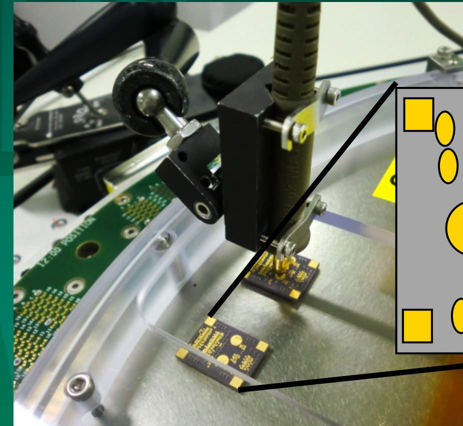


Probe Tectronix P6217
Sampling Head SD24

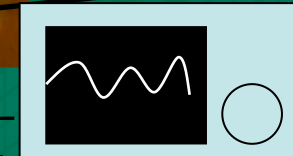


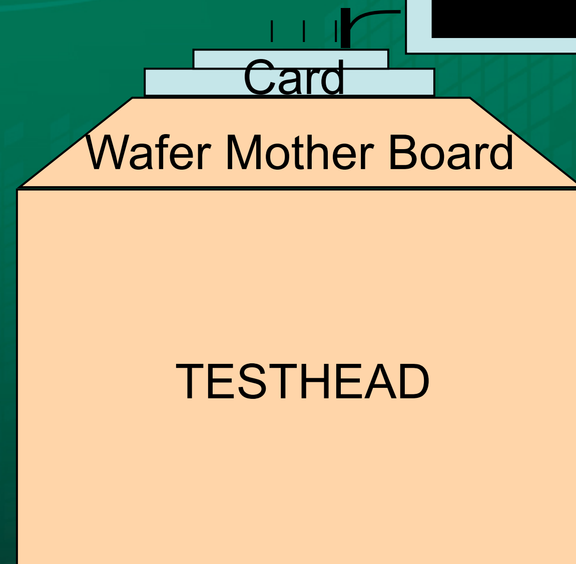
Tectronix CSA803C

Probe card Waveform



Evaluation
PAD



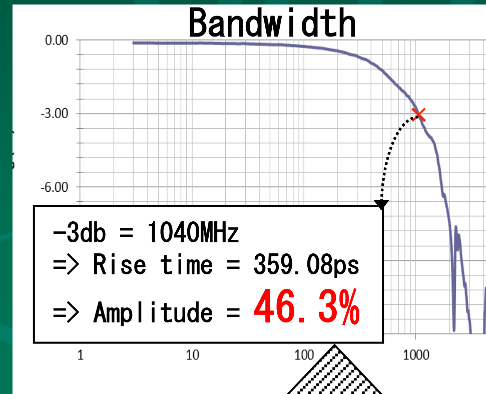


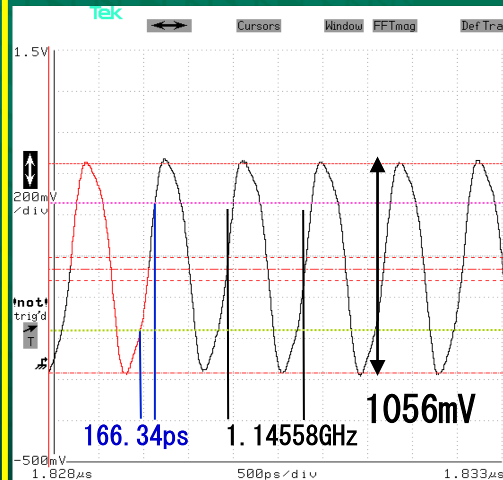
WAVEFORM Measurement

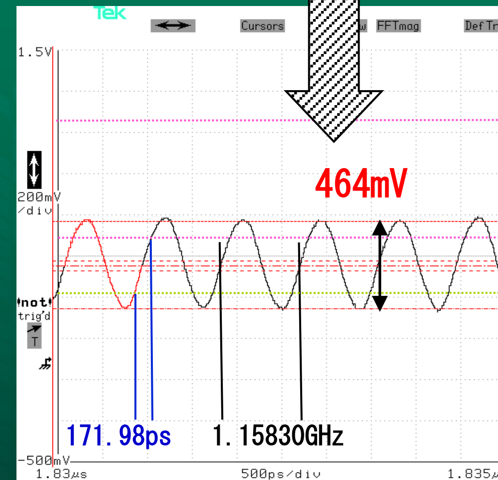
(1.14GHz 1.0V CLK_P)

Measurement Data

WMB waveform	Card waveform (Evaluation PAD)

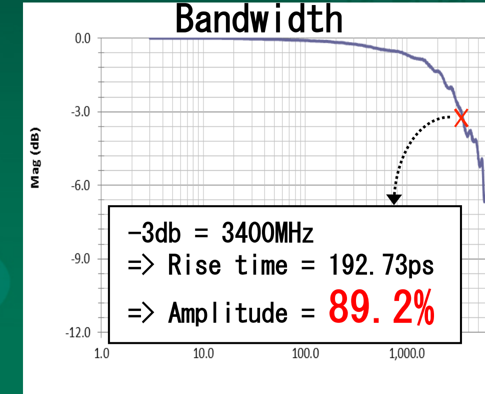


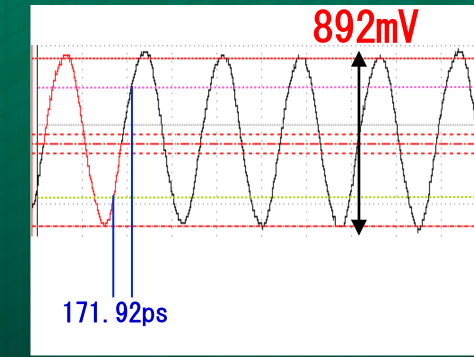




Simulation data

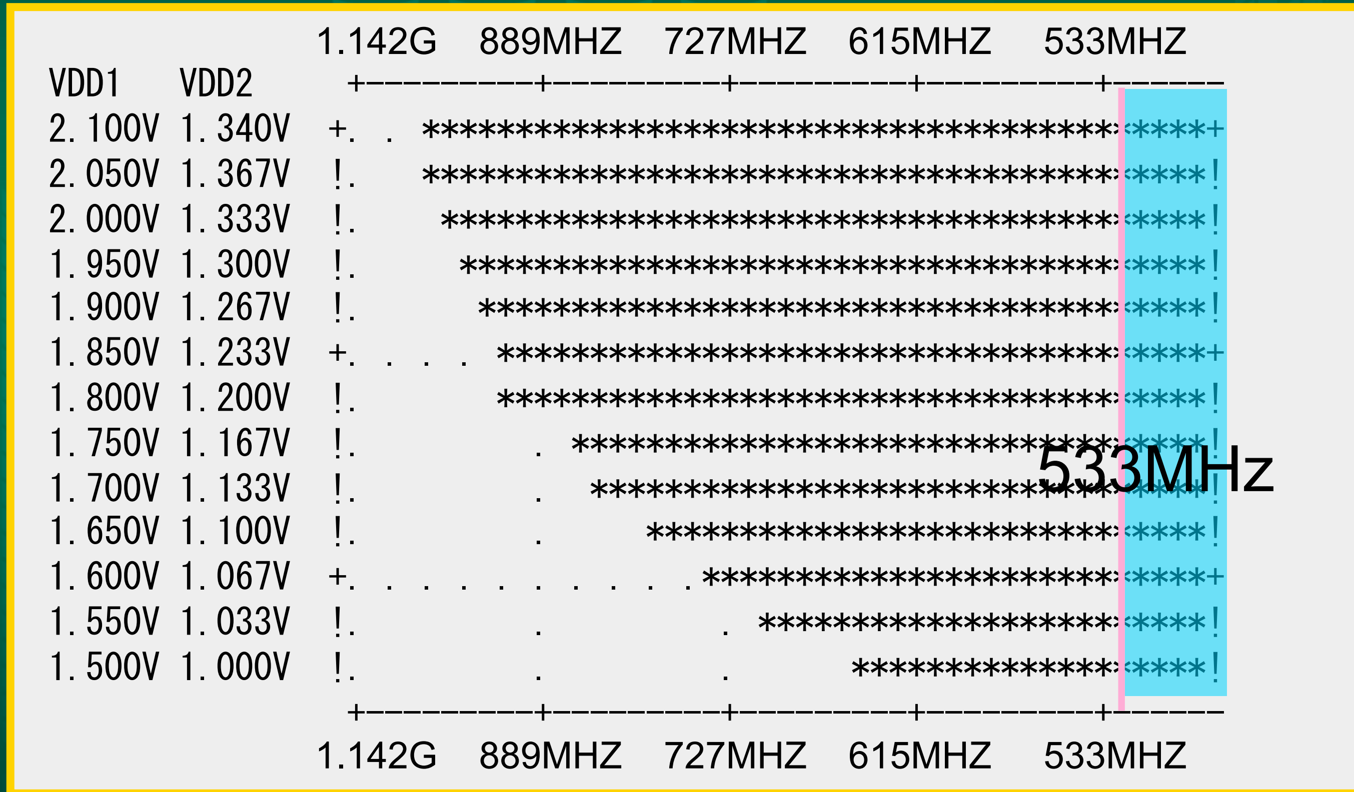
Card waveform (Normal PAD)





LPDDR2 High speed Testing

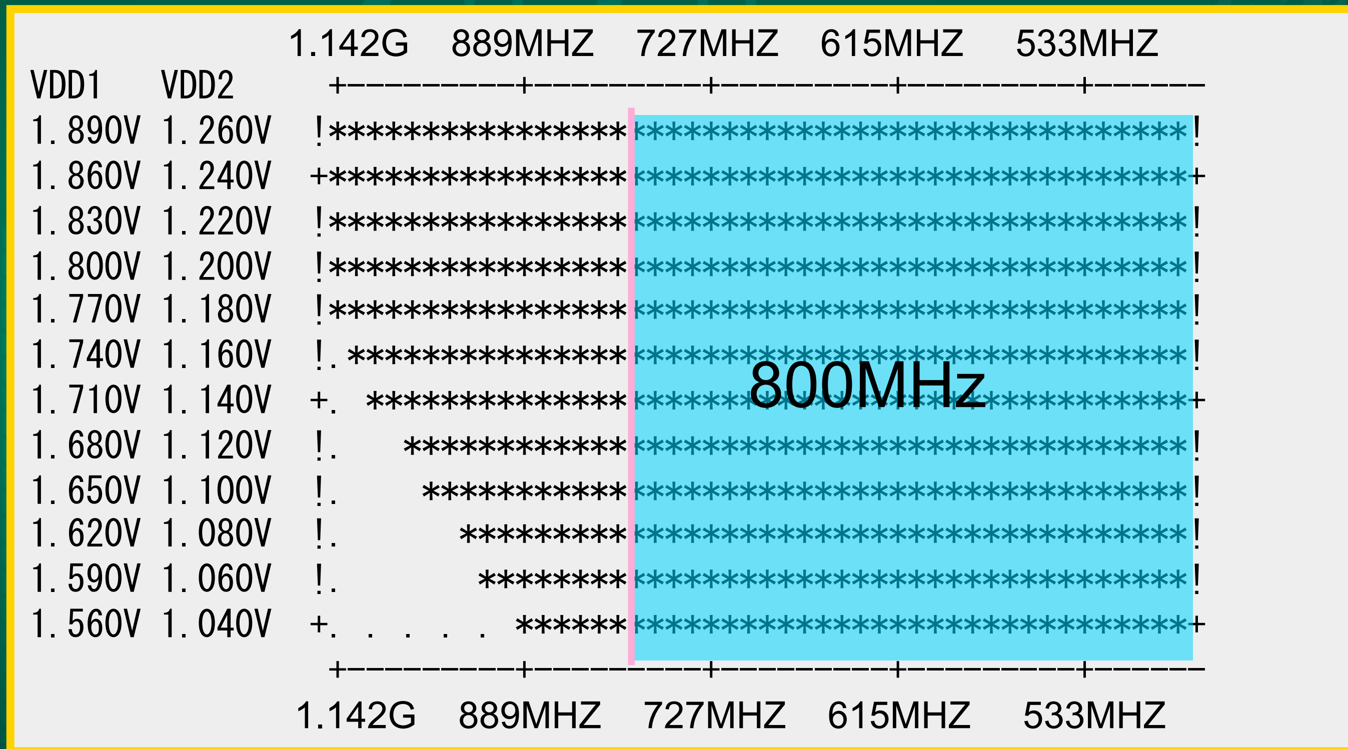
- **tCK SHMOO**
  - LPDDR2 Spec. 533MHz/VDD1=1.8V/VDD2=1.2V/RL=8



We confirmed this device work at 1.026GHz

LPDDR3 High speed Testing

- **tCK SHMOO**
  - LPDDR3 Spec. 800MHz/VDD1=1.8V/VDD2=1.2V/RL=12



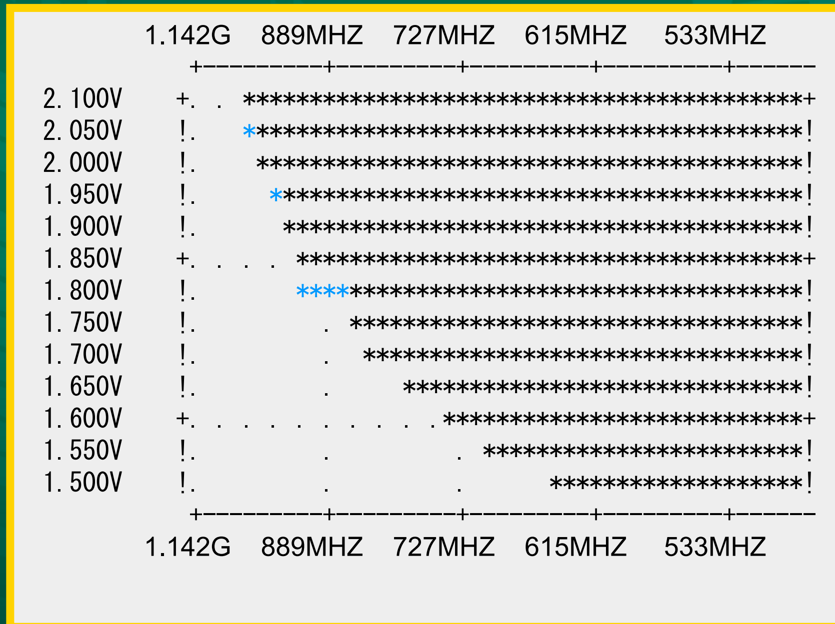
```
                   1.142G   889MHZ   727MHZ   615MHZ   533MHZ
VDD1   VDD2         +---------+---------+---------+---------+------
1.890V 1.260V      !**********************************************!
1.860V 1.240V      +**********************************************+
1.830V 1.220V      !**********************************************!
1.800V 1.200V      !**********************************************!
1.770V 1.180V      !**********************************************!
1.740V 1.160V      !.*********************************************!
1.710V 1.140V      +. ********************************************+
1.680V 1.120V      !.   ******************************************!
1.650V 1.100V      !.    *****************************************!
1.620V 1.080V      !.      ***************************************!
1.590V 1.060V      !.       **************************************!
1.560V 1.040V      +. . . . . ************************************+
                    +---------+---------+---------+---------+------
                   1.142G   889MHZ   727MHZ   615MHZ   533MHZ
```


This device works at over 1.142GHz

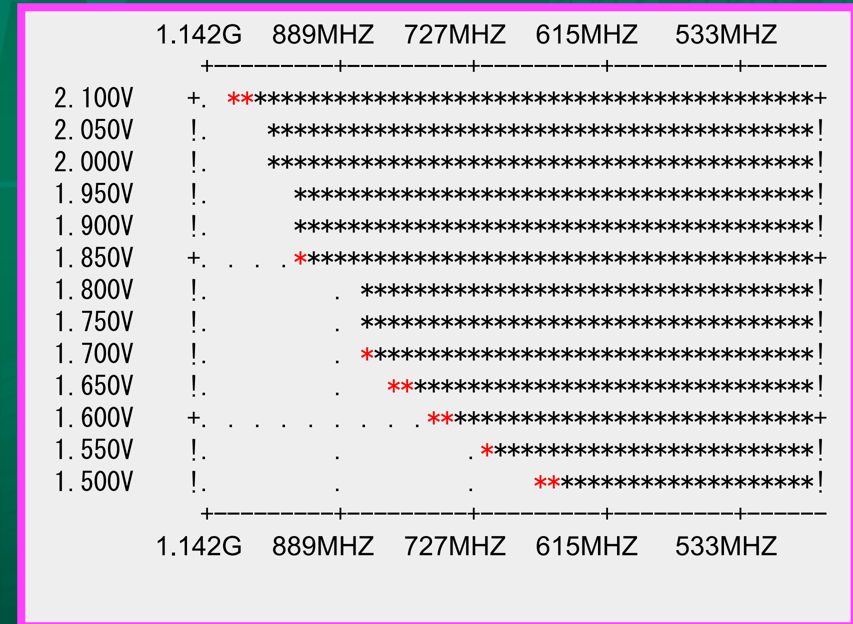
FT and WT result correlation

- **tCK SHMOO(LPDDR2)**

Wafer Test



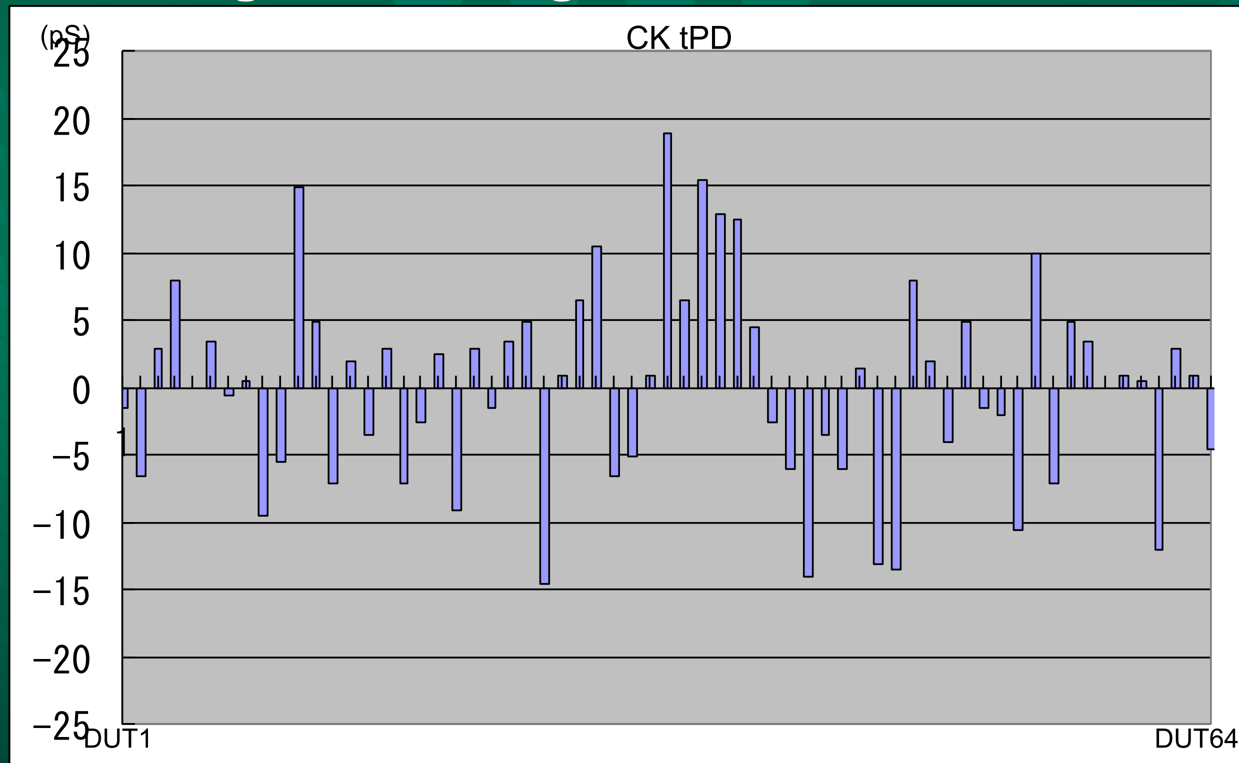
Package Test



Package Test and Wafer Test result is well correlated

Skew

- **Probe card skew specification**
  - **±50pS for single ended signals**

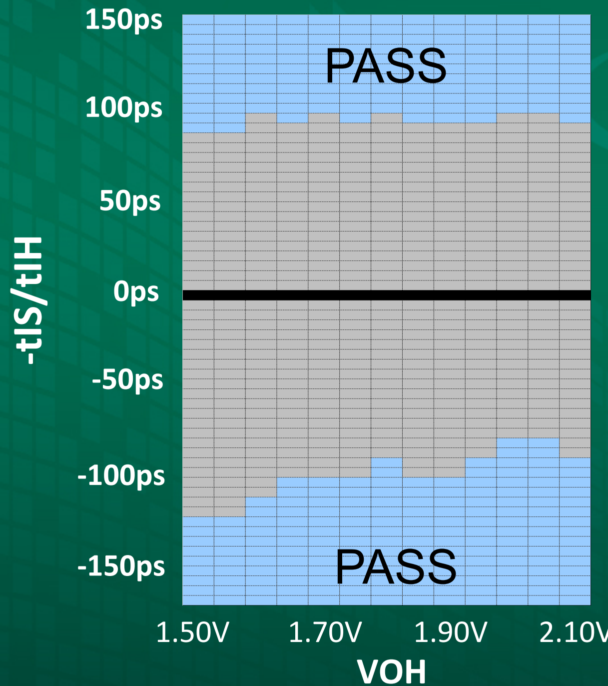


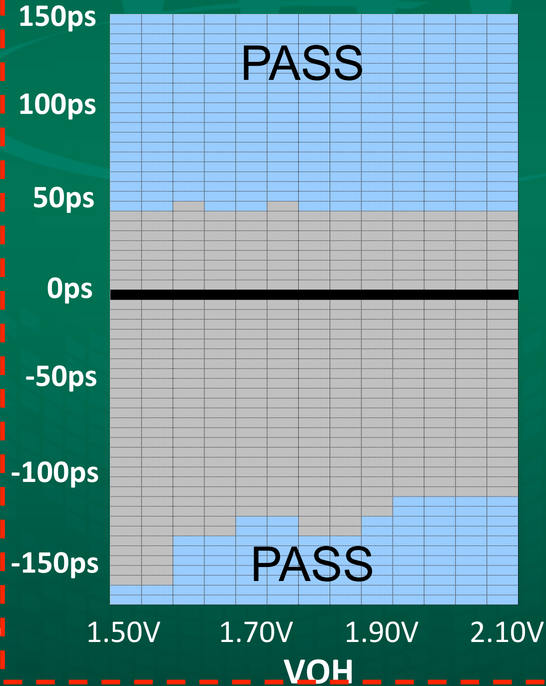
CK TPD is within 20ps for this Card(LP2).

Skew Improvement

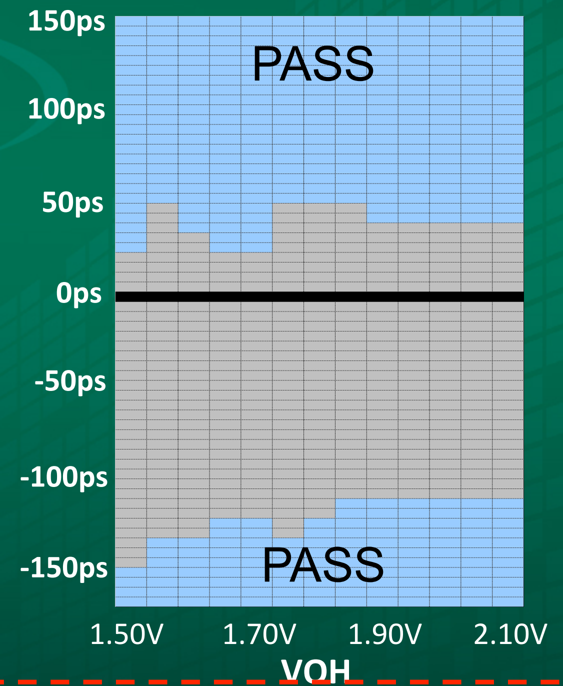
Normal SBCAL
(Used averaged tPD)

Well correlated





Improved SBCAL
(each signal tPD adjusted)



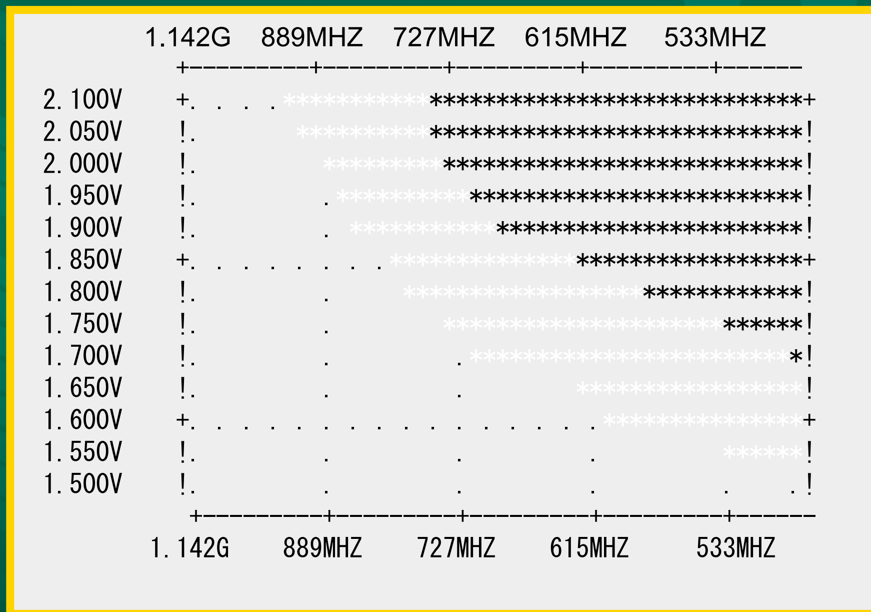
For Probe card high speed test, we need each signal tPD data to adjust skew

Measurement data from FormFactor manufacturing process

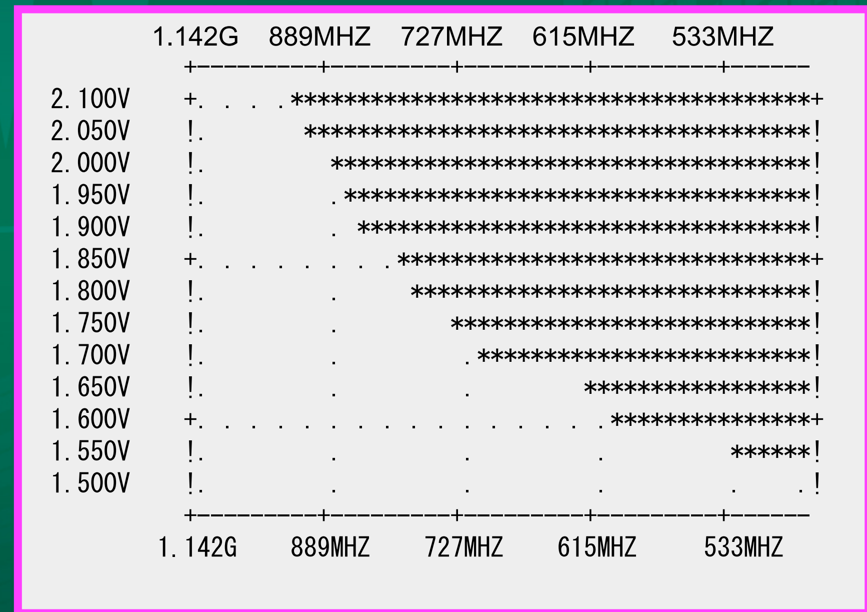
Contact Resistance Stability

- Contact resistance stability

AOT=80µm



AOT=90µm



For VDD minimum , high speed test is sensitive to Over Travel – contact resistance
We take special care to Actual Over Travel and cleaning recipe for optimum Wafer test

Next step

- **Enhance Parallel DUTs**
  – DR / PPS / IO shared

- **High speed at Solder ball contact**

- **High speed at Cupper pillar contact**

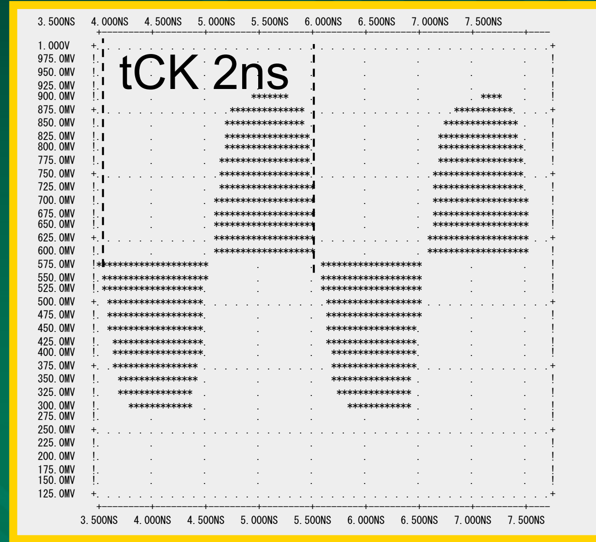
Enhance Parallel DUTs

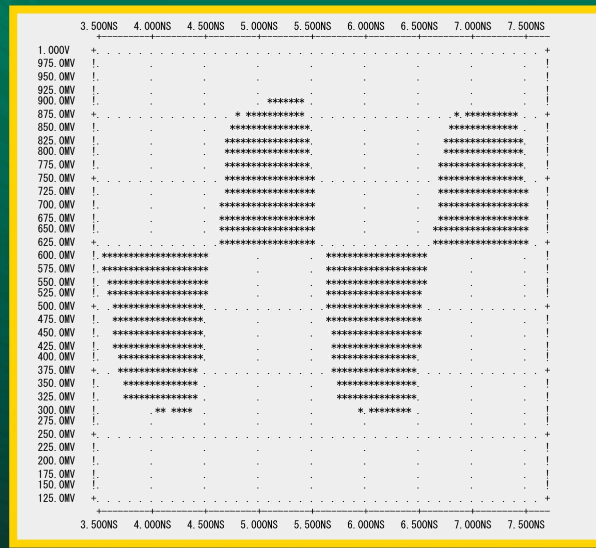
- **IO Shared**

500MHz

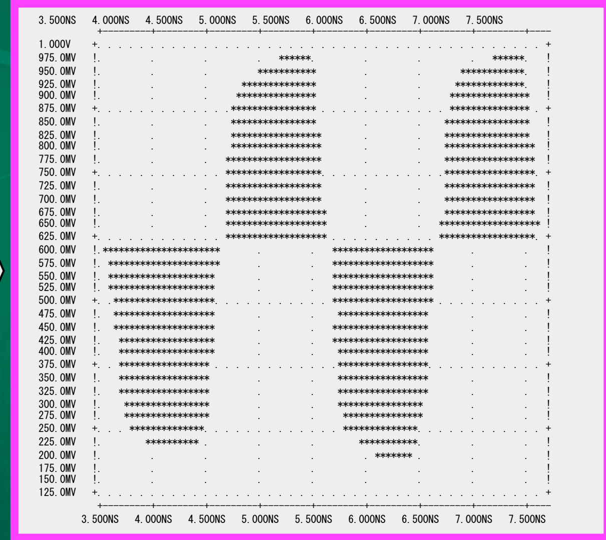
DUTA

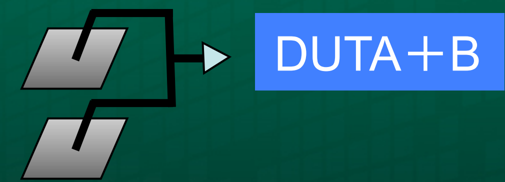
DUTB





IO shared DUT VOHL SHMOO seems good





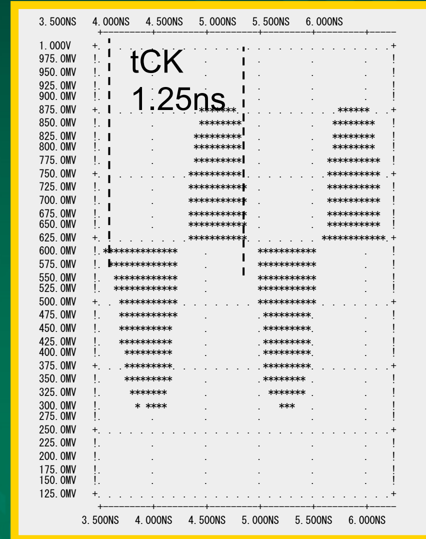
Enhance Parallel DUTs

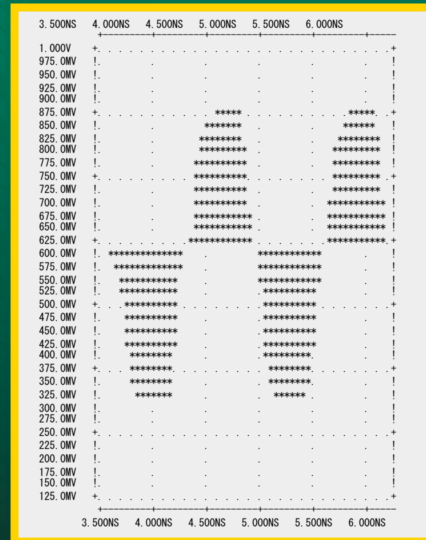
- **IO Shared**

800MHz

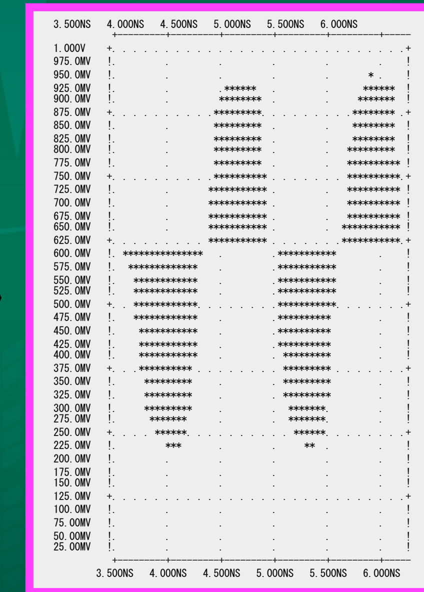
DUTA

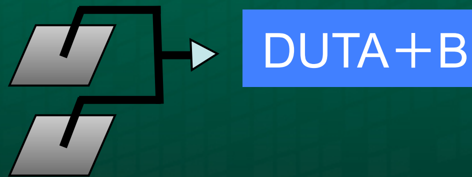
DUTB





IO shared DUT VOHL SHMOO seems good



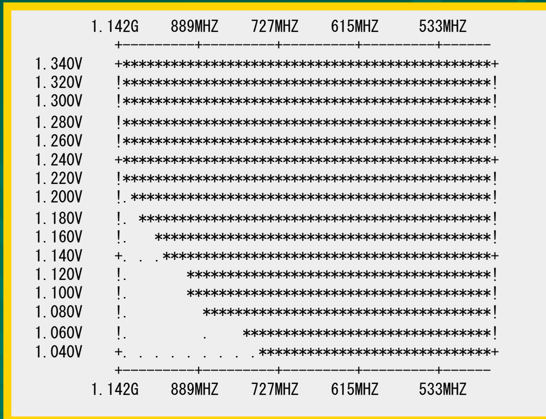


Enhance Parallel DUTs

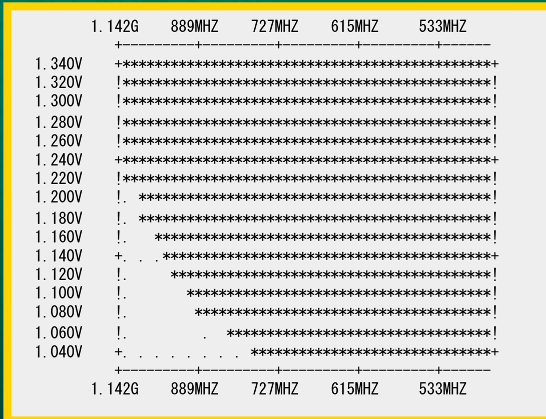
- **PPS Shared**

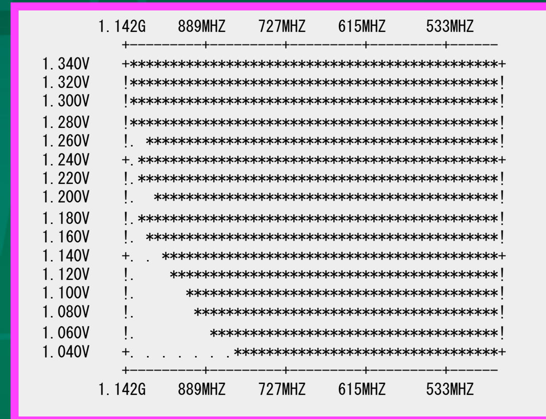
PPS shared DUT tCK seems good

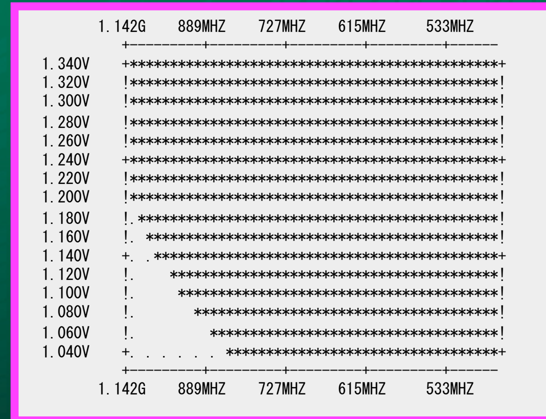
DUTA



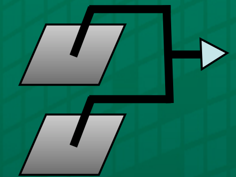
DUTB







DUTA＋B



Summary

- We develop high speed test environment for LPDDR2 and LPDDR3
- We keep improving productivity of LPDDR2 and LPDDR3 Speed testing.
- Next step : High speed test for WLP/TSV