Test & Reliability Challenges in Advance Semiconductor Geometries

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6/9/13

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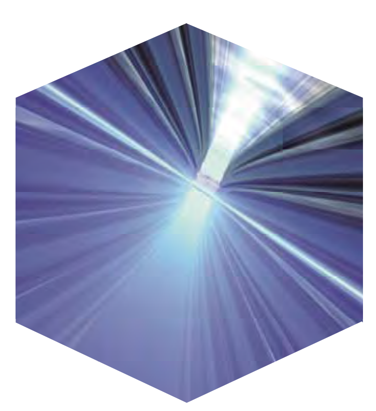
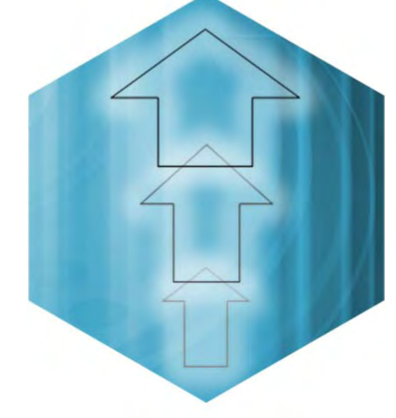
- Industry Transformational Trends
- More than Moore Challenges
- Impact on Test, Yield and Reliability
- Multi-Die stacks
- Innovation – Forward Challenges
- Conclusions

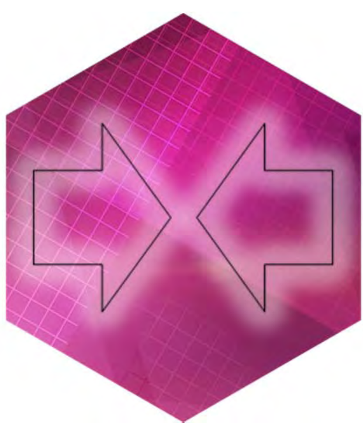
Industry Transformational Trends



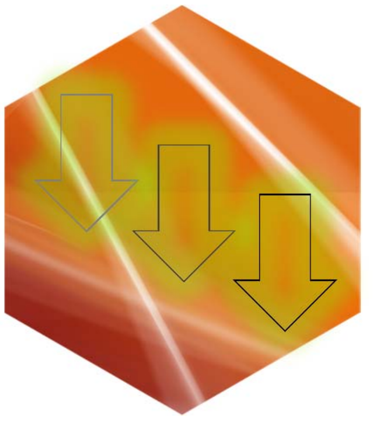
CLOUD COMPUTING



SOFTWARE
APPLICATIONS
USER EXPERIENCE

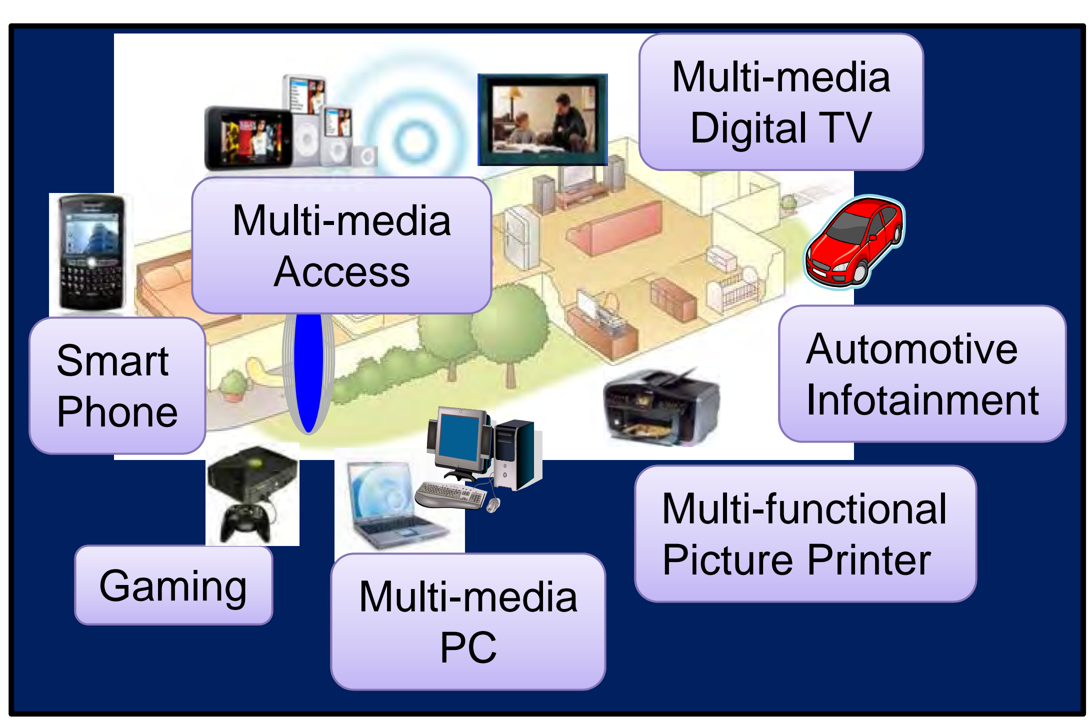


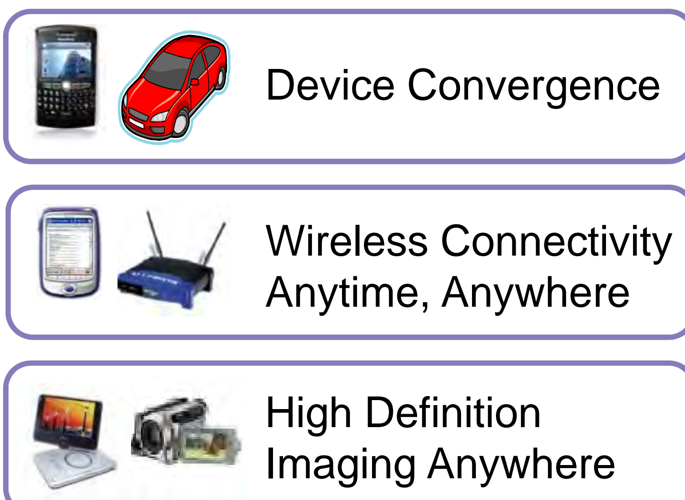
SHORTENED TIME-TO-VOLUME



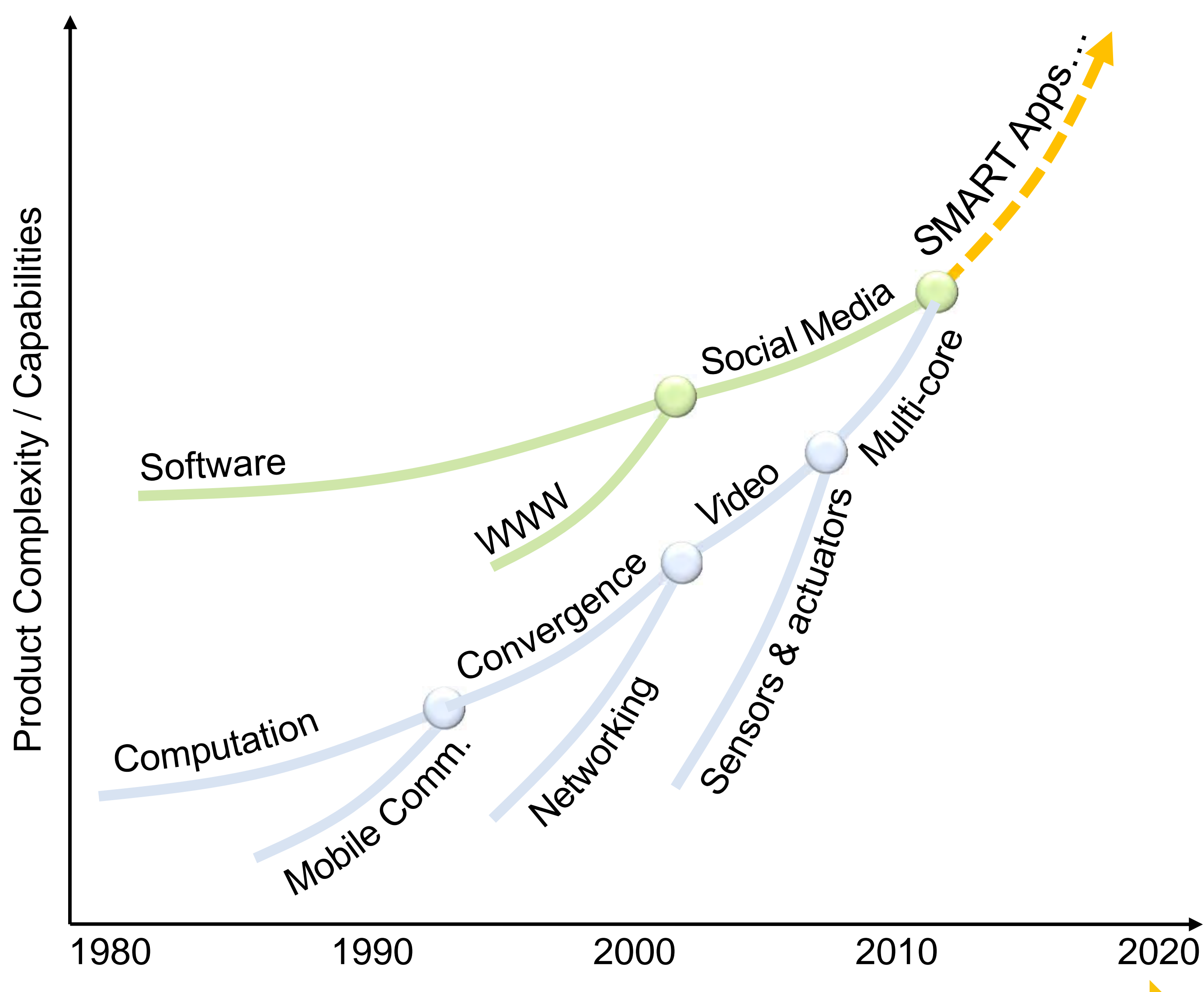
PRESSURE ON R&D PRODUCTIVITY

Consumers Driving "Smart" Electronics





Convergence



“SMART”

SYNOPSYS® Accelerating Innovation

Data Center / Cloud Computing Trends

What Happens in an **Internet Minute?**

639,800 GB of global IP data transferred

20
New victims of identity theft

204 million
Emails sent

47,000
App downloads

$83,000
In sales

61,141
Hours of music

20 million
Photo views

3,000
Photo uploads

320+
New Twitter accounts

100,000
New tweets

135
Botnet infections

6
New Wikipedia articles published

1,300
New mobile users

100+
New LinkedIn accounts

277,000
Logins

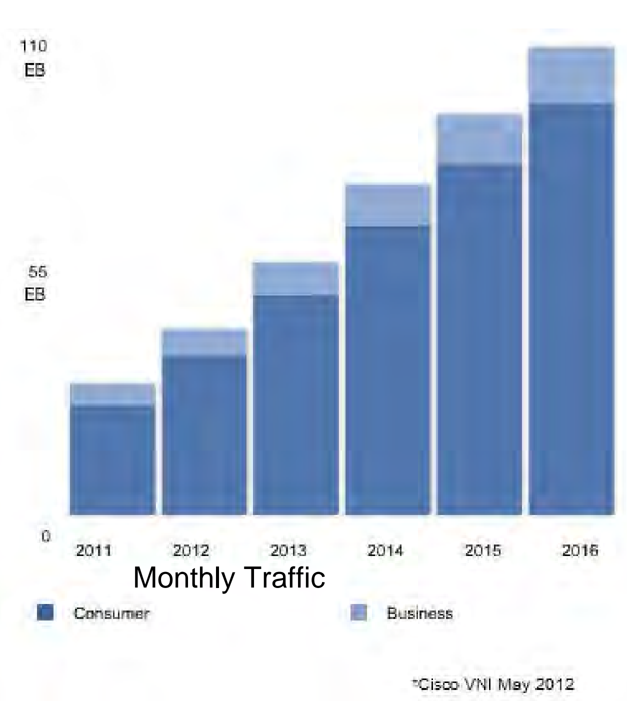
6 million
Facebook views

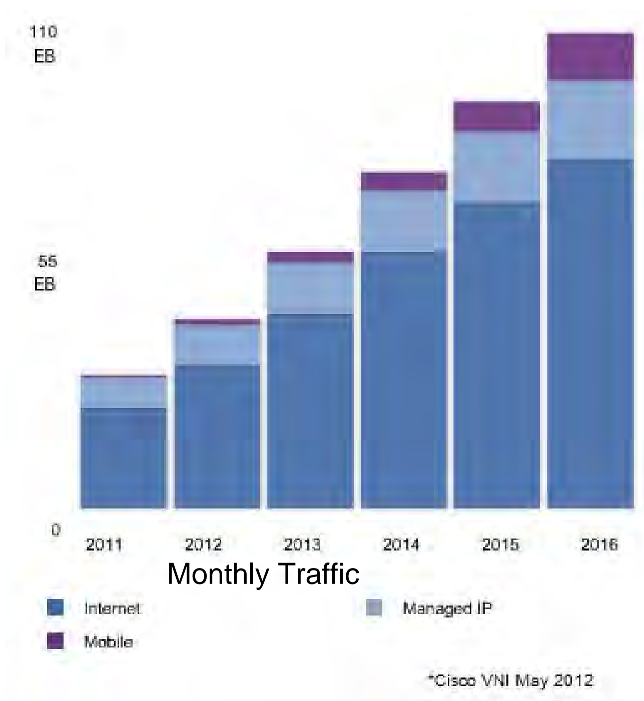
2+ million
Search queries

Source: Cisco VNI, 2011-2016

Data Traffic by Forecasts

- By 2016, total data traffic will be 4x 2011
- By 2016, global IP traffic will reach 1.3 zettabytes annually (110 exabytes per month)
- By 2016, there will be nearly 19 billion global network connections (fixed and mobile); the equivalent of two and a half connections for every person on earth.
- By 2016, there will be about 3.4 billion Internet users, which is more than 45% of the world's projected population.





System

Application | Application | Application | Application

Software Infrastructure

- Application Framework
- Libraries | O/S Runtimes
- O/S

Bare-Metal Software

- Drivers | Configuration | Test Programs
- Scheduler | … | Power Management

Silicon

- Mixed Signal | Low Power | Advanced Node
- Giga-Gates/GHz | Memories | 3D-IC

Integration

- **Before 32nm, new process was introduced every other year**
  - **Since then, a new process every year**

180nm
130nm
90nm
65nm
45nm
32nm
28nm
20nm
14nm

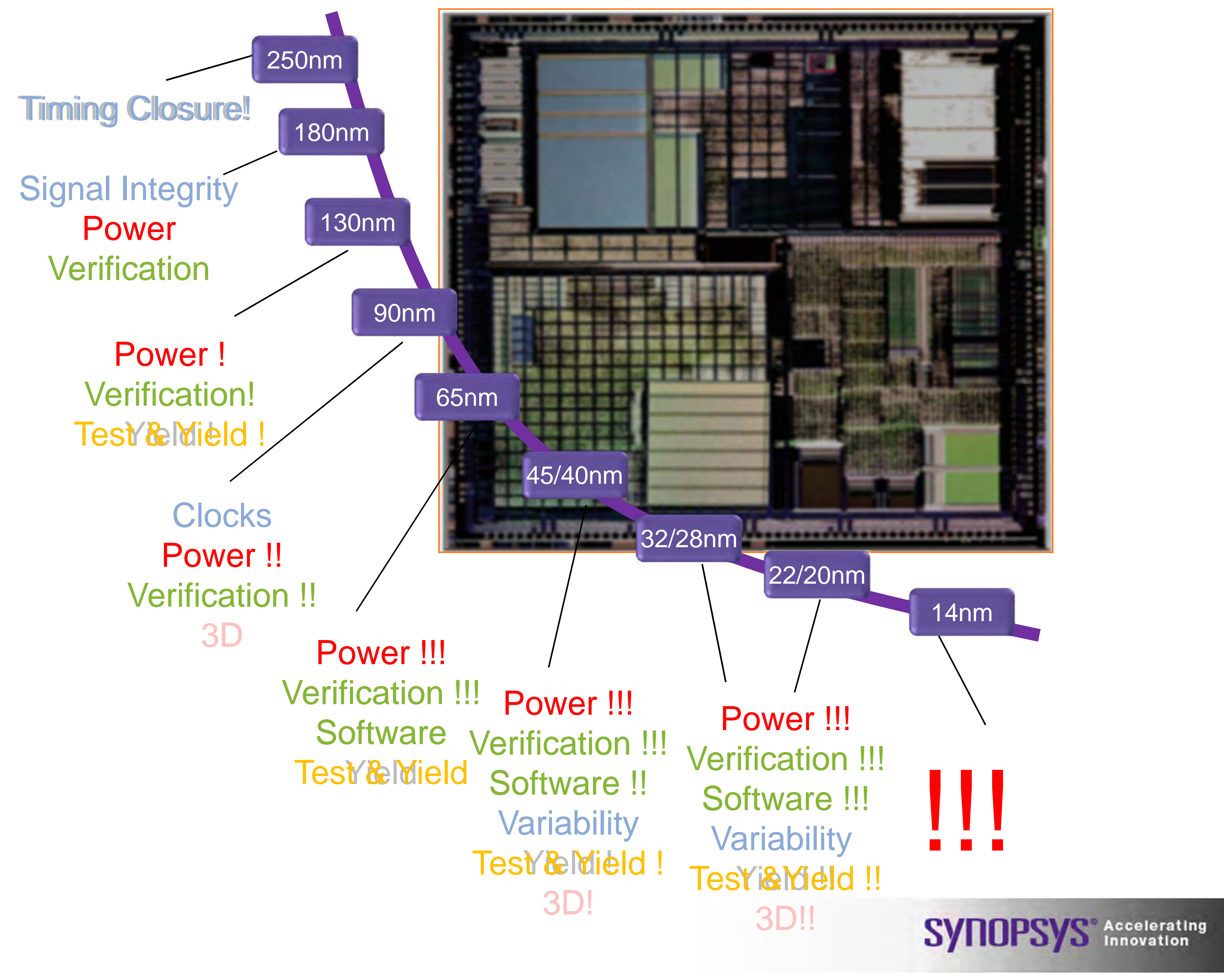
p-SiON

HK/MG

2000 2002 2004 2006 2008 2010 2012 2014

* Source : ITRS, Samsung Electronics Co.

Silicon Complexity



IC Design Expensive and Difficult

	32/28nm node	22/10nm node
Fab costs	$3B	$4B – 7B
Process R&D costs	$1.2B	$2.1B – 3B
Design costs	$50M – 90M	$120M – 500M
Mask costs	$2M – 3M	$5M – 8M
EDA costs	$400M – 500M	$1.2 – 1.5B

Source: IBS, May 2011

- Intensive customer/partner collaborative developments

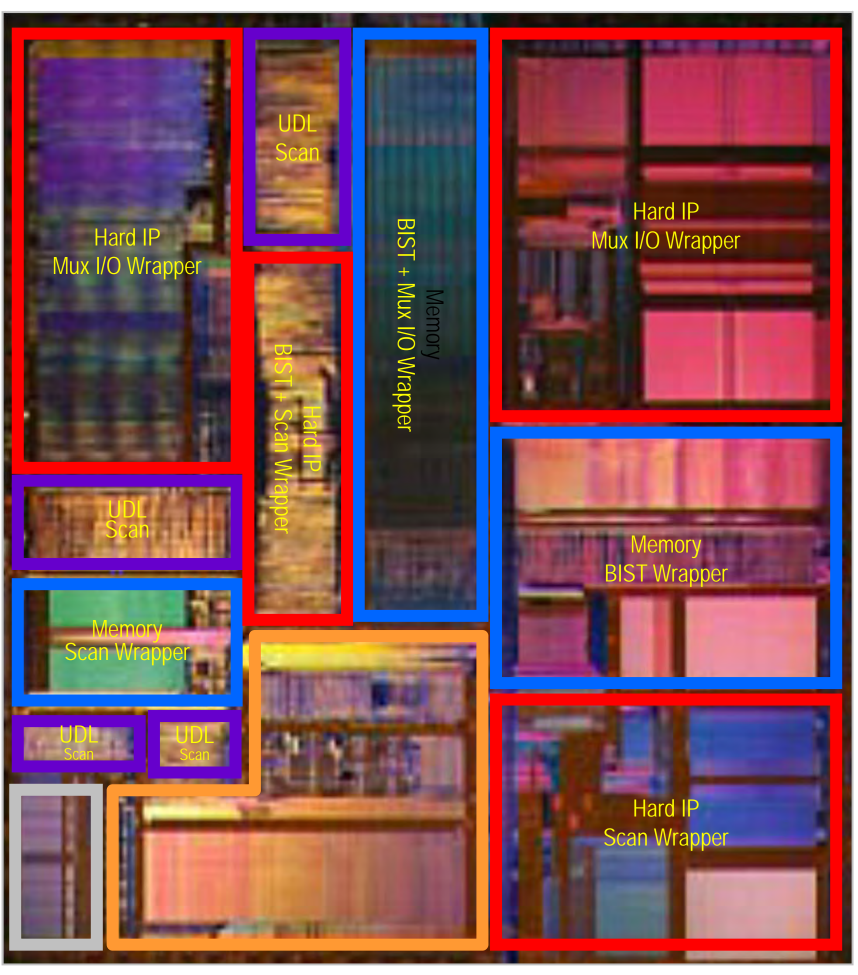
Top Semiconductor IP Vendors

Rank	Company	2010	2011	Growth	2011 Share
1	ARM Holdings	575.8	732.5	27.2%	38.3%
2	Synopsys	191.8	236.2	23.2%	12.4%
3	Imagination Te	91.5	126.4	38.1%	6.6%
4	MIPS Technolog	85.3	72.1	-15.5%	3.8%
5	Ceva	44.9	60.2	34.1%	3.2%
6	Silicon Image	38.5	42.8	11.2%	2.2%
7	Rambus	41.4	38.9	-6.0%	2.0%
8	Tensilica	31.5	36.3	15.2%	1.9%
9	Mentor Graphic	27.3	23.6	-13.8%	1.2%
10	AuthenTec	19.6	22.8	16.3%	1.2%

Source: Gartner, March 2012

Test & Yield

- Increasing design complexity
  - Many AMS and Interface IP cores
  - Many existing third-party IPs
  - Large number of memory instances
- Exploding digital logic size
  - Greater than 100M gate designs
  - Global design teams
- Increasing test & yield impact
  - Quality – DPPM
  - Total memory bit count
  - Yield Optimization
  - Designer productivity
  - Time-to-market and time-to-volume



SoC Test Challenges

Higher Test Costs

- Trend: large designs & increased on-chip memory
- Need: less test data, faster execution on the tester

Lower Productivity & Efficiency

- Trend: complex designs and implementation flows
- Need: Hierarchical SoC implementation and validation solution for memories

Functional Performance Degradation

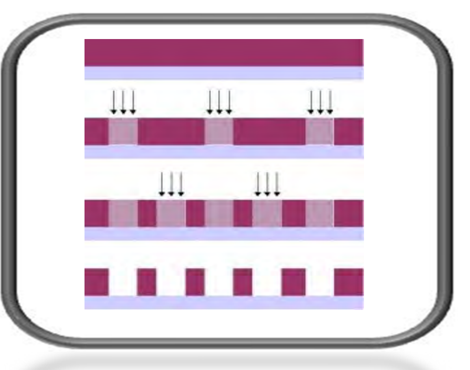
- Trend: high performance cores
- Need: test with minimal impact on functional performance, area efficient solution

Slow Ramp-up, Higher DPPM

- Trend: small geometries, subtle & hard to detect defects
- Need: advanced fault models, efficient volume diagnostics & yield analyses

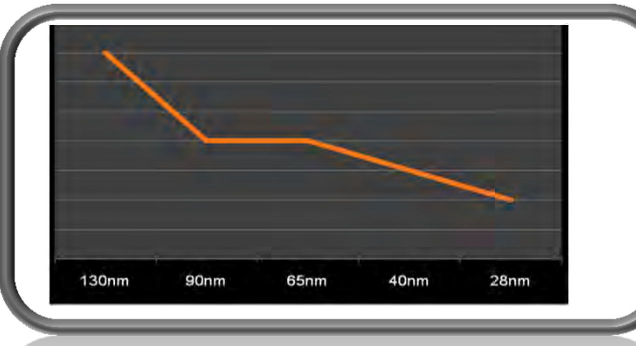
New Defects

Double Patterning



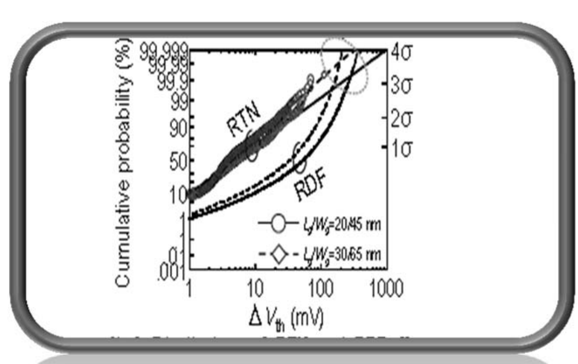
Variation from overlay shift

Voltage Scaling



Local **variation** with Voltage

Random Dopant Fluctuation



Global and local Vth **variation**

Process variation at 20nm is significant, causing bit failures

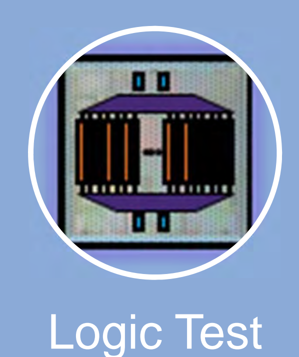
Sample SOC: DesignWare® IP based

CPU Host
CPU RISC/ DSP
DDR PHY
IIP
DDR controller
PCIe PHY
IIP
PCIe controller
HDMI PHY
IIP
HDMI controller
USB PHY
IIP
USB controller
ADCs DACs
IIP
Signal processing
Audio Codec
ARC Audio processor
Video Front End
ARC Video processor
Ethernet controller
SATA controller
MIPI DigRF, CSI, DSI controller
SD/MMC controller
IIP
Embedded Memories (SRAM, ROM, NVM)
I2C
GPIO
UART
XAUI PHY
IIP
SATA PHY
IIP
MIPI D-PHY M-PHY
IIP
Datapath
Logic Libraries

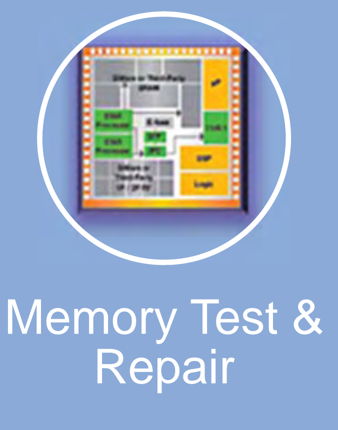
Digital IP
Physical IP
Infrastructure IP

SOC Test Solution

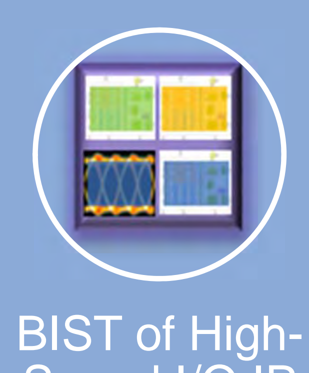
Accelerate Higher Quality, Lower Cost Test



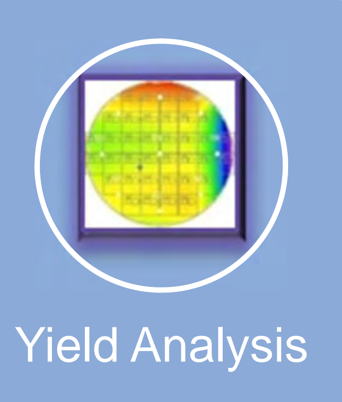
Logic Test



Memory Test & Repair



BIST of High-Speed I/O IP



Yield Analysis

Comprehensive Solution for SoC and Core-Based Designs

®

- Pin-limited compression
- Advanced fault models
- Power-aware test

- Easy integration and verification of self-test IP
- High defect coverage

- High-speed SERDES interfaces (PCI Express®, USB 3.0, etc.)
- Verification IP for integration test

- Physical-aware diagnostics
- Fast identification of systematic yield loss mechanisms

Hierarchical Design & Verification

Block A

Block B

Block C

SoC

Embedded Memory Is Growing

Key Driver Of Design Success

CPU/DSP/Ctrlr
All Other IP Blocks, Combined

Source: Semico, October 2011

ARM® Processor Cache Size

I/D Cache (Kb)

ARM3 ARM7 ARM9 Cortex

Source: Wikipedia

% Area Memory
% Area Reused Logic
% Area New Logic

Source: Semico, June 2010

Number of Processors is Growing × Cache Size / Processor is Growing + SoC Memory is Growing = Memory Dominating Chip Area

Need an efficient solution to test, repair and diagnose thousands of on-chip memories

Process Miniaturization Challenges

- Higher susceptibility and new and speed related fault types
  - ✓ Requires expanded test to detect new fault types
  - ✓ Requires high speed test capability
- Higher level of miniaturization
  - ✓ Needs fault classification and localization
  - ✓ Needs on-the-fly monitoring and analysis of volume diagnosis data
  - ✓ Requires better support for yield learning and production ramp up

Cost of Unit Out

$100,000
$10,000
$1,000
$100
$10
$1

Capital cost ($M)

Normalized cost per unit out

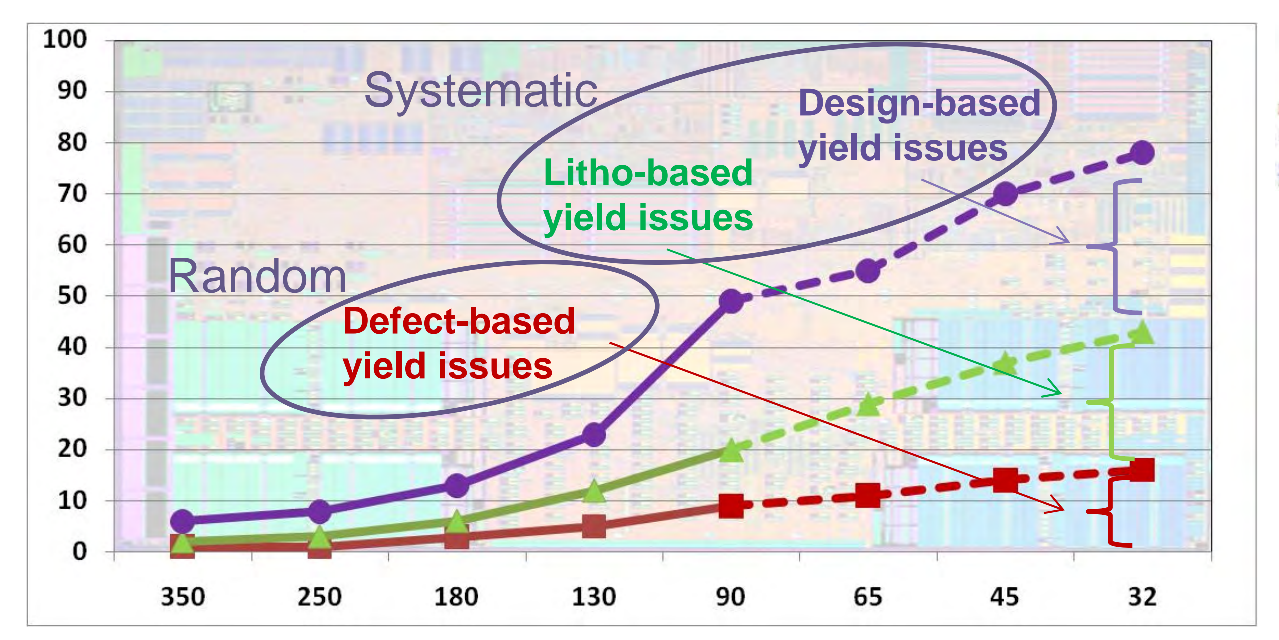
0.0001

1980 1990 2000 2010 2020

Source: IC Knowledge, 2005 & IBS 2008

Dramatic Rise in Systematic Yield Issues

Yield Fallout



Technology Node (nm)

- Cheating with physics induces more process variability at each nanometer node
- Some layout features react strongly to variability causing systematic yield issues
- **Each successive nanometer node faces more systematic yield loss**

**Chart data source - IBS

Embedded Test & Diagnosis

High Manufacturing Test Quality

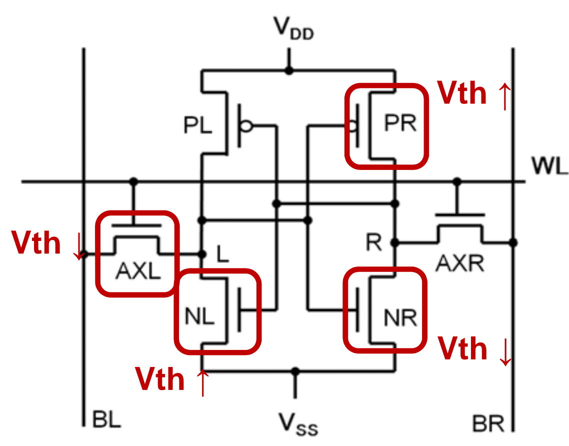
- Out-of-box enhanced test algorithms
- Fully characterized for each advanced node
- Provides 100% fault coverage
  - New fault types appear at advanced nodes
    - Resistive faults
    - Performance faults
    - Bridging faults
    - Parametric variation
  - Generic algorithms are not as granular, resulting in test escapes
- Fault injection based analysis

Fault Types
Static/dynamic
Write mask
Weak
Address decoder
Bit-line leakage
Intra & Inter-port
Delay coupling
Data setup/hold

Process Variation- Read Failures in SRAM

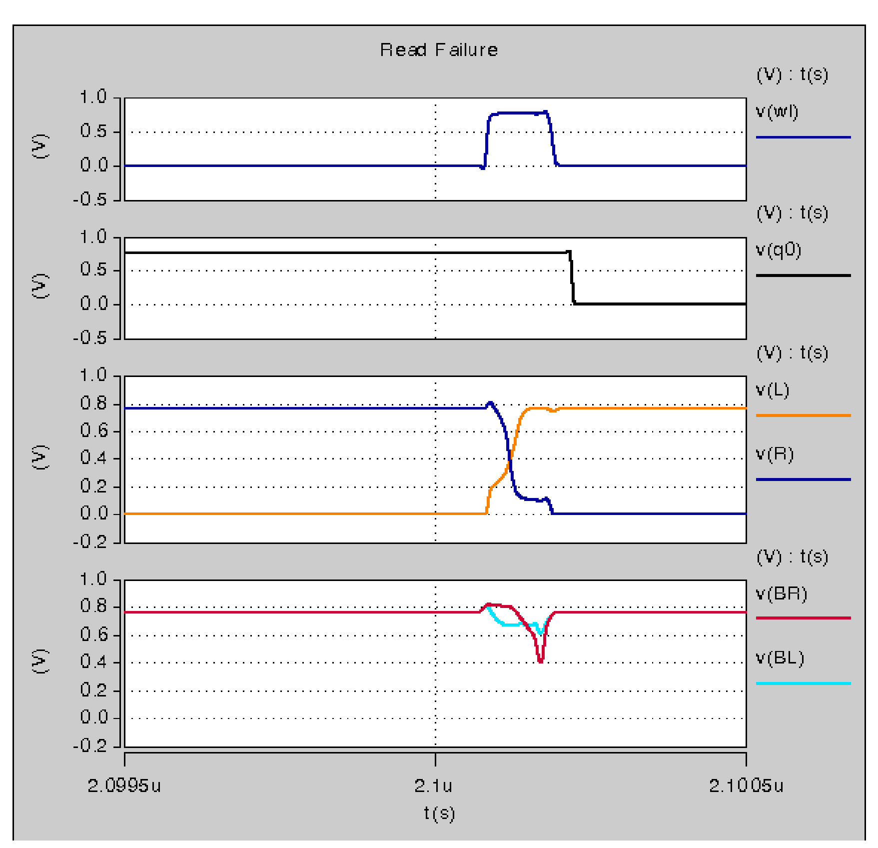
Read Failures should be tested in (VDD_max,T_max) corner

- More than 22% variation of Vth brings to a failure



T \ V	VDD_min (0.765V)	VDD_typ (0.85V)	VDD_max (0.935V)
-40			
25			X
125	X	X	X

for 30% L and W variation



Repair Solution Impacts Memory Yields

1 Mb 2 Mb 4 Mb 8 Mb 16 Mb 24 Mb 32 Mb

Memory Yield (%)

100 90 80 70 60 50 40 30 20 10 0

3 5 11 22 43 65 86

Amount of Memory on the die (Mb)

Embedded Test & Repair

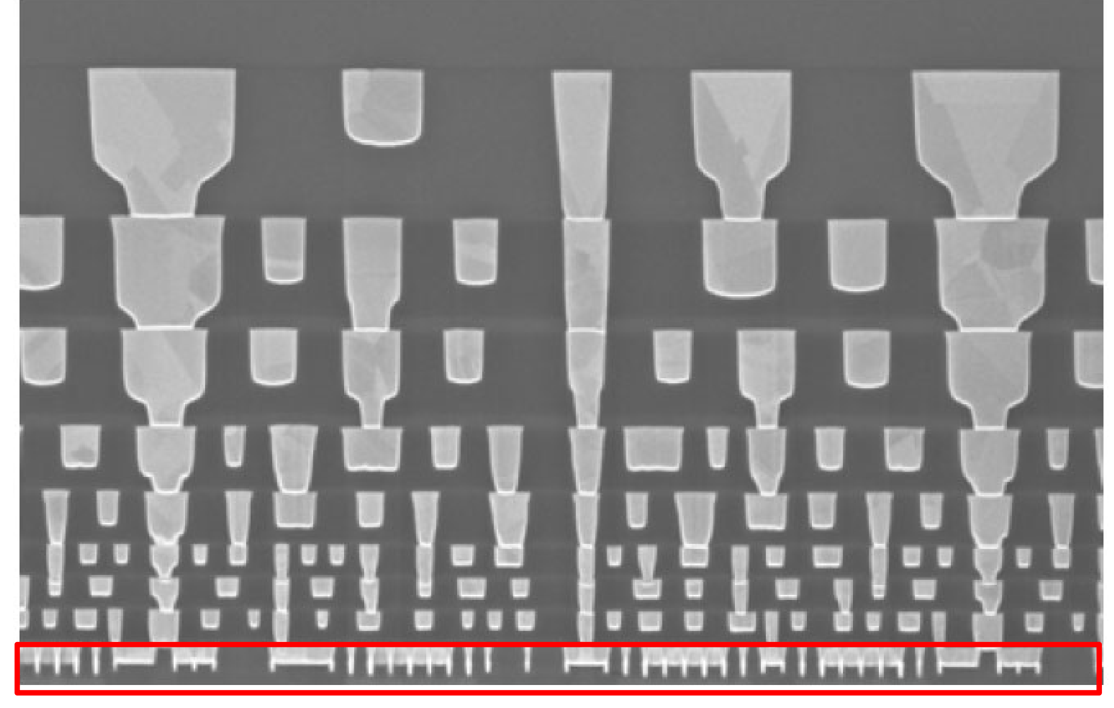
Memory without Repair

Repair Efficiency

- Redundancy allocation algorithm maximizes available repair resources
  - Numerous types and amount of redundancies
- Repair methodologies to maximize repair
  - Multi-corner cumulative repair
  - Multi-zone fuse containers
  - In-system periodic repair capability
  - Fastest system recovery with multi-power island chips

Why FinFETs

As predicted for many years, but often postponed, the device level of the chip is finally changing

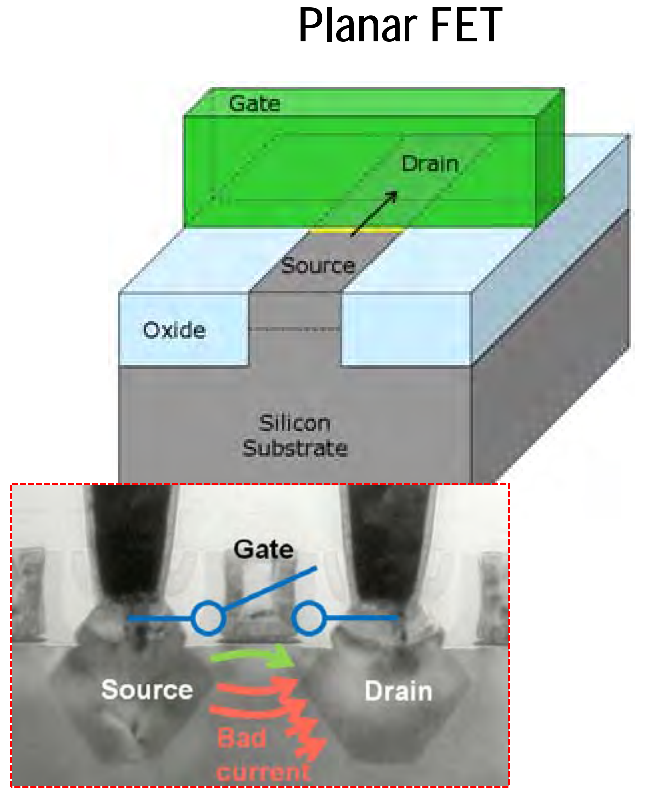


- "Conventional" planar transistors are reaching the limits of scaling and have become "leaky": They use too much power
- FinFETs enable products with higher performance and lower power consumption
- There are alternatives, but FinFETs promise better continuation of Moore's Law

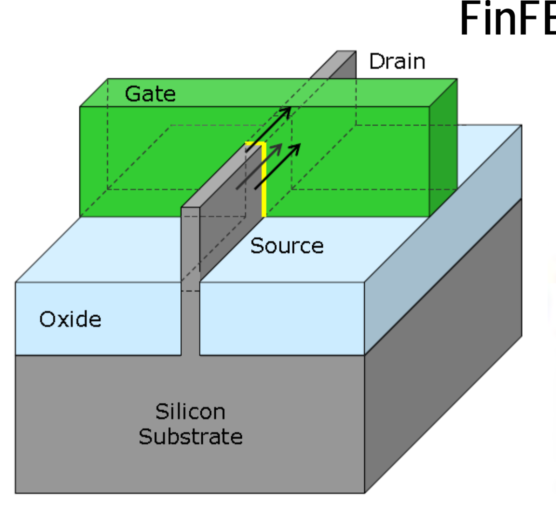
How FinFETs Work

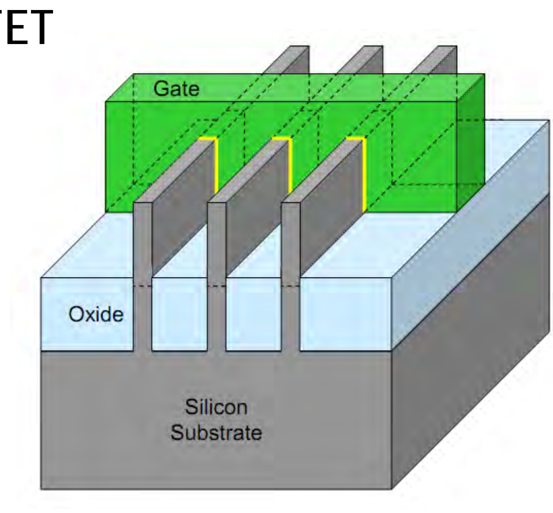
Field effect transistors: The field from the gate controls the channel

Planar FET



FinFET

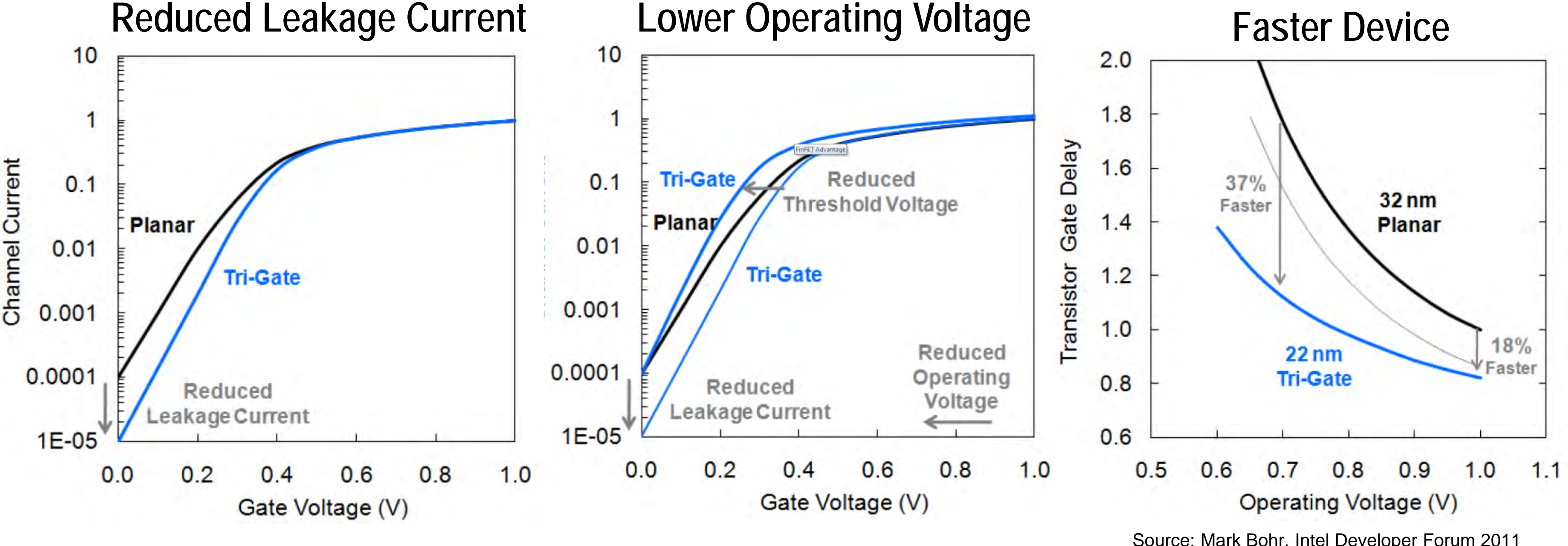




Single gate channel control is limited at 20nm and below

“**Multiple” gate** surrounds a thin channel and can “fully deplete” it of carriers. This results in much better electrical characteristics.

FinFET Advantage: Intel's Perspective



Source: Mark Bohr, Intel Developer Forum 2011

- Benefit of Intel's FinFET with respect to Intel's 32nm planar technology
  - Tri-Gate transistors provide an unprecedented 37% delay improvement at low voltage.
  - Tri-Gate transistors can operate at lower voltage, providing ~50% active power reduction

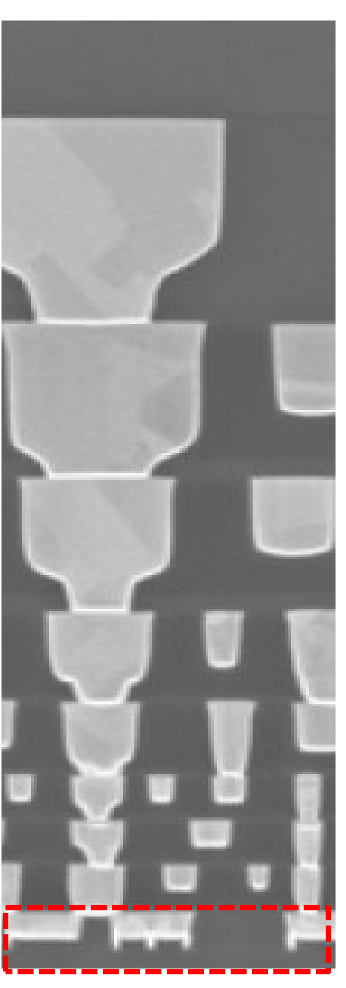
FinFET Impact on Design for Test

SoC Designers

Libraries and tools will minimize the impact on digital design.

Foundries

Significantly impacted.



The impact of FinFETs is largest below Metal 1

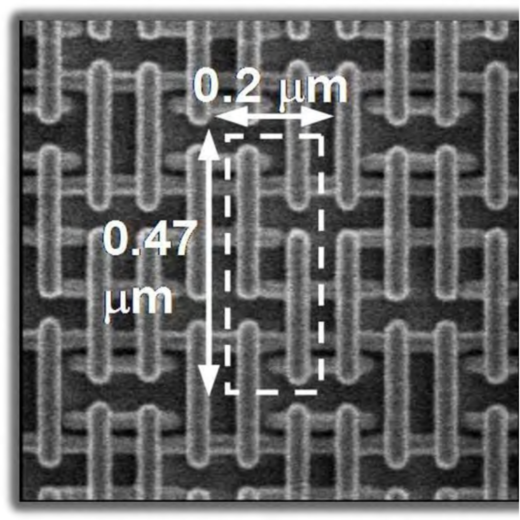
Double patterning and restricted design rules, while often associated with FinFETs, are not unique to them and also necessary for planar technologies

IP Designers

Standard cells, memory compilers and custom design are impacted.

FinFETs in SRAMs

- Special focus on low voltage operation
  - Read assist and write assist circuitry to improve robustness
  - Compile time options to maximize
- Large SRAM macros provide alternatives to embedded DRAMs
- Enhancing Memory Test & Repair to handle FinFET related failures
  - Fault models for planar FETs need to be extended to cover FinFETs
  - Further enhancements in compression of test and repair algorithms



Source: IBM Research, 2010 Symposium on VLSI Technology

Realistic Faults in FinFET SRAMs

- Traditional faults
  - stuck-at fault, stuck-open fault, transition fault, address decoder fault, coupling fault, etc.
- Process variation faults
  - Transistor threshold voltage is affected by gate length (L) and fin thickness (Tfin).
- **FinFET specific faults**
  - Opens in FinFET transistor back gate cause delay and leakage faults (transistor threshold voltage is affected by back gate voltage)

Detection Programmable

TAP
tck
tms
tdi
tdo
trstn

JPC
p1500

STAR processor
TBOX
p1500
p1500
p1500

New MARCH based test algorithm

W(P)R(P)W(~P)

R(~P)……

WGL pattern

Tester

TBOX_SEL

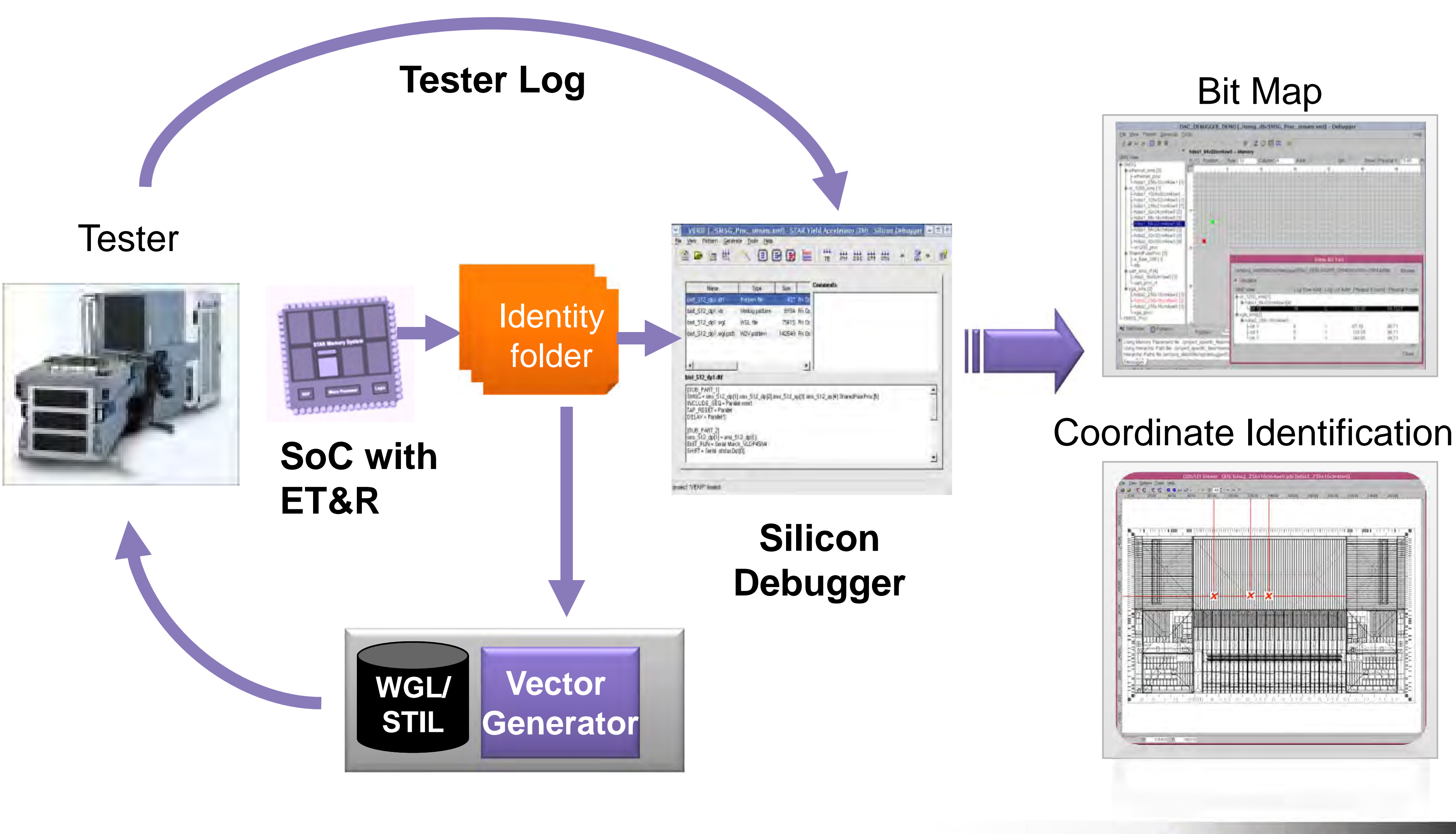
Load generated TEST algorithm

Continue with test flow

Select test algorithm register for serial access

Load alternative test algorithm

Automated Rapid Fault Isolation and Identification



Multi-level Precision Diagnostics

- Level 1: Memory Instance Failure
- Level 2: Logical Address of Failure
- Level 3: Physical Address of Failure (row, col)
- Level 4: Physical X,Y coordinates of failing bit
- Level 5: Defect classification (sing bit, paired bit, col, row etc.)
- Level 6: Fault Classification (stuck-at, transition, coupling, etc.)
- Level 7: Fault localization (aggressor/victim cell coordinates etc.)

Low Cost Failure Diagnostics Solution

Silicon Browser

- Visualization of Test Results
- Memory Dump

Identity folder

SoC Design with ET&R

Interactive data exchange

Chip with STAR Memory System

JTAG

- Diagnostics
- Fault localization
- Memory Characterization

Yield Optimization

Tester

- Embedded Test & Repair
  - Test/Repair IP Insertion
  - Vector Generation
  - Localization & Signatures
- Yield Optimization
  - Failure Visualizations
  - Cross-Domain Correlations
  - Dominant Failure Modes

Fail Data

Identity Folder

Bitmap

Coordinates

Silicon Debugger

Visualizations

Correlations

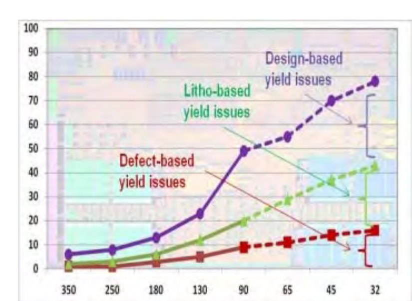
Statistical Prioritization of Failure Modes

Yield Optimization

Identifying Dominant Failure Mechanism

How to get the largest yield improvement

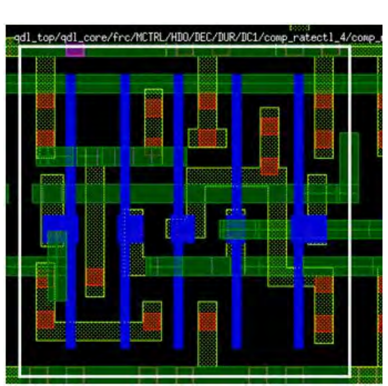
- Rise in systematic defects
  - Very few dirt particles or fall-on defects

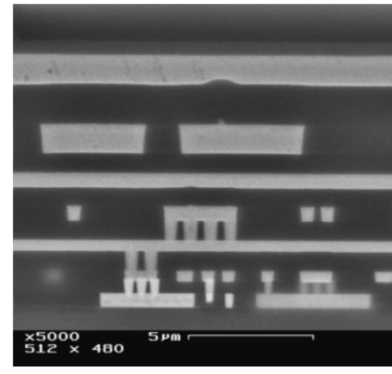


- 100s of failed dies in first silicon

- 10-50 fault candidates per failed and diagnosed die

- 15-20 metal segments & Via per candidate net



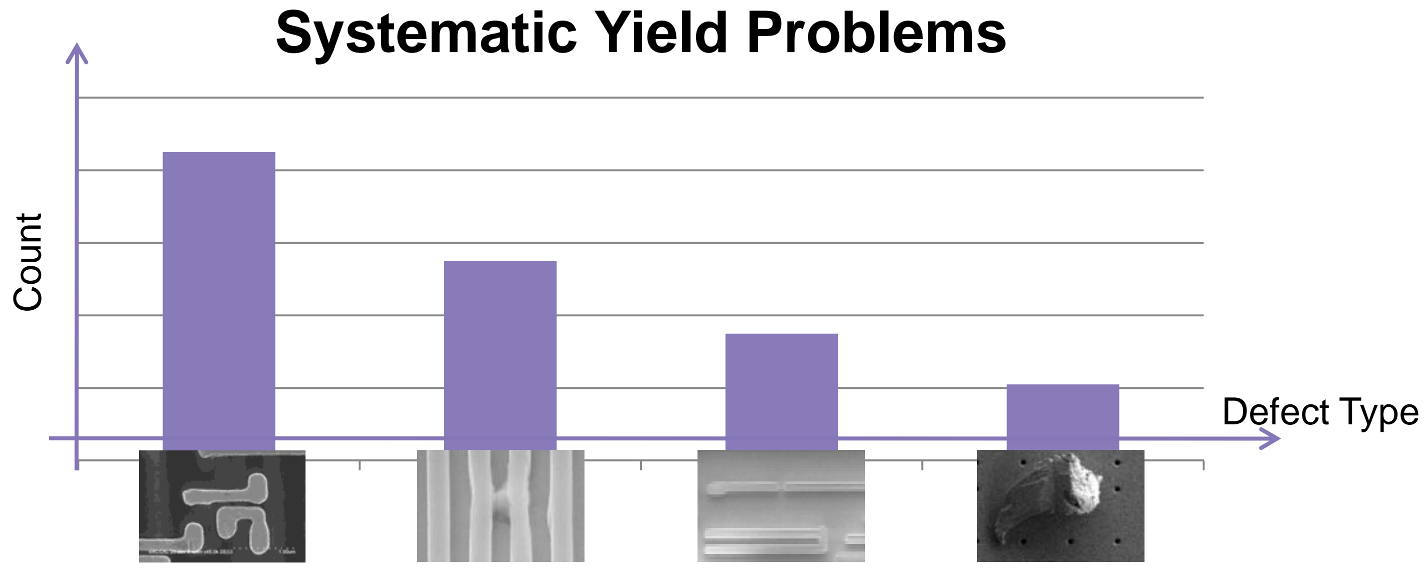


- 100x10x10 = 10k sites for FA
  - For each silicon lot during ramp

- FA cycle time per site: 4-8 hours
  - Can manage <10 sites only

How Does Volume Diagnostics Help?

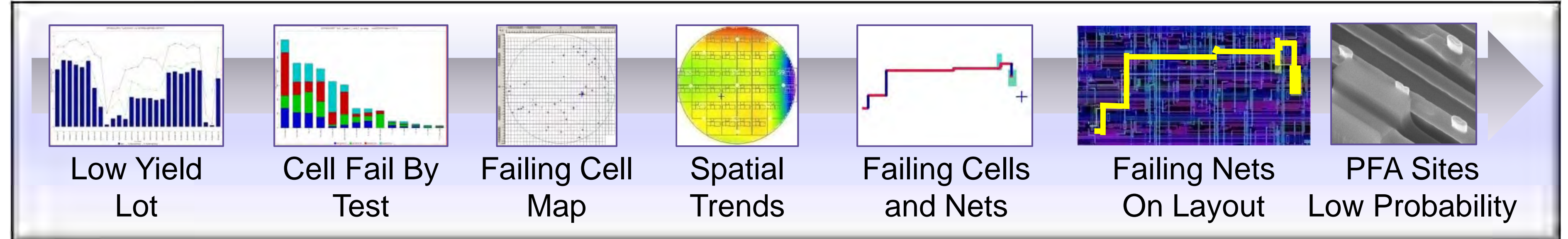
- Volume Diagnostics
  - Statistical Analysis of Diagnostics results from multiple failing chips
  - Identifies systematic, yield-limiting issues by using design data
  - Produce outputs for Physical Failure Analysis (PFA)

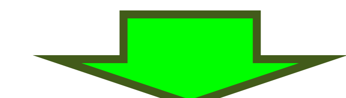


Design-Centric Volume Diagnostics

Multi-Tool Manual Flow

2-3 Weeks





Yield Optimization Automated Flow

2-3 Days

*PFA – Physical Failure Analysis

- An order of magnitude faster systematic failure localization
- Prioritization of failure types based on yield impact
- Success in capturing dominant systematic failure mechanisms

Shortest Time to Volume

Tape Out to First Silicon

Pattern Generation

Weeks

Silicon Bring Up

Pattern Optimization & Silicon Debug

Tester

Months

Production

Defect Analysis for Yield Optimization

Months

FAB

IP

DESIGN

Typical Time-to-Volume

Using ET&R

Reduced Time-to-Volume

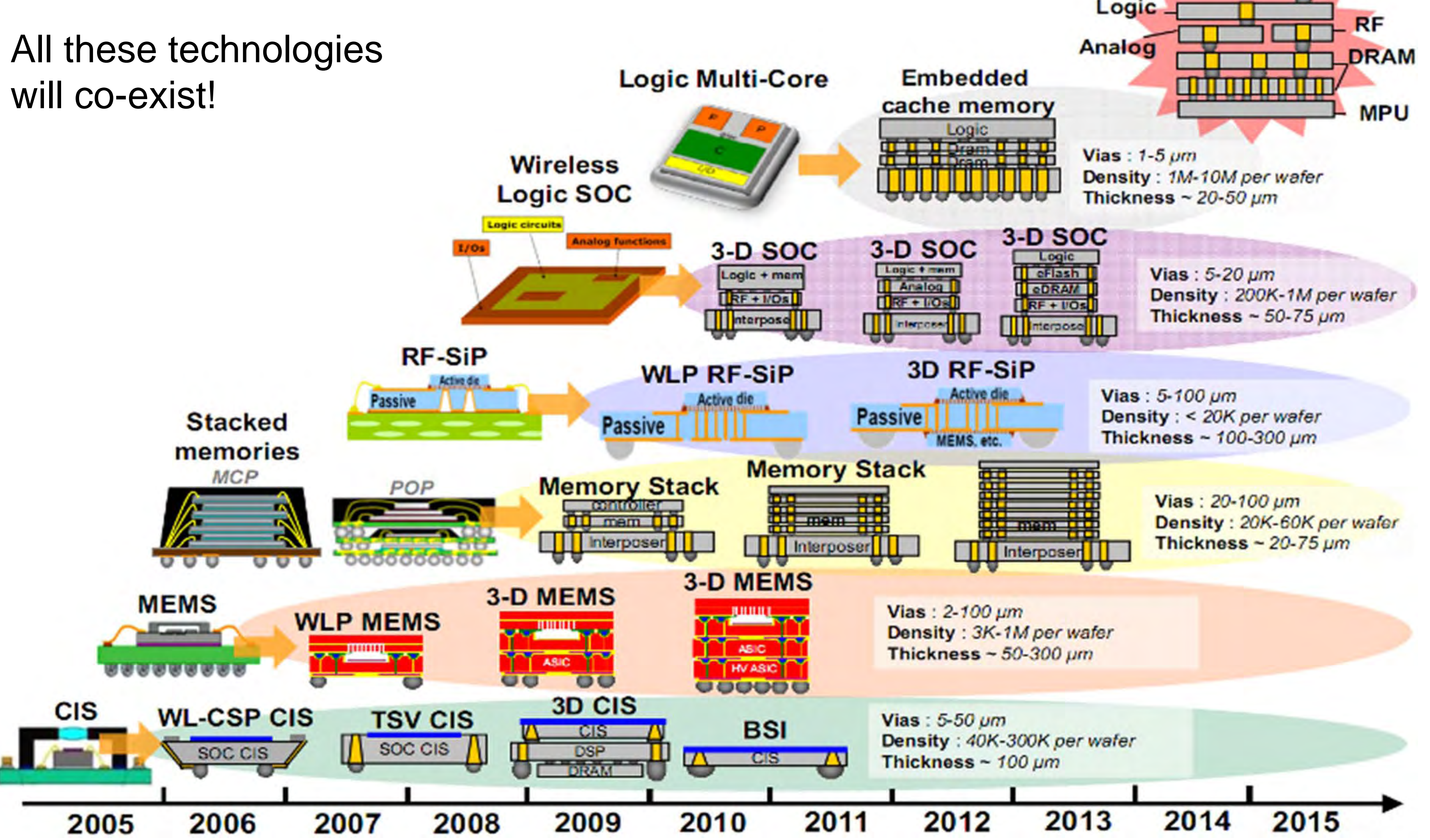
Days

Days

Weeks

Trends for 3D Stacking

All these technologies
will co-exist!

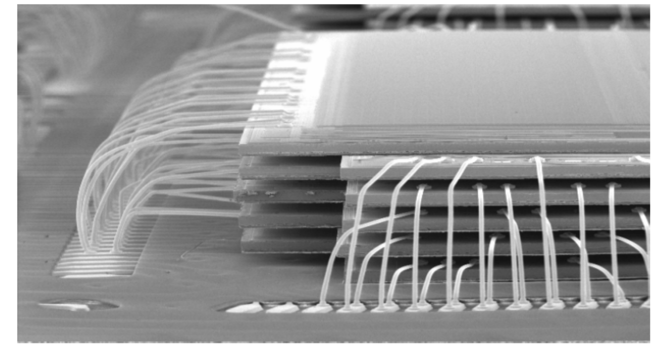


Source: Yole Développement 2008

3D Packaging in cell phones

- 3D packaging used in cell phones for several years
  - Stacked dies with Wire bond

Memory

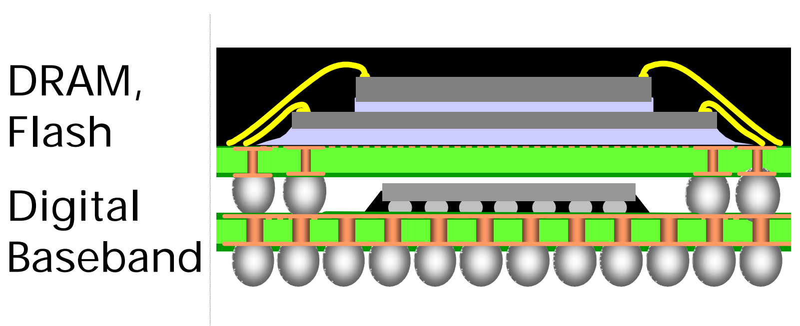


  - Package on Package (PoP)

2003 STM « world record »

DRAM, Flash

Digital Baseband



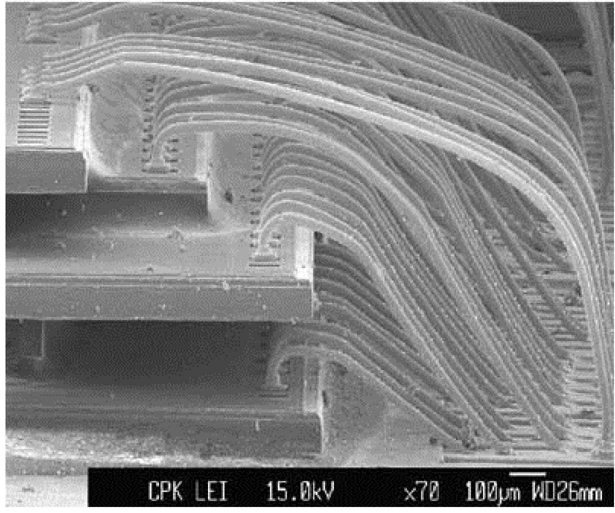
Source: Prismark

Beyond SoC: SiP Alternatives

- SoC: System-on-Chip. Integrate combinations of logic, processor, SRAM, DSP, A/RF, DRAM, NVM
- SiP: 3D Stacked Dies
  1. Non-TSV
     – bare die stacking: wirebond, flipchip, embedded die substrate
     – package stacking: PoP, PiP
  2. TSV
     – via first, via middle, via last

Evolution in 3D Technologies

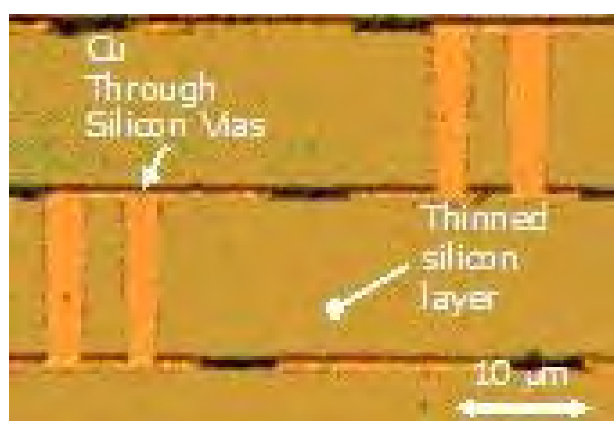
non-TSV



Limitations

- Peripheral bonds only
- Long wire bonds (high inductance, high crosstalk, low speed interconnect)
- **➔ Limited to low-density interconnects and with specific I/O pad routing**

TSV

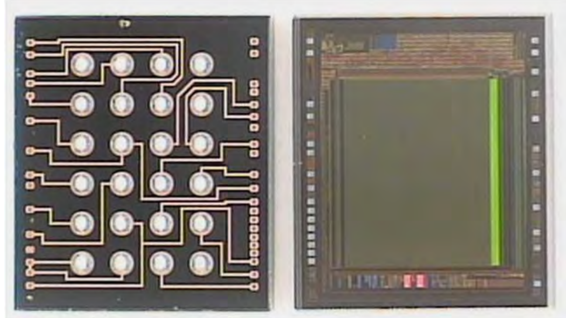


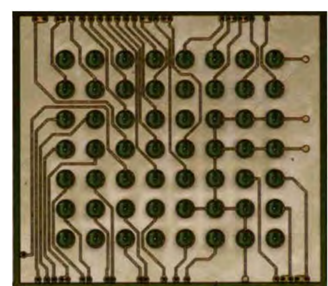
Benefits

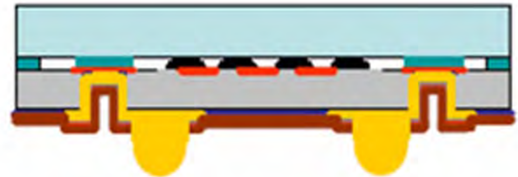
- Area placement
- Excellent electrical characteristics
- High densities
- **➔ Orders of magnitude higher interconnect densities between dies**

Through Silicon Via Pros and Cons

- Pros
  - Allow even smaller package outline
  - No pad extension needed
  - Lower sensitivity to foreign material at Camera assembly
  - Wire bonding compatible layout
  - Reflow process compatible
  - Better interconnect routing capability
- Cons
  - More complex technology
    - Glass
    - Silicon
    - Back-end processes
  - Cost

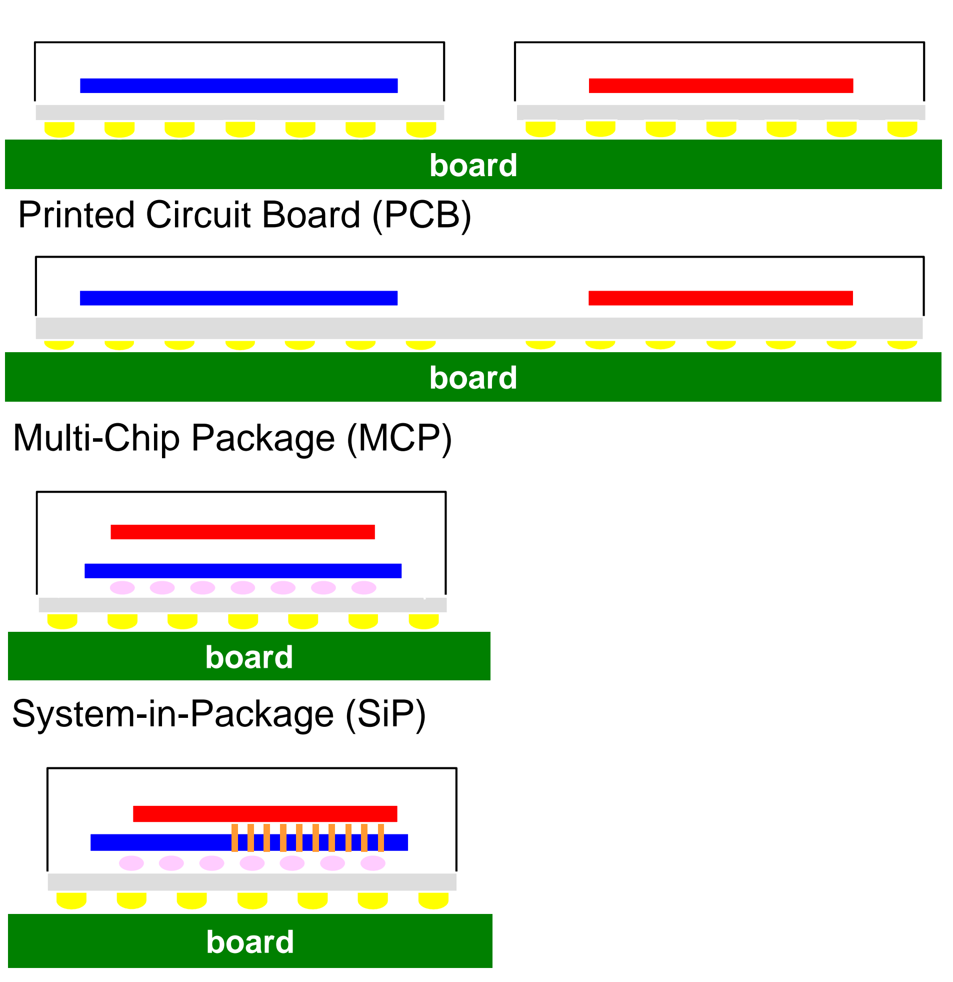






Through via contacts
From top to bottom

3D Stacking is Not New…But TSVs Are!



- **Multi-Chip Packaging**
  - Dense integration
  - Heterogeneous technologies
- **Vertical Stacking**
  - Denser integration
  - Smaller footprint
- **Through-Silicon Vias (TSVs)**
  - Even denser integration
  - Increased bandwidth
  - Increased performance
  - Lower power dissipation
  - Lower manufacturing cost

Yield Implication Due to 3D Levels

Assembled Product Yield=(Probability of Good Devices)Number of Devices

Probability of Good Devices = 99%

95%

90%

80%

70%

60%

Assembled product Yield

1.0
0.8
0.6
0.4
0.2

2 4 6 8 10

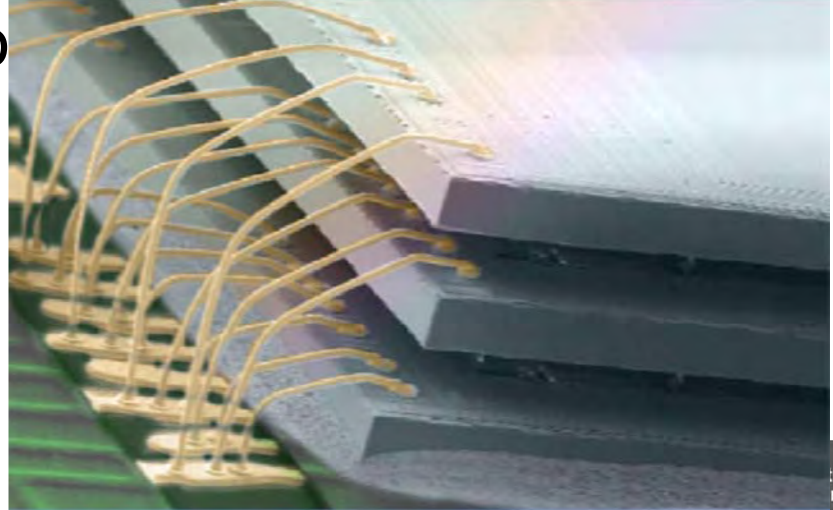
Number of Devices

Tests for 3D Induced Effects

- Test Coverage for TSV Interconnect
- Defect Coverage for due to
  - Thinning Process
  - Thermal Dissipation

Known Good Die Challenge:

- Conventional burn-in challenge
  - Full speed test and burn-in prior to packaging
  - Higher pin count with finer pitch
  - Increased functionality and frequency
- KGD requires
  - Extra stress during probe, carriers, or WLBI
- Necessary for SiP productio

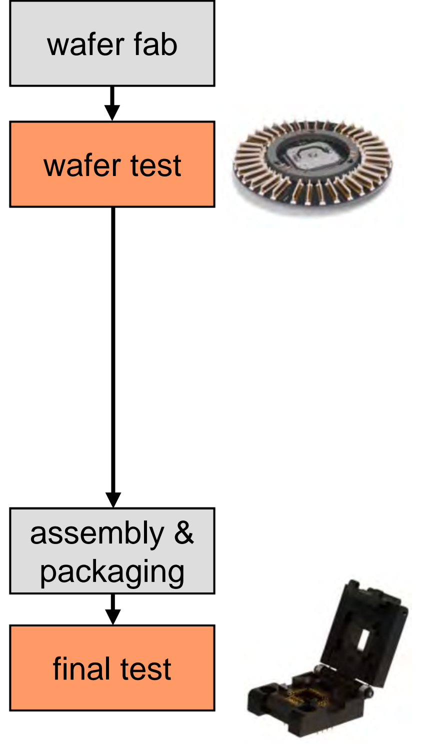


Wafer Level Burn-in and Test

- Greatly simplifies backend IC fabrication line

Conventional 2D Test Flow

Conventional 2D



- Main role of Final Test (FT): guarantee outgoing product quality
- Main role of Wafer Test (WT): prevent unnecessary package cost

- WT executed only if benefits exceed costs:

$$(1-y) \cdot d \cdot p > t$$

with

y: fabrication yield

d: fraction of faulty products that the WT can detect ('test quality')

p: preventable product cost

t: test execution cost

2D Test Flow vs. 3D Test Flow

Conventional 2D

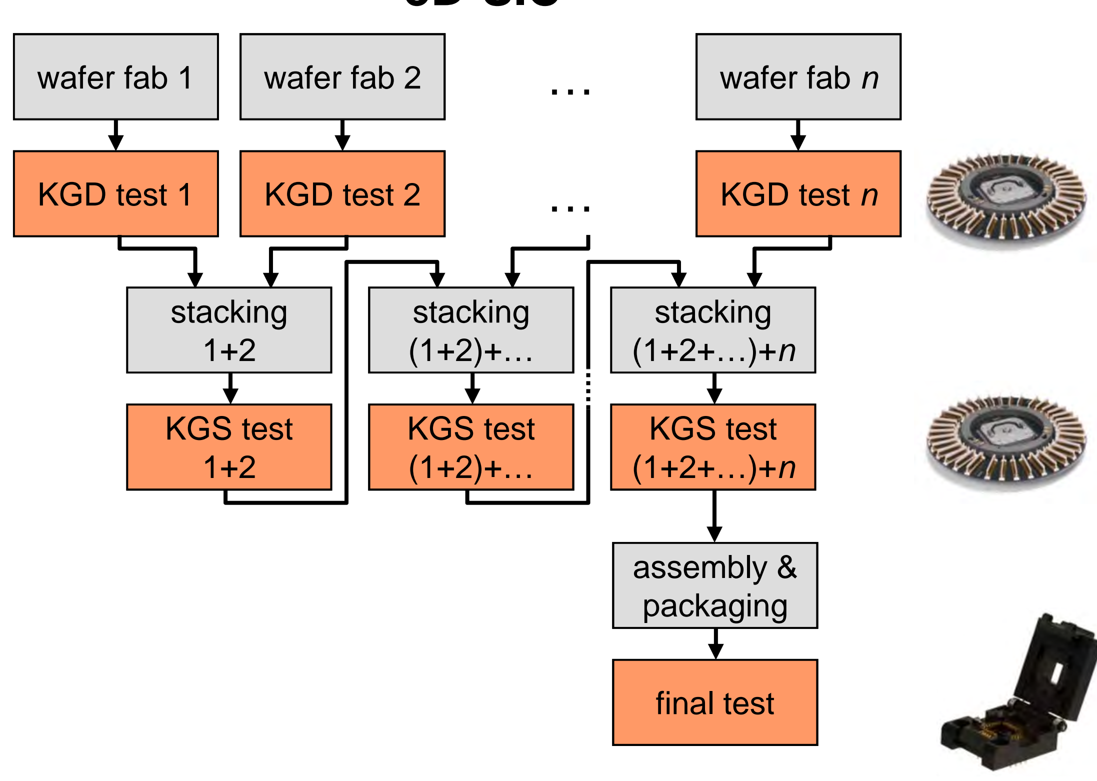
wafer fab

wafer test

assembly & packaging

final test

3D-SIC



- Terminology
  - **KGD** : Known-Good Die test
  - **KGS** : Known-Good Stack test

  } Test access is distinctly different! Test contents might be different.

- Better name would have been "Known-**Bad** Die/Stack" test ☺

Required Infrastructure

- Language for test description transfer
  - Core Test Language, CTL (IEEE Std. 1450.6) [Kapur – 2002]
- On-chip Design-for-Test for electrical test access
  - Test wrappers
    - Around cores: IEEE Std. 1500 [Da Silva et al. – 2006]
    - Around dies: to be developed NEW!
    - Around full-stack product: IEEE Std. 1149.1 [Parker – 2003]
  - Test Access Mechanisms
    - Intra-die: test bus, TestRail [Marinissen et al. – ITC'98]
    - Inter-die: TestElevator

- EDA support for automated 'test expansion' from module-level test into chip-level test

All What Is Known – And Some More…

- All manufacturing defects that can occur in conventional 2D chips,
  can also occur in 3D-SICs

- Hence, we need to apply all known test methods
  - Logic: stuck-at, transition, delay, VLV, …
  - Memory: array, decoder, control, data-lines, …
  - Analog: INL, THD, …

- In addition:
  1. Tests for new intra-die defects
  2. TSV interconnect tests

Advanced TSV-Interconnect Test

- ***Advanced fault models*** for TSV interconnects
  - Delay faults

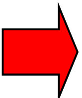
- Testing of ***infrastructure*** TSV interconnect
  - Power/ground TSV interconnects
  - Clock TSV interconnects

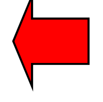
- TSV interconnect ***Redundancy & Repair***
  - Crank up bonding yield
  - Evaluate benefit/cost trade-offs

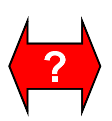
Wrapper Style: P1838

IEEE Std. 1149.1 ('JTAG')

- Interface
  - Single-bit for data and control: TDI-TDO
- Wrapper cells with double FFs
  - No ripple-through during shift
- Control via TAP Controller: fixed-protocol Finite State Machine

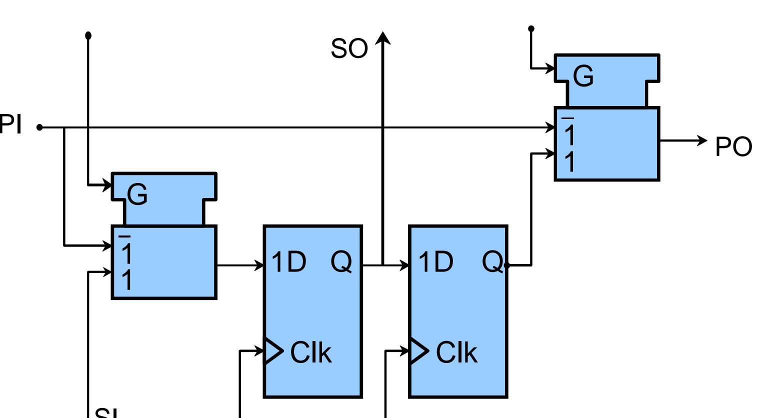


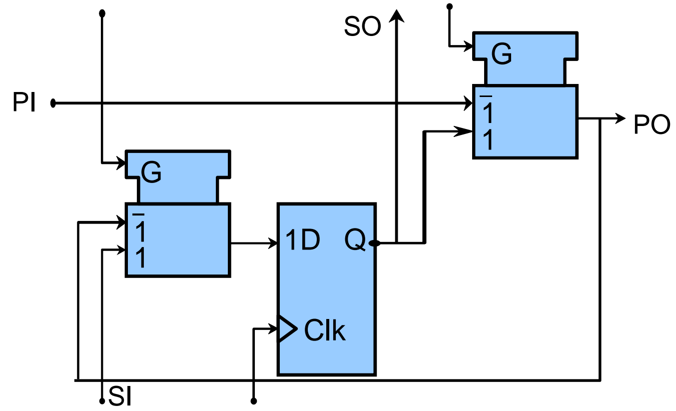




IEEE Std. 1500

- Interface
  - Mandatory single-bit: WSI-WSO
  - Optional *n*-bit: WPI-WPO
- Scalable wrapper cells
  - Single-FF cell most common
- Control via flexible instruction shift register





The Role of Advanced DfT Techniques

- **RPCT – Reduced Pad-Count Testing**
  Reduce width of scan-test interface
  - Useful to limit additional probe pads for KGD testing
  - Same test data volume: smaller interface → longer test length

- **TDC – Test Data Compression**
  Reduce off-chip test data volume by on-chip (de-)compression
  - Definitely applicable to 3D-SIC 'super chips'
  - Great combination with RPCT

- **BIST – Built-In Self-Test**
  On-chip stimulus generation and response evaluation
  - Reduces off-chip test data volume to (virtually) zero
  - Narrow TAMs / TestElevators
  - Protection of proprietary test contents – execute and trust
  - Especially attractive for memory dies – MBIST

3D Test Resource Partitioning

- 3D-SICs offer new opportunities to system architects
- 3D-SICs offer new opportunities to DfT architects
  - Which DfT resource to put in which die?
    $\Rightarrow$ **Test Resource Partitioning**

- **Example: DRAM-on-Logic**
  1. MBIST in DRAM Die
     - "3D-Prepared" DRAM
     - Proprietary memory content does not need to be released
  2. MBIST in Logic Die
     - Drop-in MBIST module provided by DRAM vendor
     - MBIST implemented in logic process technology
     - Communication over TSV-based interconnects

Reliability Faults

- **Intermittent Faults:**
  - unstable hardware activated by environmental changes (lower voltage, temperature)
  - often become permanent faults
  - identifying requires characterization
  - process variation – main cause of IF
- **Transient Faults:**
  - occur because of temporary environmental conditions
  - neutrons and α-particles
  - power supply and interconnect noise
  - electromagnetic interference
  - electrostatic discharge

Reliability Faults (cont)

- Infant Mortality
  - rate worsens due to transistor scaling effects and new process technology and material
- Aging Induced Hard Failures
  - performance degradation over time (burn-in shows)
  - degradation varies over chip-chip and core-core
- Soft Errors
  - Random logic still at risk
  - RAM decreasing SEU per bit
- Low Vmin increases bit failures in memories
- Transient Errors, such as timing faults, crosstalk are major signal integrity problems

Field Reliability Challenge

Normlized FIT Rate

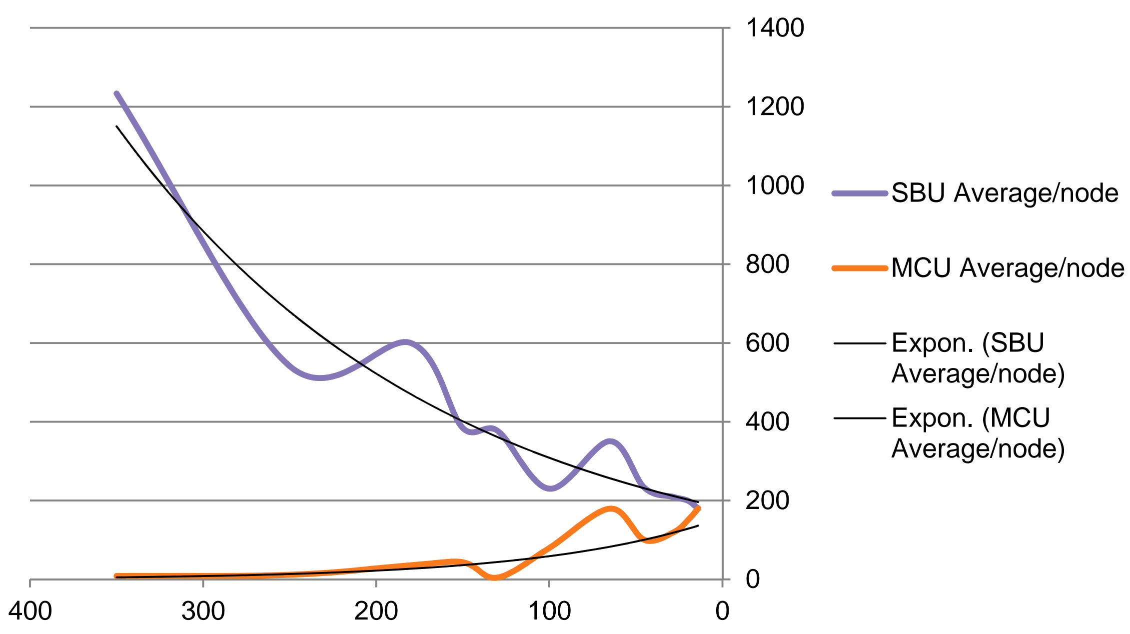
100000
10000
1000
100
10
1
0.1

0
0.05
0.1
0.15
0.2
0.25

2012
2008
2005
2003
2001
1999
1997

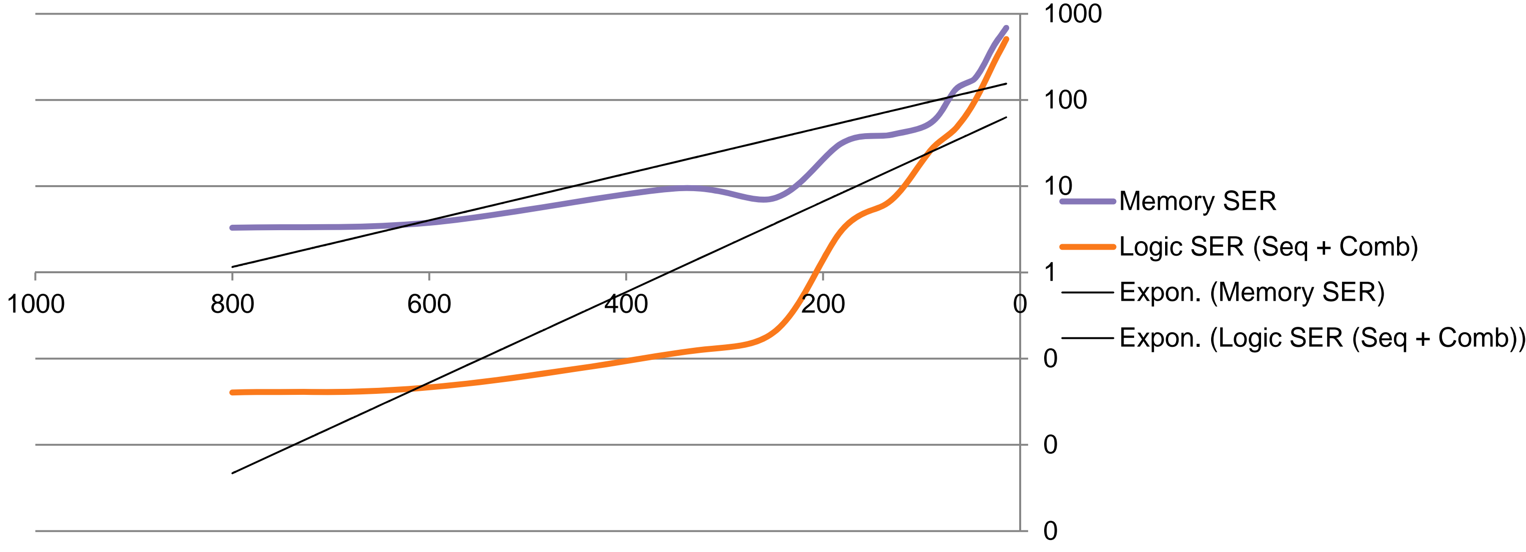
The error bars account for the range of supply voltage. The SER increases **exponentially** at 2.1-2.2 decades/volt, e.g 200X in 2005.

MCU Growth Over Technology Nodes



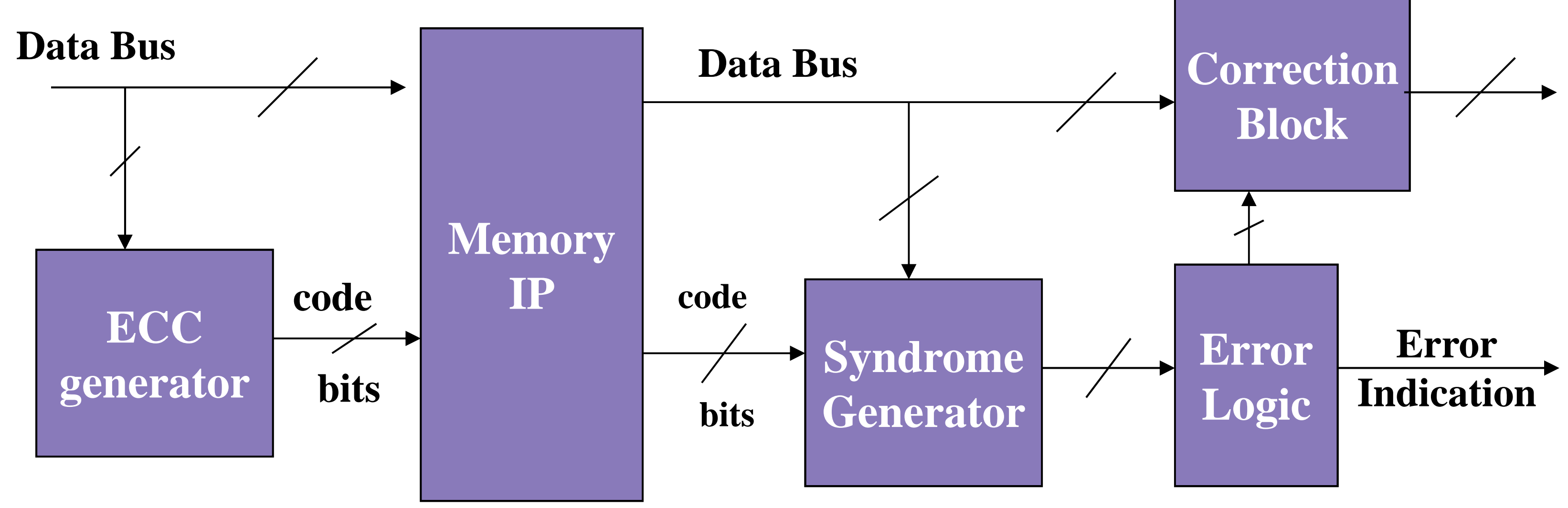
Source: iRoC

SER Growth at SOC Level



Source: iRoC

Robustness IP for ECC



- Standard ECC architecture provides single bit repair
- RAM multi-bit upset probability depends on cell to cell distance

Thank You
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