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Description of the MEMS CIS Probe Card – electrical characteristic, Parallelism & Reliability

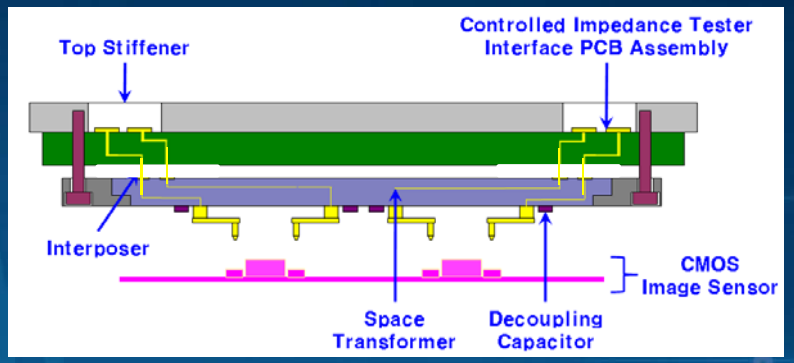
Jung Keun Park
Willtechnology

Overview

- **Background**
  - Design limitation, Things to consider, Trend
- **CIS Probe Card**
  - Cantilever, MEMS
- **Electrical Performance**
- **Multi Para Extension**
- **Reliability**
- **Summary**

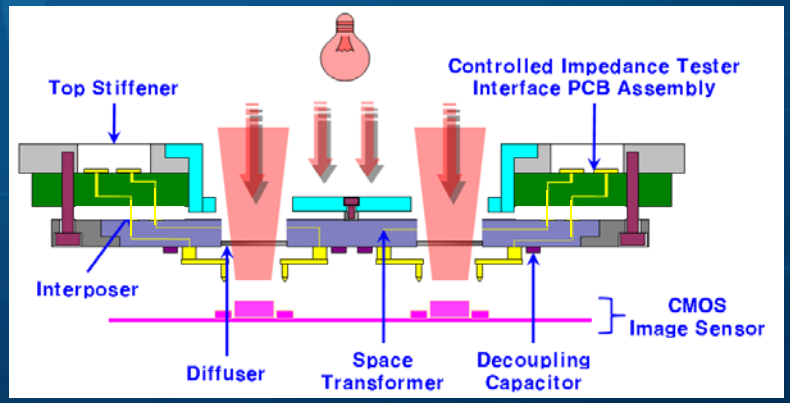
Background

- Increasing STF layers
- Reduced SI, PI performance as a result of additional layers
- Cost increase



Normal Logic Card

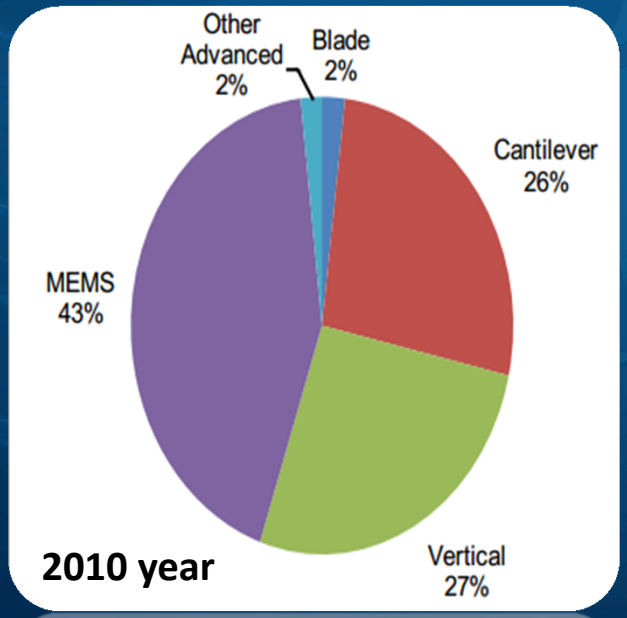
- Mobile application required
  Low Current product : PI characteristics Review
- Increased Data rate on MIPI PIN :
  SI characteristics review
- Limitation on optimization of Touch Down due to Image hole
  - Initial Review 2X2 Skip, 1X1 skip
    mass production (STF technology development)
- 64Para 1x1 Skip mass-production



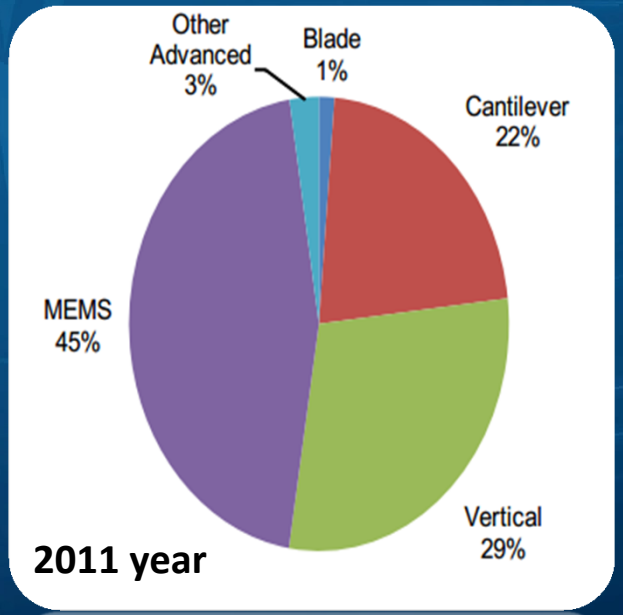
CMOS Image Sensor Card

Background

- Probe Card market shift : Cantilever Type -> MEMS and Vertical Type
- CIS Probe card is moving from Cantilever to MEMS
- Comparison between Cantilever and MEMS Probe Cards
- Why MEMS?



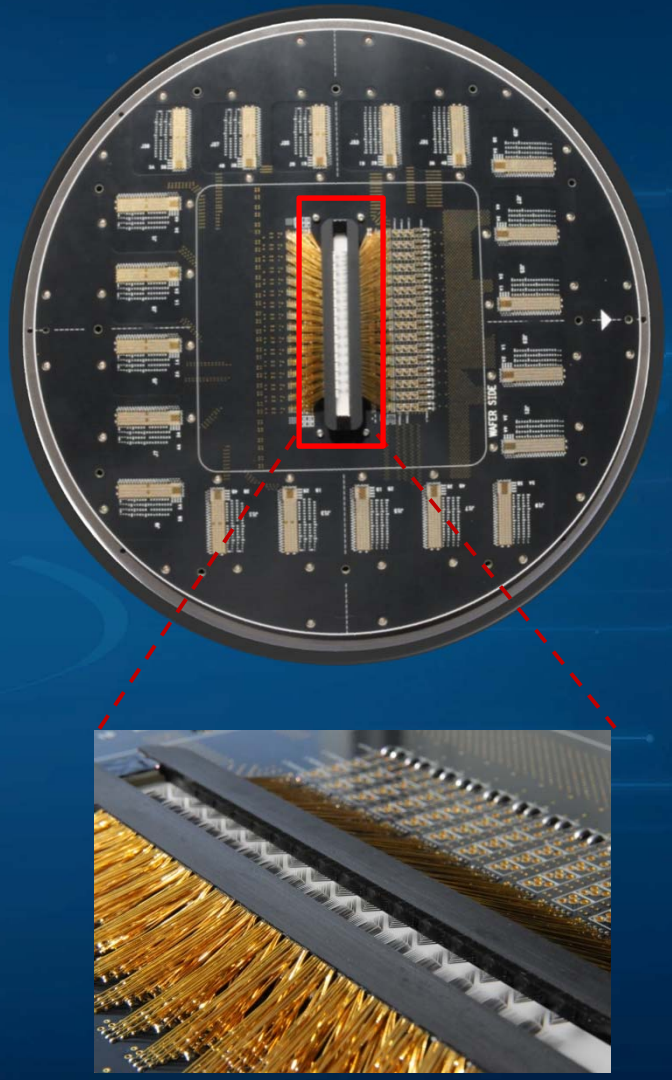
▪ Each Probe Card revenue
(VLSI Research 2012)



Cantilever CIS Probe Card

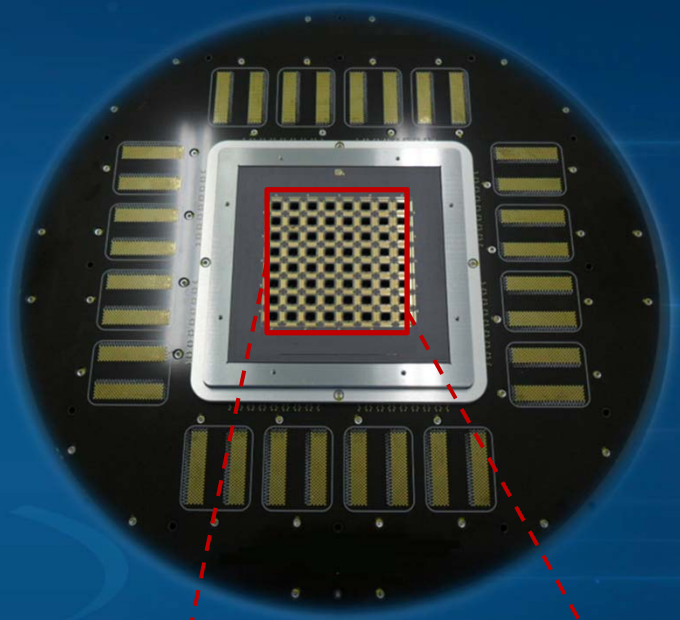
- **ADVANTAGE**
  - Quick turn out
  - Low Cost
  - Suitable for Fine Pitch

- **DISADVANTAGE**
  - Unsuitable for High Speed TEST
  - Limitation on Multi Para expansion (Max 16 ~32 para)
  - Difficult to ensure Electrical uniformity throughout

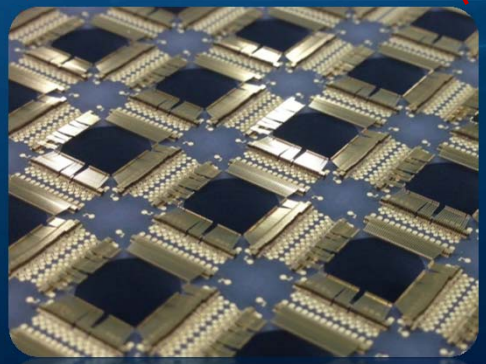


MEMS CIS Probe Card

- **Advantage**
  - Suitable for High Speed Test
  - Multi Para (64para) or Full Wafer Contact expansion capable
  - Reduction in Wafer test time
  - Able to achieve Electrical uniformity



- **Disadvantage**
  - Longer production time compared to Cantilever
  - Higher production cost



CIS Probe Card

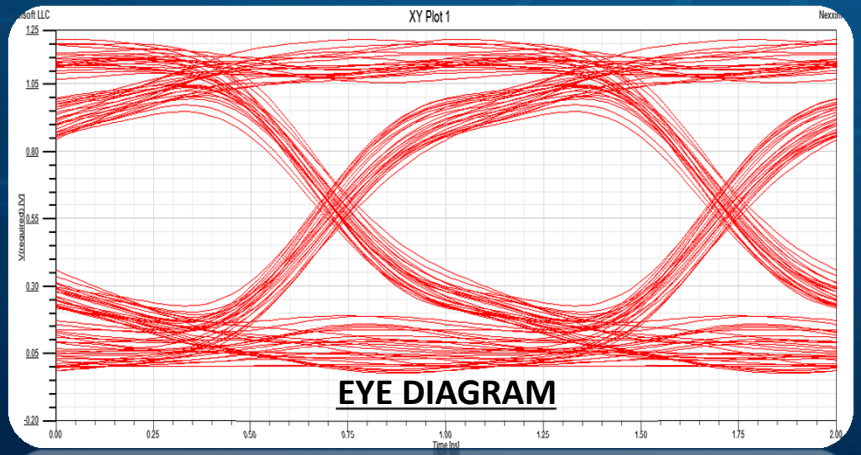
Cantilever Probe Card vs MEMS Probe Card

	Cantilever	MEMS
Electric Performance	△	O
Multi Parallelism	<32Para	<64Para or FWC
Mass Production	△	O
Scrub Length uniformity	△	O
Fine Pitch	O	△
Cost	Low	High
Delivery	O	△
Wafer Test efficiency	△	O

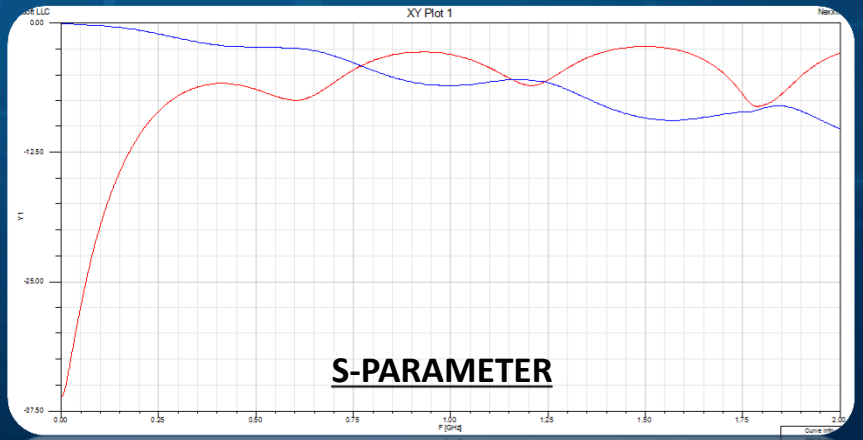
Electrical Performance

- **Signal Integrity**
  - Signal integrity is a measure of the quality of an electrical signal.
  - Zo, Transmission, Reflection, Crosstalk, Current return path etc..
  - Minimization of Impedance Mismatching Sections

Tester Power → **Probe Card Connector(ZIF, POGO), PCB, Interposer, STF, Needle etc..** → **Wafer**



EYE DIAGRAM

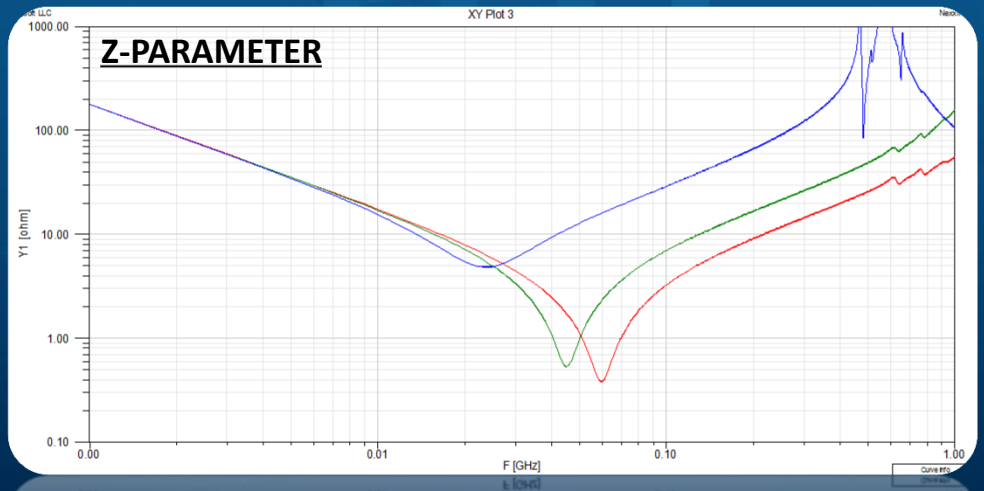


S-PARAMETER

Electrical Performance

- **Power Integrity**
  - Technology to minimize noise between Power and Ground
  - Simultaneously consider Tester + Probe Card + Wafer (Operating Current)

Tester Power → **PDN(Power Delivery Network) Connector(ZIF, POGO), PCB, Interposer, STF, Decoupling Capacitor etc..** → **Wafer (Operating Current)**



Electrical Performance

Method for SI Characteristic Improvement

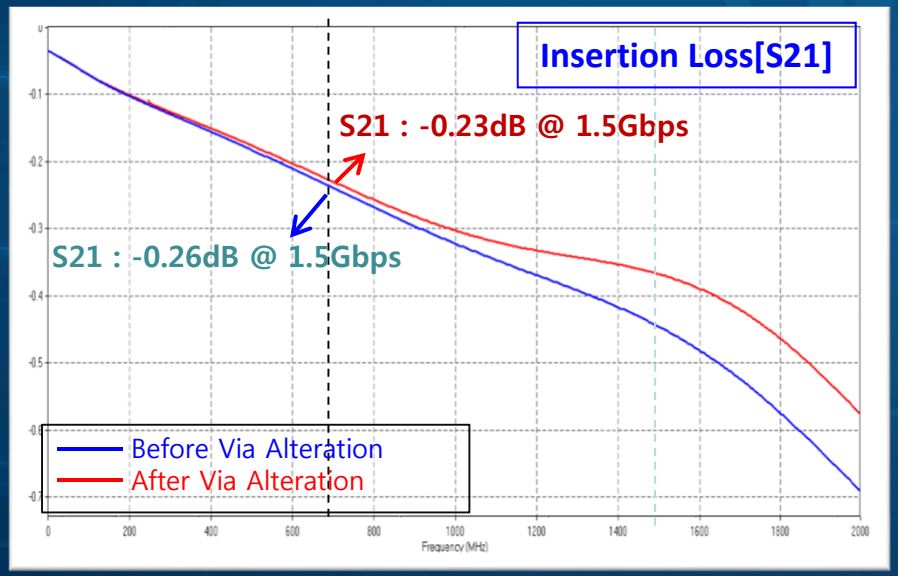
- **Optimize Via Design**
  - By Using Blind Via, Placement of GND Via alters signal characteristics
  - Just like Traces, S-G distances determines the Impedance
  - For uniform Via Impedance matching, GND Via design is required

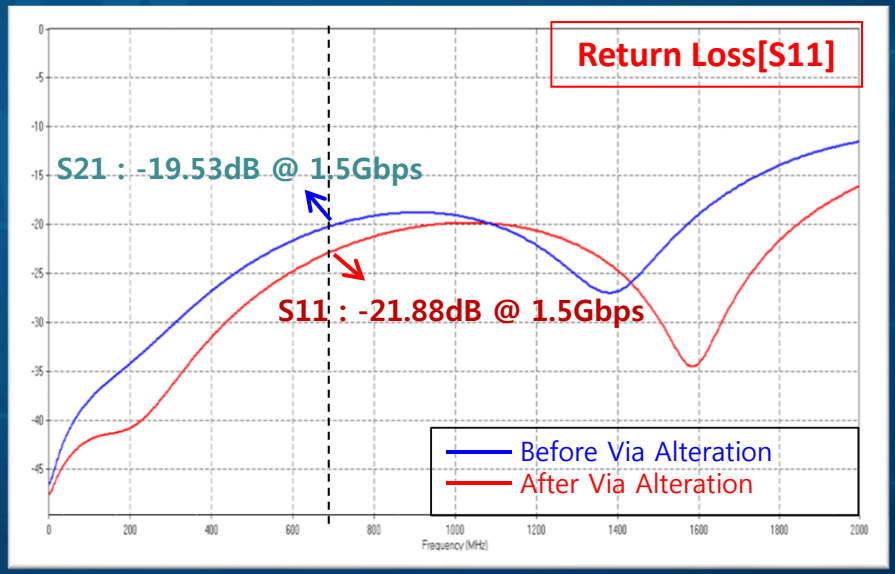
- **GND Shielding**
  - For High Speed Signal operation, Noise minimizing design is required
  - In most cases, Use GND Patterns to shield Signal Patterns

    Minimizes Coupling Noise from other signal lines

Electrical Performance

- **Via influences on SI characteristic improvements**
  - Analysis on signal characteristics improvements on various Via Discontinuity sections
  - Via improvements results in reduction of Impedance mismatching section
    -> Better SI characteristics
  - Impedance Control needed in Via sections as well

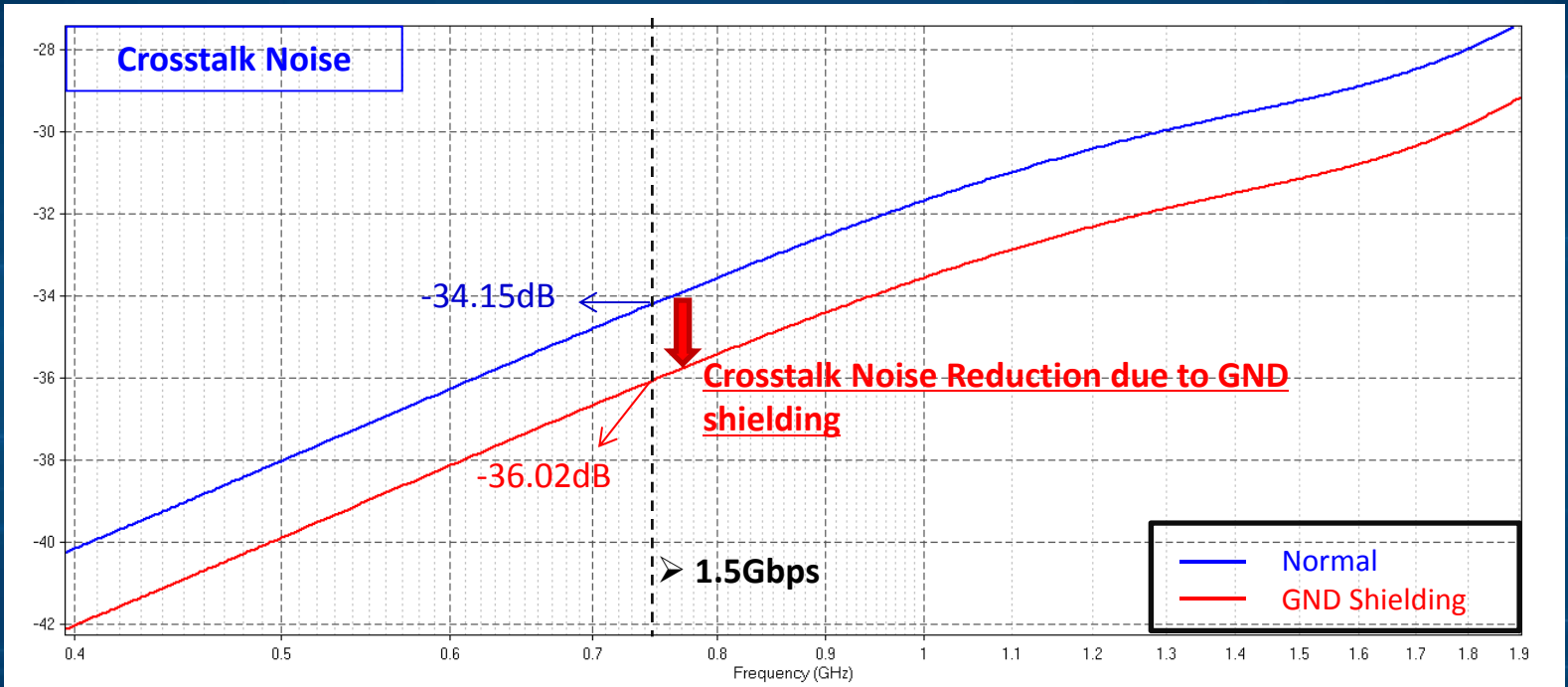




SI improvements by minimizing Impedance Discontinuity in via sections

Electrical Performance

- **Crosstalk noise improvements due to GND Shielding**

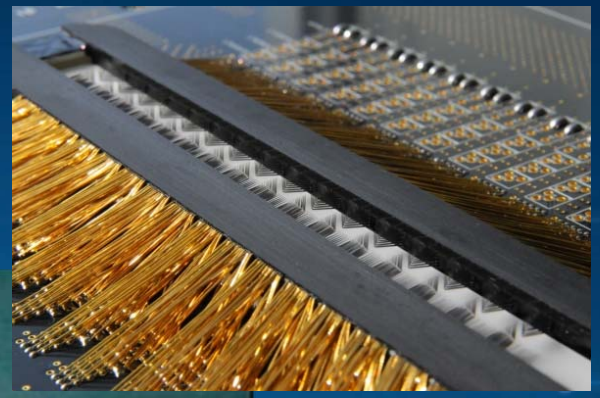


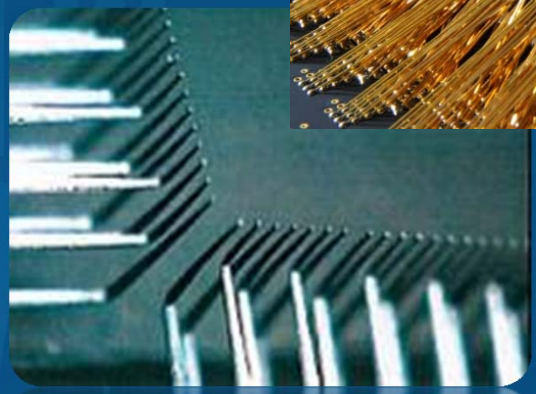
Reduction in Crosstalk Noise due to GND Shielding

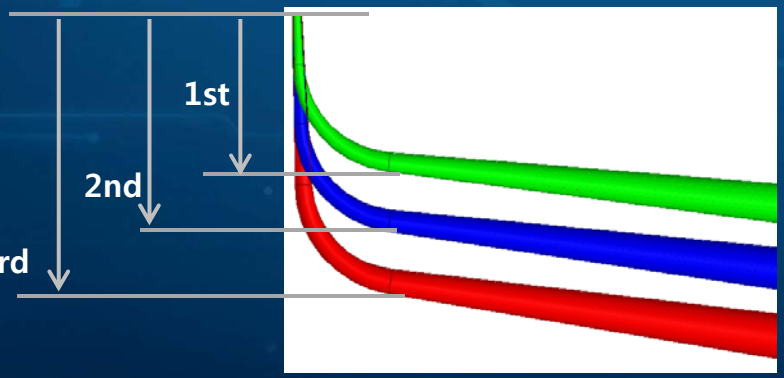
Electrical Performance

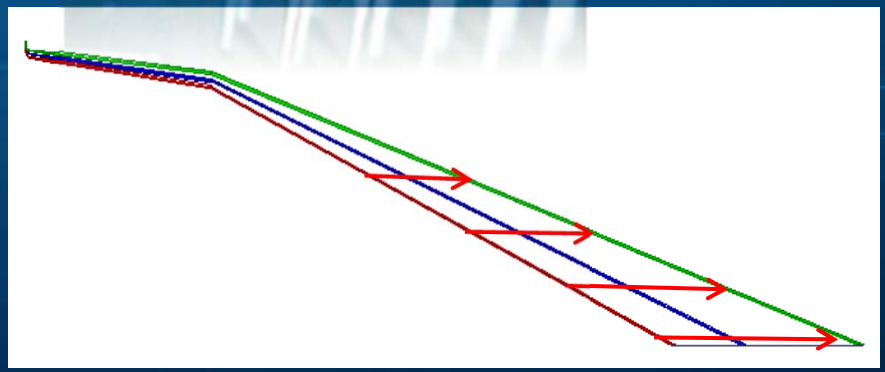
Cantilever / MEMS Probe Structure

- **Cantilever CIS Probe Card**
  - Length : 30 ~ 60mm
  - Stacked structure (Max 10 layers)
  - Longer Length degrades signal quality
  - Increasing distance between Pins





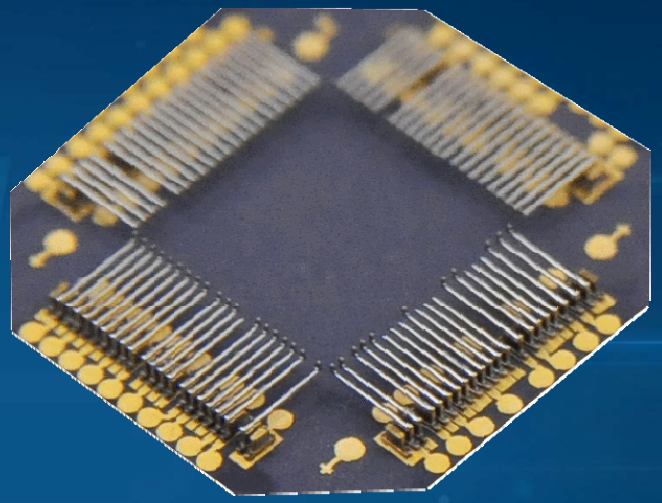


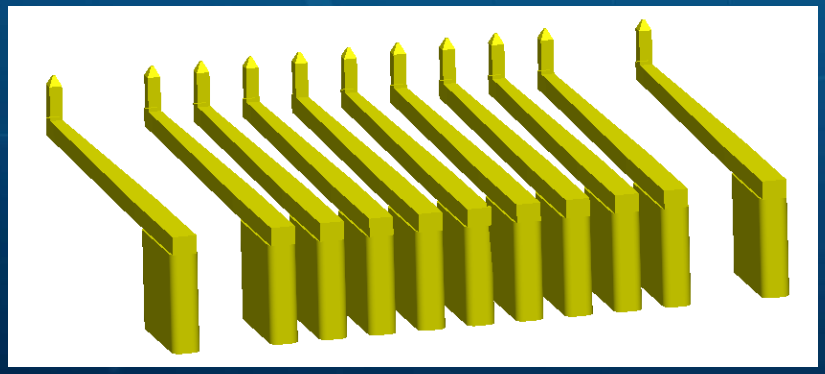


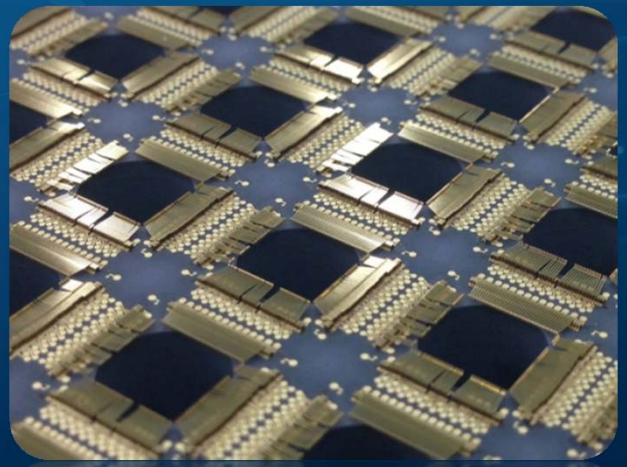
Electrical Performance

Cantilever / MEMS Probe Structure

- **MEMS CIS Probe Card**
  - Length : < 2mm
  - Short Length results in smaller signal Loss
  - Possibility of Mass Production with MEMS Fabrication techniques
  - Technical challenges exist to cope with Fine Pitch



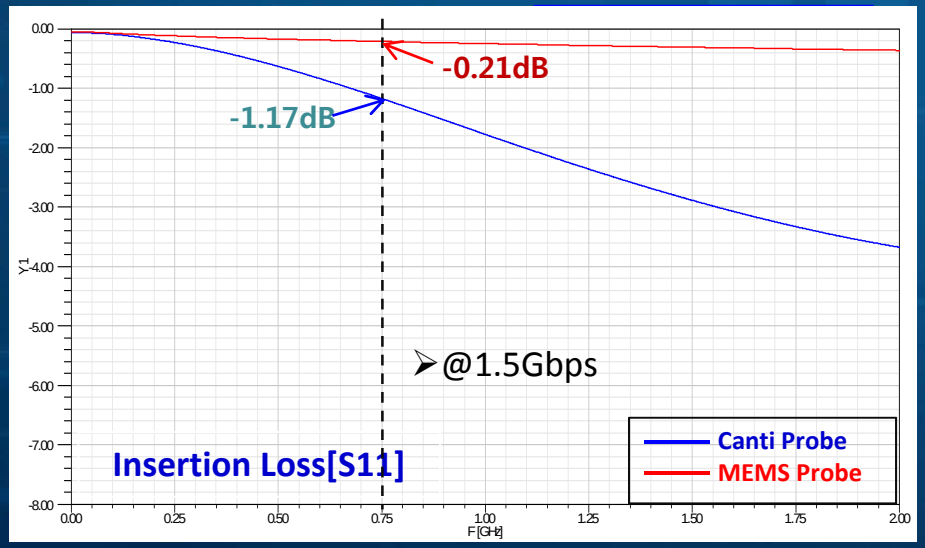


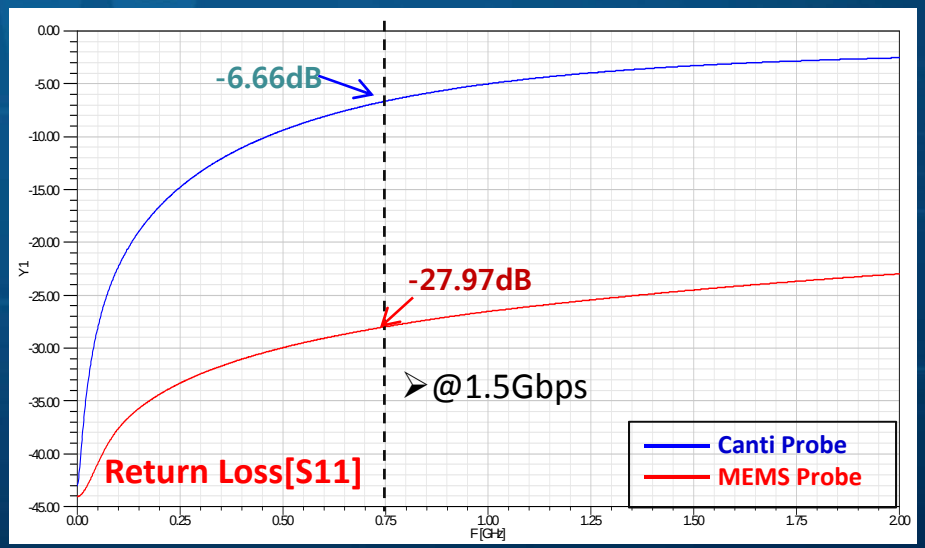


Electrical Performance

Cantilever / MEMS Probe Signal characteristics comparison

- Insertion Loss @ 1.5Gbps: Cantilever -1.17dB , MEMS -0.21dB
- Increasing gap between pins on Cantilever results in higher signal reflection
- By differences in signal reflection, and Length, MEMS demonstrates superior quality over Cantilever





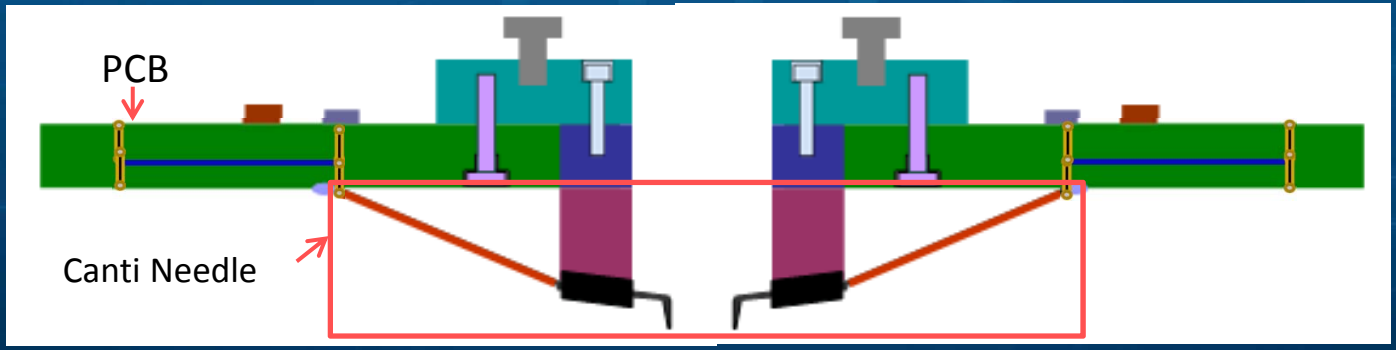
Electrical Performance

- **Cantilever CIS**
  - Long Needle Length increases Impedance Mismatching section

  ➡ **Increase in signal reflection is unsuitable**

  - DUT – PCB distance relatively longer

  ➡ **Inadequate PI property due to greater Inductance**



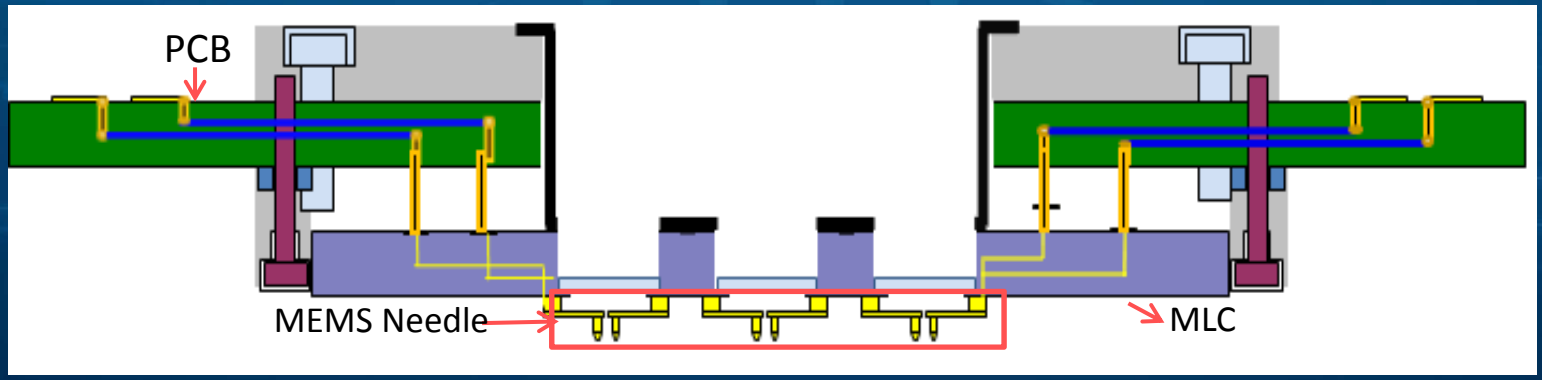
Electrical Performance

- **MEMS CIS**
  - Multi Layer Ceramic (MLC) is used
  - Short Needle Length, Impedance Matched within MLC

  ➞ **Decrease in Impedance Mismatching section achieves favorable SI property**

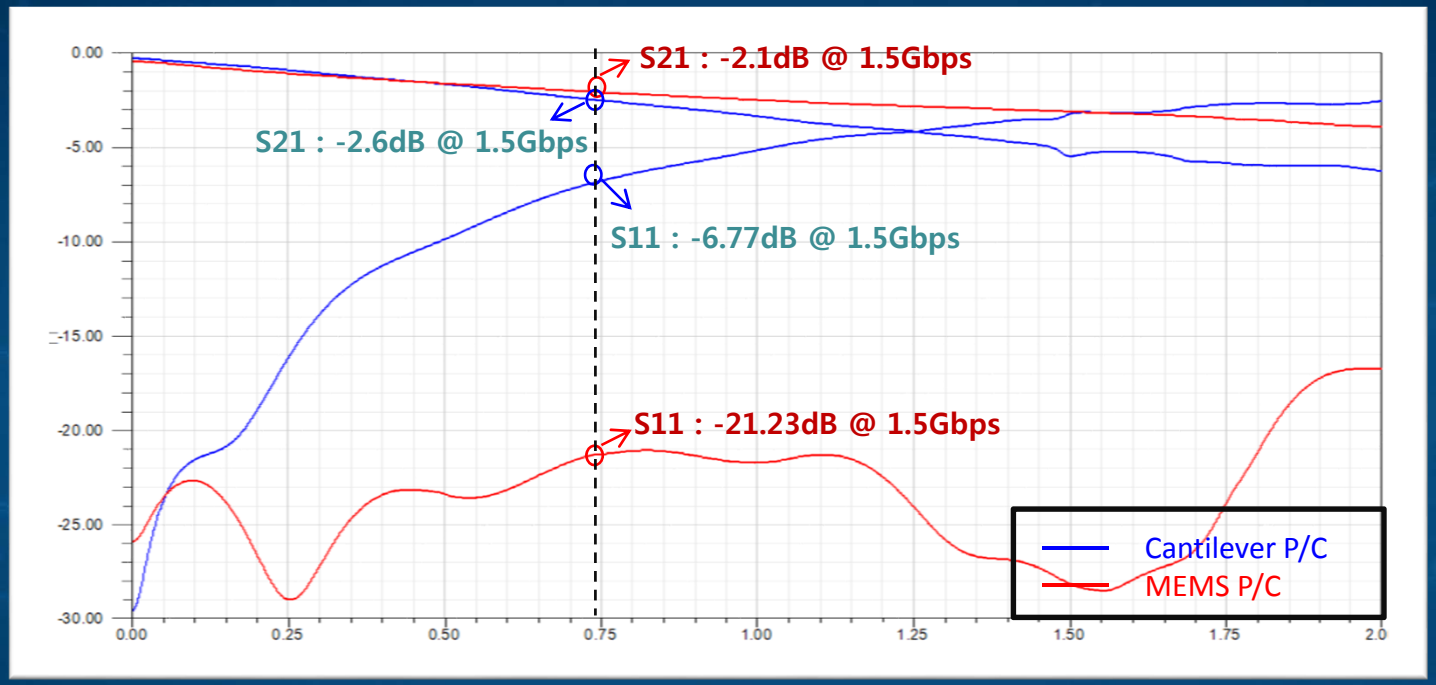
  - Able to design Power Plane at MLC level, Short DUT – MLC length

  ➞ **Low Inductance, favorable in respect to PI property**



Electrical Performance

Cantilever P/C vs MEMS P/C SI Characteristics (S-Parameter)



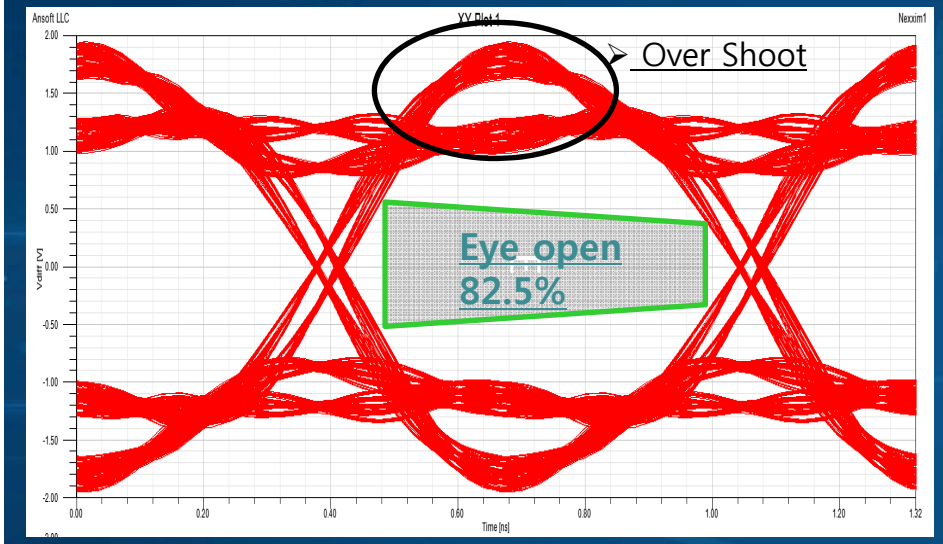
Cantilever P/C		MEMS P/C
Transmission : -2.6dB (@1.5Gbps)	<	Transmission : -2.1dB (@1.5Gbps)
Reflection : -6.77dB (@1.5Gbps)	<	Reflection : -21.23dB (@1.5Gbps)

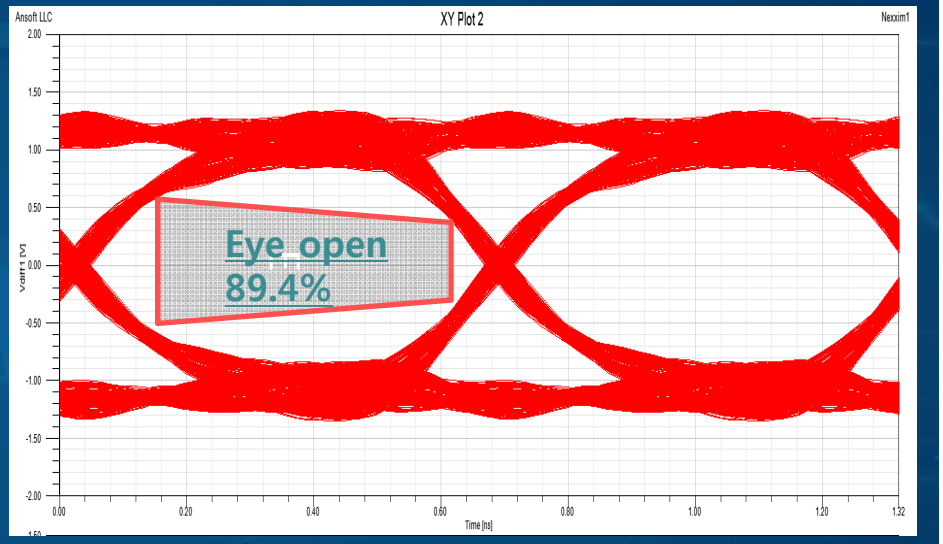
Cantilever with Longer Impedance Mismatching length in comparison results in higher reflection

Electrical Performance

Cantilever P/C vs MEMS P/C SI characteristics (Eye Diagram @ 1.5Gbps)

- **Cantilever CIS Probe Card**
- **MEMS CIS Probe Card**





Cantilever P/C		MEMS P/C
EYE OPEN : 82.5%	<	EYE OPEN : 89.4%
Large Overshoot	<	Small Overshoot

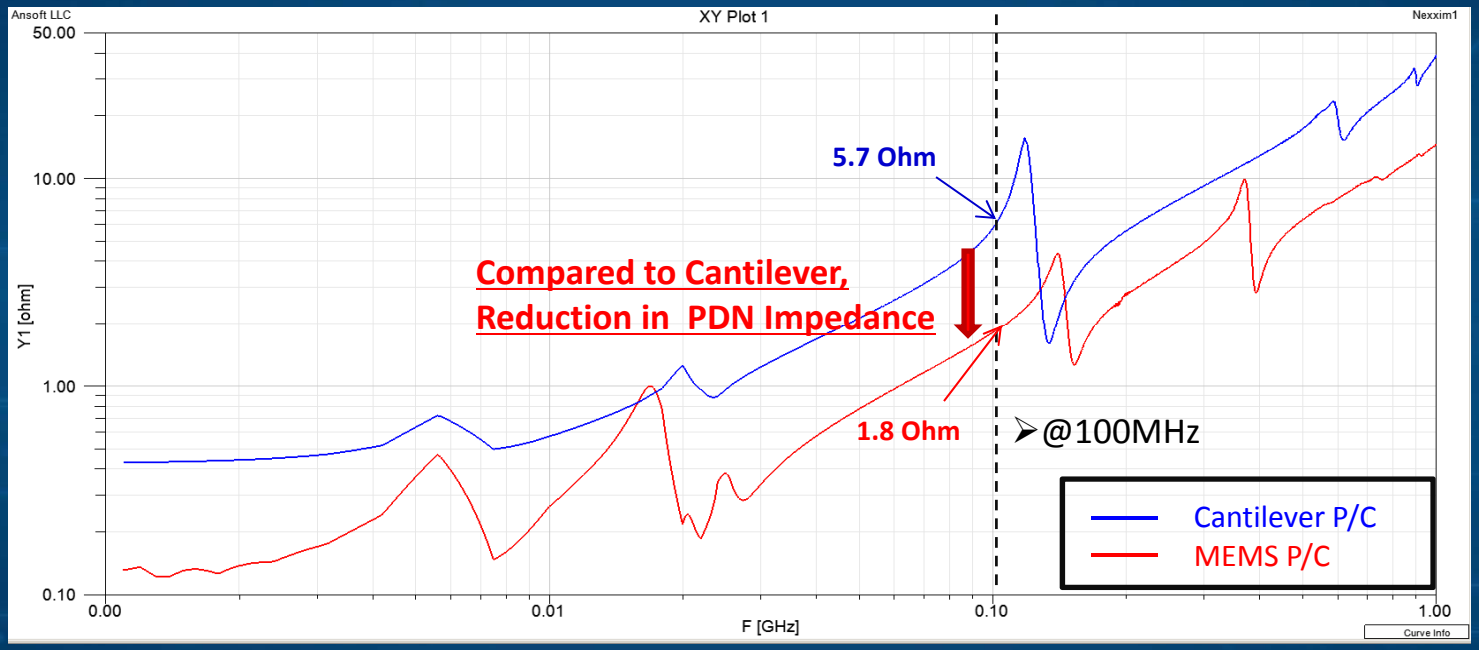
Cantilever P/C with large signal reflection results in large Over Shoot

MEMS P/C is more stable with large EYE Opening

Electrical Performance

Cantilever P/C vs MEMS P/C PI characteristics (Z-Parameter)

Cantilever P/C Impedance : 5.7 Ohm (@100MHz) > **MEMS P/C** Impedance : 1.8 Ohm (@100MHz)



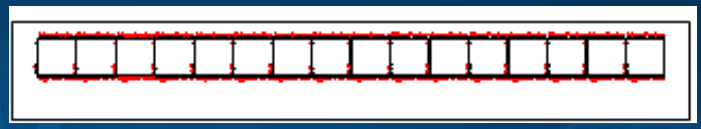
MEMS P/C

- Short Needle Length
- Power Plane Design using MLC

→ **Improvements in PI**

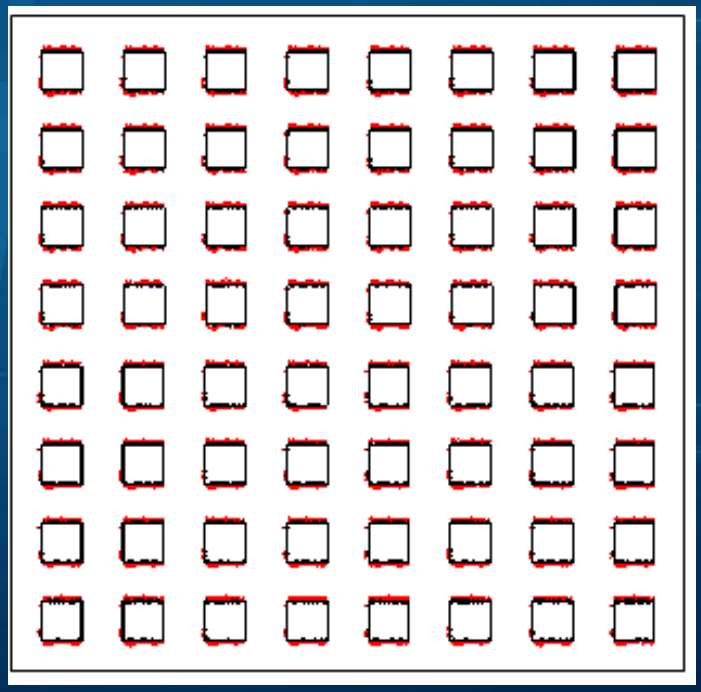
Multi Parallelism

- **Cantilever CIS Probe Card**
  - Max 16 ~ 32Para
  - 16 x 1 (No Skip)
  - Multi-para expansion Limited by number of Pin & Pin arrangement



CANTILEVER CIS : 16 X 1

- **MEMS CIS Probe Card**
  - Max 64Para
  - Capable of Full Wafer Contact expansion
  - 8 x 8 (X, Y 1Skip)
  - MEMS Probe structure results in X,Y Skip



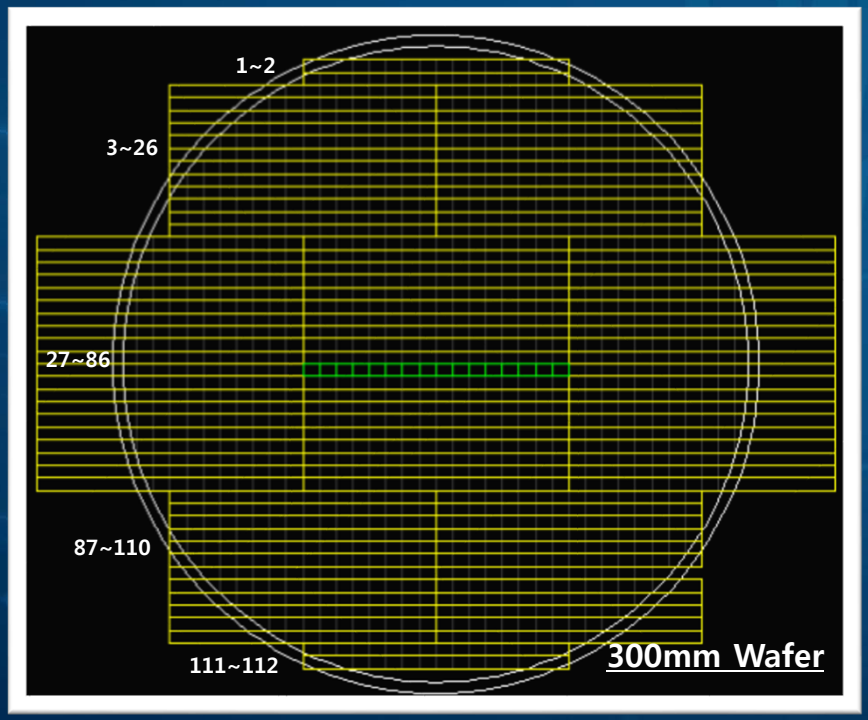
MEMS CIS : 8 X 8

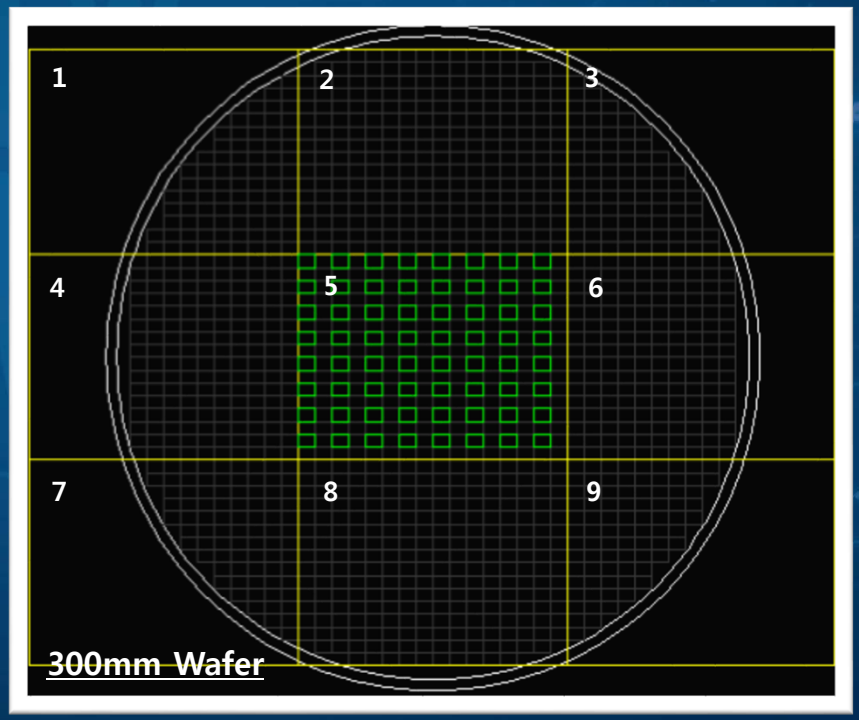
Multi Parallelism

Touch Down Efficiency (300mm Wafer)

- **Cantilever CIS**
  - 16 x 1 = 16 para
  - Per box 1 Shoot x 112 = Total 112 shoot

- **MEMS CIS**
  - 8 x 8 = 64para (X, Y 1Skip)
  - Per box 4 Shoot x 9 = Total 36 shoot





Cantilever P/C (112shoot) – MEMS P/C (36Shoot) -> Saves 76 shoot

Multi Parallelism

EX) TEST Efficiency (300mm Wafer)

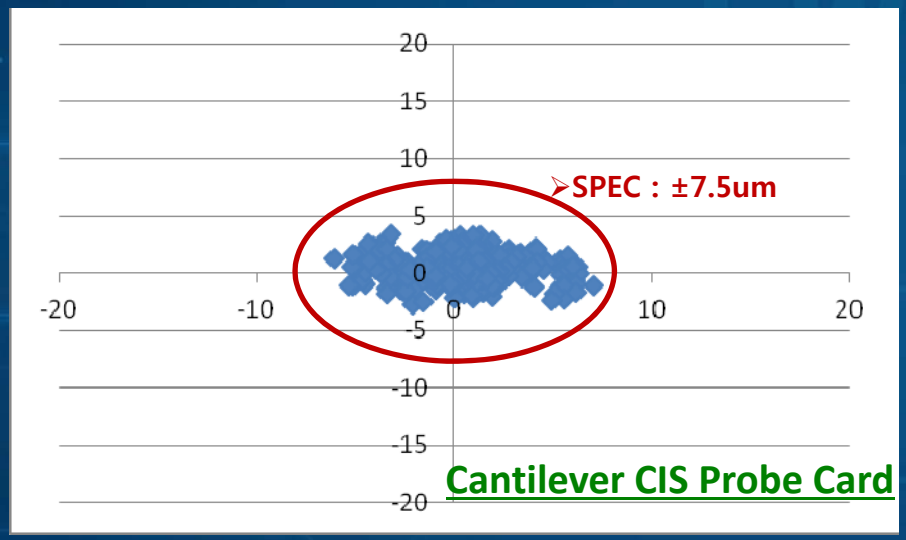
	Parallelism	Shoot	Test Time/ WF	Efficiency
CANTI CIS	16 (16X1)	112	53m	BASE
MEMS CIS	64(8X8)	36	17m	68% Reduction

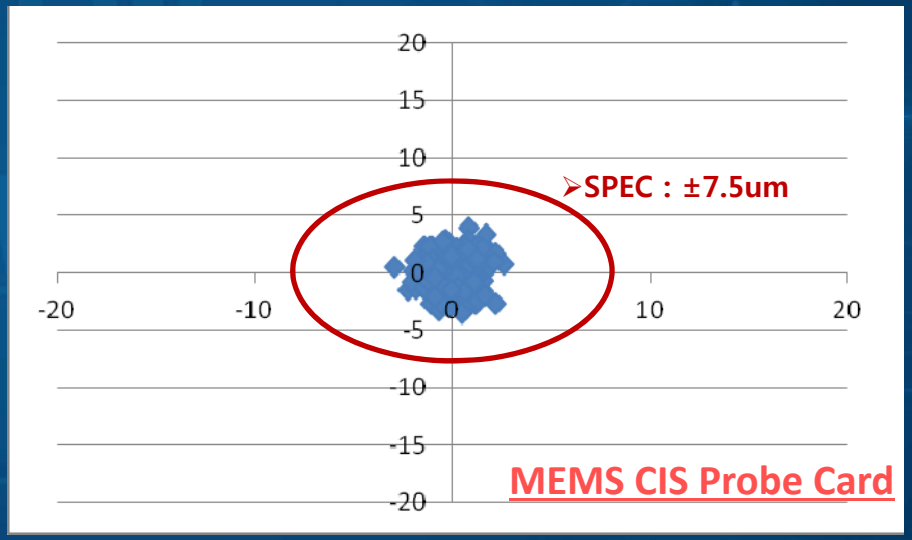
- **Cantilever CIS Probe Card**
  - Total 112 shoot required
  - Each Wafer takes 53m
- **MEMS CIS Probe Card**
  - Total 36 shoot required
  - Each Wafer takes 17m

Test time, reduced by 68%

Reliability

- **PIN Alignment**
  - Examine the Pin Alignment uniformity of Pin Cantilever P/C and MEMS P/C
  - Both type achieves uniformity within spec, However MEMS Type obtains superior uniformity

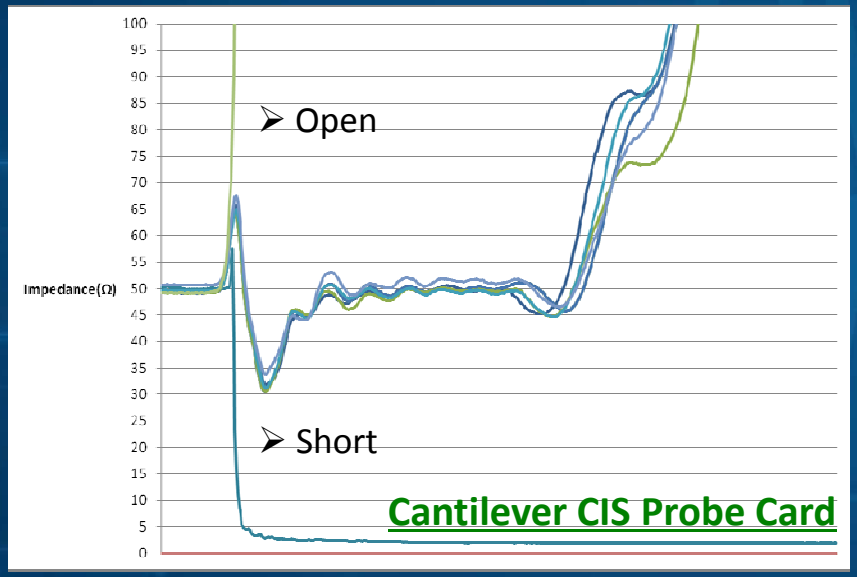


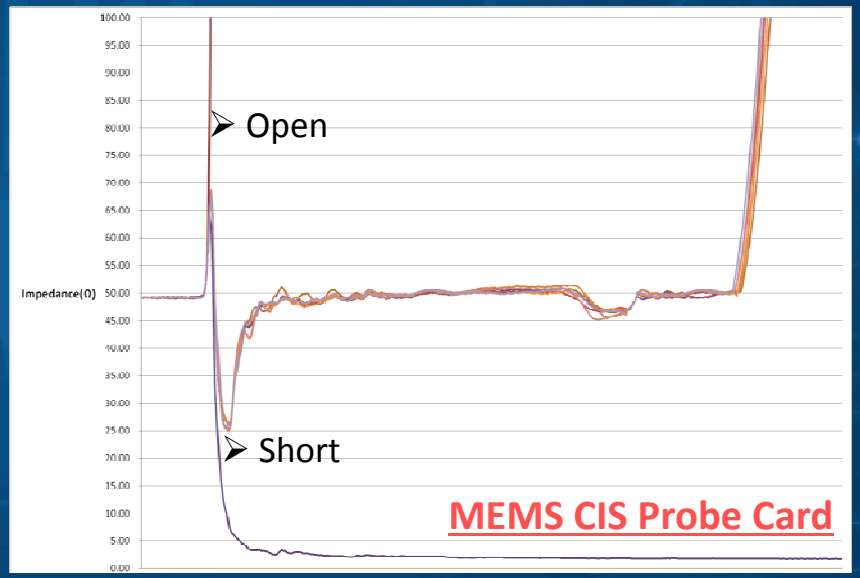


Cantilever P/C		MEMS P/C
Pin Alignment : within ±7.5um	>	Pin Alignment : within ± 5um

Reliability

- **Time Domain Reflectometry (TDR)**
  - TDR characteristic analysis of Cantilever P/C and MEMS P/C
  - MEMS Type achieves superior uniformity and greater stability over Cantilever





MEMS P/C	• PIN Alignment Uniformity • TDR Uniformity	→ Higher Reliability inMass Product

Conclusion

- MEMS is superior over Cantilever with respect to SI and PI characteristics
- Better touchdown efficiency leading to reduced test Cost
- MEMS suitable for Mass Production
- Challenges remain in FWC or 64 or greater para expansion
- To overcome such obstacles, Collaborations with Tester House and wafer development company is necessary